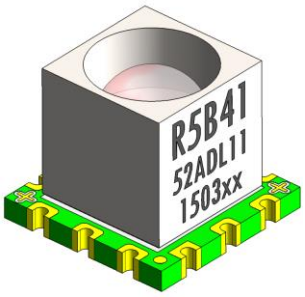
Preliminary Technical data sheet

850nm F-Light short distance optical receiver

PART NUMBER **FLR-500-IL-B4-001**

Features

- Digital optical receiver
- Data rate up to 5 Gbps
- Complies with IEEE Std. 802.3z Gigabit Ethernet 1000 Base-Sx PMD, ARINC 804 and PCI express
- Controls for better link reliability
- [-40;+85°C] operating temperature range
- SMT electrical interface
- Optimized for short distance and board to board communication
- Vibration tolerant
- Low power consumption (~160 mW)
- Compliant with MIL-STD 810/883 and DO-160D standards for temperature, damp heat, shocks and vibrations



Applications

- Severe environment interconnects
- Sensors interconnects
- Numerical video transmission
- Board-to-board communications
- Data communications
- On-board communications

Product Description

F-Light FLR-500-IL-B4-001 optoelectronic module is an high performance receiver optimized for high data rate short distance Free-space optical (FSO) communications. It is protocol independent and can be applied to Gigabit Ethernet, Fibre Channel, Infiniband, PCI Express or any specific communication application. The F-Light family is designed for Free-space communication within severe environments and complies with AEEC / ARINC 804 transceiver specifications.
The FLR-500-IL-B4-001 Free-Space Optical receiver is optimized for high speed DC-coupled serial links operating from 0.1 to 5 Gbps. The module is 3.3 Volts single supplied for low power consumption.
The receiver is based on high speed GaAs photodiode and high performances BiCMOS transimpedance (TIA) and limiting (LA) amplifiers.

The device has to be coupled with a Flight transmitter module FLT-500-xx-yy to set a full free space optical link.

Absolute maximum rating

Stress beyond these values may cause permanent damage to the device.

Table 1 - Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Storage temperature	T_{st}	-55	+125	°C	-
Soldering temperature	T_{sol}	-	260	°C	1,2
Soldering time	t_{sol}	-	30	s	1,2
Supply voltage	V_{CC}	-0.3	+4.0	V	3
Signal pins voltage range	V_{pin}	V_{EE}-0.3	V_{CC}+0.3	V	-
Junction temperature	TB_{JB}	-	130	°C	-
ESD resistance voltage	ESD	-	500	V	4

Notes:

1: MSL level 2 (J-STD-020D)
2 : compliant with ROHS solder reflow profile standard IPC/JEDEC J-STD-020D
3: V_{EE} is negative supply, V_{CC} is positive supply
4: ESD resistance based on HBM according to JESD22-A114-B

Module Optical and Electrical Specifications

Table 2 - General specifications VCC=3.3V, VEE=GND=0V

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Supply voltage	V_{CC}	3.0	3.3	3.6	V	-
Supply voltage noise	N_{VCC}	-	-	100	mV	1
Supply current	I_{ccRx}	-	30	35	mA	-
Data rate	B	0.1	-	5	Gbps	-
Operating temperature	T_{op}	-40	-	+85	°C	-

Notes:

For noise frequencies < 5MHz.

Table 3 - Electrical Specification- High Speed channels B= 5 Gbps, VCC=3.3V, VEE=GND=0V, Temp= [-40:+85°C]

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Differential output voltage	V_{OUTdif}	200	400	700	mV	-
Output impedance (differential)	Z_{out}	90	100	110	Ω	-
Output CML drive current	I_o	-	12	-	mA	-
Total jitter receiver	T_{JRx}	-	60	150	ps	-
Rise/Fall time	$\tau_{R\ Rx}$, $\tau_{F\ Rx}$	-	80	150	ps	1
Differential peak to peak noise output when squelched		-	-	10	mV	-

Notes:

1. Measured at 20% / 80% levels

Table 4 - Electrical Specification- I/O CMOS B= 5 Gbps, VCC=3.3V, VEE=GND=0V, Temp= [-40:+85°C]

Parameter		Symbol	Min	Typ.	Max	Unit	Notes
Digital inputs voltage	High	V_{INhigh}	2	-	V_{CC}+ 0.3	V	-
	Low	V_{INlow}	V_{EE} - 0.3	-	0.8	V	-
Digital input current		I_{IN}	-	-	+/-5	µA	-
Digital outputs voltage	High	V_{OH}	V_{CC} -0.2	-	-	V	-
	Low	V_{OL}	-	-	0.2	V	-
Digital output currents		I_{Out}	+/- 2	-	-	mA	-

Table 5 - Optical Specification B= 5 Gbps, VCC=3.3V, VEE=GND=0V, Temp= [-40:+85°C]

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Center wavelength	λ_c	840	850	860	nm	-
Spectral width – rms	$\Delta\lambda$	-	-	1	nm	-
Squelch turn-on threshold (peak to peak current @4 Gbit)	SQtn	-	-	-16	dBm	-

Remark: ambient light has no impact on FLR specifications

Data output stage:

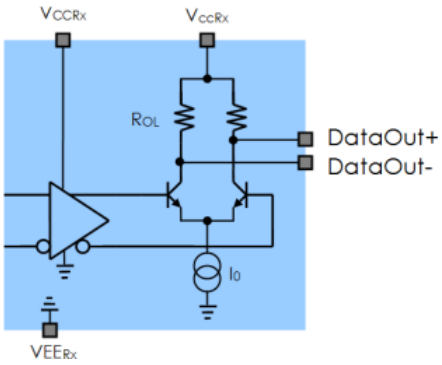
The output stage is a differential current-mode-logic (CML) driver. The pull-up resistors are tied to the pin Vcc.The general characteristics of the output stage are the following :

- Switched current I_0 of 9mA,
- pull-ups R_{OL} 2x50Ω to Vcc.

❑ For Differential DC-coupled termination with negative power supply. The outputs are then connected to 50Ω tracks, terminated by two 50Ω loads to ground, or a floating 100Ω load.

❑ For single-ended AC-coupled: both outputs should see equal load impedances.

Fig.1 - FLR Ouput stage



Power supply filtering

The module is 3.3 Volts single power supply and includes internal decoupling components. Supply filtering is recommended, with roll-off frequency at 10 MHz or lower.

An additional filtering can reduce the noise penalty above 10 MHz. For a supply noise V_{PSN} = 100 mV_{PP} a 0.5dB sensitivity penalty can be reached over the whole frequency range by using a first order low-pass filter with f_c = 10 MHz on the power supply (See the following figure for component values).

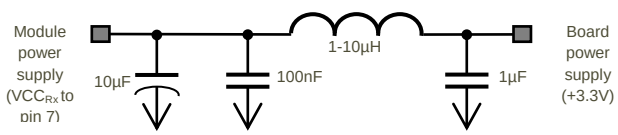


Fig.2 - Power supply filtering recommendation

Surface mount package mechanical drawing

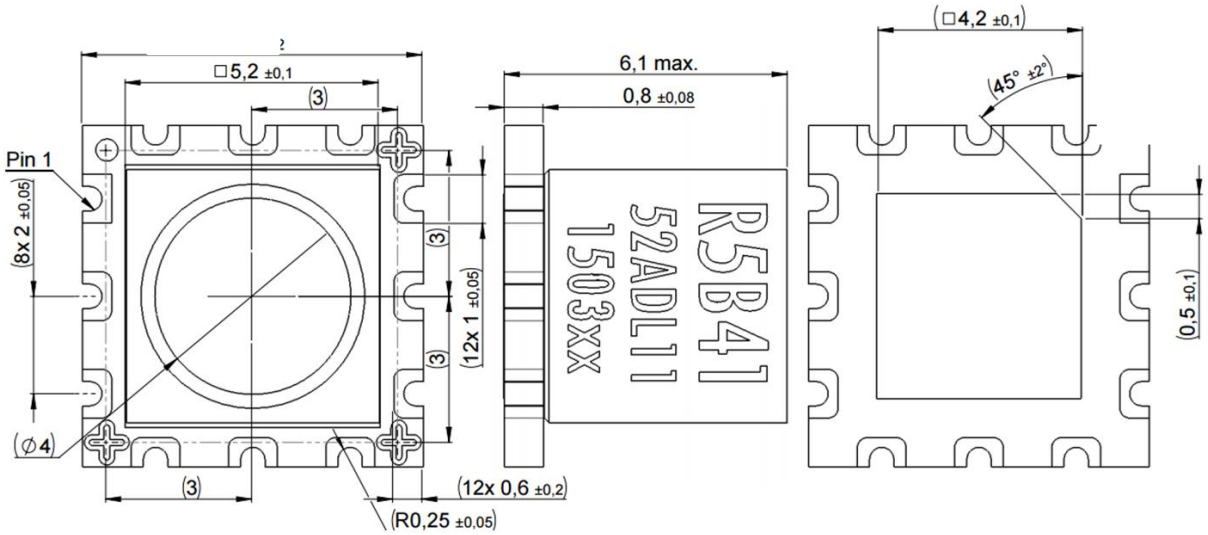


Fig.3 - FLR mechanical drawing

All dimensions in millimeters.

Notes:
1. Mass of the receiver module: 0.650g

Protection and handling cap mechanical drawing

A protection cap is delivered with the FLR-500-IL-B4-001 This cap can be used to handle the module during positioning and soldering phases..

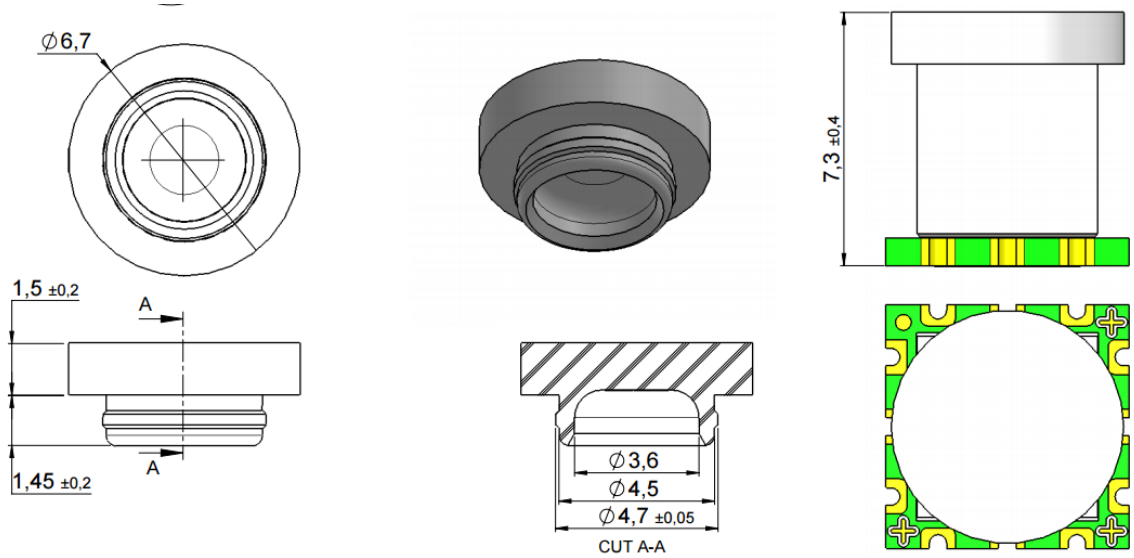


Fig.4 - FLR protection cap

All dimensions in millimeters. Colour : white.

Notes:
1. Mass of the cap: 0.085g

Pin-out description

Signal	Pin number	Type	Description
DataOut+	1	HS[1] Output	**Positive Data Output:** CML positive high speed output.
DataOut-	2	HS[1] Output	**Negative Data Output:** CML negative high speed output.
Squelch	3	Digital input[5]	**Squelch:** This pin controls the squelch function of the receiver. If low, the differential output data are hold to the common mode output voltage if the signal detect signal is low. If this pin is high the receiver does not squelch.
CONFRx	4	Digital input[5]	**Mode selection:** connect to VccRx (stand-alone mode [2])
SDA	6	Digital Input/ Output	**I²C serial data pin :** left unconnected for stand-alone use
V_{CC}	7	Power	**Positive supply:** +3.3Volts positive power supply for the receiver.
SCL	10	Digital Input	**I²C serial Clock pin :** left unconnected for stand-alone use
RSSI	11	Analog Output	**Receiver Signal Strength Indicator (Average optical power)**: this Analog output pin allows the user to monitor the average incident optical power. The current on this pin is proportional to the input optical power. [3]
RxFault	12	Digital output[5]	**Receiver Fault:** this signal detect output allows the user to detect that no light or insufficient light is seen by the receiver (open link for instance). RxFault low: normal (lighted) RxFault high: abnormal (unlighted)
V_{EE}	5,8,9,13 [4]	Power	**Negative supply:** negative power supply tied to 0 Volt for the transmitter and receiver

Notes:

1. HS pin type: High Speed inputs / output pins.
2. Radiall imposes the use of the stand-alone mode to operate the device. The I²C-controlled mode is currently reserved for internal use.
3. see following §
4. Pin n°13 is the central rear pad
5. CMOS I/O, JEDEC JESD8-C compliant

Receiver incident optical power computations

The Receiver Signal Strength Indicator (RSSI) delivers an analog current proportional to the average photo-detector current, I_{RSSI}

The user can set an external resistor to get a voltage at RSSI output. This voltage will be proportional to the input optical power of the receiver and the load resistor externally (R_{ext}) attached to the pin thought the following equation:

$$I_{RSSI} = \chi \cdot P_{opt}$$

$$V_{RSSI} = R_{ext} \cdot \chi \cdot P_{opt} \rightarrow P_{opt} = \frac{V_{RSSI}}{R_{ext} \cdot \chi} \text{ (W)}$$

Where R_{ext} is the resistor attached to RSSI pin, χ an internal coefficient and P_{opt} the incident receiver optical power in W. Note that linearity is maintained for $V_{RSSI} \leq 2.2V$.

	Symbol	Min.	Typ.	Max.
Internal coefficient for RSSI	χ	0.52	0.6	0.63

Recommended PCB layout

The PCB layout is viewed from above
All dimensions are in millimeters.

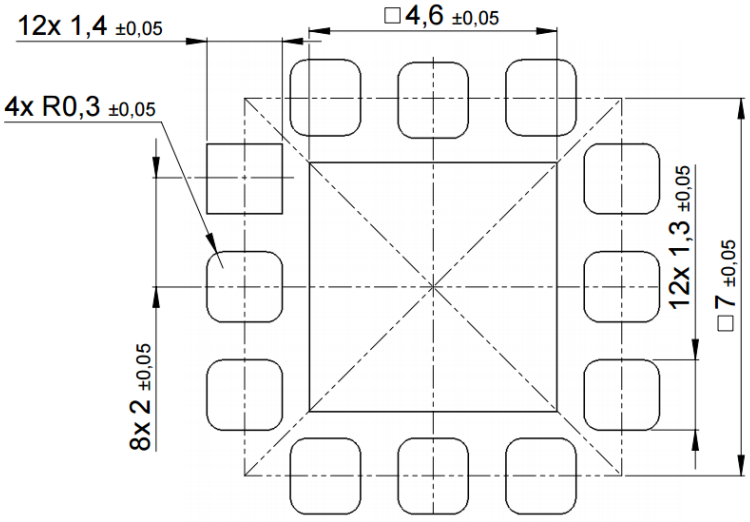


Fig.5 - FLR recommended PCB layout

Related documents

Reference	Document tittle
F-Light S15-500-A	850 nm F-Light short distance optical link
AN-FL01	F-Light soldering process
EVB-FLx-500-IL	F-Light evaluation board

Document history

Version	Date	Author	Signed-off	Notes
V1.0	20-08-2015	LP	FQ	First release
V1.1	02-10-2015	LP	FQ	Change of module view p1 Change of soldering temperature/time max values Change of module mechanical drawing Add RxFault status
V1.2	05-11-2015	LP	FQ	Change of module view p1 Add MSL level p2 Reorganize electrical and optical specs' tables p2 Add digital I/O inpout/output currents p2 Add data input stage § p3 Up-date mechanical drawings for module and protection cap p4; add parts weight and colour Up-date pin-out description §p5 Up-date RSSI computation § p5 Up-date recommended PCB layout p6 Add EVB-FLx-500-IL in related documents chart p6
V1.3	22-12-2015	FQ	MP	Correction of pin 7 pinout information p5 Change of recommended power supply filtering p3