

N-channel 650 V, 0.75 Ω typ., 10 A SuperMESH3™ Power MOSFETs
in D²PAK, TO-220FP, I²PAKFP and TO-220 packages

Datasheet - production data

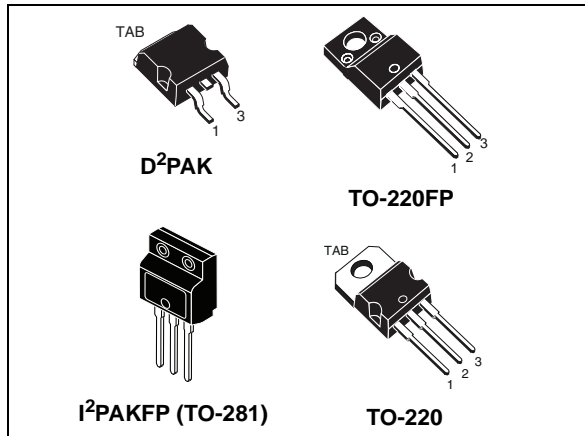
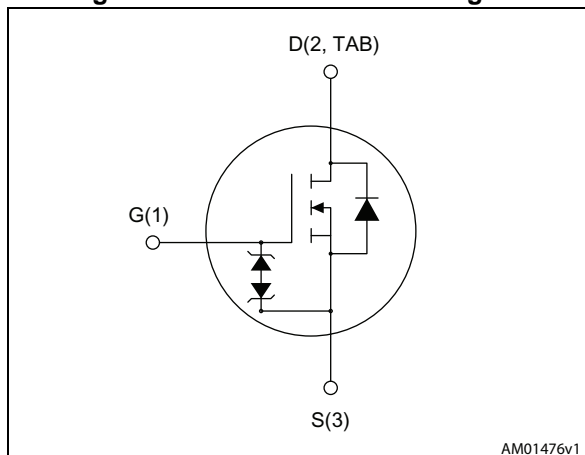


Figure 1. Internal schematic diagram



Features

Order codes	V _{DS}	R _{DS(on)} max	I _D	P _{TOT}
STB10N65K3	650 V	1 Ω	10 A	150 W
STF10N65K3				35 W
STFI10N65K3				
STP10N65K3				150 W

- 100% avalanche tested
- Extremely low on-resistance R_{DS(on)}
- Gate charge minimized
- Very low intrinsic capacitances
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- Switching applications

Description

These SuperMESH3™ Power MOSFETs are the result of improvements applied to STMicroelectronics' SuperMESH™ technology, combined with a new optimized vertical structure. These devices boast an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering them suitable for the most demanding applications.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB10N65K3	10N65K3	D ² PAK	Tape and reel
STF10N65K3		TO-220FP	Tube
STFI10N65K3		I ² PAKFP (TO-281)	
STP10N65K3		TO-220	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220FP I ² PAKFP	D ² PAK, TO-220	
V _{DS}	Drain source voltage	650		V
V _{GS}	Gate-source voltage	± 30		V
I _D	Drain current (continuous) at T _C = 25 °C	10		A
I _D	Drain current (continuous) at T _C = 100 °C	6.3		A
I _{DM} ⁽¹⁾	Drain current (pulsed)	40		A
P _{TOT}	Total dissipation at T _C = 25 °C	35	150	W
I _{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T _{JMAX})	7.2		A
E _{AS}	Single pulse avalanche energy ⁽²⁾	212		mJ
	Derating factor	0.28	1.2	W/°C
dv/dt ⁽³⁾	Peak diode recovery voltage slope	12		V/ns
ESD	Gate-source human body model (R = 1.5 kΩ, C = 100 pF)	2.8		kV
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T _C =25 °C)	2500		V
T _j	Operating junction temperature	-55 to 150		°C
T _{stg}	Storage temperature			°C

1. Pulse width limited by safe operating area.
2. Starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V
3. I_{SD} ≤ 10 A, di/dt = 100 A/μs, V_{Peak} < V_{(BR)DSS}

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		D ² PAK	TO-220FP I ² PAKFP	TO-220	
R _{thj-case}	Thermal resistance junction-case max	0.83	3.57	0.83	°C/W
R _{thj-amb}	Thermal resistance junction-ambient max		62.5		°C/W
R _{thj-pcb}	Thermal resistance junction-pcb max	30			°C/W

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0	650			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 650 V			1	μA
		V _{DS} = 650 V, T _C = 125 °C			50	μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 100 μA	3		4.5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 3.6 A		0.75	1	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0	-	1180	-	pF
C _{oss}	Output capacitance		-	125	-	pF
C _{riss}	Reverse transfer capacitance		-	14	-	pF
C _{oss eq.}	Equivalent output capacitance	V _{DS} = 0 to 520 V, V _{GS} = 0	-	77	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz, I _D = 0	-	3	-	Ω
Q _g	Total gate charge	V _{DD} = 520 V, I _D = 7.2 A, V _{GS} = 10 V (see Figure 18)	-	42	-	nC
Q _{gs}	Gate-source charge		-	7.4	-	nC
Q _{gd}	Gate-drain charge		-	23	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 310 V, I _D = 3.5 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 17)	-	14.5	-	ns
t _r	Rise time		-	14	-	ns
t _{d(off)}	Turn-off-delay time		-	44	-	ns
t _f	Fall time		-	35	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		7.2	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				28.8	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 7 \text{ A}, V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 7 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see Figure 22)	-	320		ns
Q_{rr}	Reverse recovery charge		-	2		μC
I_{RRM}	Reverse recovery current		-	13		A
t_{rr}	Reverse recovery time	$I_{SD} = 7 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ (see Figure 22)	-	410		ns
Q_{rr}	Reverse recovery charge		-	2.9		μC
I_{RRM}	Reverse recovery current		-	14		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}, I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D²PAK and TO-220

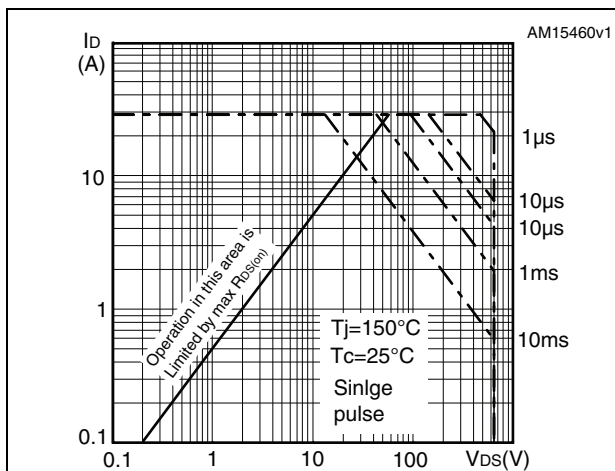


Figure 3. Thermal impedance for D²PAK and TO-220

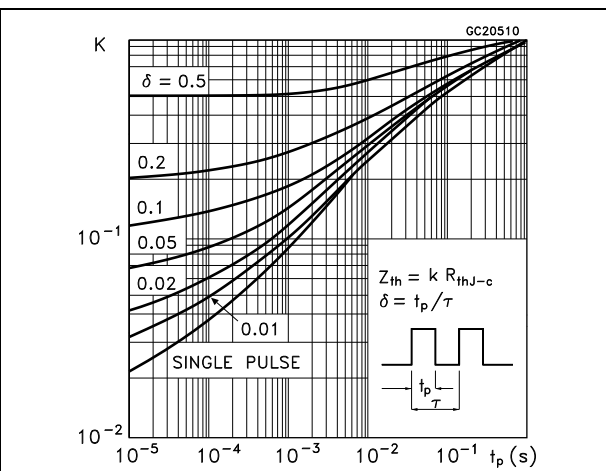


Figure 4. Safe operating area for TO-220FP and I²PAKFP

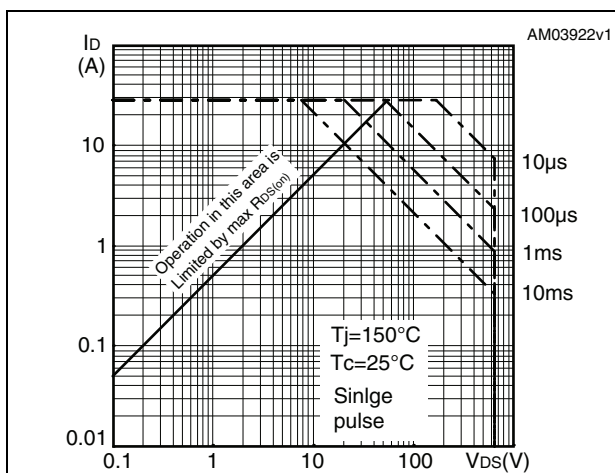


Figure 5. Thermal impedance for TO-220FP and I²PAKFP

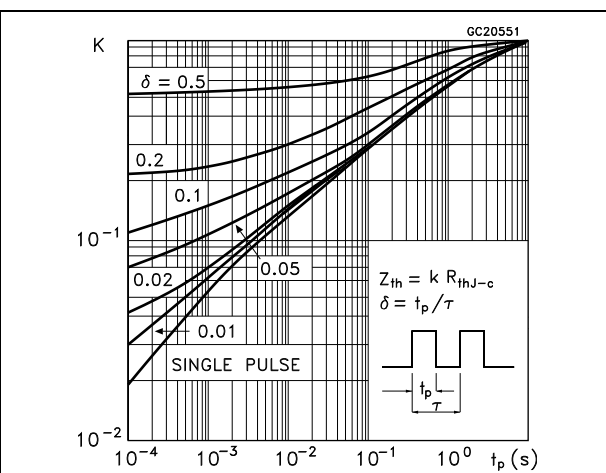


Figure 6. Output characteristics

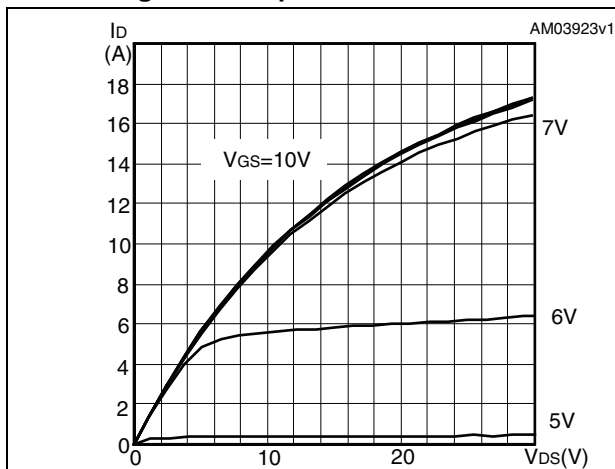


Figure 7. Transfer characteristics

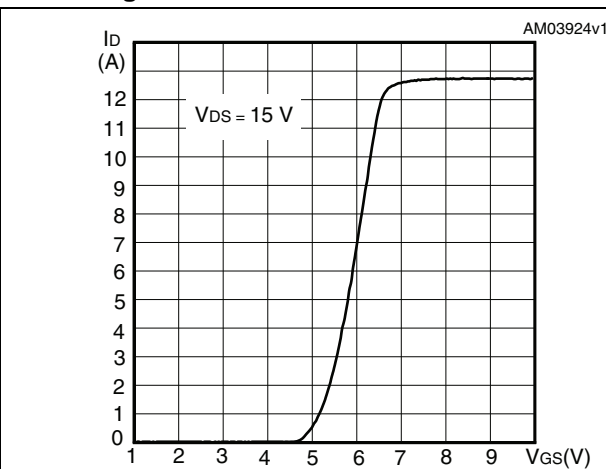


Figure 8. Normalized BV_{DSS} vs temperature

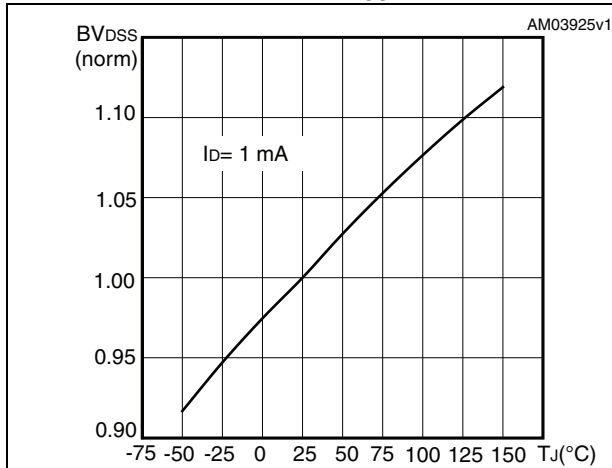


Figure 9. Static drain-source on resistance

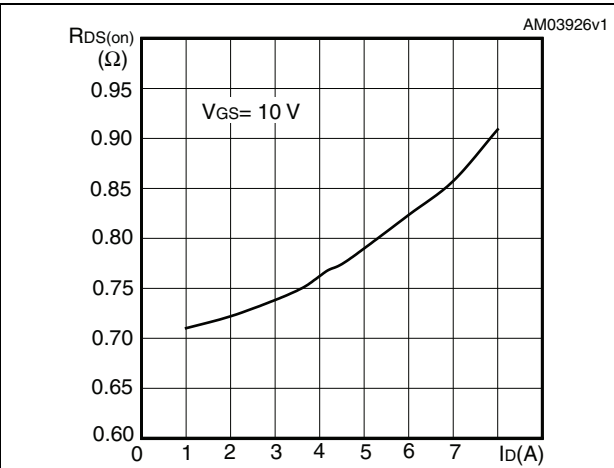


Figure 10. Output capacitance stored energy

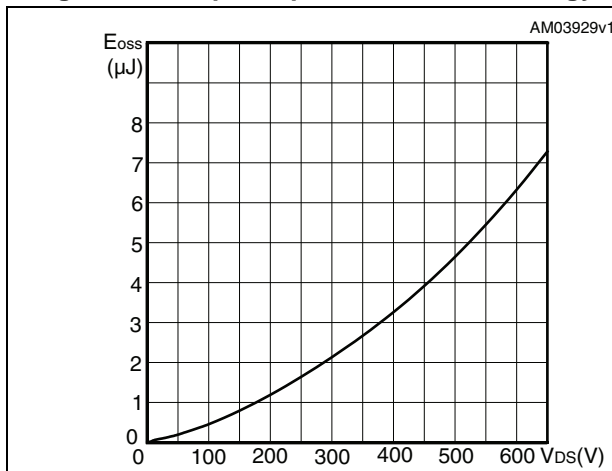


Figure 11. Capacitance variations

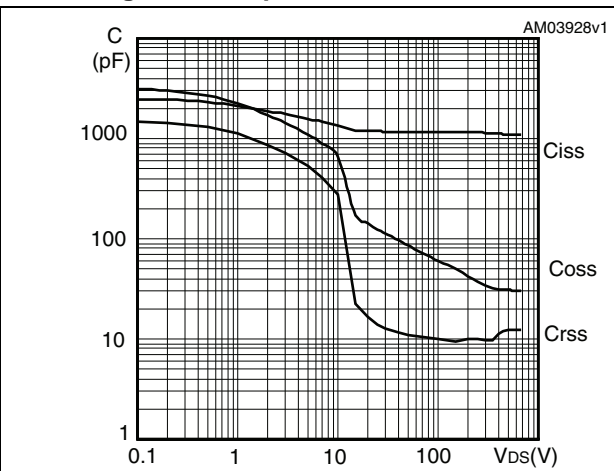


Figure 12. Gate charge vs gate-source voltage

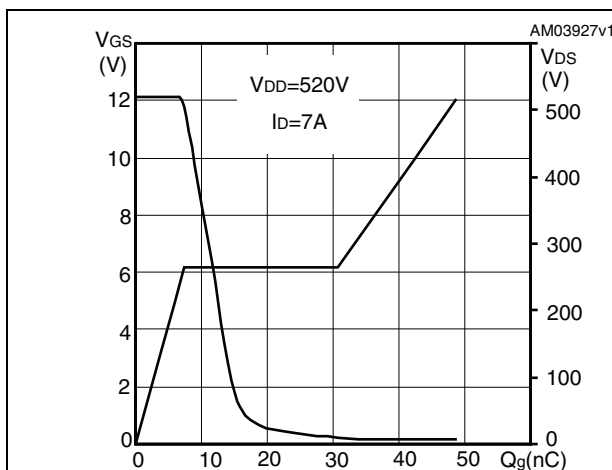


Figure 13. Normalized on-resistance vs temperature

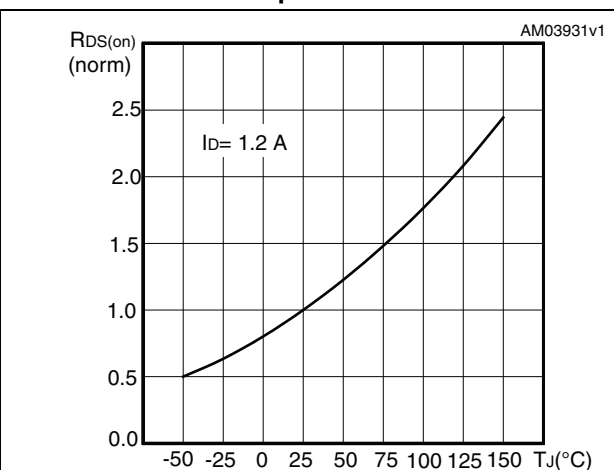


Figure 14. Normalized gate threshold voltage vs temperature

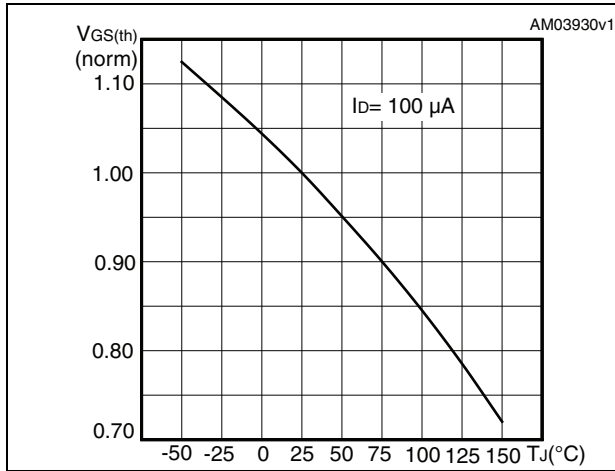


Figure 15. Maximum avalanche energy vs temperature

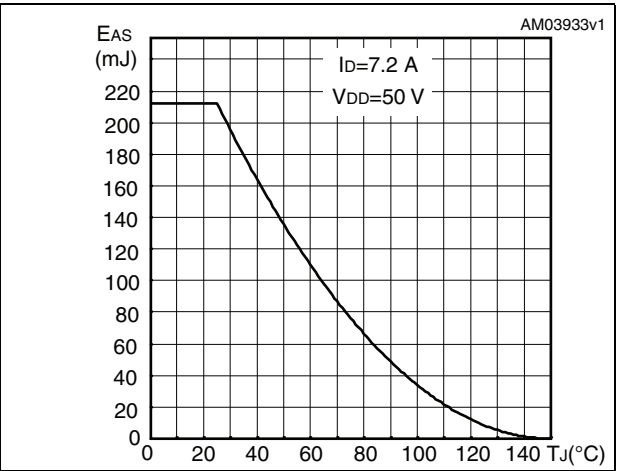
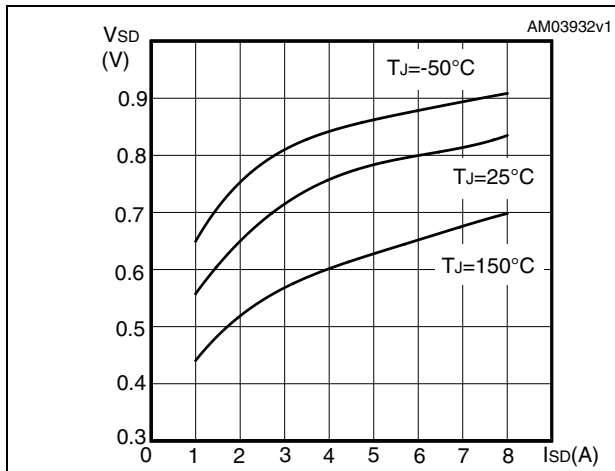


Figure 16. Source-drain diode forward characteristics



3 Test circuits

Figure 17. Switching times test circuit for resistive load



Figure 18. Gate charge test circuit

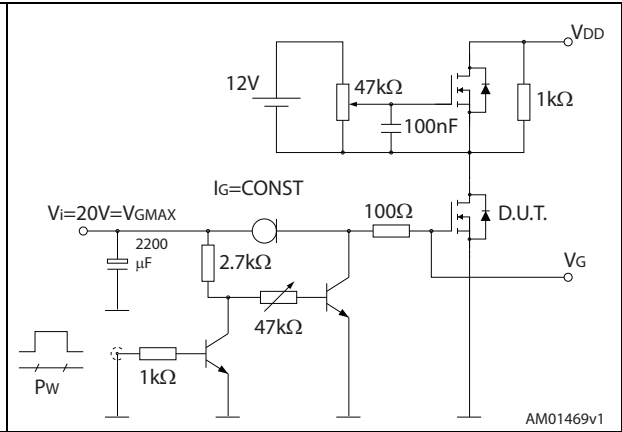


Figure 19. Test circuit for inductive load switching and diode recovery times



Figure 20. Unclamped inductive load test circuit

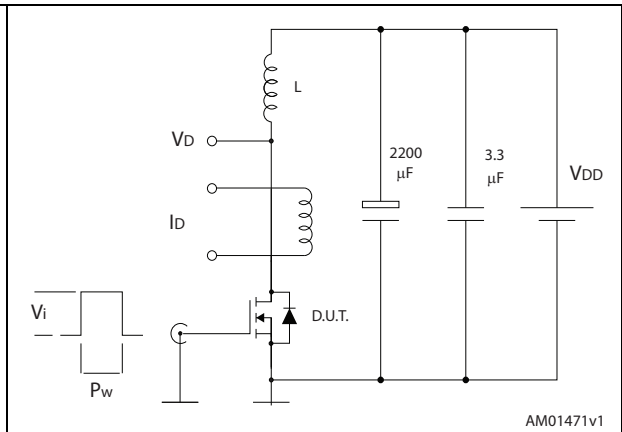


Figure 21. Unclamped inductive waveform

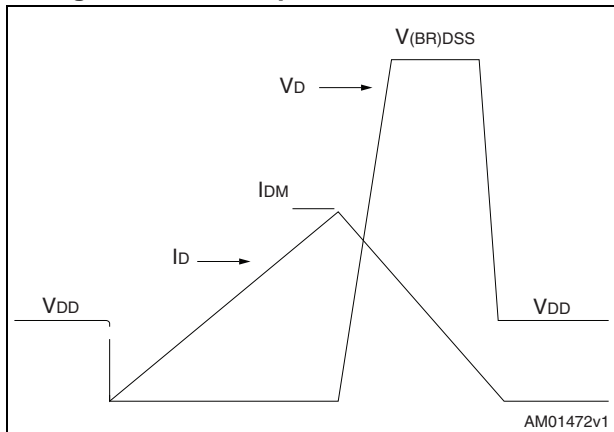
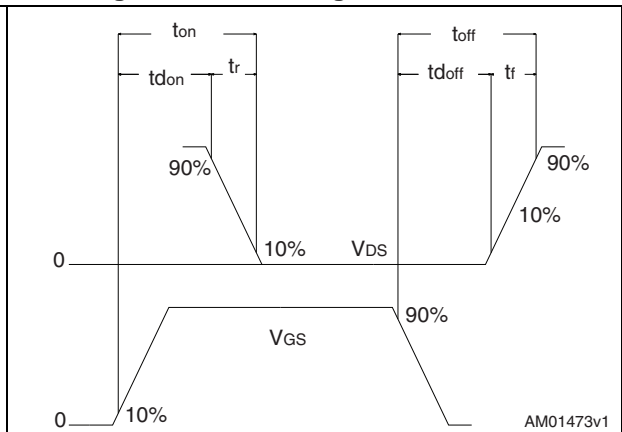


Figure 22. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 9. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 23. D²PAK (TO-263) drawing

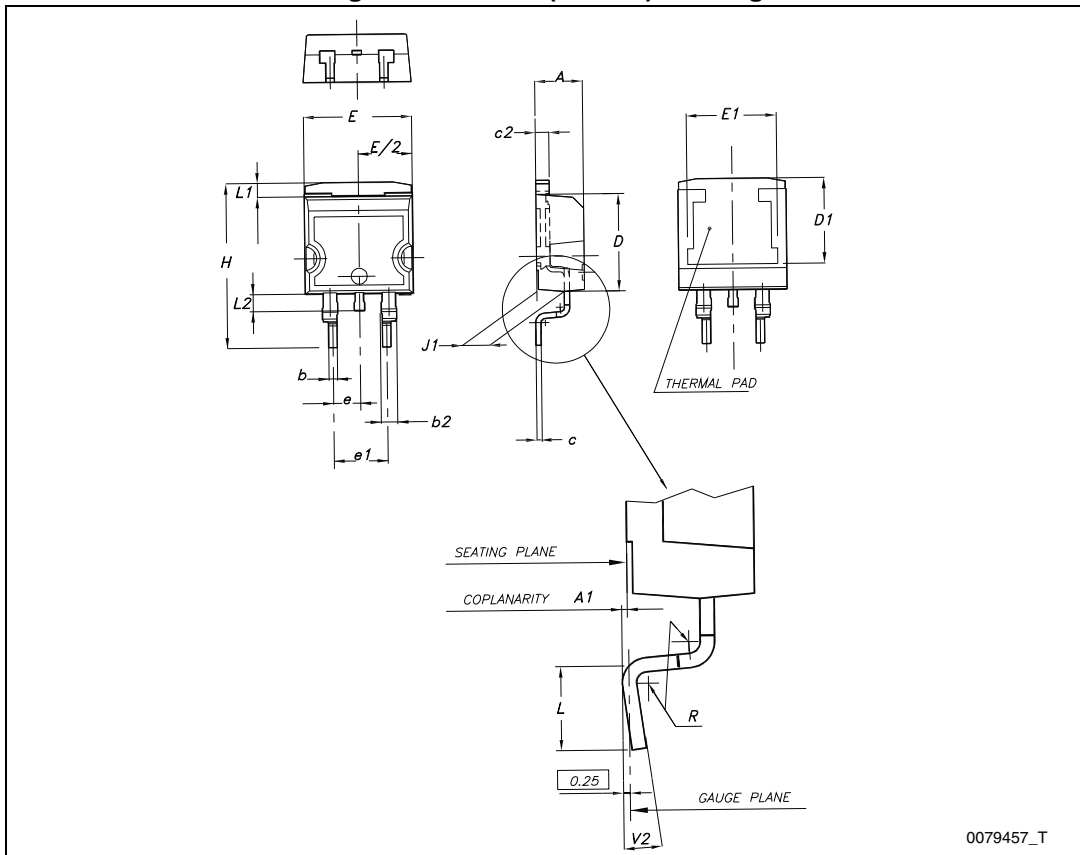
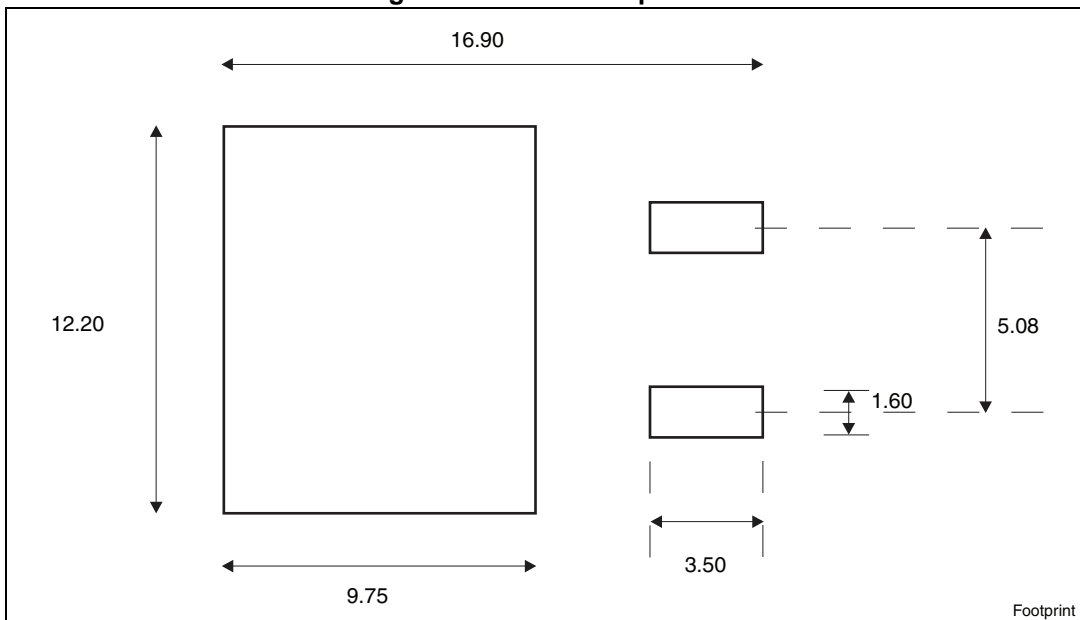


Figure 24. D²PAK footprint^(a)

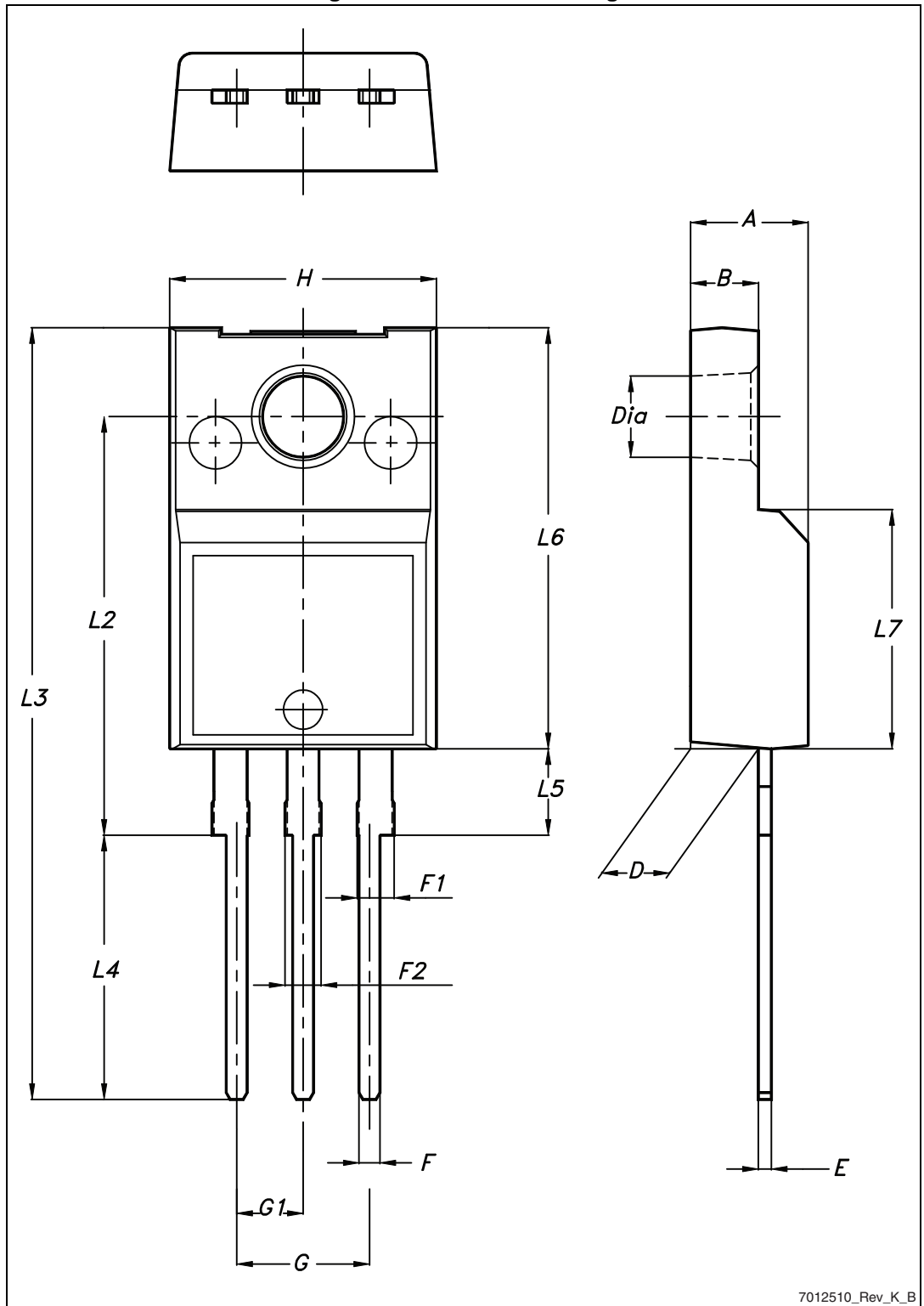


a. All dimension are in millimeters

Table 10. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 25. TO-220FP drawing

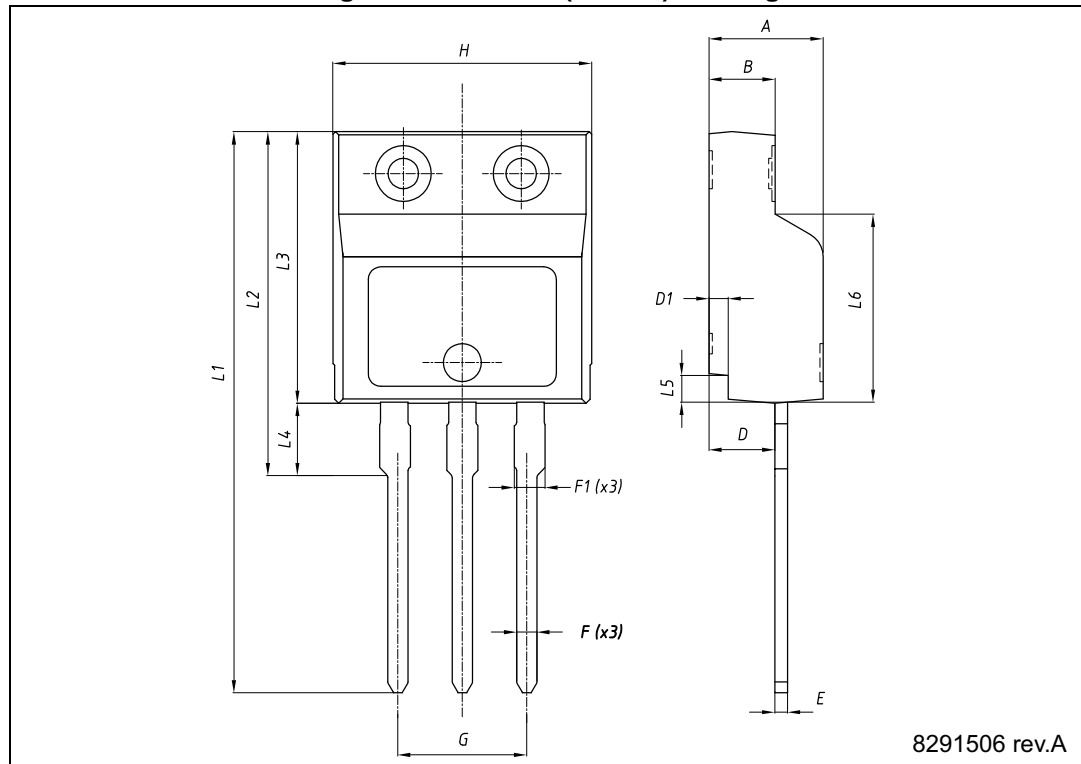


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Table 11. I²PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95	-	5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

Figure 26. I²PAKFP (TO-281) drawing

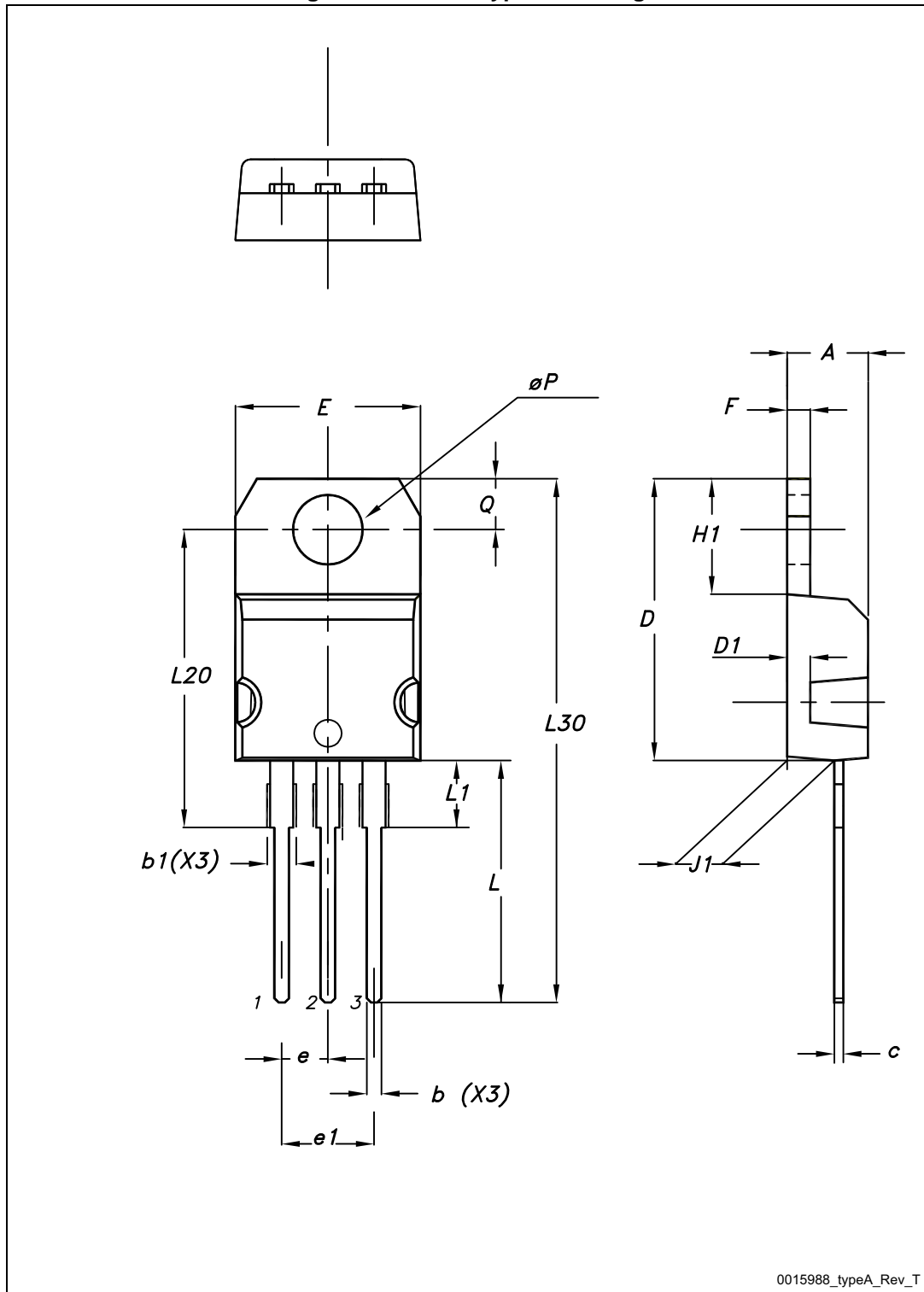


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Table 12. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 27. TO-220 type A drawing



5 Packaging mechanical data

Table 13. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 28. Tape

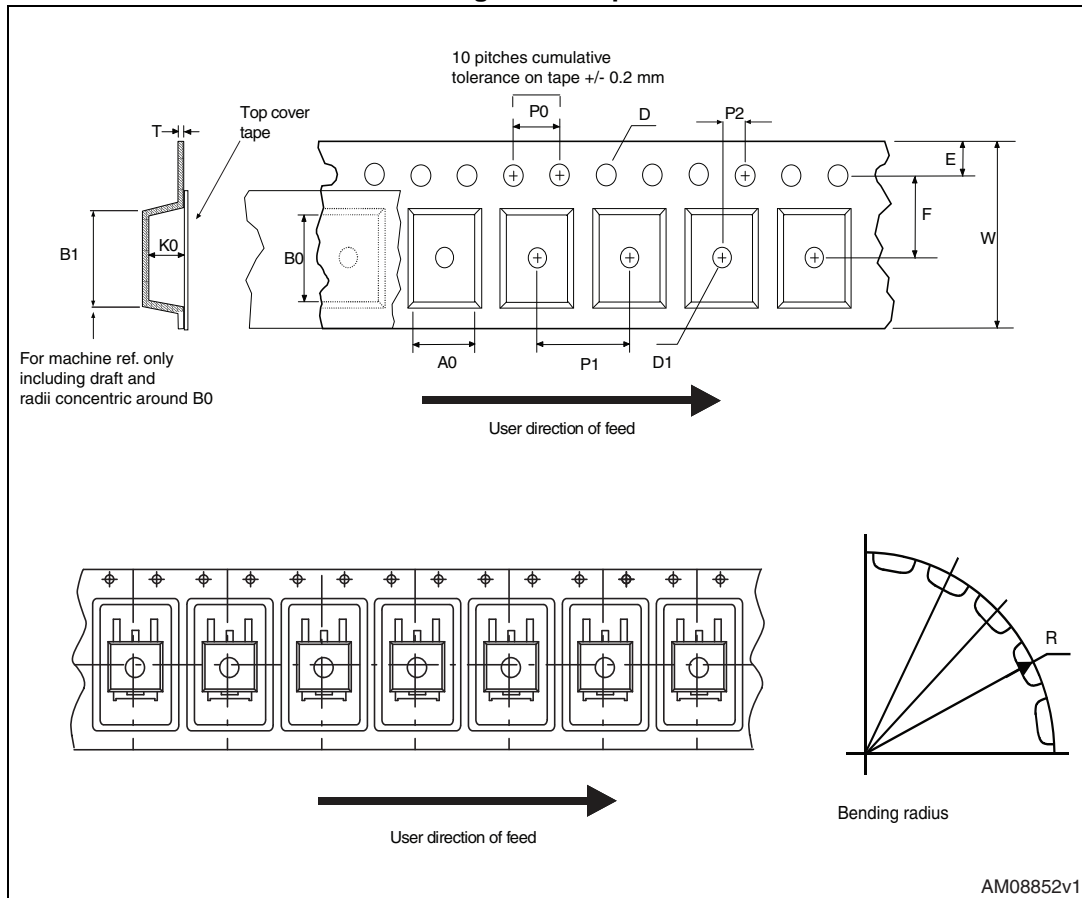
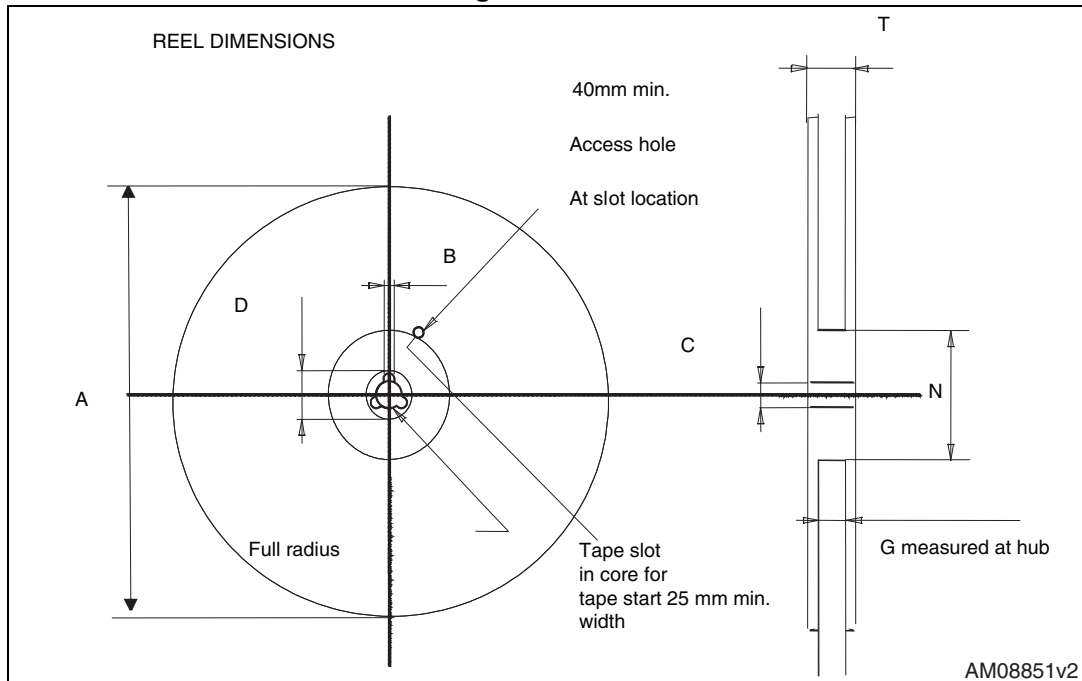


Figure 29. Reel



6 Revision history

Table 14. Document revision history

Date	Revision	Changes
30-Jun-2009	1	First release
14-Nov-2011	2	Updated mechanical data and Section 2.1: Electrical characteristics (curves) . Minor text changes.
14-Nov-2012	3	<ul style="list-style-type: none"> – Added: I²PAKFP and TO-220 – Deleted: T_l row – Added: R_{DS(on)} typical value, Figure 2 and 3 – Modified: Figure 2 – Updated: Section 4: Package mechanical data
05-Aug-2013	4	<ul style="list-style-type: none"> – Added: D²PAK package – Added: R_{thj-pcb} in Table 3 – Updated: figure Figure 17, 18, 19 and 20 – Updated: Section 4: Package mechanical data and Section 5: Packaging mechanical data – Minor text changes

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