



STS11N3LLH5

N-channel 30 V, 0.0117 Ω , 11 A, SO-8
STripFET™ V Power MOSFET

Features

Type	V _{DSS}	R _{DS(on) max}	I _D
STS11N3LLH5	30 V	< 0.0132 Ω	11 A ⁽¹⁾

1. The value is rated according R_{thj-pcb}

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™V technology. The device has been optimized to achieve very low on-state resistance, contributing to an FOM that is among the best in its class..

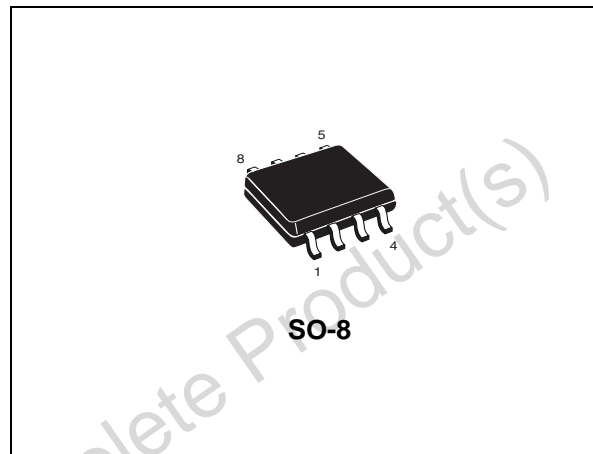


Figure 1. Internal schematic diagram

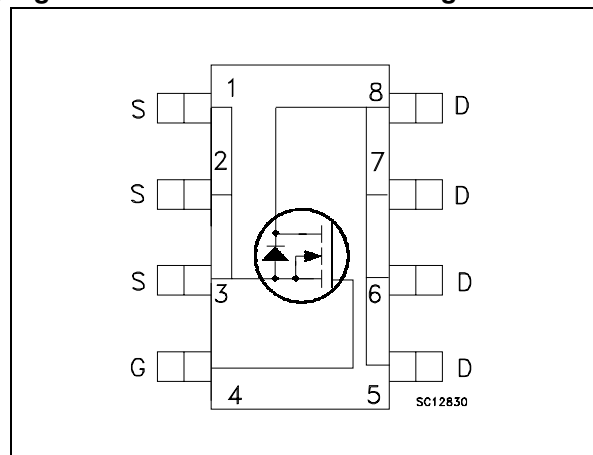


Table 1. Device summary

Order code	Marking	Package	Packaging
STS11N3LLH5	11D3L	SO-8	Tape and reel

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Obsolete Product(s) - Obsolete Product(s)

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	30	V
V_{GS}	Gate-source voltage	+ 22 / - 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	11	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	8	A
$I_{DM}^{(2)}$	Drain current (pulsed)	44	A
$P_{TOT}^{(2)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	2.7	W
	Derating factor	0.02	W/ $^\circ\text{C}$
T_J	Operating junction temperature	-55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature		

1. The value is rated according to $R_{thj-pcb}$
2. Pulse width limited by safe operating area.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	46	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10\text{sec}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 250 \mu A$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating}$, $V_{DS} = \text{max rating}$ $T_C = 125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = +22 / -20 V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 V$, $I_D = 5.5 A$ $V_{GS} = 4.5 V$, $I_D = 5.5 A$		0.0117 0.017	0.0132 0.019	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25 V$, $f = 1 \text{ MHz}$, $V_{GS} = 0$	-	724		pF
C_{oss}	Output capacitance			132		pF
C_{rss}	Reverse transfer capacitance			20		pF
Q_g	Total gate charge	$V_{DD} = 15 V$, $I_D = 11 A$ $V_{GS} = 4.5 V$ <i>Figure 14</i>	-	5		nC
Q_{gs}	Gate-source charge			2		nC
Q_{gd}	Gate-drain charge			2		nC
R_G	Intrinsic gate resistance	$f = 1 \text{ MHz}$ gate dc bias = 0 test signal level = 20 mV open drain	-		3.3	Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15 V$, $I_D = 5.5 A$, $R_G = 4.7 \Omega$, $V_{GS} = 10 V$ <i>Figure 13</i>	-	4		ns
t_r	Rise time			4.2		ns
$t_{d(off)}$	Turn-off delay time			21	-	ns
t_f	Fall time			3.5		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		44	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 11 \text{ A}, V_{GS}=0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 11 \text{ A},$ $di/dt = 100 \text{ A}/\mu\text{s},$ $V_{DD} = 25 \text{ V}, T_J = 150 \text{ }^\circ\text{C}$	-	21		ns
Q_{rr}	Reverse recovery charge			10		nC
I_{RRM}	Reverse recovery current			1		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Obsolete Product(s) - Obsolete Product(s)

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

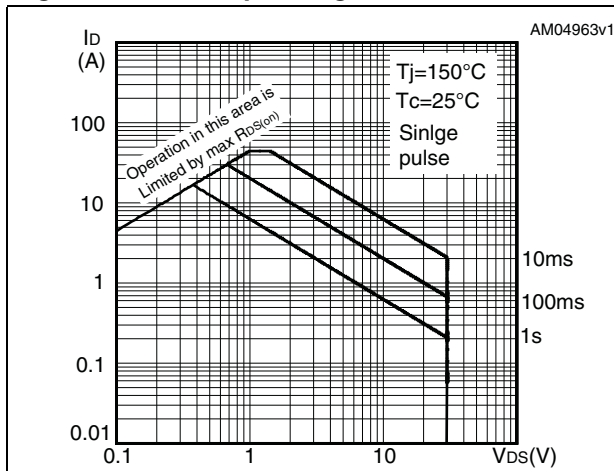


Figure 3. Thermal impedance

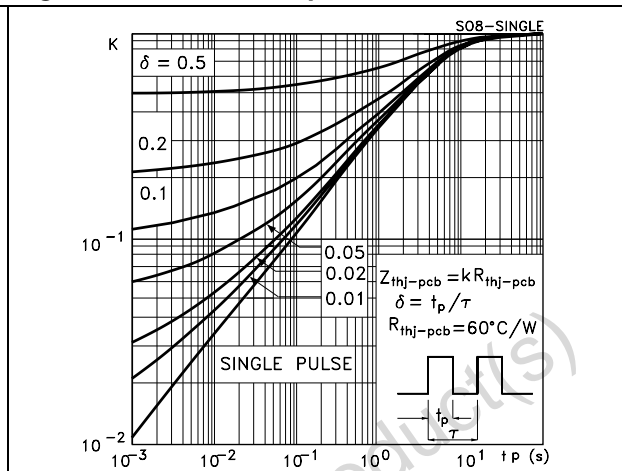


Figure 4. Output characteristics

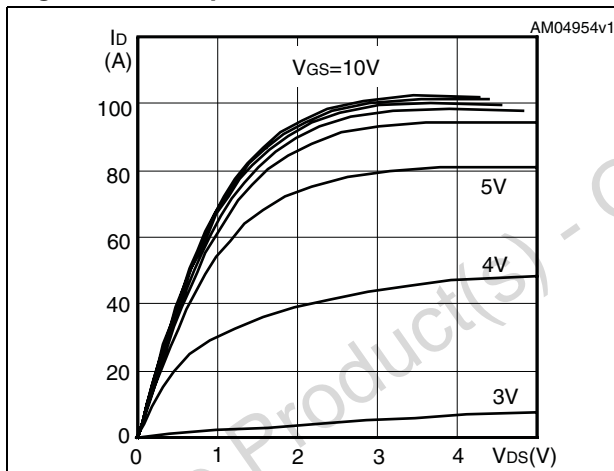


Figure 5. Transfer characteristics

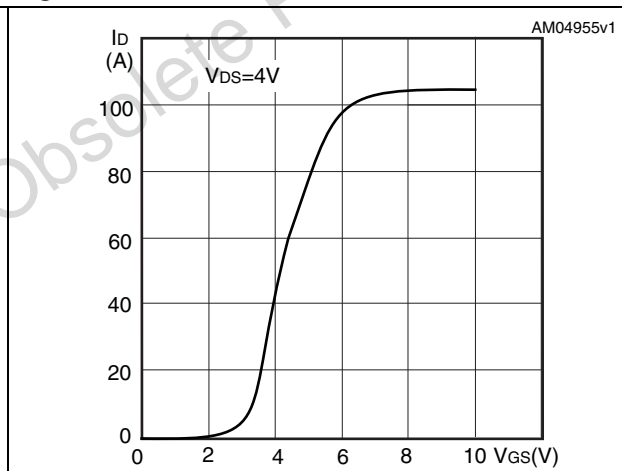


Figure 6. Normalized $B_{V_{DSS}}$ vs temperature

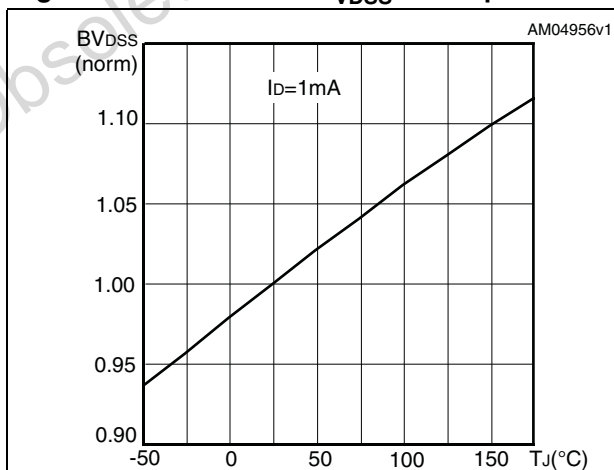


Figure 7. Static drain-source on resistance

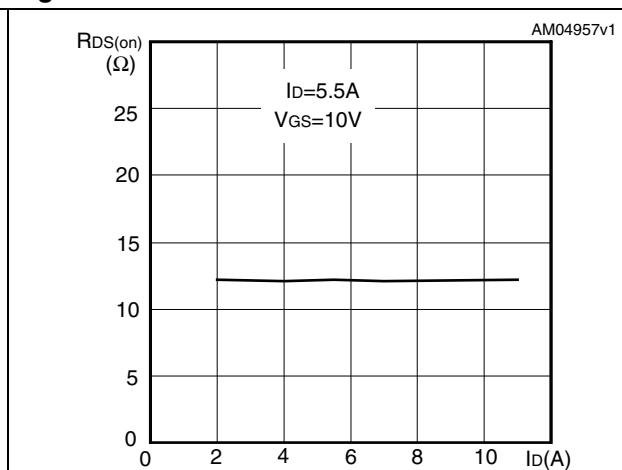


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

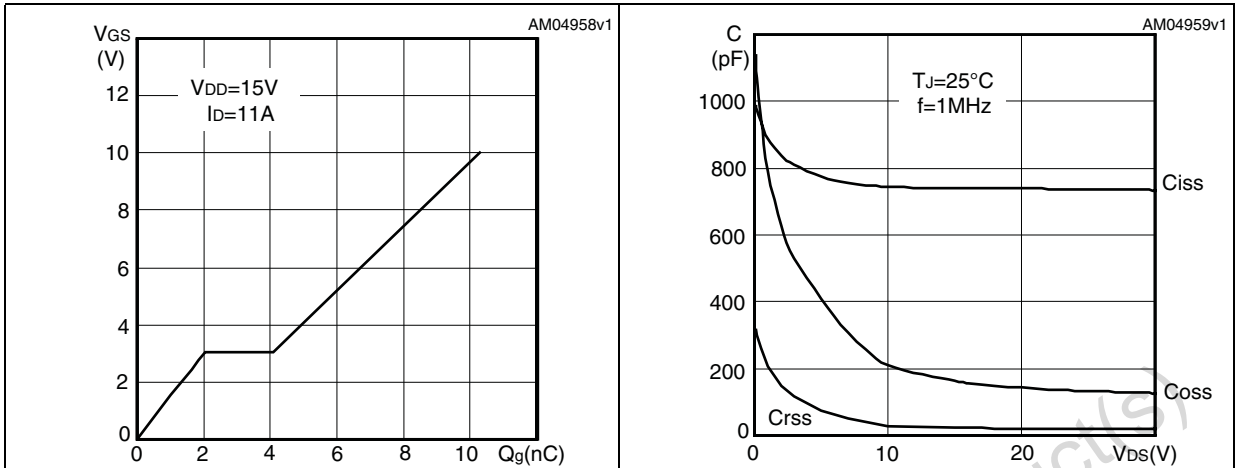


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

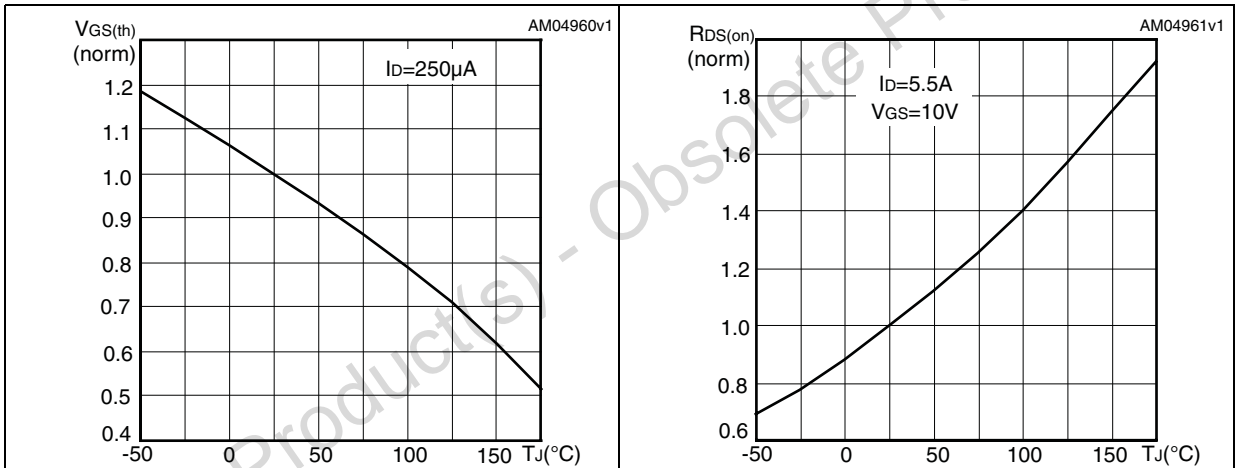
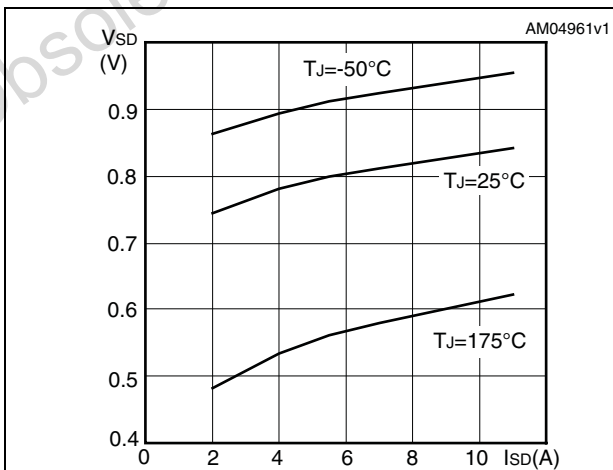
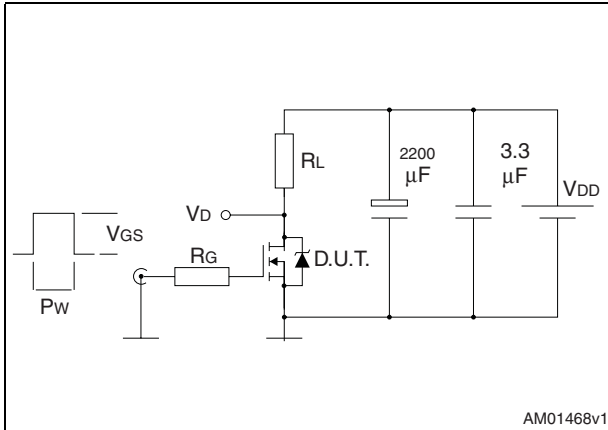


Figure 12. Source-drain diode forward characteristics



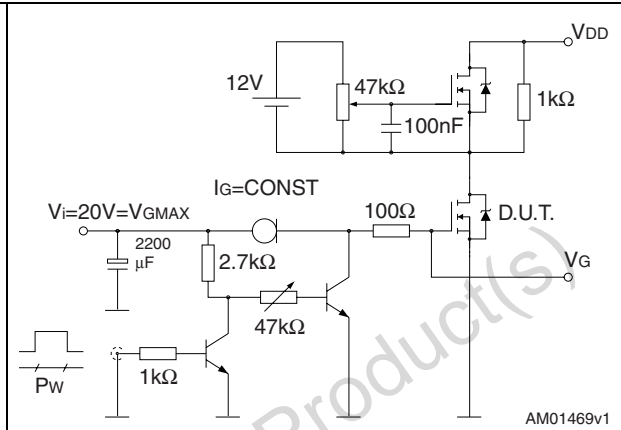
3 Test circuits

Figure 13. Switching times test circuit for resistive load



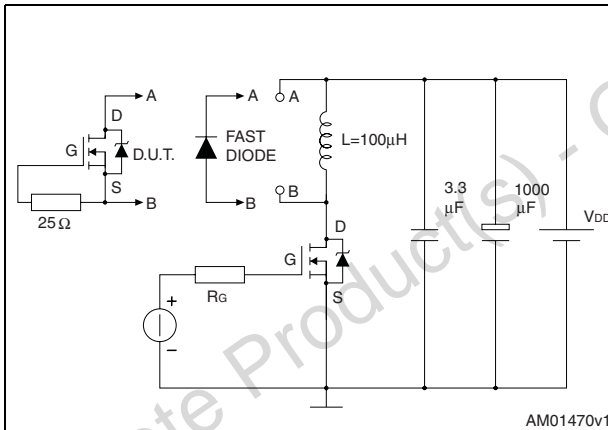
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Figure 14. Gate charge test circuit



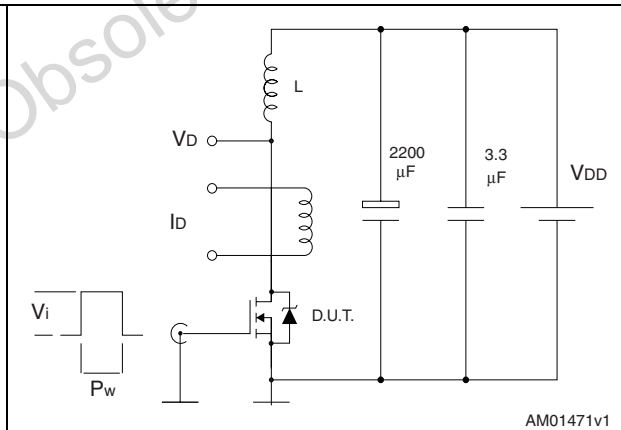
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Figure 15. Test circuit for inductive load switching and diode recovery times



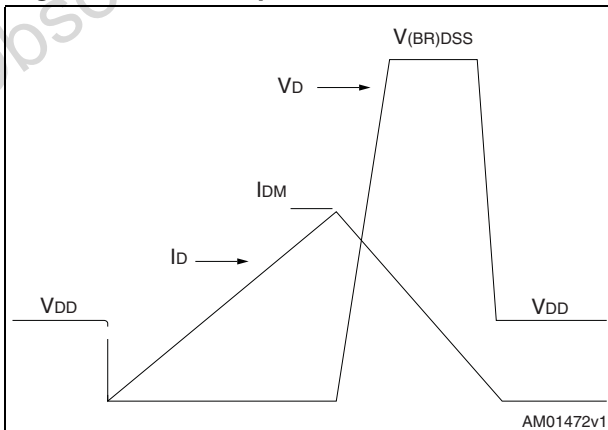
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Figure 16. Unclamped inductive load test circuit



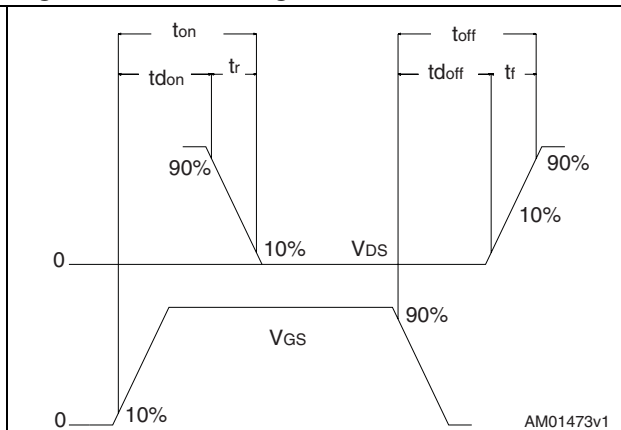
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Figure 17. Unclamped inductive waveform



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Figure 18. Switching time waveform



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4 Package mechanical data

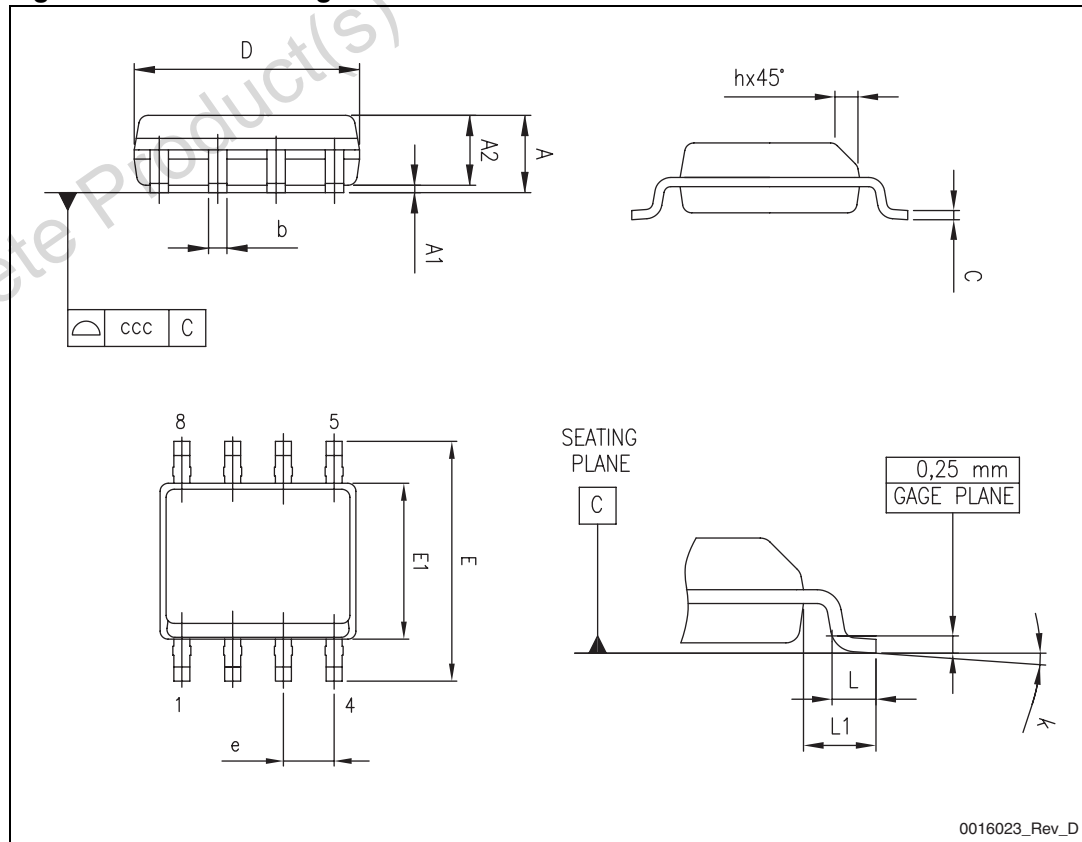
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Table 8. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

Figure 19. SO-8 drawing



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
02-Jul-2009	1	First release.
21-Jun-2011	2	New $R_{DS(on)}$ value. Updated mechanical data.

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