TS2007

3 W filter-free Class D audio power amplifer with 6-12 dB fixed gain select

Features

- Operating range from V_{CC} = 2.4 V to 5.5 V
- Standby mode active low
- Output power: 1.4 W at 5 V or 0.45 W at 3.0 V into 8 Ω with 1% THD+N max.
- Output power: 2.3 W at 5 V or 0.75 W at 3.0 V into 4 Ω with 1% THD+N max.
- Fixed gain select: 6 dB or 12 dB
- Low current consumption
- Efficiency: 88% typ.
- Signal-to-noise ratio: 94 dB typ.
- PSRR: 63 dB typ at 217 Hz with 6 dB gain
- PWM base frequency: 280 kHz
- Low pop & click noise
- Thermal shutdown protection
- DFN8 3 x 3 mm package

Applications

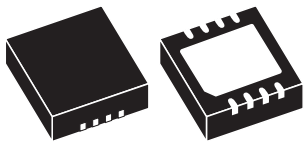
- Cellular phones
- PDAs
- Notebook PCs

Description

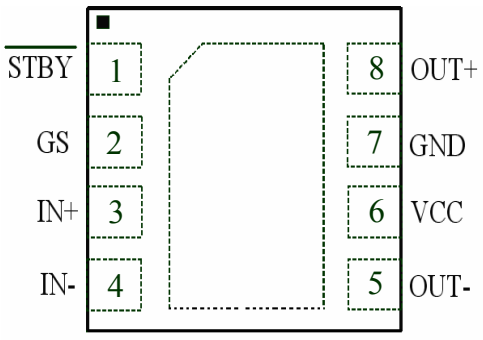
The TS2007 is a class D power audio amplifier. Able to drive up to 1.4 W into an 8 Ω load at 5 V, it achieves outstanding efficiency compared to typical class AB audio power amplifiers.

This device allows switching between two different gains: 6 or 12dB via a logic signal on the GS pin. A pop & click reduction circuitry provides low on/off switching noise while allowing the device to start within 5 ms. A standby function (active low) allows lowering the current consumption down to 10 nA typ.

TS2007IQT - DFN8



TS2007IQT - DFN8



The TS2007 is available in DFN8 3 x 3 mm lead-free packages.

Contents

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_i	Input voltage (2)	GND to V_{CC}	V
T_{oper}	Operating free air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient (3)	200	°C/W
Pd	Power dissipation	Internally limited(4)	
ESD	HBM: human body model	2	kV
ESD	MM: machine model	200	V
Latch-up	Latch-up immunity	Class A	
	Lead temperature (soldering, 10 sec)	260	°C
R_L	Minimum load resistor	3.2	Ω

1. All voltage values are measured with respect to the ground pin.
2. The magnitude of the input signal must never exceed V_{CC} + 0.3 V / GND - 0.3 V.
3. The device is protected in case of over temperature by a thermal shutdown active @ 150 °C.
4. Exceeding the power derating curves during a long period will cause abnormal operation.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.4 to 5.5	V
V_I	Input voltage range	GND to V_{CC}	V
V_{ic}	Input common mode voltage(1)	GND+0.15 V to V_{CC}-0.7 V	V
V_{STBY}	Standby voltage input (2) Device ON Device OFF	 $1.4 \leq V_{STBY} \leq V_{CC}$ $GND \leq V_{STBY} \leq 0.4$ (3)	V
GS	Gain select input: Gain =12dB Gain = 6dB	 $GND \leq V_{GS} \leq 0.4$ $1.4 \leq V_{GS} \leq V_{CC}$	V
R_L	Load resistor	≥ 4	Ω
R_{thja}	Thermal resistance junction to ambient (4)	40	°C/W

1. $I V_{oo} I \leq$ 35 mV max with both differential gains.
2. Without any signal on V_{STBY}, the device is in standby (internal 300 kΩ pull down resistor).
3. Minimum current consumption is obtained when V_{STBY} = GND.
4. When mounted on 4-layer PCB.

2 Typical application

Figure 1. Typical application schematics

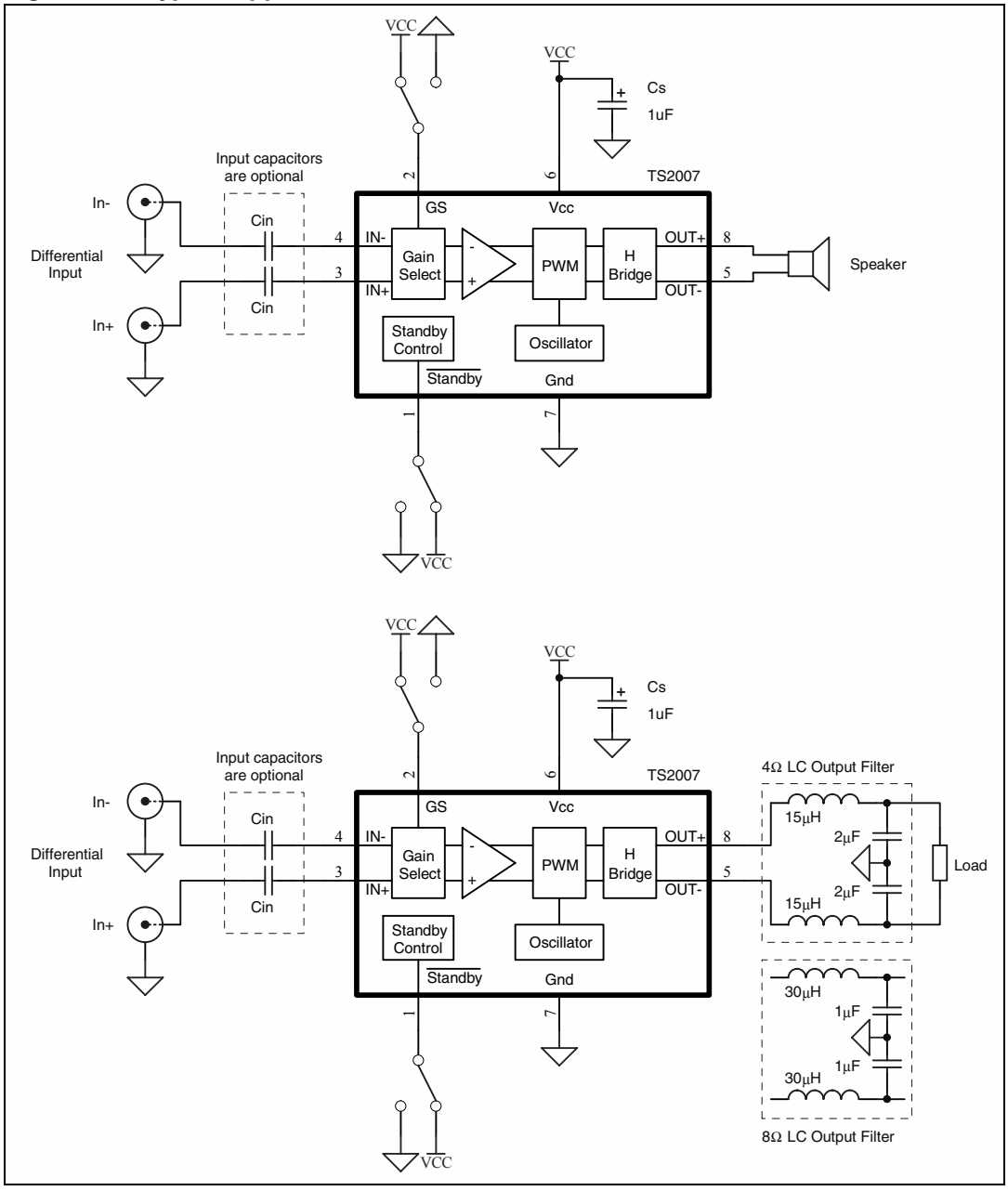


Table 3. External component descriptions

Components	Functional description
C_S	Supply capacitor that provides power supply filtering.
C_{in}	Input coupling capacitors (optional) that block the DC voltage at the amplifier input terminal. The capacitors also form a high pass filter with Z_{in} (F_{cl} = 1 / (2 x Pi x Z_{in} x C_{in})).

Table 4. Pin descriptions

Pin number	Pin name	Pin description
1	STBY	Standby pin (active low)
2	GS	Gain select input
3	IN+	Positive differential input
4	IN-	Negative differential input
5	OUT-	Negative differential output
6	VCC	Power supply
7	GND	Ground
8	OUT+	Positive differential output

3 Electrical characteristics

3.1 Electrical characteristic tables

Table 5. V_{CC} = +5 V, GND = 0 V, V_{ic}=2.5 V, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		2.3	3.3	mA
$I_{CC-STBY}$	Standby current (1) No input signal, V_{STBY} = GND		10	1000	nA
V_{oo}	Output offset voltage Floating inputs, R_L = 8Ω			25	mV
P_o	Output power THD = 1% max, f = 1 kHz, R_L = 4 Ω THD = 1% max, f = 1 kHz, R_L = 8 Ω THD = 10% max, f = 1 kHz, R_L = 4 Ω THD = 10% max, f = 1 kHz, R_L = 8 Ω		 2.3 1.4 2.8 1.7		W
THD + N	Total harmonic distortion + noise P_o = 1W_{RMS}, G = 6 dB, f =1 kHz, R_L = 8 Ω		0.4		%
Efficiency	Efficiency P_o = 2.1 W_{RMS}, R_L = 4 Ω (with LC output filter) P_o = 1.3 W_{RMS}, R_L = 8 Ω (with LC output filter)		 84 90		%
PSRR	Power supply rejection ratio with inputs grounded, C_{in}=1µF (2) f = 217 Hz, R_L = 8 Ω, Gain=6 dB,V_{ripple} = 200 mV_{pp} f = 217 Hz, R_L = 8 Ω, Gain=12 dB, V_{ripple} = 200 mV_{pp}		 63 60		dB
CMRR	Common mode rejection ratio 20 Hz < f < 20 kHz		60		dB
Gain	Gain value G_S =0 V G_S = V_{CC}	 11.5 5.5	 12 6	 12.5 6.5	dB
Z_{in}	Single input impedance (3)	68	75	82	kΩ
F_{PWM}	Pulse width modulator base frequency	190	280	370	kHz
SNR	Signal-to-noise ratio (A-weighting) Po=1.5 W, R_L=4 Ω (with LC output filter)		94		dB
t_{WU}	Wake-up time		5	10	ms

Table 5. V_{CC} = +5 V, GND = 0 V, V_{ic}=2.5 V, T_{amb} = 25 °C (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{STBY}	Standby time		5		ms
V_N	Output voltage noise f = 20 Hz to 20 kHz, R_L=4 Ω Unweighted (Filterless, G=6 dB) A-weighted (Filterless, G=6 dB) Unweighted (with LC output filter, G=6 dB) A-weighted (with LC output filter, G=6 dB) Unweighted (Filterless, G=12 dB) A-weighted (Filterless, G=12 dB) Unweighted (with LC output filter, G=12 dB) A-weighted (with LC output filter, G=12 dB)		 74 50 69 49 94 65 86 64		μV_{RMS}

1. Standby mode is active when V_{STBY} is tied to GND.
2. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinus signal to V_{CC} @ f = 217Hz.
3. Independent of Gain configuration (6 or 12 dB) and between IN+ or IN- and GND.

Table 6. V_{CC} = +4.2 V, GND = 0 V, V_{ic}=2.1 V, T_{amb} = 25 °C (unless otherwise specified)(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		2.1	3	mA
$I_{CC-STBY}$	Standby current (2) No input signal, V_{STBY} = GND		10	1000	nA
V_{oo}	Output offset voltage Floating inputs, R_L = 8 Ω			25	mV
P_o	Output power THD = 1% max, f = 1 kHz, R_L = 4 Ω THD = 1% max, f = 1 kHz, R_L = 8 Ω THD = 10% max, f = 1 kHz, R_L = 4 Ω THD = 10% max, f = 1 kHz, R_L = 8 Ω		 1.6 0.95 1.95 1.1		W
THD + N	Total harmonic distortion + noise P_o = 800 mW_{RMS}, G = 6 dB, f =1 kHz, R_L = 8 Ω		0.45		%
Efficiency	Efficiency P_o = 1.5 W_{RMS}, R_L = 4 Ω (with LC output filter) P_o = 0.95 W_{RMS}, R_L = 8 Ω (with LC output filter)		 85 90		%
PSRR	Power supply rejection ratio with inputs grounded, C_{in} = 1 µF (3) f = 217 Hz, R_L = 8 Ω, Gain = 6 dB,V_{ripple} = 200 mV_{pp} f = 217 Hz, R_L = 8 Ω, Gain = 12 dB, V_{ripple} = 200 mV_{pp}		 63 60		dB
CMRR	Common mode rejection ratio 20 Hz < f < 20 kHz		60		dB
Gain	Gain value G_S = 0 V G_S = V_{CC}	 11.5 5.5	 12 6	 12.5 6.5	dB
Z_{in}	Single input impedance (4)	68	75	82	kΩ
F_{PWM}	Pulse width modulator base frequency	190	280	370	kHz
SNR	Signal-to-noise ratio (A-weighting) Po=1.2 W, R_L=4 Ω (with LC output filter)		93		dB
t_{WU}	Wake-up time		5	10	ms
t_{STBY}	Standby time		5		ms
V_N	Output voltage noise f = 20 Hz to 20 kHz, R_L=4 Ω Unweighted (Filterless, G=6 dB) A-weighted (Filterless, G=6 dB) Unweighted (with LC output filter, G=6 dB) A-weighted (with LC output filter, G=6 dB) Unweighted (Filterless, G=12 dB) A-weighted (Filterless, G=12 dB) Unweighted (with LC output filter, G=12 dB) A-weighted (with LC output filter, G=12 dB)		 72 50 68 49 93 65 85 64		μV_{RMS}

1. All electrical values are guaranteed with correlation measurements at 2.4 V and 5 V.
2. Standby mode is active when V_{STBY} is tied to GND.
3. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinus signal to V_{CC} @ f = 217 Hz.
4. Independent of Gain configuration (6 or 12 dB) and between IN+ or IN- and GND.

Table 7. V_{CC} = +3.6 V, GND = 0 V, V_{ic}=1.8 V, T_{amb} = 25 °C (unless otherwise specified)(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		2	2.8	mA
$I_{CC-STBY}$	Standby current (2) No input signal, V_{STBY} = GND		10	1000	nA
V_{oo}	Output offset voltage Floating inputs, R_L = 8 Ω			25	mV
P_o	Output power THD+N = 1% max, f = 1 kHz, R_L = 4 Ω THD+N = 1% max, f = 1 kHz, R_L = 8 Ω THD = 10% max, f = 1 kHz, R_L = 4 Ω THD = 10% max, f = 1 kHz, R_L = 8 Ω		1.1 0.65 1.4 0.85		W
THD + N	Total harmonic distortion + noise P_o = 500 mW_{RMS}, G = 6 dB, f = 1 kHz, R_L = 8 Ω		0.3		%
Efficiency	Efficiency P_o = 1.1 W_{RMS}, R_L = 4 Ω (with LC output filter) P_o = 0.65 W_{RMS}, R_L = 8 Ω (with LC output filter)		84 90		%
PSRR	Power supply rejection ratio with inputs grounded, C_{in}=1 µF (3) f = 217 Hz, R_L = 8 Ω, Gain = 6 dB, V_{ripple} = 200 mV_{pp} f = 217 Hz, R_L = 8 Ω, Gain = 12 dB, V_{ripple} = 200 mV_{pp}		63 60		dB
CMRR	Common mode rejection ratio 20 Hz < f < 20 kHz		60		dB
Gain	Gain value G_S = 0 V G_S = V_{CC}	11.5 5.5	12 6	12.5 6.5	dB
Z_{in}	Single input impedance (4)	68	75	82	kΩ
F_{PWM}	Pulse width modulator base frequency	190	280	370	kHz
SNR	Signal-to-noise ratio (A-weighting) Po = 0.9 W, R_L = 4 Ω (with LC output filter)		92		dB
t_{WU}	Wake-up time		5	10	ms
t_{STBY}	Standby time		5		ms
V_N	Output voltage noise f = 20 Hz to 20 kHz, R_L=4 Ω Unweighted (Filterless, G=6 dB) A-weighted (Filterless, G=6 dB) Unweighted (with LC output filter, G=6 dB) A-weighted (with LC output filter, G=6 dB) Unweighted (Filterless, G=12 dB) A-weighted (Filterless, G=12 dB) Unweighted (with LC output filter, G=12 dB) A-weighted (with LC output filter, G=12 dB)		72 50 68 49 93 65 85 64		μV_{RMS}

1. All electrical values are guaranteed with correlation measurements at 2.4 V and 5 V.
2. Standby mode is active when V_{STBY} is tied to GND.
3. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinus signal to V_{CC} @ f = 217 Hz.
4. Independent of Gain configuration (6 or 12 dB) and between IN+ or IN- and GND.

Table 8. V_{CC} = +3.0 V, GND = 0 V, V_{ic}=1.5 V, T_{amb} = 25 °C (unless otherwise specified)(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		1.9	2.7	mA
$I_{CC-STBY}$	Standby current (2) No input signal, V_{STBY} = GND		10	1000	nA
V_{oo}	Output offset voltage Floating inputs, R_L = 8 Ω			25	mV
P_o	Output power THD+N = 1% Max, f = 1 kHz, R_L = 4 Ω THD+N = 1% Max, f = 1 kHz, R_L = 8 Ω THD = 10% Max, f = 1 kHz, R_L = 4 Ω THD = 10% Max, f = 1 kHz, R_L = 8 Ω		0.75 0.45 1 0.6		W
THD + N	Total harmonic distortion + noise P_o = 400 mW_{RMS}, G = 6 dB, f = 1 kHz, R_L = 8 Ω		0.5		%
Efficiency	Efficiency P_o = 0.75 W_{RMS}, R_L = 4 Ω (with LC output filter) P_o = 0.45 W_{RMS}, R_L = 8 Ω (with LC output filter)		83 90		%
PSRR	Power supply rejection ratio with inputs grounded, C_{in} = 1 µF (3) f = 217 Hz, R_L = 8 Ω, Gain=6 dB,V_{ripple} = 200 mV_{pp} f = 217 Hz, R_L = 8 Ω, Gain=12 dB, V_{ripple} = 200 mV_{pp}		63 60		dB
CMRR	Common mode rejection ratio 20 Hz < f < 20 kHz		60		dB
Gain	Gain value G_S = 0 V G_S = V_{CC}	11.5 5.5	12 6	12.5 6.5	dB
Z_{in}	Single input impedance (4)	68	75	82	kΩ
F_{PWM}	Pulse width modulator base frequency	190	280	370	kHz
SNR	Signal-to-noise ratio (A-weighting) Po = 0.6 W, R_L = 4 Ω (with LC output filter)		90		dB
t_{WU}	Wake-up time		5	10	ms
t_{STBY}	Standby time		5		ms
V_N	Output voltage noise f = 20 Hz to 20 kHz, R_L=4 Ω Unweighted (Filterless, G=6 dB) A-weighted (Filterless, G=6 dB) Unweighted (with LC output filter, G=6 dB) A-weighted (with LC output filter, G=6 dB) Unweighted (Filterless, G=12 dB) A-weighted (Filterless, G=12 dB) Unweighted (with LC output filter, G=12 dB) A-weighted (with LC output filter, G=12 dB)		 71 50 67 49 92 65 85 64		μV_{RMS}

1. All electrical values are guaranteed with correlation measurements at 2.4 V and 5 V.
2. Standby mode is active when V_{STBY} is tied to GND.
3. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinus signal to V_{CC} @ f = 217 Hz.
4. Independent of Gain configuration (6 or 12 dB) and between IN+ or IN- and GND.

Table 9. V_{CC} = +2.4 V, GND = 0 V, V_{ic}=1.2 V, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		1.7	2.4	mA
$I_{CC-STBY}$	Standby current (1) No input signal, V_{STBY} = GND		10	1000	nA
V_{oo}	Output offset voltage Floating inputs, R_L = 8 Ω			25	mV
P_o	Output power THD+N = 1% Max, f = 1 kHz, R_L = 4 Ω THD+N = 1% Max, f = 1 kHz, R_L = 8 Ω THD = 10% Max, f = 1 kHz, R_L = 4 Ω THD = 10% Max, f = 1 kHz, R_L = 8 Ω		 0.48 0.3 0.6 0.36		W
THD + N	Total harmonic distortion + noise P_o = 200 mW_{RMS}, G = 6 dB, f = 1 kHz, R_L = 8 Ω		0.1		%
Efficiency	Efficiency P_o = 0.38 W_{RMS}, R_L = 4 Ω (with LC output filter) P_o = 0.25 W_{RMS}, R_L = 8 Ω (with LC output filter)		 82 90		%
PSRR	Power supply rejection ratio with inputs grounded, C_{in} = 1 µF (2) f = 217 Hz, R_L = 8 Ω, Gain=6 dB,V_{ripple} = 200 mV_{pp} f = 217 Hz, R_L = 8 Ω, Gain=12 dB, V_{ripple} = 200 mV_{pp}		 63 60		dB
CMRR	Common mode rejection ratio 20 Hz < f < 20 kHz		60		dB
Gain	Gain value G_S = 0 V G_S = V_{CC}	 11.5 5.5	 12 6	 12.5 6.5	dB
Z_{in}	Single input impedance (3)	68	75	82	kΩ
F_{PWM}	Pulse width modulator base frequency	190	280	370	kHz
SNR	Signal-to-noise ratio (A-weighting) Po=0.4 W, R_L=4 Ω (with LC output filter)		88		dB
t_{WU}	Wake-up time		5	10	ms
t_{STBY}	Standby time		5		ms
V_N	Output voltage noise f = 20 Hz to 20 kHz, R_L = 4 Ω Unweighted (filterless, G=6 dB) A-weighted (filterless, G=6 dB) Unweighted (with LC output filter, G=6 dB) A-weighted (with LC output filter, G=6 dB) Unweighted (filterless, G=12 dB) A-weighted (filterless, G=12 dB) Unweighted (with LC output filter, G=12 dB) A-weighted (with LC output filter, G=12 dB)		 70 50 66 49 91 65 84 64		μV_{RMS}

1. Standby mode is active when V_{STBY} is tied to GND.
2. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinus signal to V_{CC} @ f = 217 Hz.
3. Independent of Gain configuration (6 or 12 dB) and between IN+ or IN- and GND.

3.2 Electrical characteristic curves

The graphs shown in this section use the following abbreviations:

- R_L+ 15 µH or 30 µH = pure resistor + very low series resistance inductor
- Filter = LC output filter (1 µF+30 µH for 4 Ω and 0.5 µF+60 µH for 8 Ω)

All measurements are done with C_{S1}=1 µF and C_{S2}=100 nF (see *Figure 2*, except for the PSRR where C_{S1} is removed (see *Figure 3*).

Figure 2. Test diagram for measurements

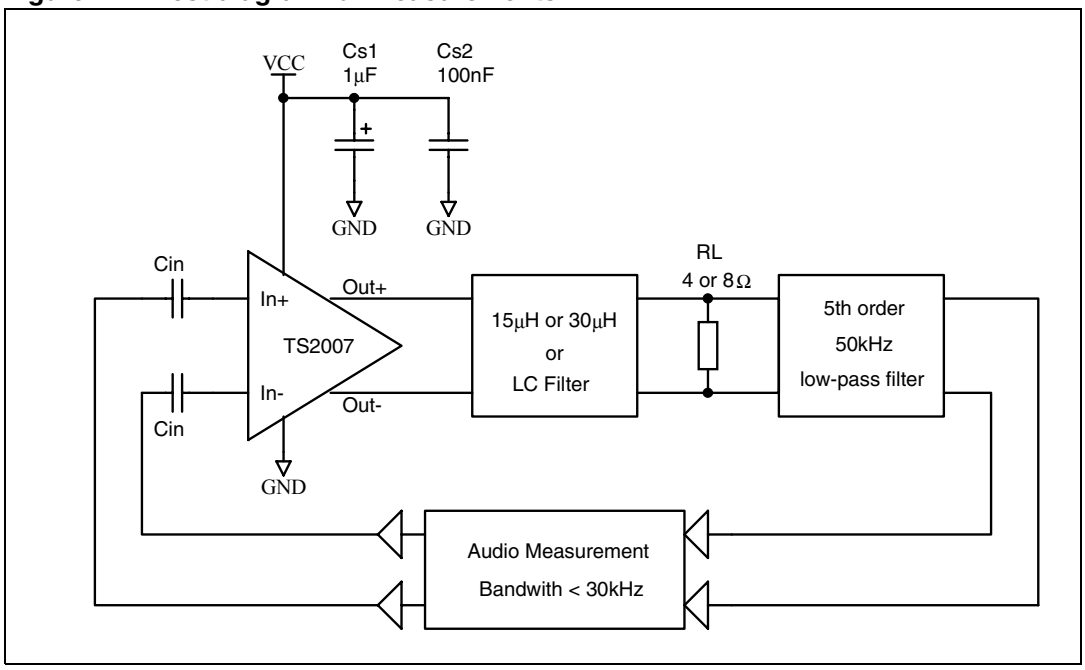


Figure 3. Test diagram for PSRR measurements

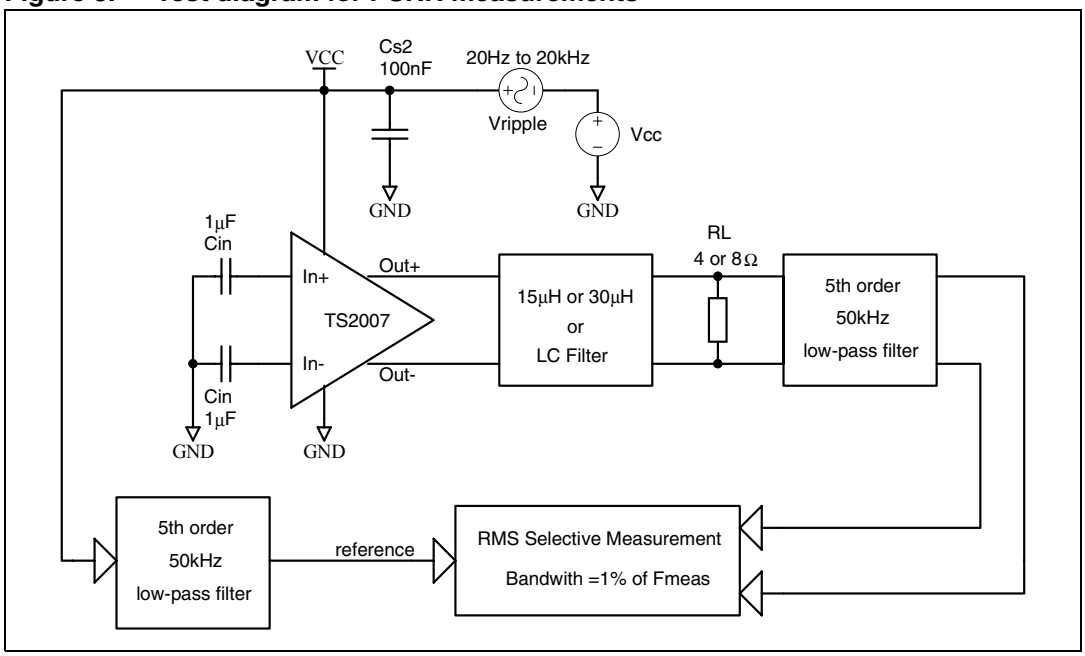


Table 10. Index of graphics

Description	Figure
Current consumption vs. power supply voltage	*Figure 4*
Current consumption vs. standby voltage	*Figure 5*
Efficiency vs. output power	*Figure 6* - *Figure 9*
Output power vs. power supply voltage	*Figure 10*, *Figure 11*
PSRR vs. common mode input voltage	*Figure 12*
PSRR vs. frequency	*Figure 13* - *Figure 17*
CMRR vs. common mode input voltage	*Figure 18*
CMRR vs. frequency	*Figure 19* - *Figure 23*
Gain vs. frequency	*Figure 24*, *Figure 25*
THD+N vs. output power	*Figure 26* - *Figure 33*
THD+N vs. frequency	*Figure 34* - *Figure 45*
Power derating curves	*Figure 46*
Startup and shutdown time	*Figure 47* - *Figure 49*

Figure 4. Current consumption vs. power supply voltage

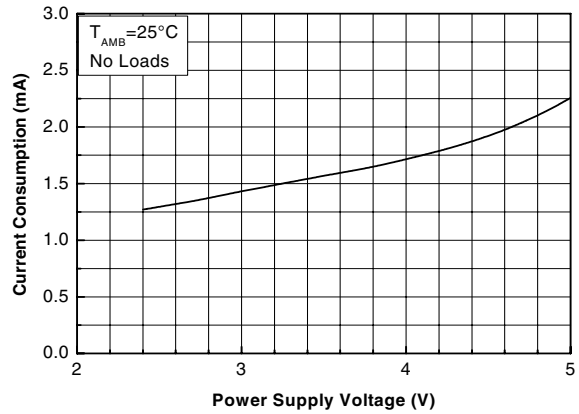


Figure 5. Current consumption vs. standby voltage

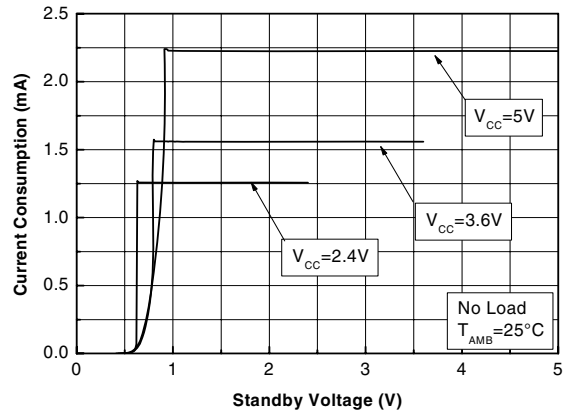


Figure 6. Efficiency vs. output power

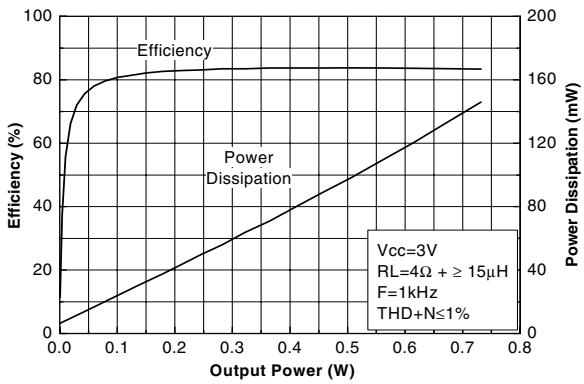


Figure 7. Efficiency vs. output power

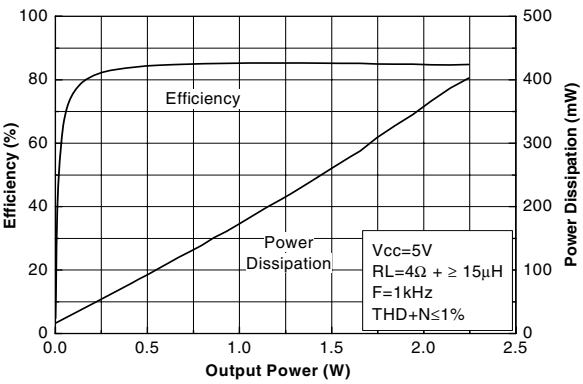


Figure 8. Efficiency vs. output power

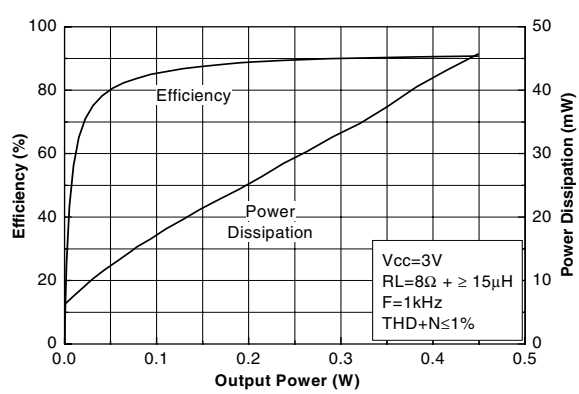


Figure 9. Efficiency vs. output power

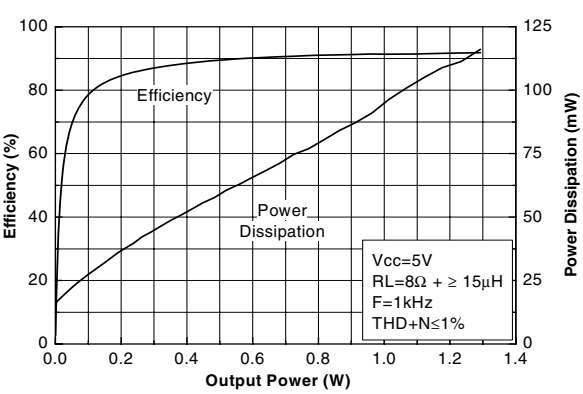


Figure 10. Output power vs. power supply voltage

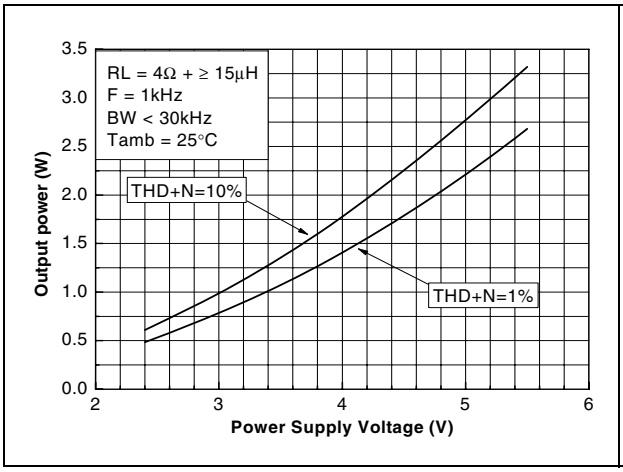


Figure 11. Output power vs. power supply voltage

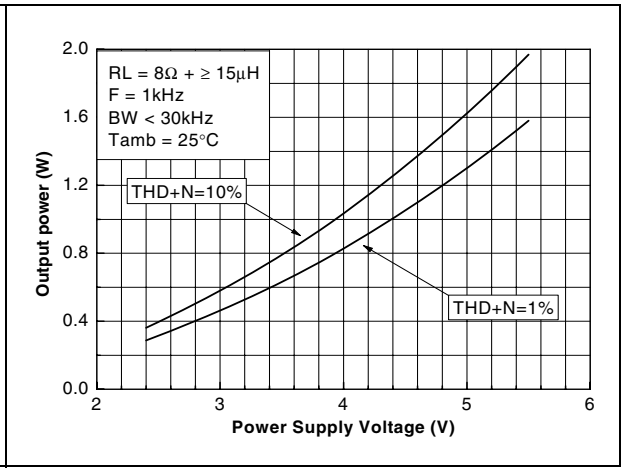


Figure 12. PSRR vs. common mode input voltage

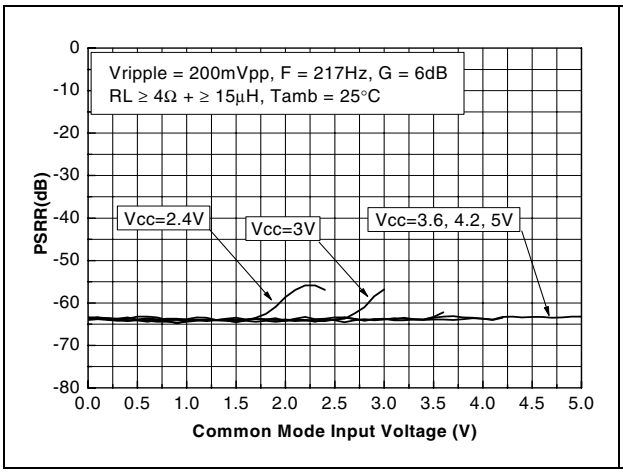


Figure 13. PSRR vs. frequency

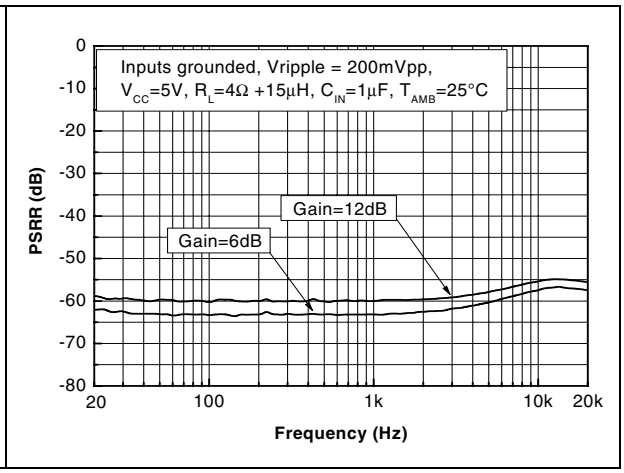


Figure 14. PSRR vs. frequency

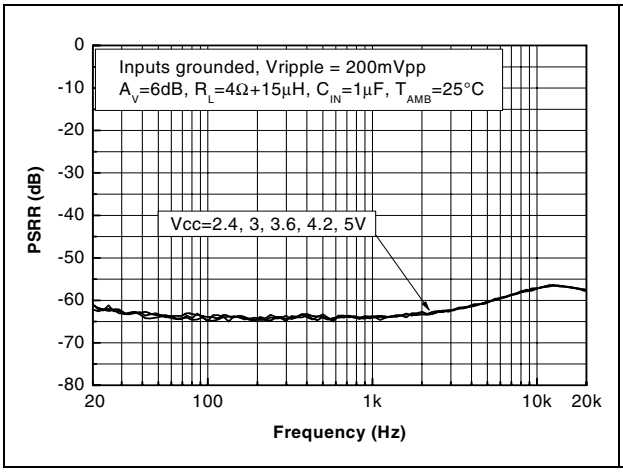


Figure 15. PSRR vs. frequency

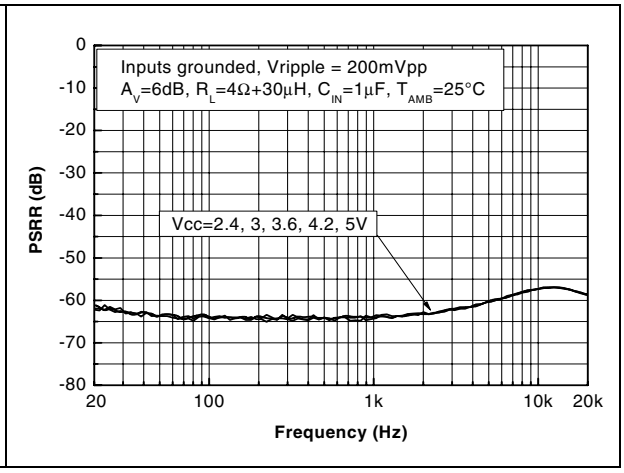


Figure 16. PSRR vs. frequency

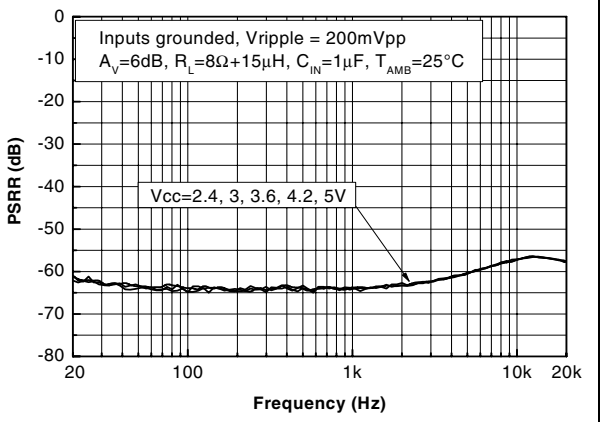


Figure 17. PSRR vs. frequency

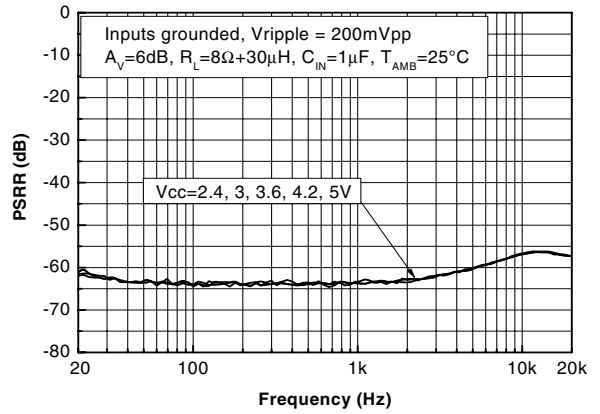


Figure 18. CMRR vs. common mode input voltage

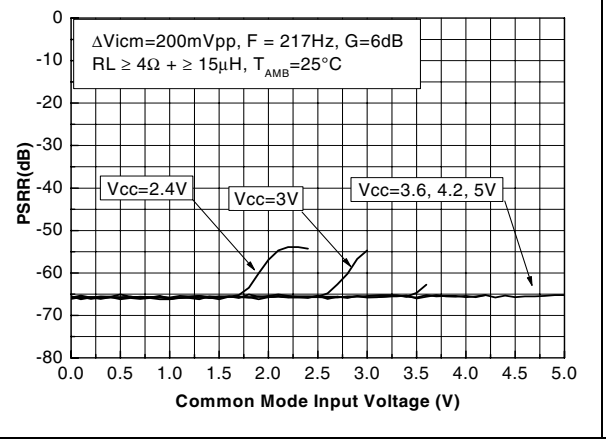


Figure 19. CMRR vs. frequency

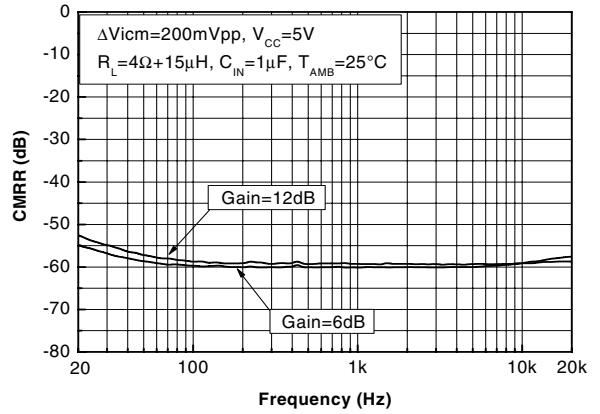


Figure 20. CMRR vs. frequency

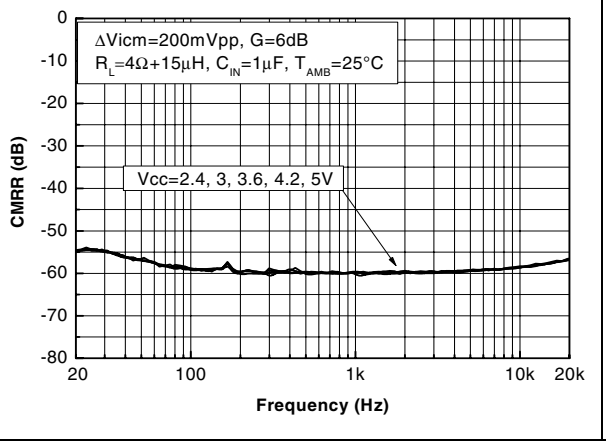


Figure 21. CMRR vs. frequency

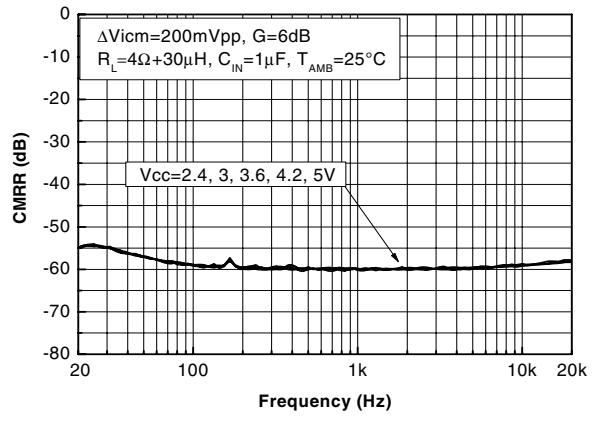


Figure 22. CMRR vs. frequency

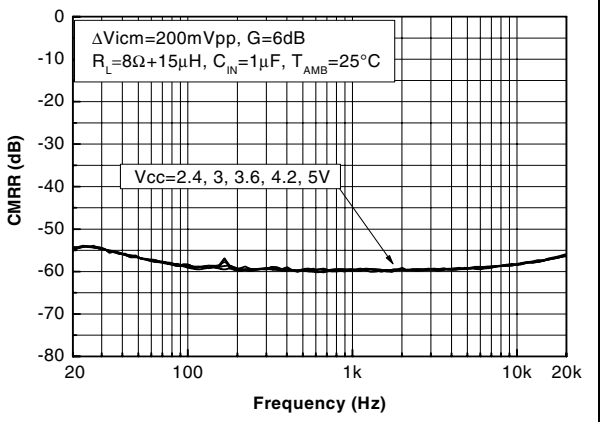


Figure 23. CMRR vs. frequency

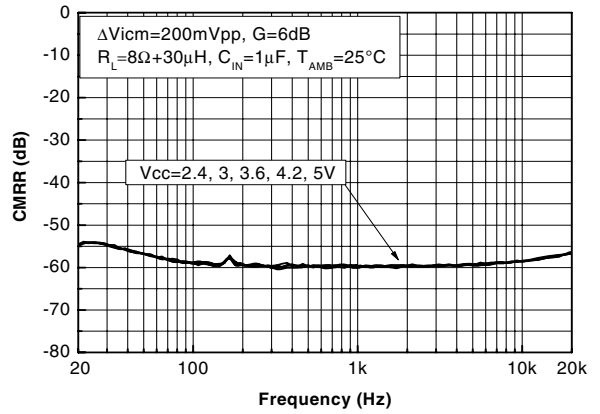


Figure 24. Gain vs. frequency

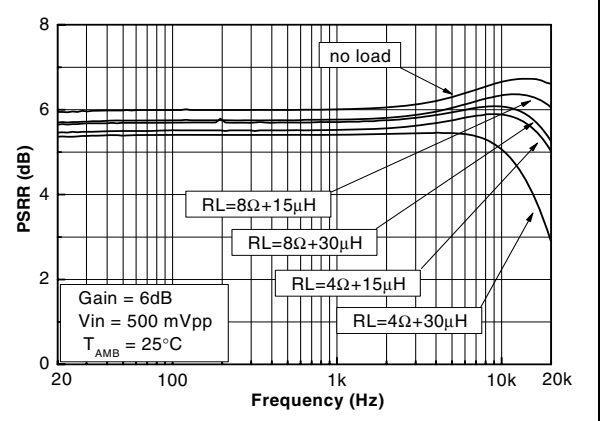


Figure 25. Gain vs. frequency

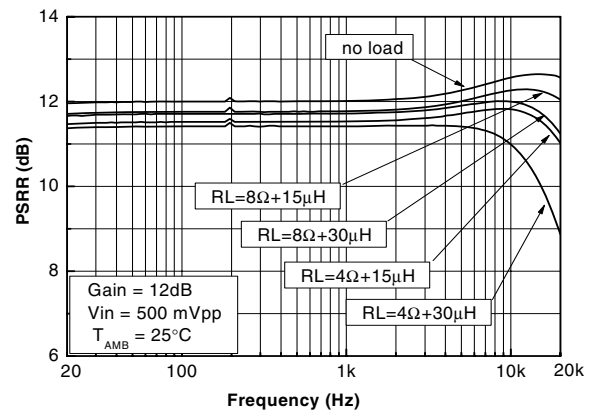


Figure 26. THD+N vs. output power

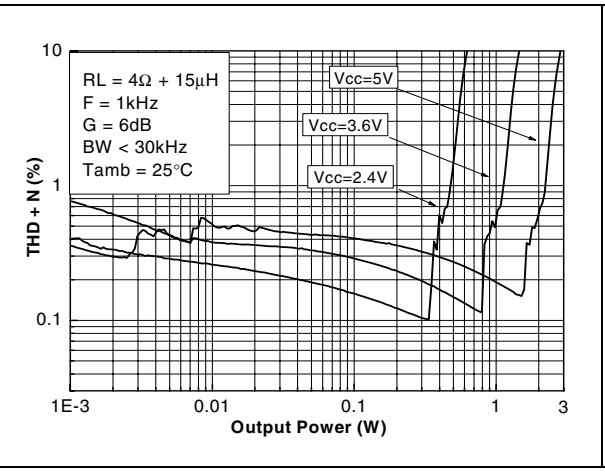


Figure 27. THD+N vs. output power

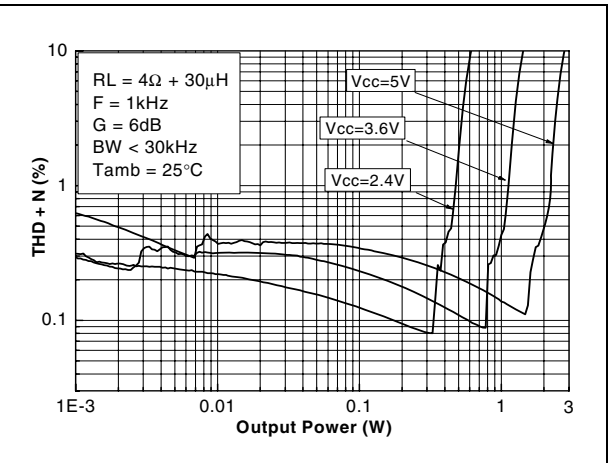


Figure 28. THD+N vs. output power

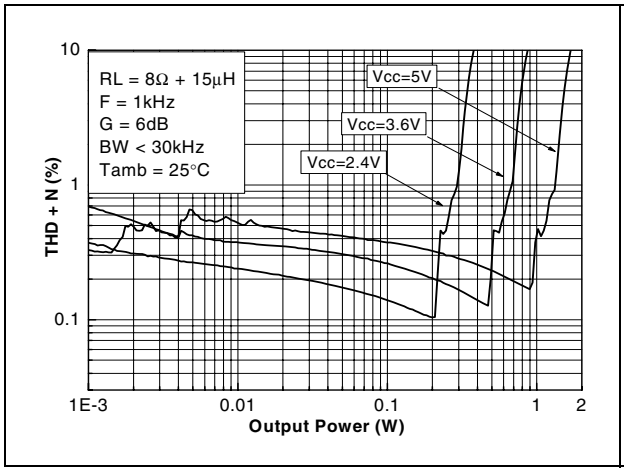


Figure 29. THD+N vs. output power

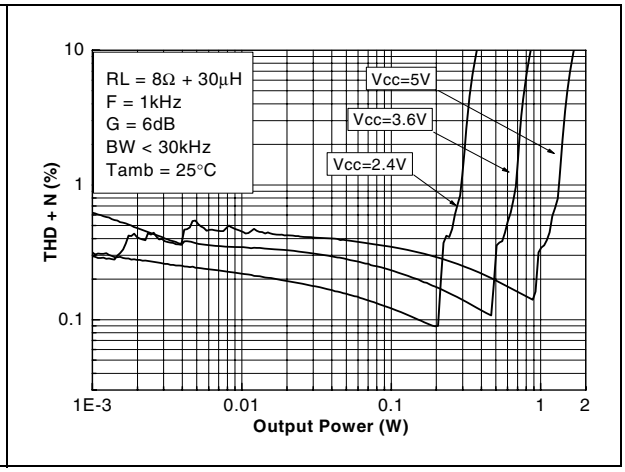


Figure 30. THD+N vs. output power

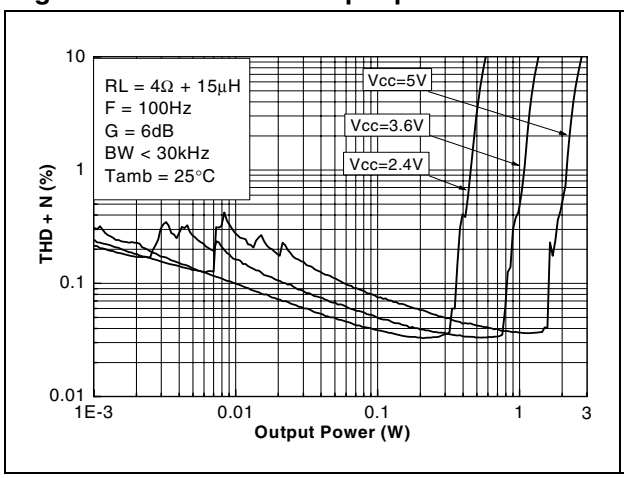


Figure 31. THD+N vs. output power

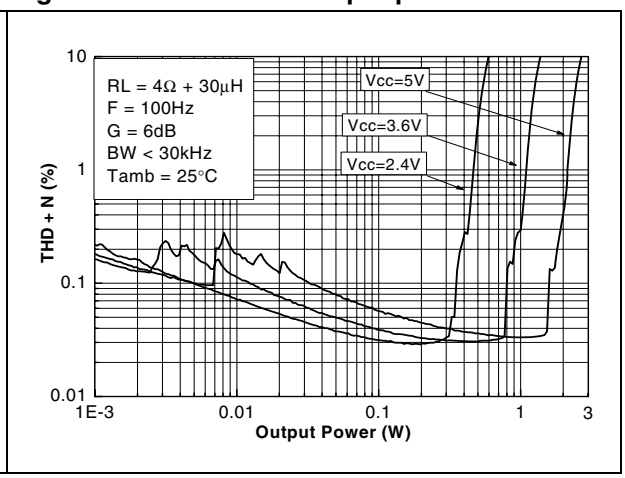


Figure 32. THD+N vs. output power

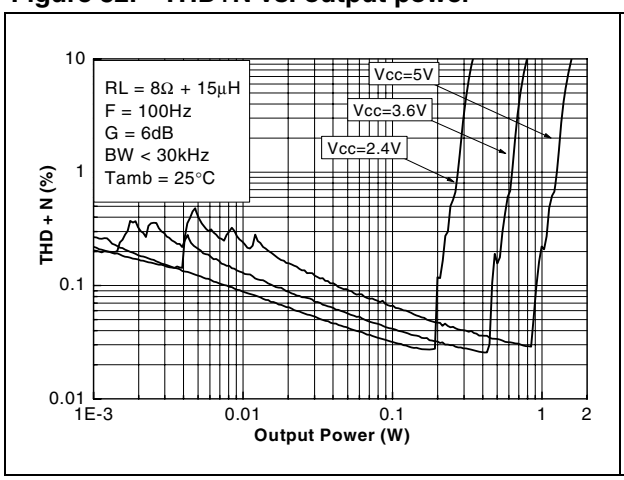


Figure 33. THD+N vs. output power

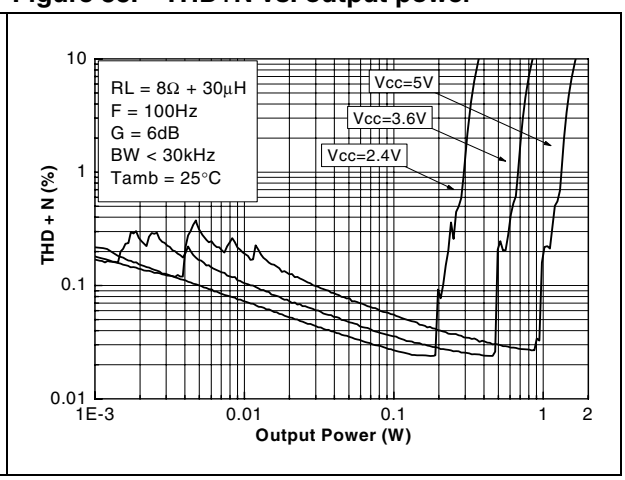


Figure 34. THD+N vs. frequency

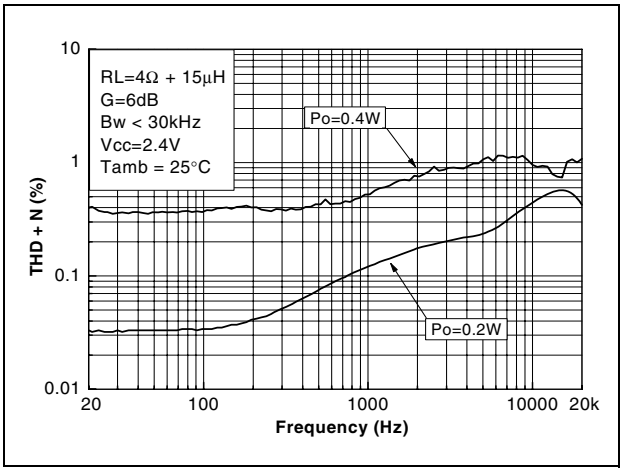


Figure 35. THD+N vs. frequency

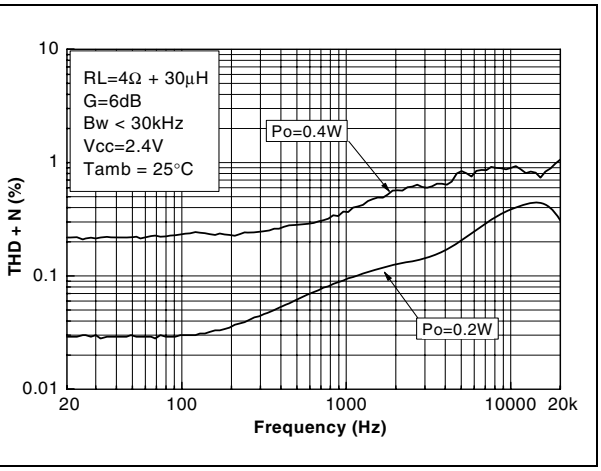


Figure 36. THD+N vs. frequency

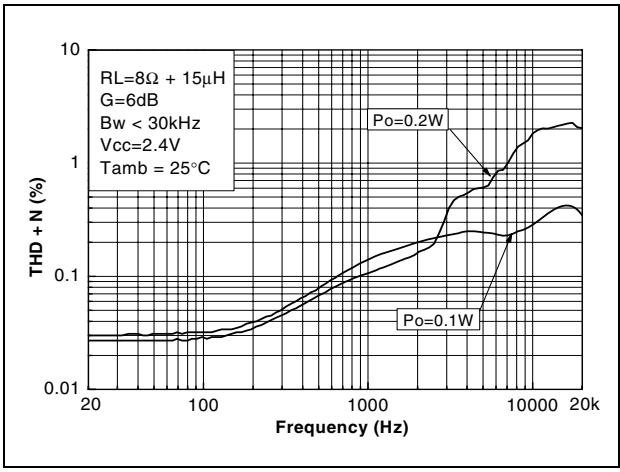


Figure 37. THD+N vs. frequency

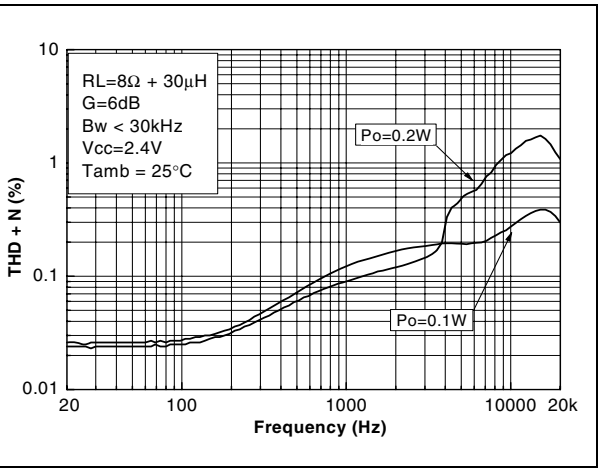


Figure 38. THD+N vs. frequency

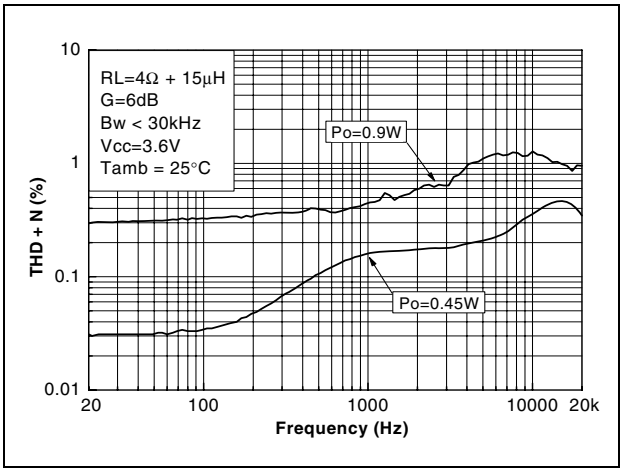


Figure 39. THD+N vs. frequency

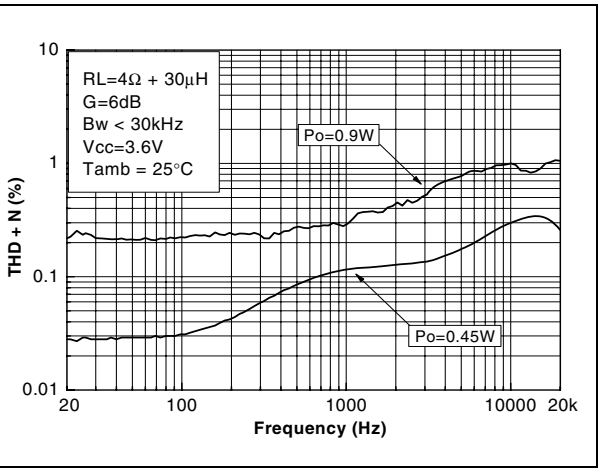


Figure 40. THD+N vs. frequency

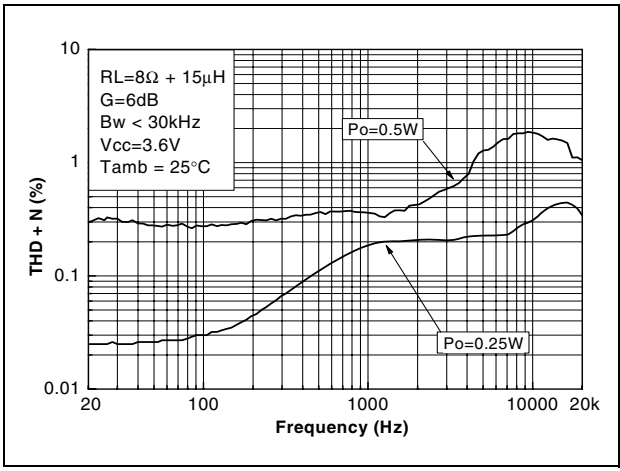


Figure 41. THD+N vs. frequency

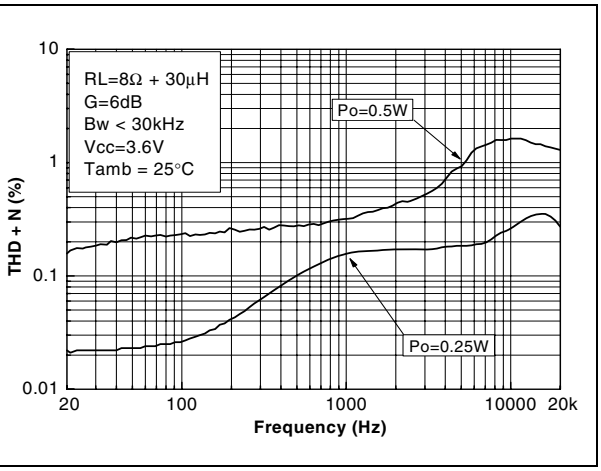


Figure 42. THD+N vs. frequency

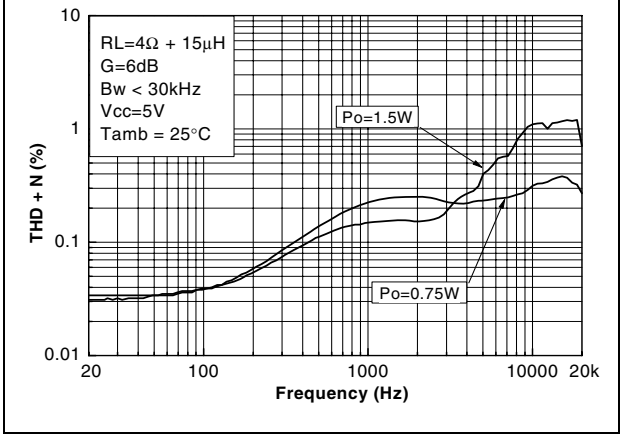


Figure 43. THD+N vs. frequency

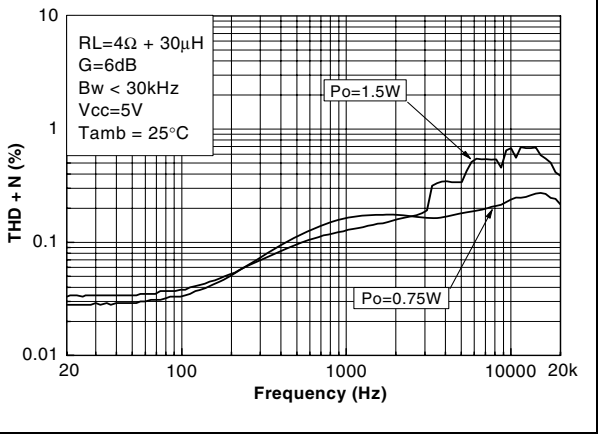


Figure 44. THD+N vs. frequency

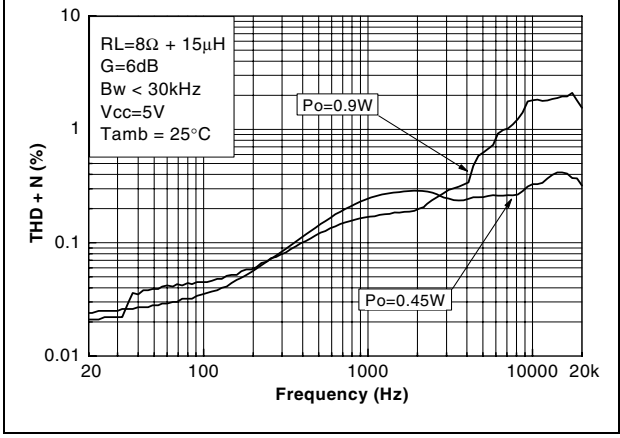


Figure 45. THD+N vs. frequency

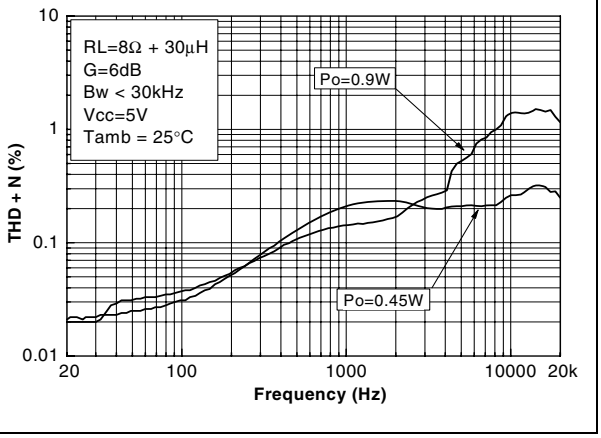


Figure 46. Power derating curves

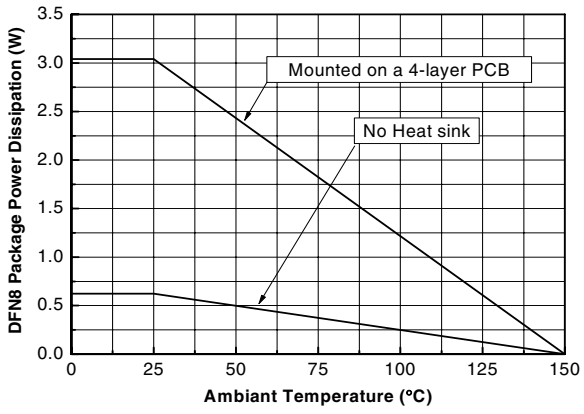


Figure 47. Startup and shutdown phase V_{CC}=5 V, G=6 dB, C_{in}=1 µF, inputs grounded

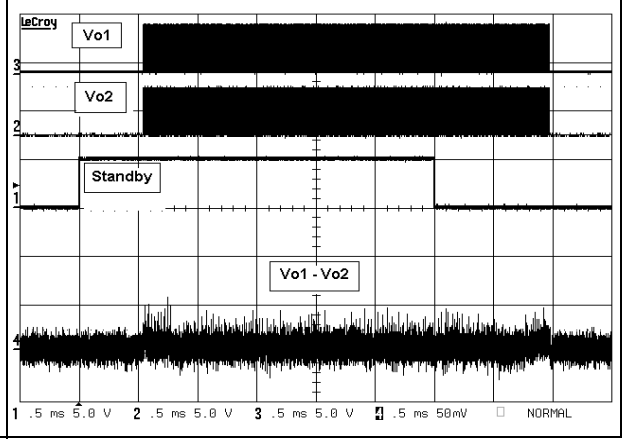


Figure 48. Startup and shutdown phase V_{CC}=5 V, G=6 dB, C_{in}=1 µF, V_{in}=1 V_{pp}, F=10 kHz

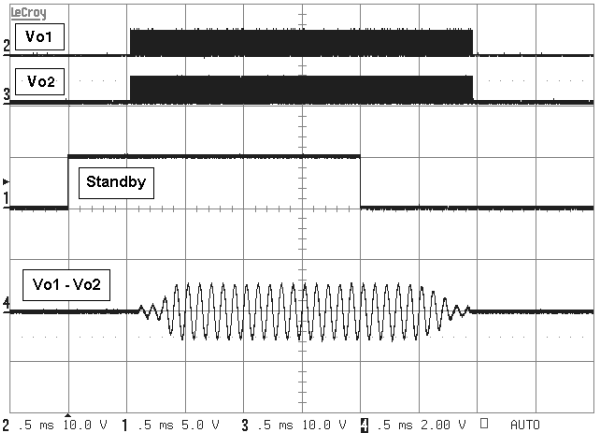
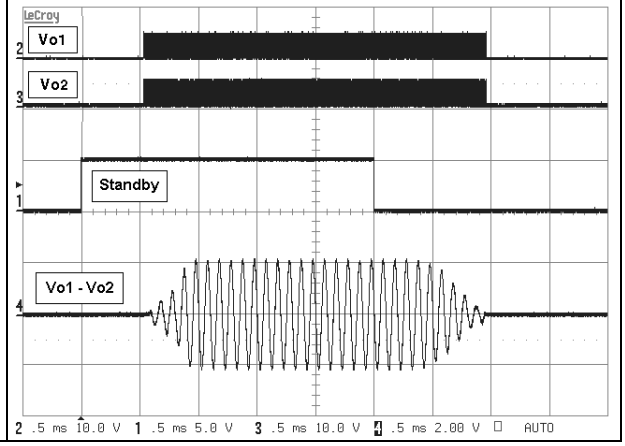


Figure 49. Startup and shutdown phase V_{CC}=5 V, G=12 dB, C_{in}=1 µF, V_{in}=1 V_{pp}, F=10 kHz



4 Application information

4.1 Differential configuration principle

The TS2007 is a monolithic fully-differential input/output class D power amplifier. The TS2007 also includes a common-mode feedback loop that controls the output bias value to average it at $V_{CC}/2$ for any DC common-mode input voltage. This allows the device to always have a maximum output voltage swing, and by consequence, maximize the output power. Moreover, as the load is connected differentially compared to a single-ended topology, the output is four times higher for the same power supply voltage.

The **advantages** of a full-differential amplifier are:

- High PSRR (power supply rejection ratio)
- High common-mode noise rejection
- Virtually zero pop without additional circuitry, giving a faster startup time compared to conventional single-ended input amplifiers
- Easier interfacing with differential output audio DAC
- No input coupling capacitors required thanks to common-mode feedback loop

4.2 Gain settings

In the flat region of the frequency-response curve (no input coupling capacitor or internal feedback loop + load effect), the differential gain can be set to either 6 or 12 dB depending on the logic level of the GS pin:

GS	Gain (dB)	Gain (V/V)
1	6 dB	2
0	12 dB	4

Note: Between the GS pin and V_{CC} there is an internal 300 kΩ resistor. When the pin is floating the gain is 6 dB.

4.3 Common-mode feedback loop limitations

As explained previously, the common-mode feedback loop allows the output DC bias voltage to be averaged at $V_{CC}/2$ for any DC common-mode bias input voltage.

Due to the V_{ic} limitation of the input stage (see *Table 2: Operating conditions on page 3*), the common-mode feedback loop can fulfill its role only within the defined range.

4.4 Low frequency response

If a low frequency bandwidth limitation is required, it is possible to use input coupling capacitors. In the low frequency region, the input coupling capacitor C_{in} starts to have an effect. C_{in} forms, with the input impedance Z_{in}, a first order high-pass filter with a -3 dB cutoff frequency (see *Table 5* to *Table 9*).

$$F_{CL} = \frac{1}{2 \cdot \pi \cdot Z_{in} \cdot C_{in}}$$

So, for a desired cutoff frequency F_{CL} we can calculate C_{in}:

$$C_{in} = \frac{1}{2 \cdot \pi \cdot Z_{in} \cdot F_{CL}}$$

with F_{CL} in Hz, Z_{in} in Ω and C_{in} in F.

The input impedance Z_{in} is for the whole power supply voltage range, typically 75 kΩ. There is also a tolerance around the typical value (see *Table 5* to *Table 9*). With regard to the tolerance, you can also calculate tolerance of F_{CL}:

- $F_{CLmax} = 1.103 \cdot F_{CL}$
- $F_{CLmin} = 0.915 \cdot F_{CL}$

4.5 Decoupling of the circuit

A power supply capacitor, referred to as C_S, is needed to correctly bypass the TS2007.

The TS2007 has a typical switching frequency of 280 kHz and output fall and rise time of about 5 ns. Due to these very fast transients, careful decoupling is mandatory.

A 1 µF ceramic capacitor is enough, but it must be located very close to the TS2007 in order to avoid any extra parasitic inductance created by a long track wire. Parasitic loop inductance, in relation with di/dt, introduces overvoltage that decreases the global efficiency of the device and may cause, if this parasitic inductance is too high, a TS2007 breakdown.

In addition, even if a ceramic capacitor has an adequate high frequency ESR value, its current capability is also important. A 0603 size is a good compromise, particularly when a 4 Ω load is used.

Another important parameter is the rated voltage of the capacitor. A 1µF/6.3V capacitor used at 5 V, loses about 50% of its value. With a power supply voltage of 5 V, the decoupling value, instead of 1 µF, could be reduced to 0.5 µF. As C_S has particular influence on the THD+N in the medium to high frequency region, this capacitor variation becomes decisive. In addition, less decoupling means higher overshoots which can be problematic if they reach the power supply AMR value (6 V).

4.6 Wake-up time (t_{wu})

When the standby is released to set the device ON, there is a wait of 5 ms typically. The TS2007 has an internal digital delay that mutes the outputs and releases them after this time in order to avoid any pop noise.

Note: The gain increases smoothly (see Figure 49) from the mute to the gain selected by the GS pin (Section 4.2).

4.7 Shutdown time

When the standby command is set, the time required to put the two output stages into high impedance and to put the internal circuitry in shutdown mode, is typically 5 ms. This time is used to decrease the gain and avoid any pop noise during shutdown.

Note: The gain decreases smoothly until the outputs are muted (see Figure 49).

4.8 Consumption in shutdown mode

Between the shutdown pin and GND there is an internal 300 kΩ resistor. This resistor forces the TS2007 to be in shutdown when the shutdown input is left floating.

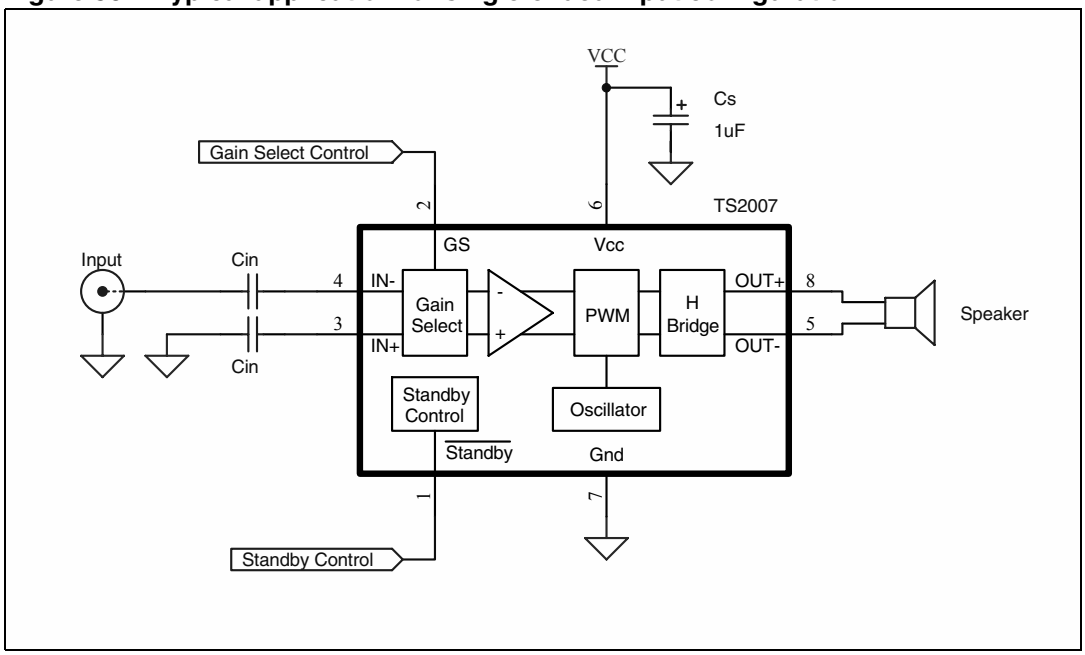
However, this resistor also introduces additional shutdown power consumption if the shutdown pin voltage is not 0 V.

Referring to *Table 2: Operating conditions on page 3*, with a 0.4 V shutdown voltage pin for example, you must add 0.4V/300k = 1.3 µA in typical (0.4V/273 k = 1.46 µA in maximum) to the shutdown current specified in *Table 5* to *Table 9*.

4.9 Single-ended input configuration

It is possible to use the TS2007 in a single-ended input configuration. However, input coupling capacitors are needed in this configuration. The following schematic diagram shows a typical single-ended input application.

Figure 50. Typical application for single-ended input configuration



4.10 Output filter considerations

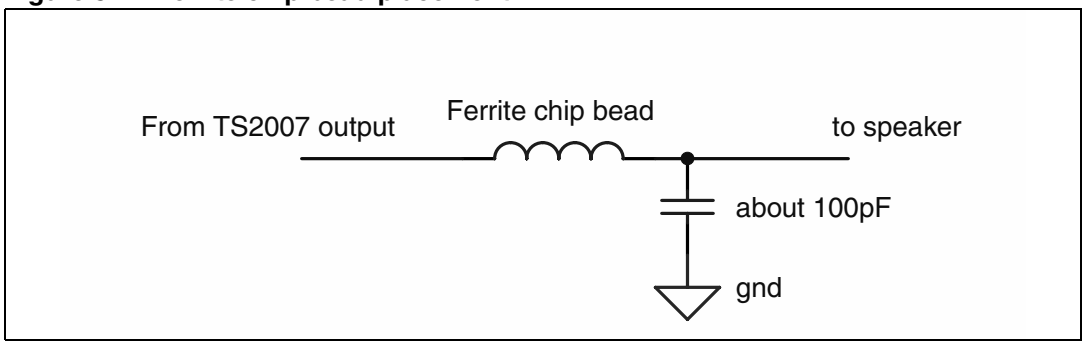
The TS2007 is designed to operate without an output filter. However, due to very sharp transients on the TS2007 output, EMI radiated emissions may cause some standard compliance issues.

These EMI standard compliance issues can appear if the distance between the TS2007 outputs and loudspeaker terminal are long (typically more than 50 mm, or 100 mm in both directions, to the speaker terminals). As the PCB layout and internal equipment device are different for each configuration, it is difficult to provide a one-size-fits-all solution.

However, to decrease the probability of EMI issues, there are several simple rules to follow:

- Reduce, as much as possible, the distance between the TS2007 output pins and the speaker terminals.
- Use a ground plane for “shielding” sensitive wires.
- Place, as close as possible to the TS2007 and in-series with each output, a ferrite bead with a rated current of minimum 2.5 A and impedance greater than 50 Ω at frequencies above 30 MHz. If, after testing, these ferrite beads are not necessary, replace them by a short-circuit.
- Allow extra footprint to place, if necessary, a capacitor to short perturbations to ground (see *Figure 51*).

Figure 51. Ferrite chip bead placement



In the case where the distance between the TS2007 output and the speaker terminals is too long, it is possible to have low frequency EMI issues due to the fact that the typical operating frequency is 280 kHz. In this configuration, it is necessary to use the output filter represented in *Figure 1 on page 4* as close as possible to the TS2007.

5 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

Figure 52. Pinout (top view)

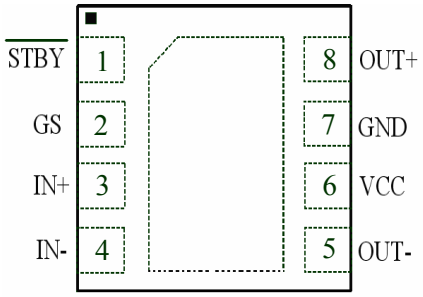


Figure 53. Marking (top view)

Logo: **ST**
Part number: **K007**
Three digit date code: **YWW**
The dot is for marking pin **1**

Figure 54. Recommended footprint for the TS2007 DFN8 package

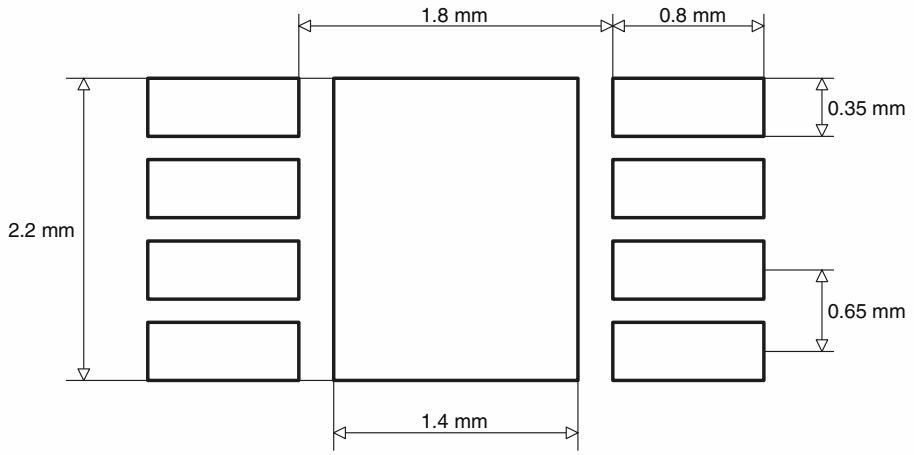
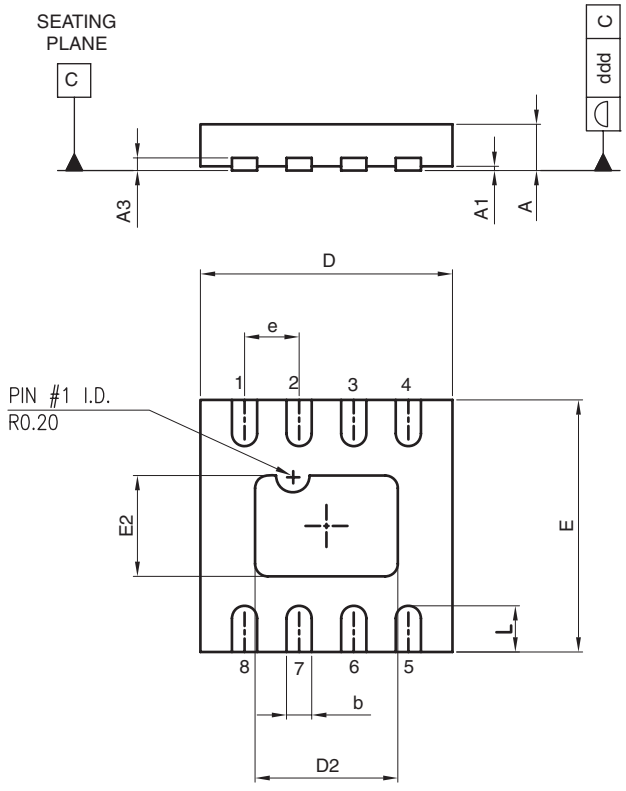


Figure 55. DFN8 package mechanical data

Ref	Dimensions					
	Millimeters			Mils		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.60	0.65	19.6	23.6	25.6
A1		0.02	0.05		0.8	1.9
A3			0.22			8.6
b	0.25	0.30	0.35	9.8	11.8	13.8
D	2.85	3.00	3.15	112.2	118.1	124
D2	1.60	1.70	1.80	63	66.9	70.8
E	2.85	3.00	3.15	112.2	118.1	124
E2	1.10	1.20	1.30	43.3	47.2	51.2
e		0.65			25.5	
L(1)	0.50	0.55	0.60	19.6	21.6	23.6
ddd			0.08			3.1



1. The dimension of L is not compliant with JEDEC MO-248 which recommends 0.40 mm +/-0.10 mm.

Note: The DFN8 package has an exposed pad E2 x D2. For enhanced thermal performance, the exposed pad must be soldered to a copper area on the PCB, acting as a heatsink. This copper area can be electrically connected to pin 7 or left floating.

6 Ordering information

Table 11. Order code

Part number	Temperature range	Package	Marking
TS2007IQT	-40 °C, +85 °C	DFN8	K07

7 Revision history

Date	Revision	Changes
11-Jan-2007	1	Initial release (preliminary data).
11-May-2007	2	First complete datasheet. This release of the datasheet includes electrical characteristics curves and application information.
24-May-2007	3	Corrected error in *Table 4: Pin descriptions*: descriptions of pin 5 and pin 8 were inverted.
02-May-2011	4	Added minimum R_L to *Table 1: Absolute maximum ratings*

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com