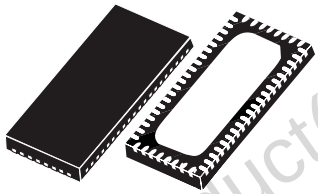
# ST3DV520A

## High bandwidth switch with 20- to 10-bit MUX/DEMUX

**Datasheet - production data**

## Features

- Low $R_{ON}$: 4.0 Ω typical
- $V_{CC}$ operating range: 3.0 to 3.6 V
- Enhanced ESD protection: > 8 kV (contact) and 15 kV (HBM)
- Channel on capacitance: 9.5 pF typical
- Switching time speed: 9 ns
- Near to zero propagation delay: 250 ps
- Very low crosstalk: -45 dB at 250 MHz
- Bit-to-bit skew: 200 ps
- > 600 MHz -3 dB typical bandwidth (or data frequency)
- Package: QFN56



QFN56

**Table 1. Device summary**

| Order code | Package | Packing |
|---|---|---|
| ST3DV520AQTR | QFN56 | Tape and reel |

# Contents

# 1 Description

The ST3DV520A 20- to 10-bit multiplexer/demultiplexer is a high bandwidth bidirectional switch with low $R_{ON}$ suitable for analog video applications.

The signal from each input is multiplexed into one of two selected outputs, while the unselected switch goes into Hi-Z status. The device is designed for very low crosstalk, low bit-to-bit skew and low I/O capacitance.

The ST3DV520A supports high definition (HD) video switching standards and is also suitable for general-purpose switching that requires high signal integrity.

# 2 Pin description

**Figure 1. Pin connection (top through view)**

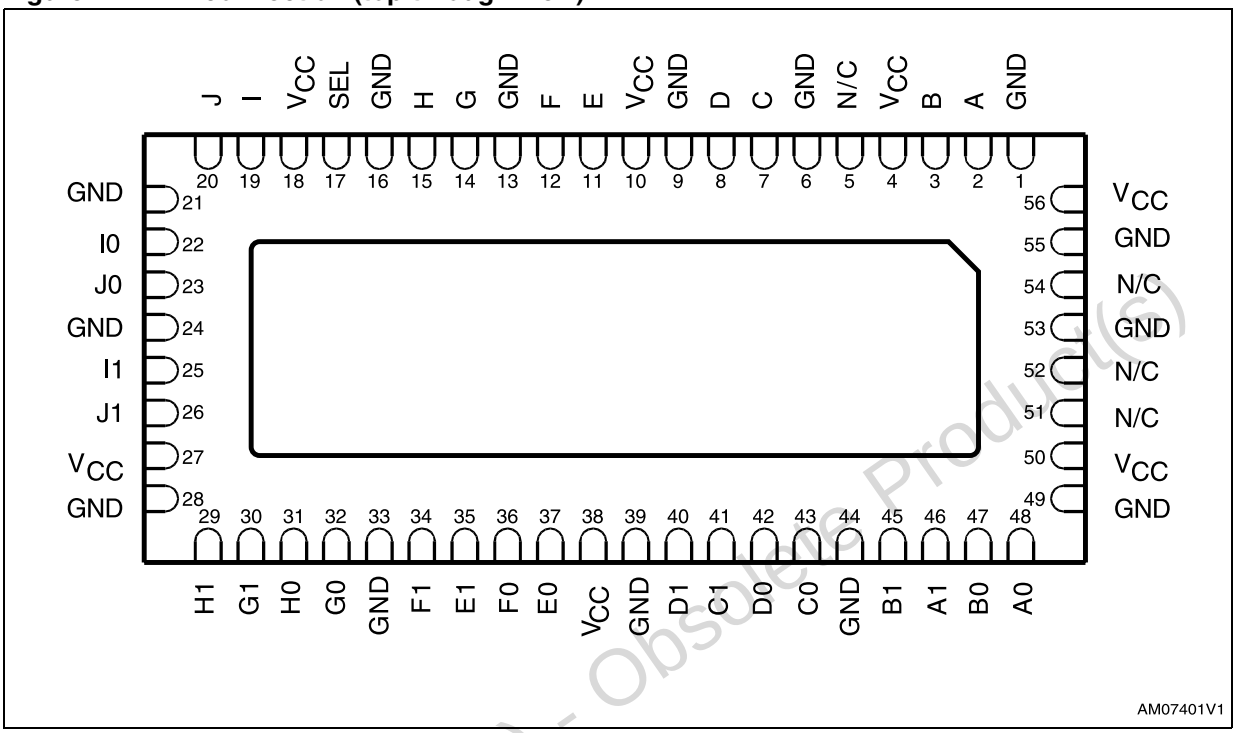



**Table 2. Pin description**

| Pin | Symbol | Name and function |
|---|---|---|
| 2, 3, 7, 8, 11, 12, 14, 15, 19, 20 | A, B, C, D, E, F, G, H, I, J | 10-bit bus |
| 48, 47, 43, 42, 37, 36, 32, 31, 22, 23 | A0, B0, C0, D0, E0, F0, G0, H0, I0, J0 | 10-bit multiplexed to bus 0 |
| 46, 45, 41, 40, 35, 34, 30, 29, 25, 26 | A1, B1, C1, D1, E1, F1, G1, H1, I1, J1 | 10-bit multiplexed to bus 1 |
| 5, 51, 52, 54 | N/C | Not connected |
| 17 | SEL | Bus and LED switch selection |
| 4, 10, 18, 27, 38, 50, 56 | $V_{CC}$ | Supply voltage |
| 1, 6, 9, 13, 16, 21, 24, 28, 33, 39, 44, 49, 53, 55 | GND | Ground |

**Figure 2. Input equivalent circuit**

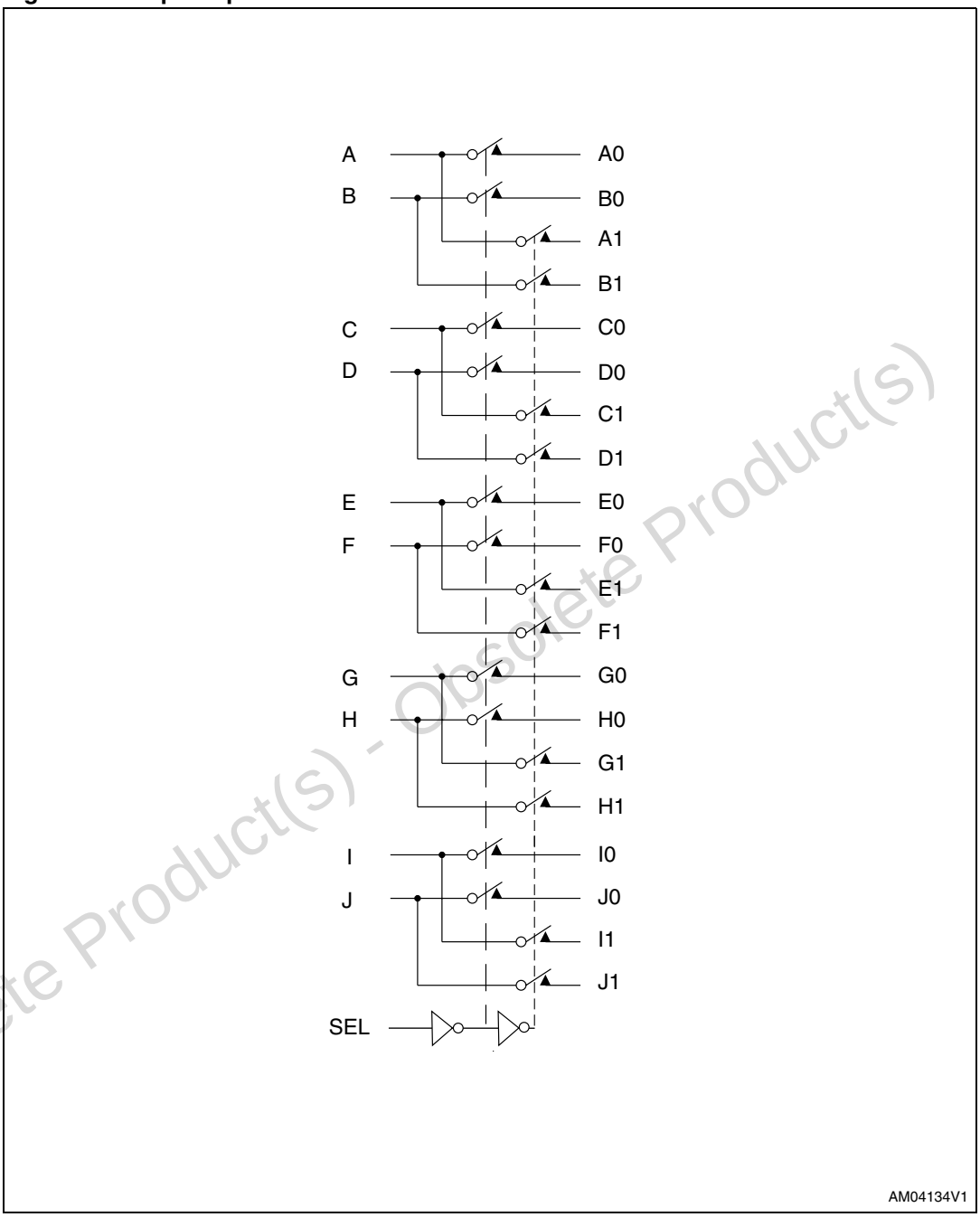





**Table 3. Switch function table**

| SEL | Function |
|---|---|
| L | 10-bit bus to 10-bit multiplexed bus 0 |
| H | 10-bit bus to 10-bit multiplexed bus 1 |

# 3 Maximum ratings

Stressing the device above the rating listed in *Table 4: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in *Table 5: Recommended operating conditions* of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply voltage to ground | -0.5 to 4.6 | V |
| $V_{IO}$ | DC input output voltage | -0.5 to 4.6 | V |
| $V_{IC}$ | DC control input voltage | -0.5 to 4.6 | V |
| $I_O$ | DC output current(1) | 120 | mA |
| $P_D$ | Power dissipation | 0.5 | W |
| $T_{stg}$ | Storage temperature | -65 to 150 | °C |
| $T_L$ | Lead temperature (10 sec.) | 300 | °C |

1. If $V_{IO}$ x $I_O$ does not exceed the maximum limit of $P_D$.

## Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $V_{CC}$ | Supply voltage to ground | 3 | – | 3.6 | V |
| $V_{IC}$ | DC control input voltage (SEL) | 0 | – | 5 | V |
| $V_{IO}$ | DC input/output voltage | 0 | – | $V_{CC}$ | V |
| $T_A$ | Operating temperature | -40 | – | 85 | °C |

# 4 Electrical characteristics

**Table 6. DC electrical characteristics ($V_{CC}$ = 3.3 V ±10%)**

| Symbol | Parameter | Test condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | -40 to 85 °C | | | |
| | | | Min. | Typ. | Max. | |
| $V_{IH}$ | Voltage input high (SEL) | High level guaranteed | 2 | – | – | V |
| $V_{IL}$ | Voltage input low (SEL) | Low level guaranteed | -0.5 | – | 0.8 | V |
| $V_{IK}$ | Clamp diode voltage (SEL) | $V_{CC}$ = 3.6 V<br>$I_{IN}$ = -18 mA | – | -0.8 | -1.2 | V |
| $I_{IH}$ | Input high current (SEL) | $V_{CC}$ = 3.6 V<br>$V_{IN}$ = $V_{CC}$ | – | – | ±5 | µA |
| $I_{IL}$ | Input low current (SEL) | $V_{CC}$ = 3.6 V<br>$V_{IN}$ = GND | – | – | ±5 | µA |
| $I_{OFF(SW)}$ (1) | Leakage current through the switch common terminals (A to J) | $V_{CC}$ = 3.6 V<br>A to J = $V_{CC}$<br>LED1 to LED3 = $V_{CC}$<br>A0 to J0 = 0 V<br>A1 to J1 = floating<br>SEL = $V_{CC}$ | – | – | ±1 | µA |
| $I_{OFF(SEL)}$ | SEL pin leakage current | $V_{CC}$ = 0 V<br>SEL = 0 to 3.6 V | – | – | ±1 | µA |
| $R_{ON}$ | Switch ON resistance(2) | $V_{CC}$ = 3.0 V<br>$V_{IN}$ = 1.5 to $V_{CC}$<br>$I_{IN}$ = -40 mA | – | 4.0 | 6.5 | Ω |
| $R_{FLAT}$ | ON resistance flatness (2),(3) | $V_{CC}$ = 3.0 V<br>$V_{IN}$ at 1.5 and $V_{CC}$<br>$I_{IN}$ = -40 mA | – | 0.5 | – | Ω |
| $\Delta R_{ON}$ | ON resistance match between channel<br>$\Delta R_{ON} = R_{ONMAX}-R_{ONMIN}$ (2),(4) | $V_{CC}$ = 3.0 V<br>$V_{IN}$ = 1.5 to $V_{CC}$<br>$I_{IN}$ = -40 mA | – | 0.4 | 1 | Ω |

1. Refer to *Figure 4: Test circuit for leakage current ($I_{OFF}$) on page 11*.
2. Measured by voltage drop between channels at indicated current through the switch. ON resistance is determined by the lower of the voltages.
3. Flatness is defined as the difference between the $R_{ONMAX}$ and $R_{ONMIN}$ of ON resistance over the specified range.
4. $\Delta R_{ON}$ measured at same $V_{CC}$, temperature and voltage level.

**Table 7. Capacitance ($T_A$ = 25 °C, f = 1 MHz)**

| Symbol | Parameter | Test condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $C_{IN}$ | SEL pin input capacitance(1) | DC = 0.25 V<br>AC = 0.5 $V_{PP}$<br>f = 1 MHz | – | 2 | 3 | pF |
| $C_{OFF}$ | Switch off capacitance(2) | DC = 0.25 V<br>AC = 0.5 $V_{PP}$<br>f = 1 MHz | – | 4 | 5 | pF |
| $C_{ON}$ | Switch on capacitance(3) | DC = 0.25 V<br>AC = 0.5 $V_{PP}$<br>f = 1 MHz | – | 9.5 | 11 | pF |

1. Refer to *Figure 5 on page 11*.
2. Refer to *Figure 6 on page 12*.
3. Refer to *Figure 7 on page 12*.

**Table 8. Power supply characteristics**

| Symbol | Parameter | Test condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | -40 to 85 °C | | | |
| | | | Min. | Typ. | Max. | |
| $I_{CC}$ | Quiescent power supply | $V_{CC}$ = 3.6 V, $V_{IN}$ = $V_{CC}$ or GND | – | 150 | 500 | µA |

**Table 9. Dynamic electrical characteristics ($V_{CC}$ = 3.3 V ±10%)**

| Symbol | Parameter | Test condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | -40 to 85 °C | | | |
| | | | Min. | Typ. | Max. | |
| $X_{talk}$ | Crosstalk(1) | $R_L$= 100 Ω<br>f = 250 MHz | – | -45 | – | dB |
| $O_{IRR}$ | Off isolation(2) | $R_L$= 100 Ω<br>f = 250 MHz | – | -37 | – | dB |
| BW | -3 dB bandwidth(3) | $R_L$= 100 Ω<br>$0 < V_{IN} \leq 3.6$ V | – | 600 | – | MHz |

1. Refer to *Figure 9 on page 14*.
2. Refer to *Figure 10 on page 15*.
3. Refer to *Figure 8 on page 13*.

**Table 10. Switching characteristics ($T_A$ = 25 °C, $V_{CC}$ = 3.3 V ±10%)**

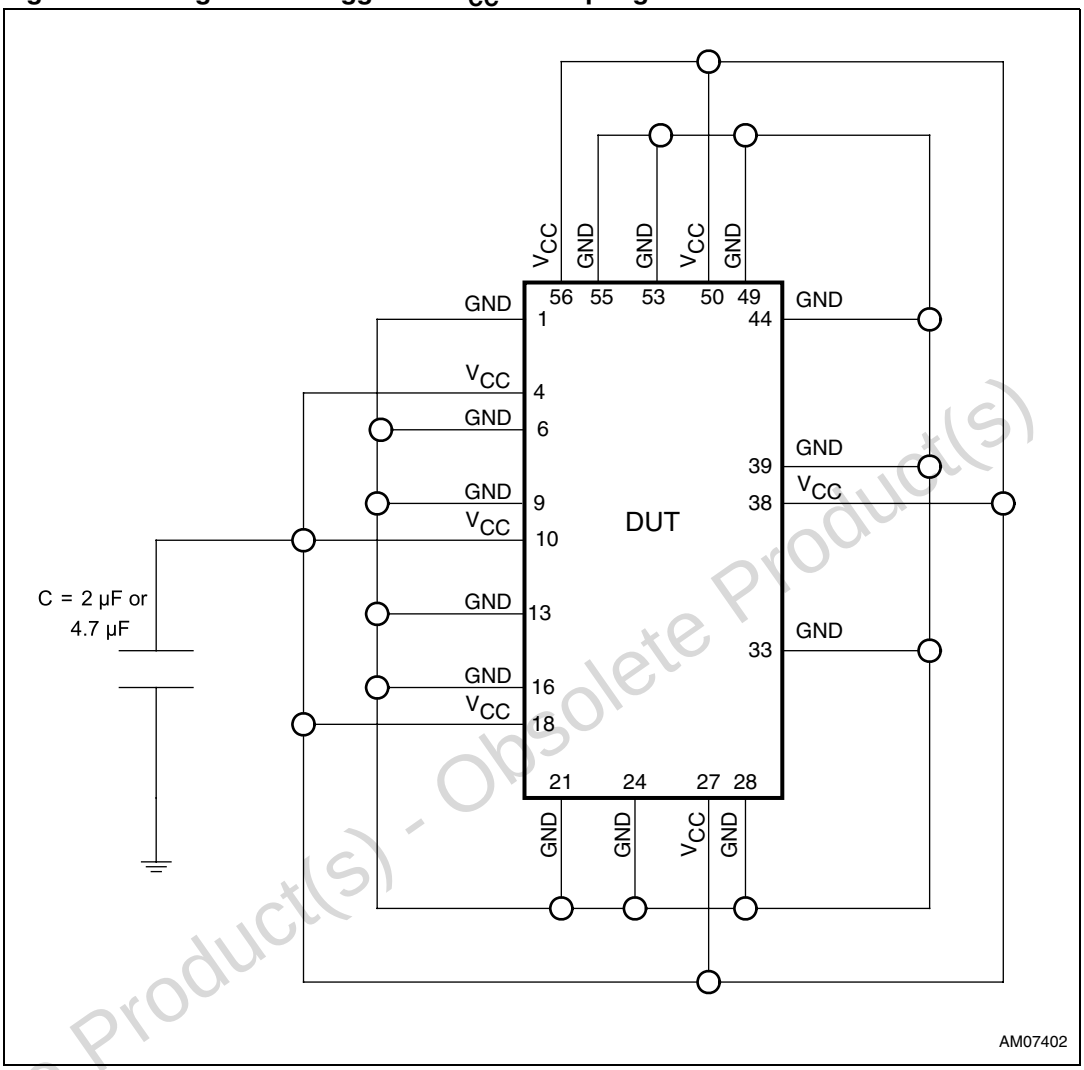
| Symbol | Parameter | Test condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{PD}$ | Propagation delay | $V_{CC}$ = 3 to 3.6 V | – | 0.25 | – | ns |
| $t_{PZH}$, $t_{PZL}$ | Line enable time, SE to x to x0 or x to x1 | $V_{CC}$ = 3 to 3.6 V | 0.5 | 6.5 | 15 | ns |
| $t_{PHZ}$, $t_{PLZ}$ | Line disable time, SE to x to x0 or x to x1 | $V_{CC}$ = 3 to 3.6 V | 0.5 | 6.5 | 8.5 | ns |
| $t_{SK(O)}$ | Output skew between center port to any other port | $V_{CC}$ = 3 to 3.6 V | – | 0.1 | 0.2 | ns |
| $t_{SK(P)}$ | Skew between opposite transition of the same output ($t_{PHL}$, $t_{PLH}$) | $V_{CC}$ = 3 to 3.6 V | – | 0.1 | 0.2 | ns |

**Table 11. ESD performance**

| Symbol | Test condition | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| ESD | Contact discharge[1] IEC61000-4-2 | – | ±8 | – | kV |
| | Human body model (MIL-STD-883) | – | ±15 | – | kV |

1. Refer to *Figure 3: Diagram for suggested $V_{CC}$ decoupling on page 10*.

**Figure 3. Diagram for suggested $V_{CC}$ decoupling**




1. Applicable for system level ESD test.
2. 100 nF capacitors must be used as local bypass capacitors between the adjacent $V_{CC}$ and GND pairs (total 7).

**Figure 4. Test circuit for leakage current ($I_{OFF}$)**

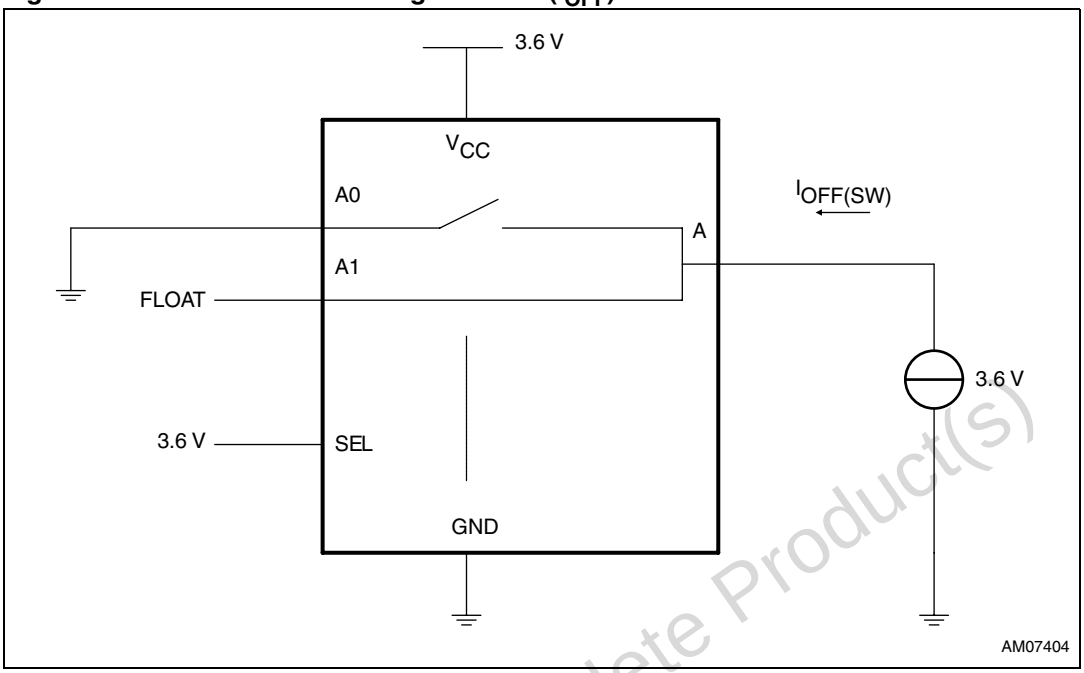



**Figure 5. Test circuit for SEL pin input capacitance ($C_{IN}$)**

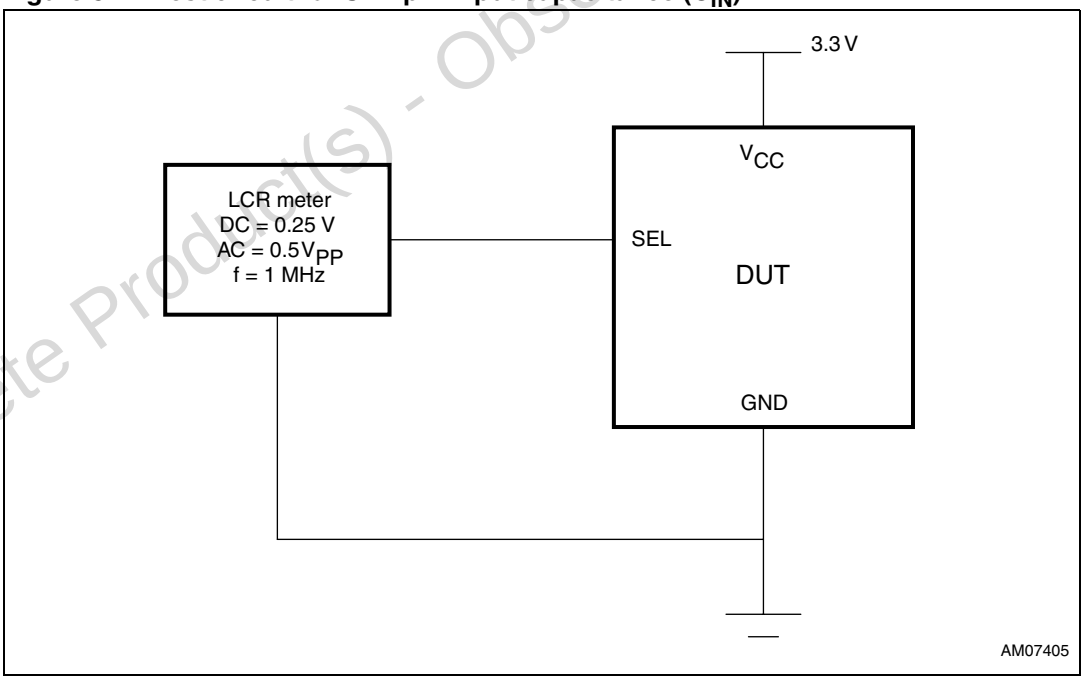


**Figure 6. Test circuit for switch off capacitance ($C_{OFF}$)**

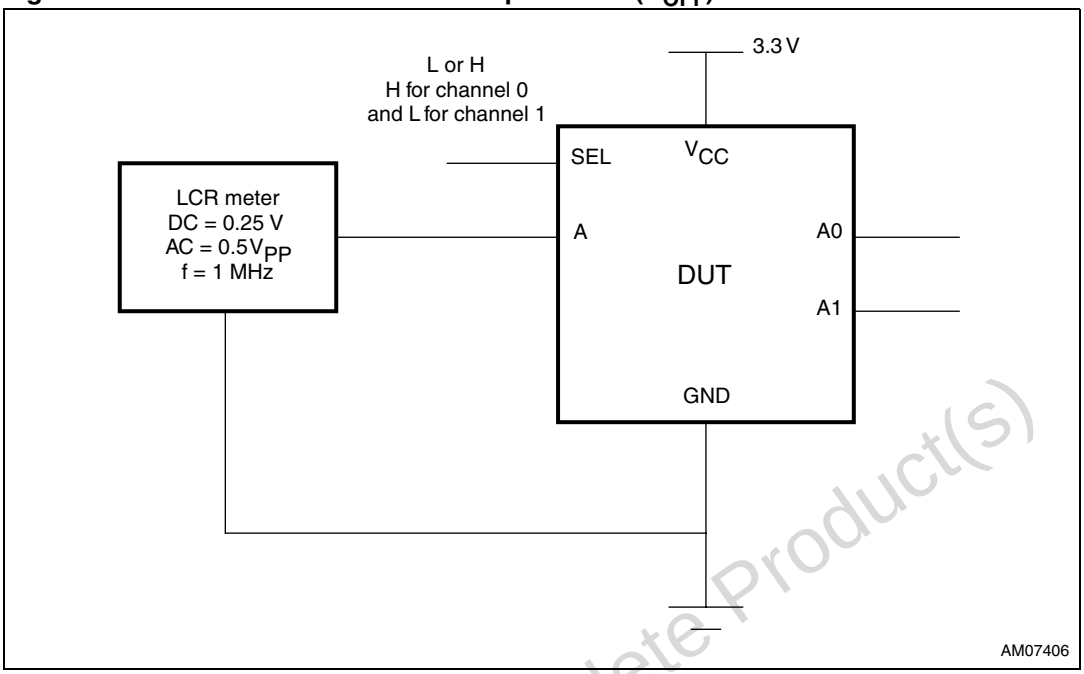



**Figure 7. Test circuit for switch on capacitance ($C_{ON}$)**

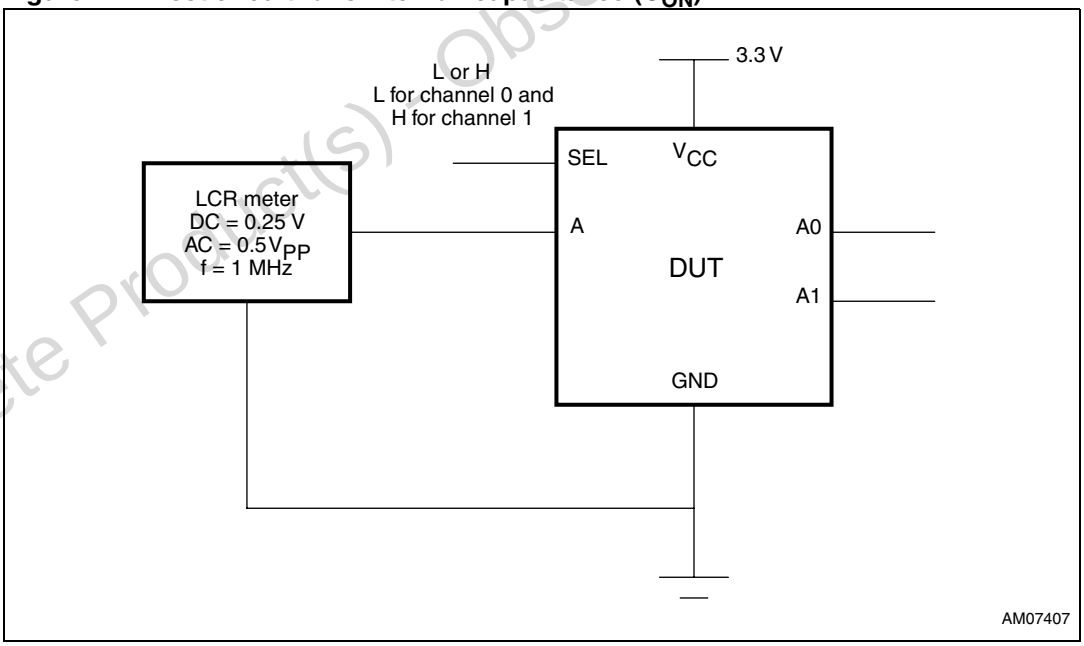
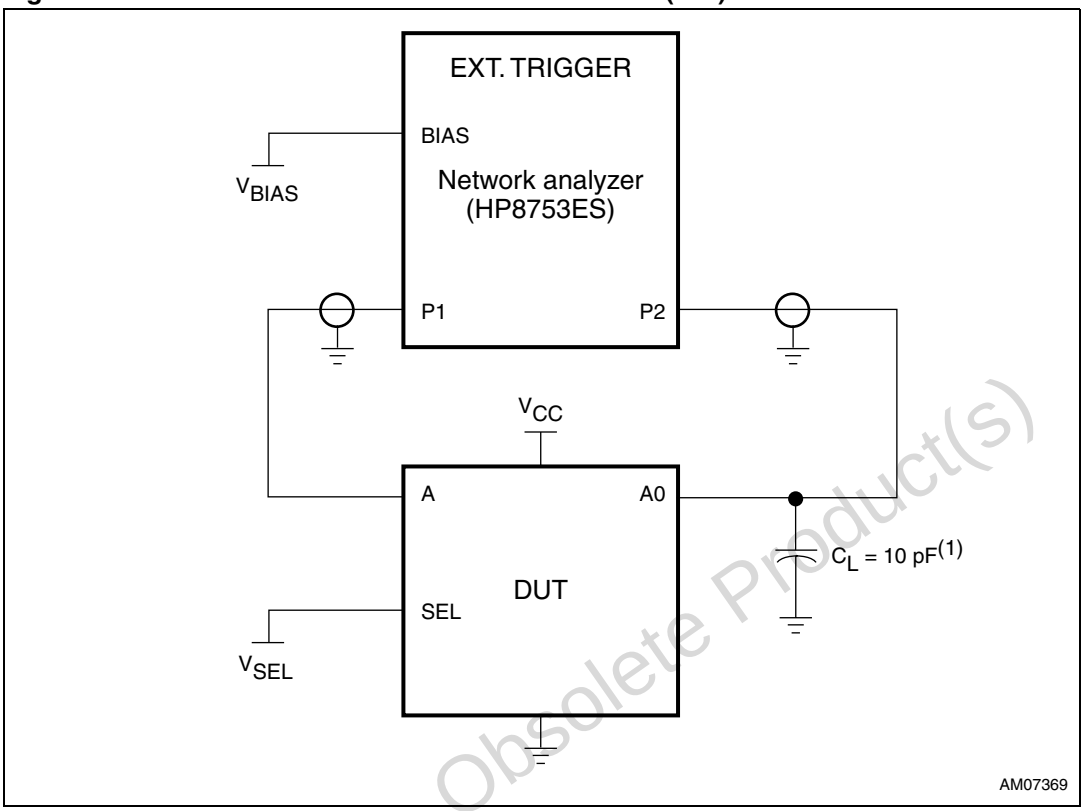


**Figure 8. Test circuit for bandwidth measurement (BW)**




1. $C_L$ includes probe and jig capacitance.

Frequency response is measured at the output of the ON channel. For example, when $V_{SEL}$ = 0 and A is the input, the output is measured at A0. All unused analog I/O ports are left open.

**HP8753ES setup:**

Average = 4

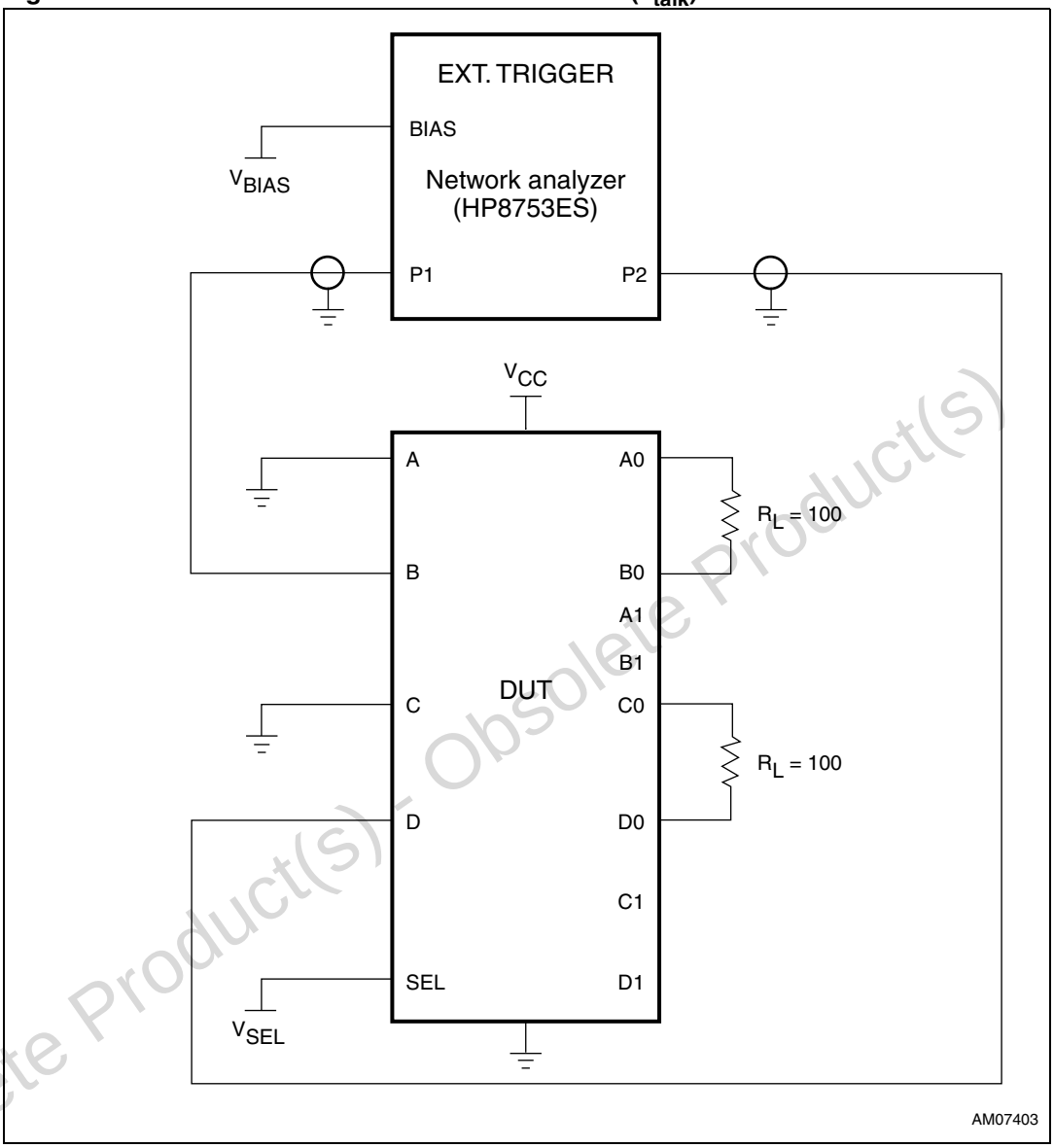
$R_{BW}$ = 3 kHz

$V_{BIAS}$ = 0.35 V

ST = 2 s

P1 = 0 dBm

**Figure 9. Test circuit for crosstalk measurement ($x_{talk}$)**




1. $C_L$ includes probe and jig capacitance.
2. A 50 Ω termination resistor is needed to match the loading of the network analyzer.

Crosstalk is measured at the output of the non-adjacent ON channel. For example, when $V_{SEL}$ = 0, and B is the input, the output is measured at D. All unused analog input ports are connected to GND and output ports are left open.

**HP8753ES setup:**

Average = 4

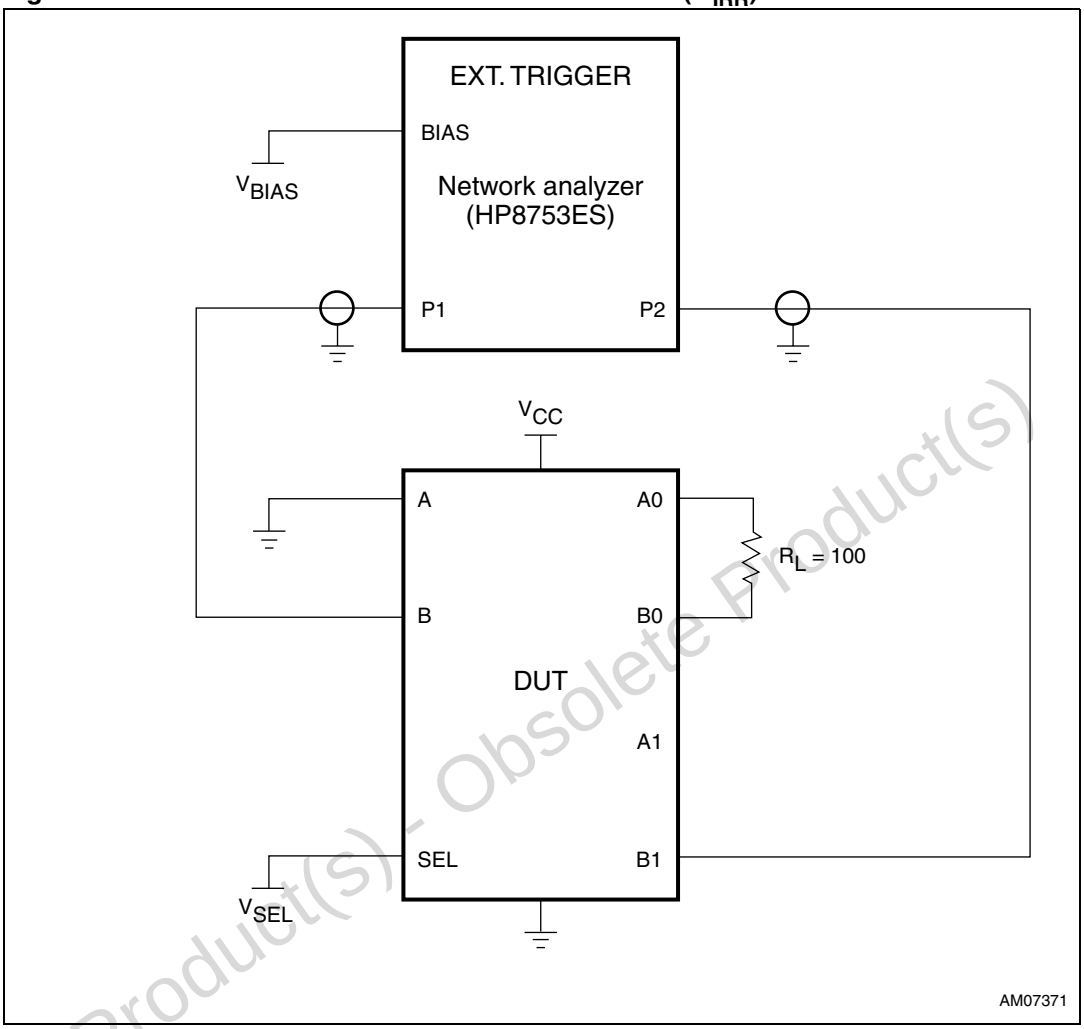
$R_{BW}$ = 3 kHz

$V_{BIAS}$ = 0.35 V

ST = 2 s

P1 = 0 dBm

**Figure 10. Test circuit for off isolation measurement ($O_{IRR}$)**




1. $C_L$ includes probe and jig capacitance.
2. A 50 Ω termination resistor is needed to match the loading of the network analyzer.

Off isolation is measured at the output of the OFF channel. For example, when $V_{SEL}$ = 0, and B is the input, the output is measured at B1. All unused analog input ports are connected to GND and output ports are left open.

**HP8753ES setup:**

Average = 4

$R_{BW}$ = 3 kHz

$V_{BIAS}$ = 0.35 V

ST = 2 s

P1 = 0 dBm

# 5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

**Figure 11. Package outline for QFN56 (11 x 5 mm) - pitch 0.5 mm**

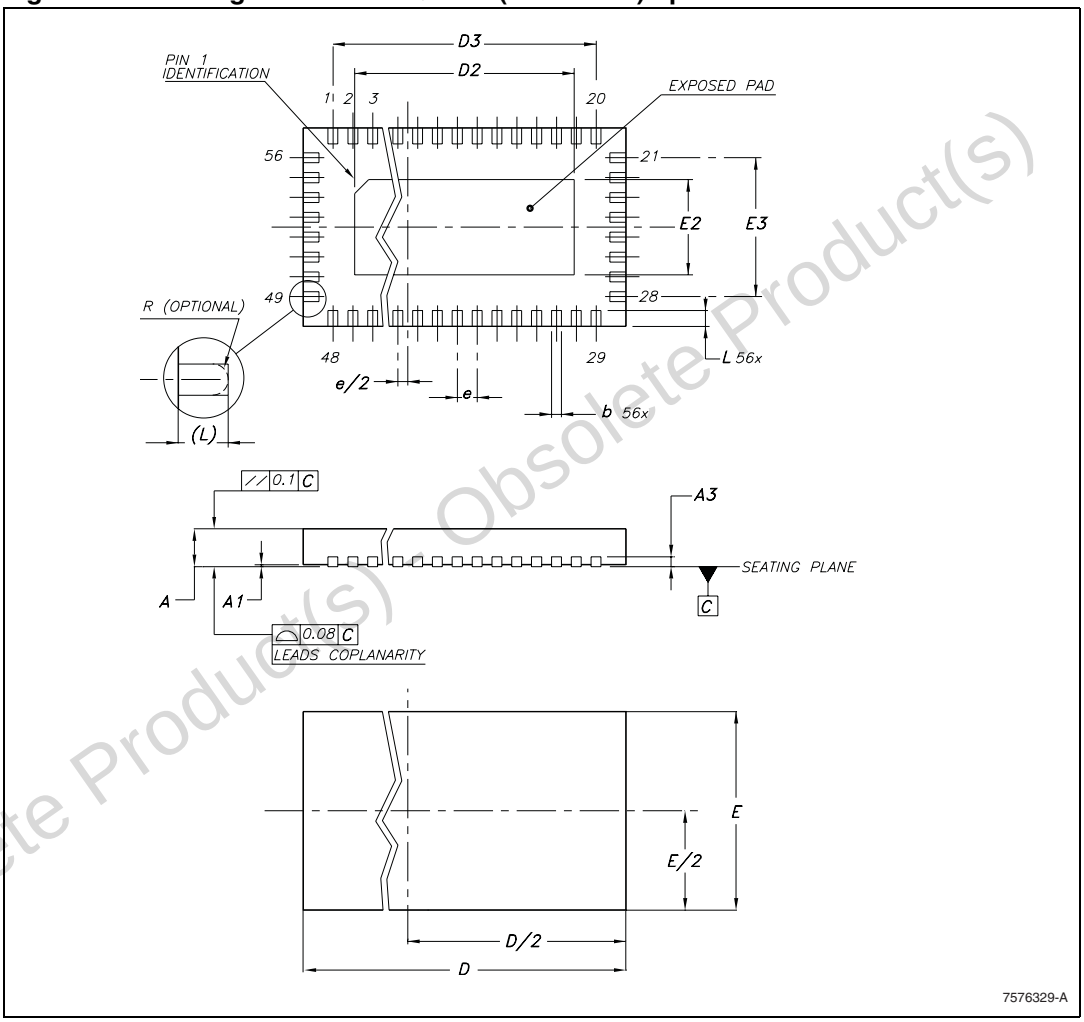


Table 12. Mechanical data for QFN56 (11 x 5 mm) - pitch 0.5 mm

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.70 | 0.75 | 0.80 |
| A1 | – | – | 0.05 |
| A3 | | 0.20 | – |
| b | 0.20 | 0.25 | 0.30 |
| D | 10.90 | 11.00 | 11.10 |
| D2 | 8.30 | 8.40 | 8.50 |
| D3 | – | 9.50 | – |
| E | 4.90 | 5.00 | 5.10 |
| E2 | 2.30 | 2.40 | 2.50 |
| E3 | – | 3.50 | – |
| e | – | 0.50 | – |
| L | 0.30 | 0.40 | 0.50 |

Figure 12. Footprint recommendation for QFN56 (11 x 5 mm) - pitch 0.5 mm

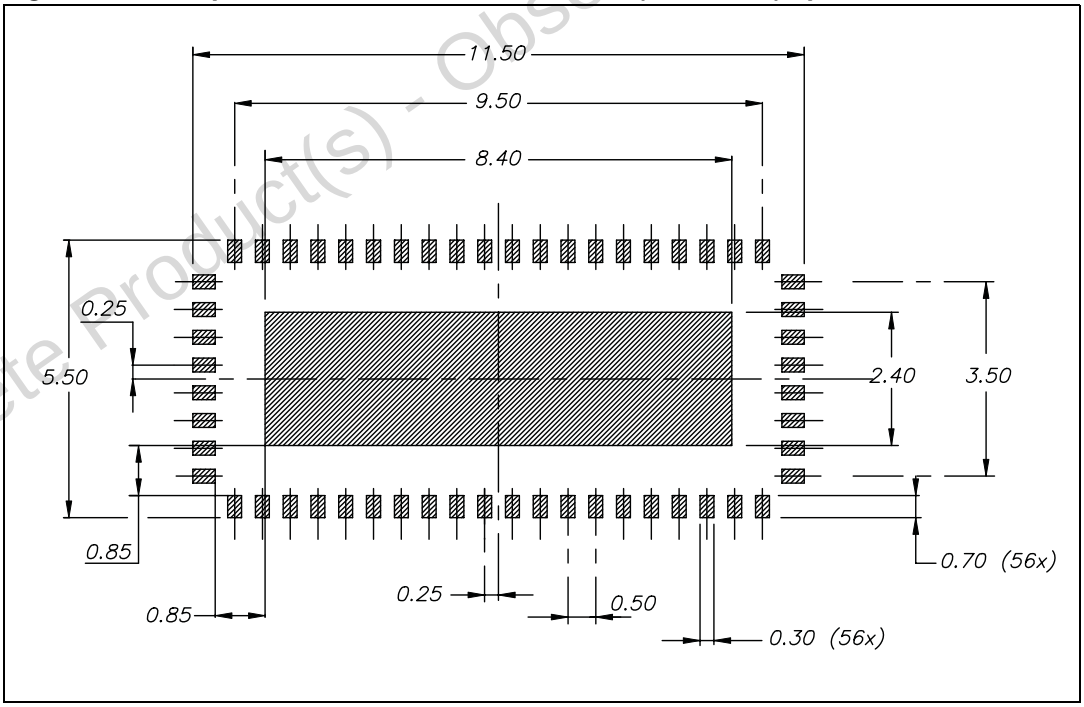
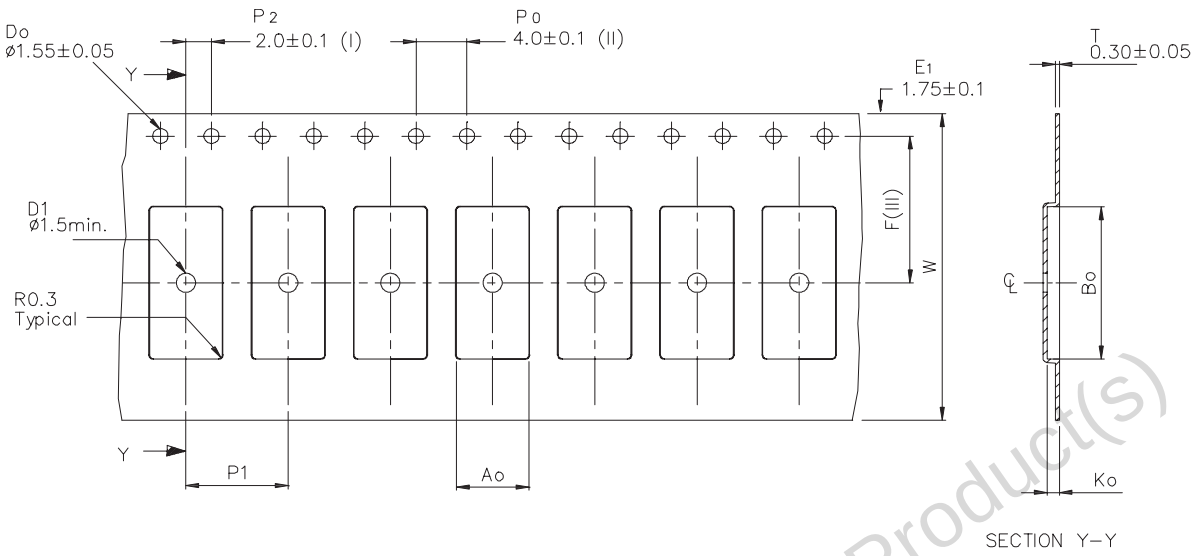


**Figure 13. Carrier tape information for QFN56 (11 x 5 mm) - pitch 0.5 mm**




| | | | |
|---|---|---|---|
| Ao | 5.70 | +/– | 0.1 |
| Bo | 11.90 | +/– | 0.1 |
| Ko | 0.95 | +/– | 0.1 |
| F | 11.50 | +/– | 0.1 |
| $P_1$ | 8.00 | +/– | 0.1 |
| W | 24.00 | +/– | 0.3 |

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

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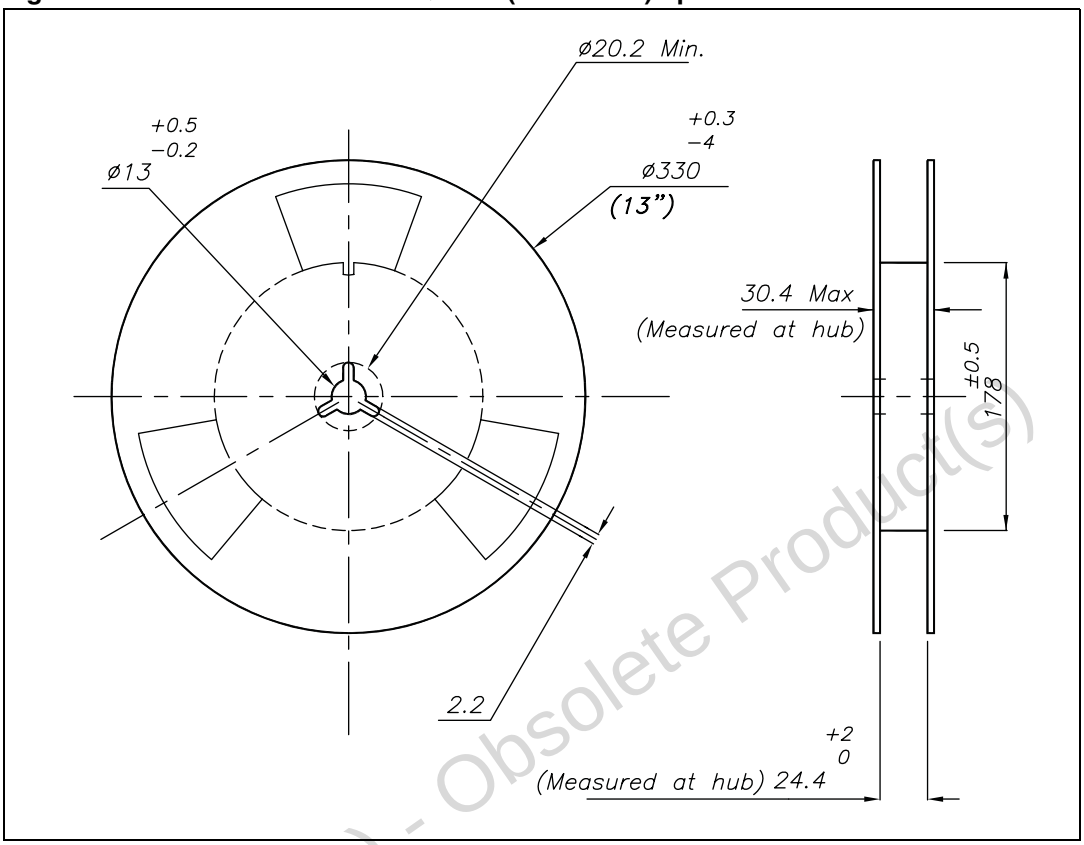
**Figure 14. Reel information for QFN56 (11 x 5 mm) - pitch 0.5 mm**



# 6 Revision history

**Table 13. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 11-Dec-2009 | 1 | Initial release. |
| 07-Apr-2010 | 2 | Corrected circuit drawing errors in *Figure 2: Input equivalent circuit*.<br>Modified text in the Description on page 1. |
| 11-Jan-2011 | 3 | Document reformatted, replaced $V_{DD}$ by $V_{CC}$ in *Figure 1*, *Table 2*, *Figure 3*, to *Figure 10*, moved notes below *Figure 8* to *Figure 10*, corrected typo in *Table 5* to *Table 7*, *Table 9*, *Figure 3* to *Figure 10*. |
| 17-Jan-2013 | 4 | Updated *Figure 1* (added numbers to pins) and *Table 2* (updated order of pins).<br>Added cross-references in *Section 3*.<br>Minor modifications throughout document. |

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