

# STHDLS101T

# AC coupled HDMI level shifter with configurable HPD output

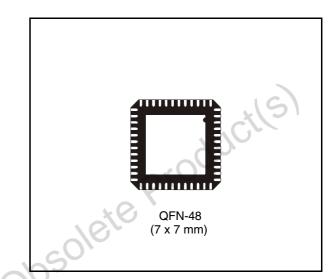
### Features

- Converts low-swing alternating current (AC) coupled differential input to high-definition multimedia interface (HDMI) rev 1.3 compliant
- HDMI level shifting operation up to 2.7 Gbps per lane
- Integrated 50-Ω termination resistors for ACcoupled differential inputs
- Input/output transition minimized differential signaling (TMDS) enable/disable
- Output slew rate control on TMDS outputs to minimize electromagnetic interference (EMI)
- Fail safe outputs for backdrive protection
- No re-timing or configuration required
- Inter-pair output skew < 250 ps</li>
- Intra-pair output skew < 10 ps</p>
- Single power supply of 3.3 V
- ESD protection: ±6 KV HBM on all I/O pins
- Integrated display data channel (DDC) level shifters. Pass-gate voltage limiters allow 3.3 V termination on graphics and memory controller hub (GMCH) pins and 5 V DDC termination on HDMI connector pins
- Level shifter and configurable output for HPD signal from HDMI/DVI connector
- Integrated pull-down resistor on HPD\_SINK and OE\_N inputs

### Applications

- Notebooks
- PC motherboards and graphic cards
- Dongles/cable adapters

### Table 1.Device summary



### Description

The STHDLS101T is a high-speed high-definition multimedia interface (HDMI) level shifter that converts low-swing AC coupled differential input to HDMI 1.3 compliant open-drain current steering RX-terminated differential output. Through the existing PCI-E pins in the graphics and memory controller hub (GMCH) of PCs or notebook motherboards, the pixel clock provides the required bandwidth (1.65 Gbps, 2.25 Gbps) for the video supporting 720p, 1080i, 1080p with a total of 36-bit resolution. The HDMI is multiplexed onto the PCIe pins in the motherboard where the AC coupled HDMI at 1.2 V is output by GMCH. The AC coupled HDMI is then level shifter by this device to 3.3 V DC coupled HDMI output.

The STHDLS101T supports up to 2.7 Gbps, which is enough for 12-bits of color depth per channel, as indicated in HDMI rev 1.3. The device operates from a single 3.3 V supply and is available in a 48-pin QFN package.

Order code	Package	Packaging
STHDLS101TQTR	QFN-48	Tape and reel

# Contents

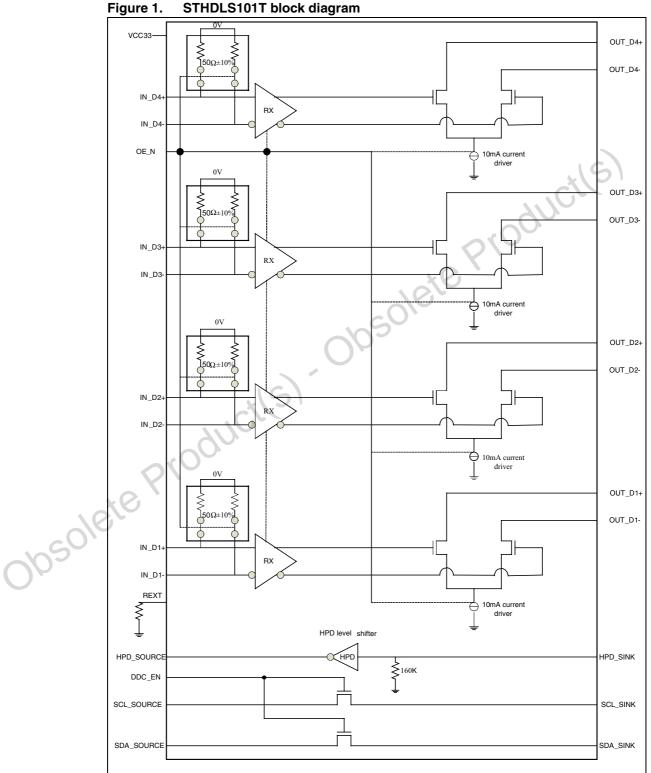
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#### **Block diagram** 1

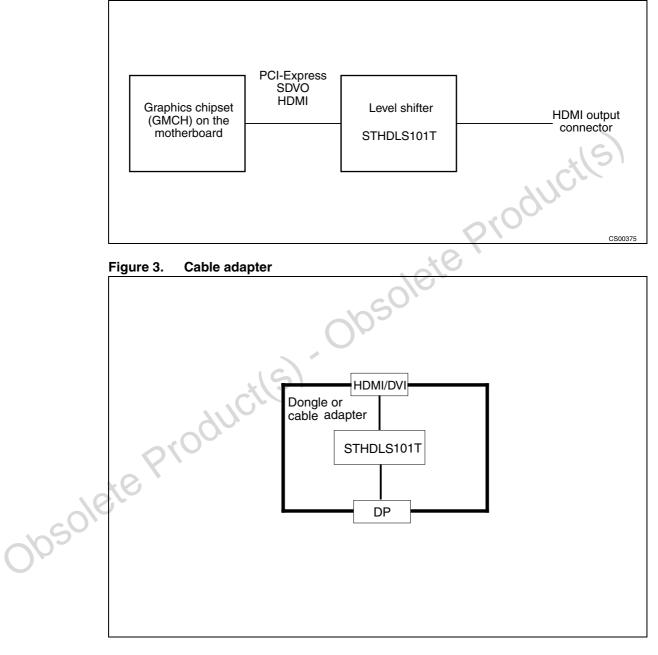


### STHDLS101T block diagram



# 2 System interface





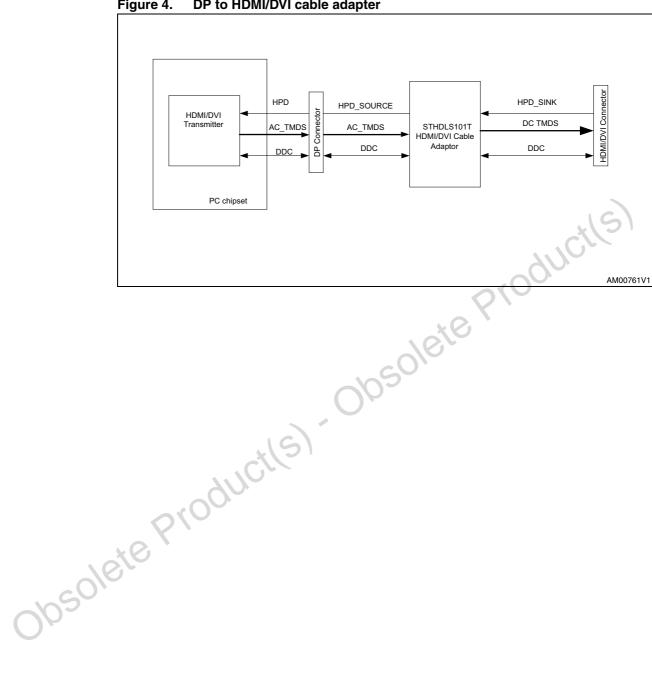
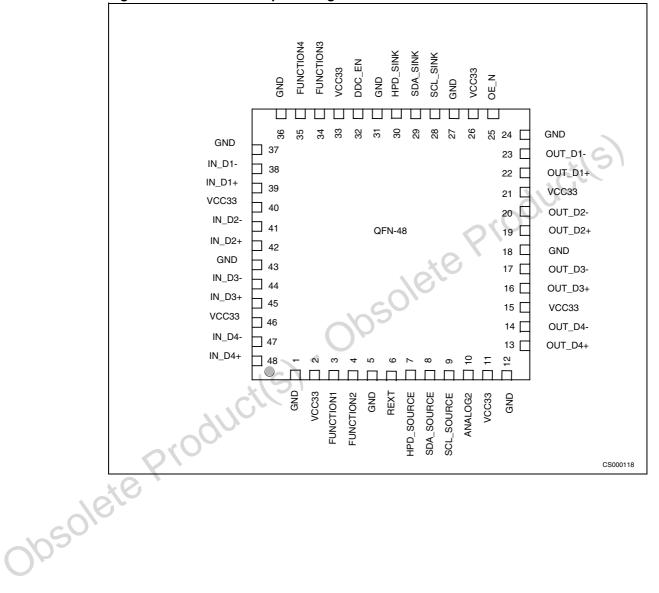


Figure 4. DP to HDMI/DVI cable adapter



# 3 Pin configuration







# 3.1 Pin description

	Pin number	Name	Туре		Function	
	1	GND	Power	Ground		
	2	VCC33	Power	3.3V±10% DC supp	oly	
	3	FUNCTION1	Vendor-specific control or test pins	For normal operation, these bins are tied to Give or		
	4	FUNCTION2	Vendor-specific control or test pins	or test VCC33		e tied to GND or
	5	GND	Power	Ground		
	6	REXT	Analog	Connection to external resistor. Resistor value specified by device manufacturer. Acceptable connections to this pin are: - Resistor to GND - Resistor to 3.3V; - NC (direct connections to V <sub>CC</sub> or GND are th 0-Ù resistor for layout compatibility		re:
	7	HPD_SOURCE	Output	Buffer from the 0 V buffer stage is conf pin settings as desi	igurable based of	n the FUNCTION3
	× 0 `			FUNCTION3	HPD_SINK	HPD_SOURCE
Obsole				0	Low	Open-drain, connected an external pull up to the desired supply (normally 1 V)
				0	High (5 V)	Low (0 V)
				1	Low (0 V)	Low (0 V)
				1	High (5 V)	High (3 V)
	8	SDA_SOURCE	I/O	3.3 V DDC data I/C to 3.3 V. Connected limiting integrated N	to SDA_SINK th	
	9	SCL_SOURCE	Input	3.3 V DDC clock I/0 to 3.3 V. Connected limiting integrated N	to SCL_SINK th	



Pin numberNameTypeFunction10ANALOG2AnalogAnalog connection determined by vendor. Acceptable connections to this pin are: - Resistor or capacitor to GND - Resistor or capacitor to GND - NC11VCG33Power3.3 V ±10% DC supply12GNDPowerGround13OUT_D4+OutputHDMI 1.3 compliant TMDS output. OUT_D4+ makes a differential output signal with OUT_D4- makes a differential output signal with OUT_D4- makes a differential output signal with OUT_D3+14OUT_D3+OutputHDMI 1.3 compliant TMDS output. OUT_D4- makes a differential output signal with OUT_D4- makes a differential output signal with OUT_D4- makes a differential output signal with OUT_D3+16OUT_D3+OutputHDMI 1.3 compliant TMDS output. OUT_D3- OUT_D3-18GNDPowerGround19OUT_D2+OutputHDMI 1.3 compliant TMDS output. OUT_D3+20OUT_D2+OutputHDMI 1.3 compliant TMDS output. OUT_D3+21VCC33PowerGround22OUT_D2+OutputHDMI 1.3 compliant TMDS output. OUT_D2+23OUT_D1+OutputHDMI 1.3 compliant TMDS output. OUT_D2+24GNDPowerGround25OE_NInputHDMI 1.3 compliant TMDS output. OUT_D1+26OE_NInputHDMI 1.3 compliant TMDS output. OUT_D1+21VCC33PowerGround22OUT_D1+OutputHDMI 1.3 compliant TMDS output. OUT_D1+		Table 2.	Pin descrip	tion (continue	ued)		
10         ANALOG2         Analog         Acceptable connections to this primate: -Resistor or capacitor to GND -Resistor or capacitor to GND -Resistor or capacitor to GND -Resistor or capacitor to GND -NC           11         VCC33         Power         3.3 V ±10% DC supply           12         GND         Power         Ground           13         OUT_D4+         Output         OUT_D4+ makes a differential output signal with OUT_D4- makes a differential output signal with OUT_D4+.           14         OUT_D4-         Output         OUT_D4- makes a differential output signal with OUT_D4+.           15         VCC33         Power         3.3 V±10% DC supply           16         OUT_D3+         Output         OUtput           17         OUT_D3-         Output         OUT_D3- makes a differential output signal with OUT_D3- makes a differential output signal with OUT_D2+ makes a differential output signal with OUT_D1+ makes a differential outp			Name	Туре		Function	
12     GND     Power     Ground       13     OUT_D4+     Output     HDMI 1.3 compliant TMDS output. OUT_D4+ makes a differential output signal with OUT_D4+.       14     OUT_D4+     Output     HDMI 1.3 compliant TMDS output. OUT_D4+.       15     VCC33     Power     3.3 V±10% DC supply       16     OUT_D3+     Output     HDMI 1.3 compliant TMDS output. OUT_D3+ makes a differential output signal with OUT_D3+ makes a differential output signal with OUT_D3+.       18     GND     Power     Ground       19     OUT_D2+     Output     HDMI 1.3 compliant TMDS output. OUT_D2+ makes a differential output signal with OUT_D2+.       20     OUT_D2+     Output     HDMI 1.3 compliant TMDS output. OUT_D2+.       21     VCC33     Power     3.3 V±10% DC supply       22     OUT_D1+     Output     HDMI 1.3 compliant TMDS output. OUT_D2+.       23     OUT_D1+     Output     HDMI 1.3 compliant MDS output. OUT_D1+ makes a differential output signal with OUT_D1+.       24     GND     Power     Ground       25     OE_N     Input     Enable for level shifter path. 3.3 V tolerant low-voltage single-ended input. Internal pull-down enables chip when unconnected.       25     OE_N     Input     Input.		10	ANALOG2	Analog	Acceptable connect - Resistor or capace - Resistor or capace - Short to 3.3 V or 1	tions to this pin a itor to GND itor to 3.3 V	
13     OUT_D4+     Output     HDMI 1.3 compliant TMDS output. OUT_D4+ makes a differential output signal with OUT_D4.       14     OUT_D4-     Output     HDMI 1.3 compliant TMDS output. OUT_D4- makes a differential output signal with OUT_D4+.       15     VCC33     Power     3.3 V±10% DC supply       16     OUT_D3+     Output     HDMI 1.3 compliant TMDS output. OUT_D4+ makes a differential output signal with OUT_D4+ makes a differential output signal with OUT_D3+ makes a differential output signal with OUT_D3+ makes a differential output signal with OUT_D3+ makes a differential output signal with OUT_D3+.       17     OUT_D2+     Output     HDMI 1.3 compliant TMDS output. OUT_D3+ makes a differential output signal with OUT_D3+.       19     OUT_D2+     Output     HDMI 1.3 compliant TMDS output. OUT_D2+ makes a differential output signal with OUT_D2+.       20     OUT_D2-     Output     HDMI 1.3 compliant TMDS output. OUT_D2+.       21     VCC33     Power     3.3 V±10% DC supply       22     OUT_D1+     Output     HDMI 1.3 compliant TMDS output. OUT_D1+ makes a differential output signal with OUT_D2+.       23     OUT_D1+     Output     HDMI 1.3 compliant TMDS output. OUT_D1+ makes a differential output signal with OUT_D1+.       24     GND     Power     Ground       25     OE_N     Input     Enable for level shifter path. 3.3 V tolerant low-voltage single-ended input. Internat pull-down enables chip when unconnected.		11	VCC33	Power	3.3 V ±10% DC su	pply	
13     OUT_D4+     Output     OUT_D4- nakes a differential output signal with OUT_D4       14     OUT_D4-     Output     HDMI 1.3 compliant TMDS output. OUT_D4+.       15     VCC33     Power     3.3 V±10% DC supply       16     OUT_D3+     Output     HDMI 1.3 compliant TMDS output. OUT_D4+.       17     OUT_D3+     Output     HDMI 1.3 compliant TMDS output. OUT_D3- makes a differential output signal with OUT_D3       18     GND     Power     Ground       19     OUT_D2+     Output     OUT_D2       20     OUT_D2-     Output     OUT_D2       21     VCC33     Power     3.3 V±10% DC supply       22     OUT_D1+     Output     HDMI 1.3 compliant TMDS output. OUT_D2       21     VCC33     Power     3.3 V±10% DC supply       22     OUT_D1+     Output     HDMI 1.3 compliant TMDS output. OUT_D2       23     OUT_D1+     Output     HDMI 1.3 compliant TMDS output. OUT_D1+ makes a differential output signal with OUT_D1+.       24     GND     Power     Ground       25     OE_N     Input     Input       1     High-Z     High-Z		12	GND	Power	Ground		
14     OUT_D4-     Output     OUT_D4- makes a differential output signal with OUT_D4+.       15     VCC33     Power     3.3 V±10% DC supply       16     OUT_D3+     Output     HDMI 1.3 compliant TMDS output. OUT_D3- makes a differential output signal with OUT_D3-       17     OUT_D3-     Output     HDMI 1.3 compliant TMDS output. OUT_D3- makes a differential output signal with OUT_D3       18     GND     Power     Ground       19     OUT_D2+     Output     HDMI 1.3 compliant TMDS output. OUT_D2- makes a differential output signal with OUT_D2       20     OUT_D2+     Output     HDMI 1.3 compliant TMDS output. OUT_D2       21     VCC33     Power     3.3 V±10% DC supply       22     OUT_D1+     Output     HDMI 1.3 compliant TMDS output. OUT_D2+.       23     OUT_D1+     Output     HDMI 1.3 compliant TMDS output. OUT_D1+ makes a differential output signal with OUT_D1       23     OUT_D1+     Output     HDMI 1.3 compliant TMDS output. OUT_D1+ makes a differential output signal with OUT_D1       24     GND     Power     Ground       25     OE_N     Input     Input     Input       0E_N     Input     Input     Input     Input		13	OUT_D4+	Output	OUT_D4+ makes a		ut signal with
16     OUT_D3+     Output     HDMI 1.3 compliant TMDS output. OUT_D3+ makes a differential output signal with OUT_D3.       17     OUT_D3-     Output     HDMI 1.3 compliant TMDS output. OUT_D3- makes a differential output signal with OUT_D3+.       18     GND     Power     Ground       19     OUT_D2+     Output     OUT_D2+ makes a differential output signal with OUT_D2+ makes a differential output signal with OUT_D2+ makes a differential output signal with OUT_D2- makes a differential output signal with OUT_D1+       21     VCC33     Power     3.3 V±10% DC supply       22     OUT_D1+     Output     HDMI 1.3 compliant TMDS output. OUT_D1+       23     OUT_D1-     Output     HDMI 1.3 compliant TMDS output. OUT_D1-       24     GND     Power     Ground       25     OE_N     Input     Input     Input signal with OUT_D1-       25     OE_N     Input     Input     Input     Input signal with OUT_D1-		14	OUT_D4-	Output	OUT_D4- makes a		it signal with
16     OUT_D3+     Output     OUT_D3+ makes a differential output signal with OUT_D3       17     OUT_D3-     Output     HDMI 1.3 compliant TMDS output. OUT_D3+.       18     GND     Power     Ground       19     OUT_D2+     Output     HDMI 1.3 compliant TMDS output. OUT_D2+.       20     OUT_D2+     Output     HDMI 1.3 compliant TMDS output. OUT_D2+.       20     OUT_D2-     Output     HDMI 1.3 compliant TMDS output. OUT_D2       21     VCC33     Power     3.3 V±10% DC supply       22     OUT_D1+     Output     HDMI 1.3 compliant TMDS output. OUT_D2+.       23     OUT_D1+     Output     HDMI 1.3 compliant TMDS output. OUT_D1+ makes a differential output signal with OUT_D1       24     GND     Power     Ground       25     OE_N     Input     Input       1     High-Z     High-Z		15	VCC33	Power	3.3 V±10% DC sup	pply	
17       OUT_D3-       Output       OUT_D3- makes a differential output signal with OUT_D3+.         18       GND       Power       Ground         19       OUT_D2+       Output       HDMI 1.3 compliant TMDS output. OUT_D2+ makes a differential output signal with OUT_D2.         20       OUT_D2-       Output       HDMI 1.3 compliant TMDS output. OUT_D2         20       OUT_D2-       Output       HDMI 1.3 compliant TMDS output. OUT_D2         21       VCC33       Power       3.3 V±10% DC supply         22       OUT_D1+       Output       HDMI 1.3 compliant TMDS output. OUT_D1+ makes a differential output signal with OUT_D2+.         23       OUT_D1+       Output       HDMI 1.3 compliant TMDS output. OUT_D1+ makes a differential output signal with OUT_D1         24       GND       Power       Ground         25       OE_N       Input       Enable for level shifter path. 3.3 V tolerant low-voltage single-ended input. Internal pull-down enables chip when unconnected.         25       OE_N       Input       OE_N       IN_D       OUT_D Outputs		16	OUT_D3+	Output	OUT_D3+ makes a		ut signal with
19OUT_D2+OutputHDMI 1.3 compliant TMDS output. OUT_D2+ makes a differential output signal with OUT_D2.20OUT_D2-OutputHDMI 1.3 compliant TMDS output. OUT_D220OUT_D2-OutputHDMI 1.3 compliant TMDS output. OUT_D2+.21VCC33Power3.3 V±10% DC supply22OUT_D1+OutputHDMI 1.3 compliant TMDS output. OUT_D1+ makes a differential output signal with OUT_D123OUT_D1-OutputHDMI 1.3 compliant TMDS output. OUT_D1- makes a differential output signal with OUT_D124GNDPowerGround25OE_NInputEnable for level shifter path. 3.3 V tolerant low-voltage single-ended input. Internal pull-down enables chip when unconnected.25OE_NInputOE_NImput1High-ZHigh-Z		17	OUT_D3-	Output	OUT_D3- makes a		it signal with
19       OUT_D2+       Output       OUT_D2+ makes a differential output signal with OUT_D2         20       OUT_D2-       Output       HDMI 1.3 compliant TMDS output. OUT_D2+ makes a differential output signal with OUT_D2+.         21       VCC33       Power       3.3 V±10% DC supply         22       OUT_D1+       Output       HDMI 1.3 compliant TMDS output. OUT_D1+ makes a differential output signal with OUT_D1         23       OUT_D1-       Output       HDMI 1.3 compliant TMDS output. OUT_D1- makes a differential output signal with OUT_D1         24       GND       Power       Ground         25       OE_N       Input       Enable for level shifter path. 3.3 V tolerant low-voltage single-ended input. Internal pull-down enables chip when unconnected.         25       OE_N       Input       OE_N       IN_D termination       OUT_D Outputs		18	GND	Power	Ground		
20       OUT_D2-       Output       OUT_D2- makes a differential output signal with OUT_D2+.         21       VCC33       Power       3.3 V±10% DC supply         22       OUT_D1+       Output       HDMI 1.3 compliant TMDS output. OUT_D1+ makes a differential output signal with OUT_D1         23       OUT_D1-       Output       HDMI 1.3 compliant TMDS output. OUT_D1- makes a differential output signal with OUT_D1+.         24       GND       Power       Ground         25       OE_N       Input       Enable for level shifter path. 3.3 V tolerant low-voltage single-ended input. Internal pull-down enables chip when unconnected.         25       OE_N       Input       OE_N       Imput. High-Z       High-Z		19	OUT_D2+	Output	OUT_D2+ makes a		ut signal with
22       OUT_D1+       Output       HDMI 1.3 compliant TMDS output. OUT_D1+ makes a differential output signal with OUT_D1         23       OUT_D1-       Output       HDMI 1.3 compliant TMDS output. OUT_D1- makes a differential output signal with OUT_D1+.         24       GND       Power       Ground         25       OE_N       Input       Enable for level shifter path. 3.3 V tolerant low-voltage single-ended input. Internal pull-down enables chip when unconnected.         25       OE_N       Input       OE_N       IN_D termination         1       High-Z       High-Z		20	OUT_D2-	Output	OUT_D2- makes a		ut signal with
22     001_D1+     0utput     differential output signal with OUT_D1       23     OUT_D1-     Output     HDMI 1.3 compliant TMDS output. OUT_D1- makes a differential output signal with OUT_D1+.       24     GND     Power     Ground       24     GND     Power     Ground       25     OE_N     Input     Enable for level shifter path. 3.3 V tolerant low-voltage single-ended input. Internal pull-down enables chip when unconnected.       25     OE_N     Input     OE_N     IN_D termination     OUT_D Outputs       1     High-Z     High-Z	10	21	VCC33	Power	3.3 V±10% DC supply		
23       OUT_D1-       Output       HDMI 1.3 compliant TMDS output. OUT_D1- makes a differential output signal with OUT_D1+.         24       GND       Power       Ground         24       GND       Power       Enable for level shifter path. 3.3 V tolerant low-voltage single-ended input. Internal pull-down enables chip when unconnected.         25       OE_N       Input       OE_N       IN_D termination       OUT_D Outputs         1       High-Z       High-Z       High-Z	anson	22	OUT_D1+	Output			
25     OE_N     Input     Enable for level shifter path. 3.3 V tolerant low-voltage single-ended input. Internal pull-down enables chip when unconnected.       25     OE_N     Input     OE_N     IN_D termination     OUT_D Outputs       1     High-Z     High-Z	06	23	OUT_D1-	Output			
25     OE_N     Input     Single-ended input. Internal pull-down enables chip when unconnected.       25     OE_N     Input     OE_N     IN_D termination     OUT_D Outputs       1     High-Z     High-Z		24	GND	Power	Ground		
Impation     Impation     Impation       1     High-Z     High-Z					single-ended input.	Internal pull-dov	0
		25	OE_N	Input	OE_N		OUT_D Outputs
0 50 Ω Active					1	High-Z	High-Z
					0	50 Ω	Active
26 VCC33 Power 3.3 V±10% DC supply		26	VCC33	Power	3.3 V±10% DC sup	pply	

 Table 2.
 Pin description (continued)



	Table 2.	Pin descrip	tion (continued	a)		
	Pin number	Name	Туре		Function	
	27	GND	Power	Ground		
	28	SCL_SINK	Output	<ul> <li>5 V DDC Clock I/O. Pulled-up by external termination to 5 V. Connected to SCL_SOURCE through voltag limiting integrated NMOS pass-gate</li> <li>5V DDC Data I/O. Pulled-up by external termination 5V. Connected to SDA_SOURCE through voltage-limiting integrated NMOS pass-gate</li> <li>Low-frequency, 0V to 5V (nominal) input signal. This signal comes from the HDMI connector. Voltage hig indicates "plugged" state; voltage low indicates "unplugged" state. HPD_SINK is pulled down by an integrated 160KΩ pull-down resistor.</li> </ul>		
	29	SDA_SINK	I/O			
	30	HPD_SINK	Input			
	31	GND	Power	Ground	000	
				Enables bias voltage to the DDC pass-gate gates. (May be implemented as a bias volt connection to the DDC pass-gate themsel		
	32	DDC_EN	Input	DDC_EN	Pass-gate	
				0 V )	Disabled	
			C	3.3 V	Enabled	
	33	VCC33	Power	3.3V±10% DC supply		
	34	FUNCTION3	Input	Used for polarity control of the HPD_SOU When L, the HPD_SOURCE is an open-disand when H, the HPD_SOURCE is a buf (O V to V <sub>CC</sub> )		
16	35	FUNCTION4	Vendor-specific control or test pins	test modes. For normal operation VCC33.	o enable vendor-specific features or on, these pins are tied to GND or operability, GND is the preferred for these signals	
	36	GND	Power	Ground		
	37	GND	Power	Ground		
	38	IN_D1-	Input	•	ial input from GMCH PCIE outputs. ferential pair with IN_D1+.	
	39	IN_D1+	Input		ial input from GMCH PCIE outputs. fferential pair with IN_D1	
	40	VCC33	Power	3.3 V±10% DC sup	ply	
	41	IN_D2-	Input		ial input from GMCH PCIE outputs. ferential pair with IN_D2+.	
	42	IN_D2+	Input		ial input from GMCH PCIE outputs. fferential pair with IN_D2	

 Table 2.
 Pin description (continued)



	Table 2.	r in descrip	tion (continue	u)
	Pin number	Name	Туре	Function
	43	GND	Power	Ground
	44	IN_D3-	Input	Low-swing differential input from GMCH PCIE outputs. IN_D3- makes a differential pair with IN_D3+.
	45	IN_D3+	Input	Low-swing differential input from GMCH PCIE outputs. IN_D3+ makes a differential pair with IN_D3
	46	VCC33	Power	3.3 V±10% DC supply
	47	IN_D4-	Input	Low-swing differential input from GMCH PCIE outputs. IN_D4- makes a differential pair with IN_D4+.
	48	IN_D4+	Input	Low-swing differential input from GMCH PCIE outputs. IN_D4+ makes a differential pair with IN_D4
obsole	te P	roduct		IN_D4+ makes a differential pair with IN_D4-

Table 2. Pin description (continued)



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### 4 Functional description

The section describes the basic functionality of the STHDLS101T device.

### **Power supply**

The STHDLS101T is powered by a single DC power supply of 3.3 V  $\pm$  10%.

### Clocking

This device does not retime any data. The device contains no state machines. No inputs or outputs of the device are latched or clocked.

### Reset

This device acts as a level shifter, reset is not required.

### **OE\_N** function

When OE\_N is asserted (low level), the IN\_D and OUT\_D signals are fully functional. Input termina-tion resistors are enabled and any internal bias circuits are turned on.

OE\_N pin has an internal pull-down that enables the chip if left unconnected.

When OE\_N is de-asserted (high level), the OUT\_D outputs are in high impedance state. The IN\_D input buffers are disabled and the IN\_D termination resistors are disabled. Internal bias circuits for the differential inputs and outputs are turned off. Power consumption of the chip is minimized.

The HPD\_SINK input and HPD\_SOURCE output are not affected by OE\_N. The SCL and SDA pass-gates are not affected by OE\_N.

OE_N	Device state	Comments
Asserted (low level) or unconnected	Differential input buffers and output buffers enabled. Input impedance = 50Ù	Normal functioning state for IN_D to OUT_D level shifting function.
	Low-power state.	Intended for lowest power condition when:
	Differential input buffers and terminations are disabled. Differential input buffers are in high-impedance state.	<ul> <li>No display is plugged in or</li> <li>The level shifted data path is disabled</li> </ul>
De-asserted (high level)	OUT_D level shifting outputs are disabled. OUT_D level shifting outputs are in a high-impedance	HPD_SINK input and HPD_SOURCE output are not affected by OE_N.
	state. Internal bias currents are turned off.	SCL_SOURCE, SCL_SINK, SDA_SOURCE and SDA_SINK signals and functions are not affected by OE_N.

Table 3. OE\_N description



Table 4.	OE N function

	OE_N	IN_Dx	OUT_Dx (TMDS outputs)	Notes
	De-asserted (high level)	High-Z	High-Z	Device disabled. Low power state. Internal bias currents are disabled.
	Asserted or unconnected (low level)	50 $\Omega$ termination	Enabled	Level shifting mode enabled.
				duct(S)
			Pr	00,0
			olete	Level shifting mode enabled.
		00.		
	20	otler		
	Produc			
sole				
262				



# 5 Maximum ratings

Stressing the device above the rating listed in the "Absolute maximum ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage to ground potential	-0.5 to +4.0	CV
VI	DC input voltage (TMDS and PCIe ports)	-0.5 to +4.0	V
	Control pins	-0.5 to +4.0	V
	SDA_SINK, SCL_SINK, HPD_SINK pins	-0.5 to +6	V
Ι <sub>Ο</sub>	DC output current	120	mA
PD	Power dissipation	1	W
T <sub>STG</sub>	Storage temperature	-65 to +150	°C
ΤL	Lead temperature (10 sec)	300	°C
$V_{\text{ESD}}$	Electrostatic discharge voltage on IOs <sup>(1)</sup> Human body model	±6	kV

Table 5. Absolute maximum ratings	Table 5.	Absolute	maximum	ratings
-----------------------------------	----------	----------	---------	---------

1. In accordance with the MIL standard 883 method 3015

### Table 6.Thermal data

	Symbol	Parameter	QFN-48	Unit
	θ <sub>JA</sub>	Junction-ambient thermal coefficient	48	°C/W
Obsole	je i			

#### **Recommended operating conditions** 5.1

#### 5.1.1 Power supply and temperature range

#### Table 7. Power supply and temperature range

Symbol	Parameter	Parameter Comments			Мах	Unit			
V <sub>CC33</sub>	3.3 V power supply	3.3 V power supply			3.6	V			
I <sub>CC</sub>	Maximum power supply current	Total current from V <sub>CC</sub> 3.3 V power supply			100	mA			
Т	Operating temperature range		-40		85	°C			
5.1.2 Table 8.									
Symbol	Parameter	Comments	Mi	n Ty	p Max	Unit			

#### Differential inputs (IN\_D signals) 5.1.2

#### Table 8. Differential input characteristics for IN\_D signals

Symbol	Parameter	Comments	Min	Тур	Max	Unit
Tbit	Unit interval	Tbit is determined by the display mode. Nominal bit rate ranges from 250 Mbps to 2.5 Gbps per lane. Nominal Tbit at 2.5 Gbps = 400 ps. 360 ps = 400 ps - 10%	360			ps
V <sub>RX-DIFFp-p</sub>	Differential input peak to peak voltage	V <sub>RX-DIFFp-p</sub> =2*IV <sub>RX-D+</sub> - V <sub>RX-</sub> <sub>D-</sub> I. Applies to IN_D signals.	0.175		1.2	V
T <sub>RX-EYE</sub>	Minimum eye width at IN_D input pair	The level shifter may add a maximum of 0.02UI jitter	0.8			Tbit
V <sub>CM-AC-pp</sub>	AC peak common mode input voltage	VCM-AC-pp=IVRX-D+ + VRX-D-I/2 - VRX-CM-DC. VRX-CM-DC=DC(avg) of IVRX-D+ + VRX-D-I/2 VCM-AC-pp includes all frequencies above 30 kHz.			100	mV
Z <sub>RX-DC</sub>	DC single-ended input impedance	Applies to IN_D+ as well as IN_D- pins (50 $\Omega \pm 20\%$ tolerance)	40	50	60	Ω
V <sub>RX-Bias</sub>	RX input termination voltage	Intended to limit power-up stress on chipset's PCIE output buffers	0		2	V
Z <sub>RX-HIGH-Z</sub>	Single-ended input resistance for IN_Dx when inputs are in high-Z state	Differential inputs must be in a high impedance state	100			KΩ

## 5.2 TMDS outputs (OUT\_D signals)

The level shifter's TMDS outputs are required to meet the HDMI 1.3 specifications. The HDMI 1.3 specification is assumed to be the correct reference in instances where this document conflicts with the HDMI 1.3 specification.

Symbol	Parameter	Comments	Min	Тур	Max	Unit
V <sub>H</sub>	Single-ended high level output voltage	$AV_{CC}$ is the DC termination voltage in the HDMI or DVI sink. $AV_{CC}$ is nominally 3.3 V	AV <sub>CC</sub> -10 mV	AV <sub>CC</sub>	AV <sub>CC</sub> +10 m V	V
VL	Single-ended low level output voltage	The open-drain output pullsAVAVdown form AVCC600 mV500 mV		AV <sub>CC</sub> - 400 mV	×	
V <sub>SWING</sub>	Single-ended output swing voltage	Swing down from TMDS termination voltage 400 mV 500 n (3.3 V ±10%)		500 mV	600 mV	V
I <sub>OFF</sub>	Single-ended current in high-Z state	Measured with TMDS outputs pulled up to $AV_{CC}$ max (3.6 V) through 50 $\Omega$ resistors	*6	Pro	10	μΑ
Τ <sub>R</sub>	Rise time	Maximum rise/fall time at 2.7 Gbps = 148ps. 125ps = 148 – 15%		0.4 Tbit	ps	
Τ <sub>F</sub>	Fall time	Maximum rise/fall time at 2.7 Gbps = 148 ps. 125ps = 148 - 15%	2.7 Gbps = 148 ps. 125 ps		0.4 Tbit	ps
T <sub>SKEW-</sub> INTRA	Intra-pair differential skew	This differential skew budget is in addition to the skew presented between D+ and D- paired input pins.		10	ps	
T <sub>SKEW-</sub> INTER	Inter-pair lane to lane output skew	This lane to lane skew budget is in addition to the skew between differential input pairs.			250	ps
Тлт	Jitter added to TMDS signals	Jitter budget for TMDS signals as they pass through the level shifter. 7.4 ps = 0.02 Tbit at 2.7 Gbps			7.4	ps

 Table 9.
 Differential output characteristics for TMDS OUT\_D signals



# 5.3 HPD input and output characteristics

Symbol	Parameter	Comment	Min	Тур	Max	Uni
V <sub>IH-HPD_SINK</sub>	HPD_SINK input high level	Low speed input changes state on cable plug/unplug	2	5.0	5.3	V
V <sub>IL-HPD_SINK</sub>	HPD_SINK input low level		0		0.8	V
I <sub>IN-HPD_SINK</sub>	HPD_SINK input leakage current	Measured with HPD_SINK at $V_{IH\text{-}HPD}$ max and $V_{IL\text{-}}$ $_{HPD}$ min			50	μA
V <sub>OH-</sub> HPD_SOURCE (INV)	HPD_SOURCE output high level when FUNCTION3 = L	$V_{CC} = 3.3 V \pm 10\%$ Based on external pull-up resistor; output is open drain.		20	ctle	5
V <sub>OL-</sub> HPD_SOURCE	HPD_SOURCE output low level when FUNCTION3 = H	V <sub>CC</sub> = 3.3 V ±10%	2.5	30.	$V_{CC}$	V
V <sub>OH-</sub> HPD_SOURCE (INV)	HPD_SOURCE output high level when FUNCTION3 = L	$V_{CC} = 3.3 \text{ V} \pm 10\%$ $I_{OL} = 1 \text{ mA}$	0		0.2	V
V <sub>OL-</sub> HPD_SOURCE	HPD_SOURCE output low level when FUNCTION3 = H	$V_{CC} = 3.3 V \pm 10\%$	0		0.2	V
T <sub>HPD</sub>	HPD_SINK to HPD_SOURCE propagation delay	Time from HPD_SINK changing state to HPD_SOURCE changing state. Includes HPD_SOURCE rise/fall time C <sub>L</sub> =10 pF			200	ns
T <sub>RF-HPD</sub>	HPD_SOURCE rise/fall time	Time required to transition from $V_{OH-HPD}SOURCE$ to $V_{OL-HPD}SOURCE$ or from $V_{OL-HPD}SOURCE$ to $V_{OH}$ HPD_SOURCE $C_L$ =10 pF	1		20	ns

Table 10. HPD\_SINK input and HPS\_SOURCE output



# 5.4 DDC input and output chatacteristics

Table 11.	SDA_SOURCE, SCL_SOURCE and SDA_SINK, SCL_SINK characteristics
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Symb ol	Parameter	Comment	Min	Тур	Max	Unit
VI	Input voltage on SDA_SINK, SCL_SINK pins	Voltage on the DDC pins on connector end	0		5.5	V
I <sub>LKG</sub>	Input leakage current on SDA_SINK, SCL_SINK pins	$V_{CC} = 3.3 \text{ V}$ $V_{I} = 0.1 V_{DD} \text{ to } 0.9 \text{ V}_{DD} \text{ to}$ isolated DDC inputs $V_{DD} = \text{ external pull-up}$ resistor voltage on SDA_SINK and SCL_SINK inputs (maximum of 5.5 V)	-10		10	μΑ
IOFF	Power-down leakage current on SDA_SINK, SCL_SINK pins	$V_{CC} = 0.0 V$ $V_{I} = 0.1 V_{DD} \text{ to } 0.9 V_{DD} \text{ to}$ $DDC \text{ sink inputs}$ $V_{DD} = \text{ external pull-up}$ $resistor voltage \text{ on}$ $SDA\_SINK \text{ and SCL}\_SINK$ $inputs (maximum of 5.5 V)$ $SDA\_SOURCE,$ $SCL\_SOURCE = 0.0 V$	-10		10	μΑ
C <sub>I/O</sub>	Input/output capacitance (switch off)	V <sub>I(pp)</sub> =1 V, 100 KHz V <sub>CC</sub> =3.3 V, T=25C		5		pF
C <sub>I/O</sub>	Input/output capacitance (switch on)	$V_{I(pp)}$ =1 V, 100KHz V <sub>CC</sub> = 3.3 V, T= 25 ° C			10	pF
R <sub>ON</sub>	Switch resistance	I <sub>O</sub> =3 mA, V <sub>O</sub> = 0.4 V V <sub>CC</sub> = 3.3 V		27	40	Ω
TPD	DDC_SINK to DDC_SOURCE propagation delay	Time from DDC_SINK changing state to DDC_SOURCE changing state while the pass gate is enabled. $C_L=10 \text{ pF}$ $R_{PU}=1.5 \text{ K} \text{ (min)}, 2.0 \text{ K}$ (max)		8	15	ns
т <sub>sx</sub>	Switch time from DDC_EN to the valid state on DDC_SOURCE	C <sub>L</sub> = 10 pF R <sub>PU</sub> = 1.5 K (min), 2.0 K (max)		8	15	ns

#### **OE\_** input characteristics 5.5

Table 12.	OE_N input characterist	ics
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Symbol	Parameter	Comment	Min	Тур	Мах	Unit
V <sub>IH-OE_N</sub>	Input high level		2		VCC33	V
V <sub>IL-OE_N</sub>	Input low level		0		0.8	V
I <sub>IN-OE_N</sub>	Input leakage current	Measured with OE_N at VIH-OE_N max and VIL- OE_N mix			200	μA

#### **HPD** input resistor 5.6

#### Table 13. **HDP** input resistor

		- =				
5.6	HPD input resistor			21	Jotle	5
Table 13.	HDP input resistor			00		
Symbol	Parameter	Comment	М	in Ty	p Max	Unit
R <sub>HPD</sub>	HPD_SINK input pull-down resistor	Guarantees HPD_SINK is LOW when no display is plugged in	s 130	) K 160	) К 190 К	Ω
5.7	ESD performance	Obse	·	·		
Table 14.	ESD performance	7				

#### ESD performance 5.7

#### ESD performance Table 14.

Symbol	Parameter	Test condition	Min	Тур	Max	Un
ESD	MIL STD 883 method 3015 (all pins)	Human Body Model (HBM)	I (HBM) -6		+6	kV
E3D			-0		+0	Ľ
	010					
	×C					
Ċ	16.					
SC	le.					



### 6 Application information

### 6.1 **Power supply sequencing**

Proper power-supply sequencing is advised for all CMOS devices. It is recommended to always apply  $V_{CC}$  before applying any signals to the input/output or control pins.

### 6.2 Supply bypassing

Bypass each of the V<sub>CC</sub> pins with 0.1  $\mu F$  and 1nF capacitors in parallel as close to the device as possible, with the smaller-valued capacitor as close to the V<sub>CC</sub> pin of the device as possible.

### 6.3 Differential traces

The high-speed inputs and TMDS outputs are the most critical parts for the device. There are several considerations to minimize discontinuities on these transmission lines between the connectors and the device.

(a) Maintain 100  $\Omega$  differential transmission line impedance into and out of the device.

(b) Keep an uninterrupted ground plane below the high-speed I/Os.

(c) Keep the ground-path vias to the device as close as possible to allow the shortest return current path.

(d) Layout of the TMDS differential outputs should be with the shortest stubs from the connectors.

Output trace characteristics affect the performance of the STHDLS101T. Use controlled impedance traces to match trace impedance to both the transmission medium impedance and termination resistor. Run the differential traces close together to minimize the effects of the noise. Reduce skew by matching the electrical length of the traces. Avoid discontinuities in the differential trace layout. Avoid 90 degree turns and minimize the number of vias to further prevent impedance discontinuities.



### 7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK<sup>®</sup> packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

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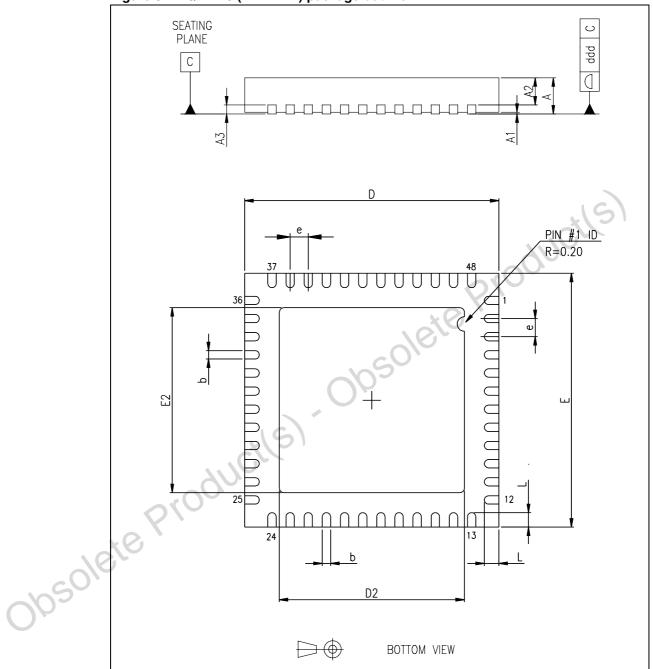


Figure 6. QFN-48 (7 x 7 mm) package outline

			age meena	nour duta		
Symbol	Min	Тур	Max	Min	Тур	Max
А	0.80	0.90	1.00	0.80	0.85	1.00
A1		0.02	0.05		0.01	0.05
A2		0.65	1.00		0.65	
A3		0.25			0.20	
b	0.18	0.23	0.30	0.18	0.23	0.30
D	6.85	7.00	7.15	6.90	7.00	7.10
D2	2.25	4.70	5.25	SEE EXPO	SED PAD VAF	IATIONS
E	6.85	7.00	7.15	6.90	7.00	7.10
E2	2.25	4.70	5.25	SEE EXPO	SED PAD VAF	IATIONS
е	0.45	0.50	0.55	0.45	0.50	0.55
L	0.30	0.40	0.50	0.30	0.40	0.50
ddd			0.08			0.08

Table 15. QFN-48 (7 x 7 mm) package mechanical data



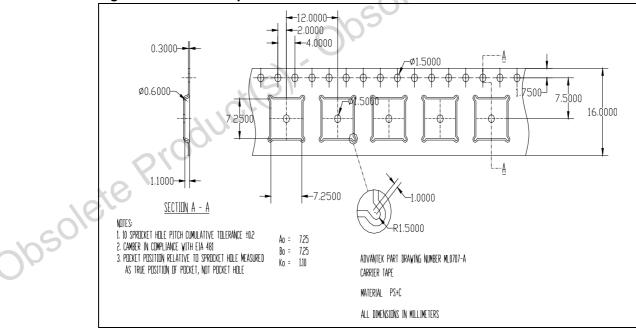


Figure 8. Reel information

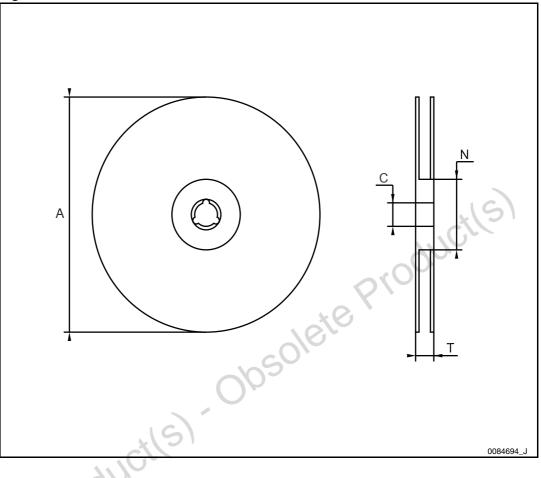


Table 16.	Reel mechanical data	(dimensions in mm)
Table To.	neel mechanical uala	

Q	A	С	Ν	т
	330.2	13 ±0.25	100	16.4
colerc				
-103				

# 8 Revision history

### Table 17. Document revision history

	Date	Revision	Changes		
	30-Jun-2008	1	Initial release.		
	24-Sep-2008	2	Document status promoted from preliminary data to datasheet. Modified: features section, <i>Table 2: Pin description on page 8</i> and <i>Section 4: Functional description</i> .		
	01-Dec-2008	3	Updated: Features section and <i>Chapter 5: Maximum ratings</i> Added: Figure 3: Cable adapter on page 5, Figure 4: DP to HDMI/DVI cable adapter on page 6, Figure 8: Reel information on page 24 and Table 16: Reel mechanical data (dimensions in mm) on page 24		
obsolete Product(s) - Obsolete Product(s) - Obsolete Product(s)					



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