STHDLS101T

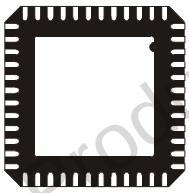
AC coupled HDMI level shifter with configurable HPD output

Features

- Converts low-swing alternating current (AC) coupled differential input to high-definition multimedia interface (HDMI) rev 1.3 compliant
- HDMI level shifting operation up to 2.7 Gbps per lane
- Integrated 50-Ω termination resistors for AC-coupled differential inputs
- Input/output transition minimized differential signaling (TMDS) enable/disable
- Output slew rate control on TMDS outputs to minimize electromagnetic interference (EMI)
- Fail safe outputs for backdrive protection
- No re-timing or configuration required
- Inter-pair output skew < 250 ps
- Intra-pair output skew < 10 ps
- Single power supply of 3.3 V
- ESD protection: ±6 KV HBM on all I/O pins
- Integrated display data channel (DDC) level shifters. Pass-gate voltage limiters allow 3.3 V termination on graphics and memory controller hub (GMCH) pins and 5 V DDC termination on HDMI connector pins
- Level shifter and configurable output for HPD signal from HDMI/DVI connector
- Integrated pull-down resistor on HPD_SINK and OE_N inputs

Applications

- Notebooks
- PC motherboards and graphic cards
- Dongles/cable adapters



QFN-48
(7 x 7 mm)

Description

The STHDLS101T is a high-speed high-definition multimedia interface (HDMI) level shifter that converts low-swing AC coupled differential input to HDMI 1.3 compliant open-drain current steering RX-terminated differential output. Through the existing PCI-E pins in the graphics and memory controller hub (GMCH) of PCs or notebook motherboards, the pixel clock provides the required bandwidth (1.65 Gbps, 2.25 Gbps) for the video supporting 720p, 1080i, 1080p with a total of 36-bit resolution. The HDMI is multiplexed onto the PCIe pins in the motherboard where the AC coupled HDMI at 1.2 V is output by GMCH. The AC coupled HDMI is then level shifter by this device to 3.3 V DC coupled HDMI output.

The STHDLS101T supports up to 2.7 Gbps, which is enough for 12-bits of color depth per channel, as indicated in HDMI rev 1.3. The device operates from a single 3.3 V supply and is available in a 48-pin QFN package.

Table 1. Device summary

Order code	Package	Packaging
STHDLS101TQTR	QFN-48	Tape and reel

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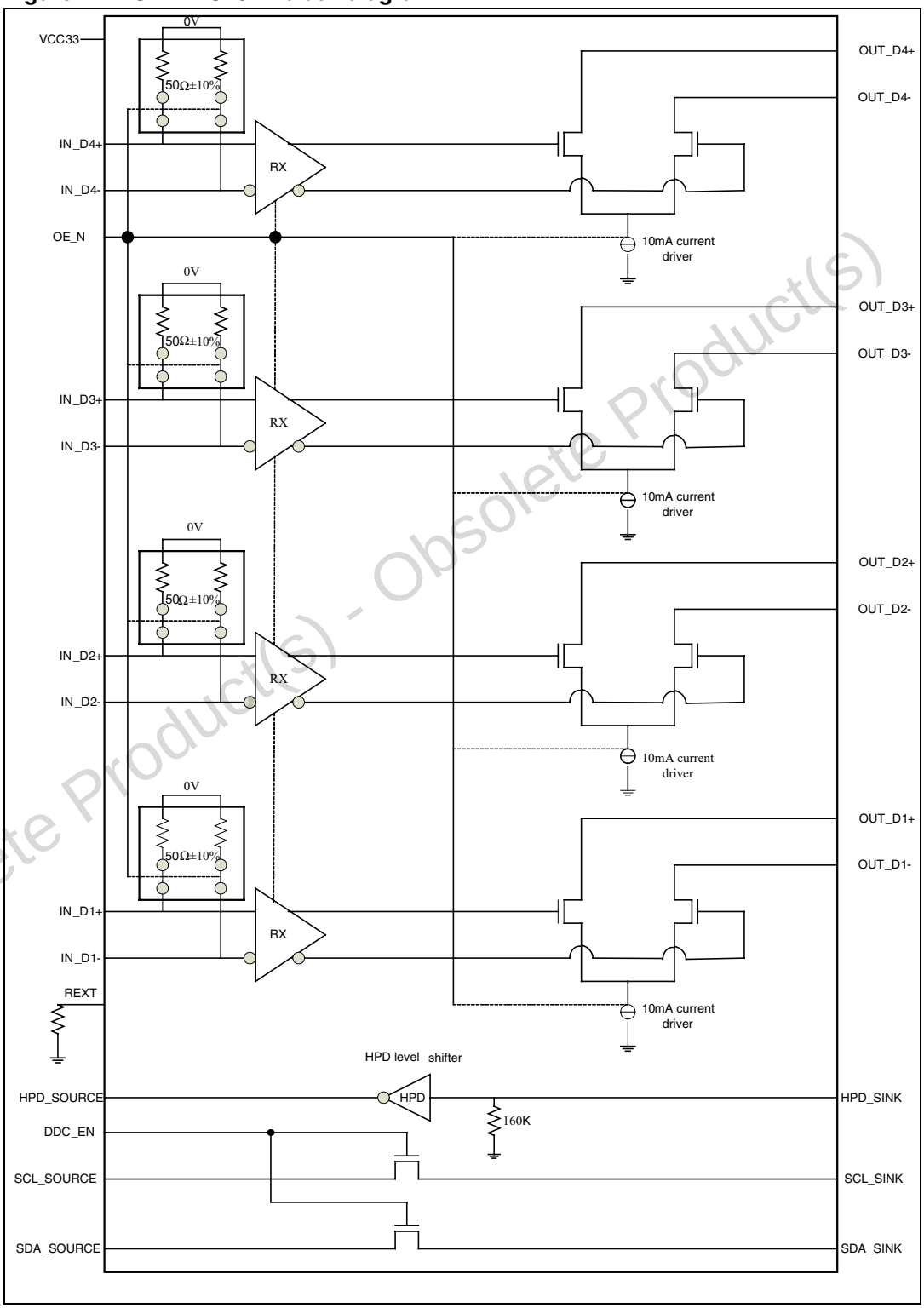
1 Block diagram

Figure 1. STHDLS101T block diagram



2 System interface

Figure 2. System inferface

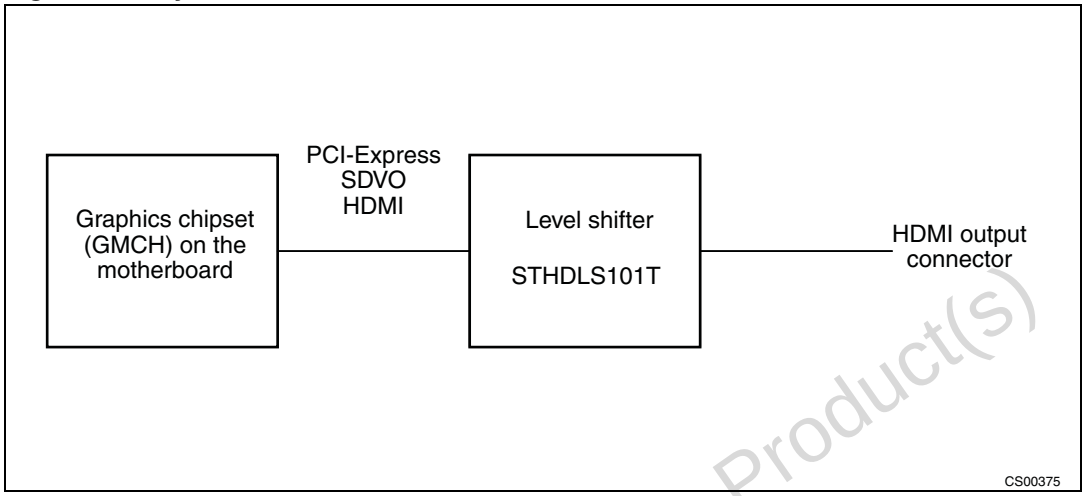


Figure 3. Cable adapter

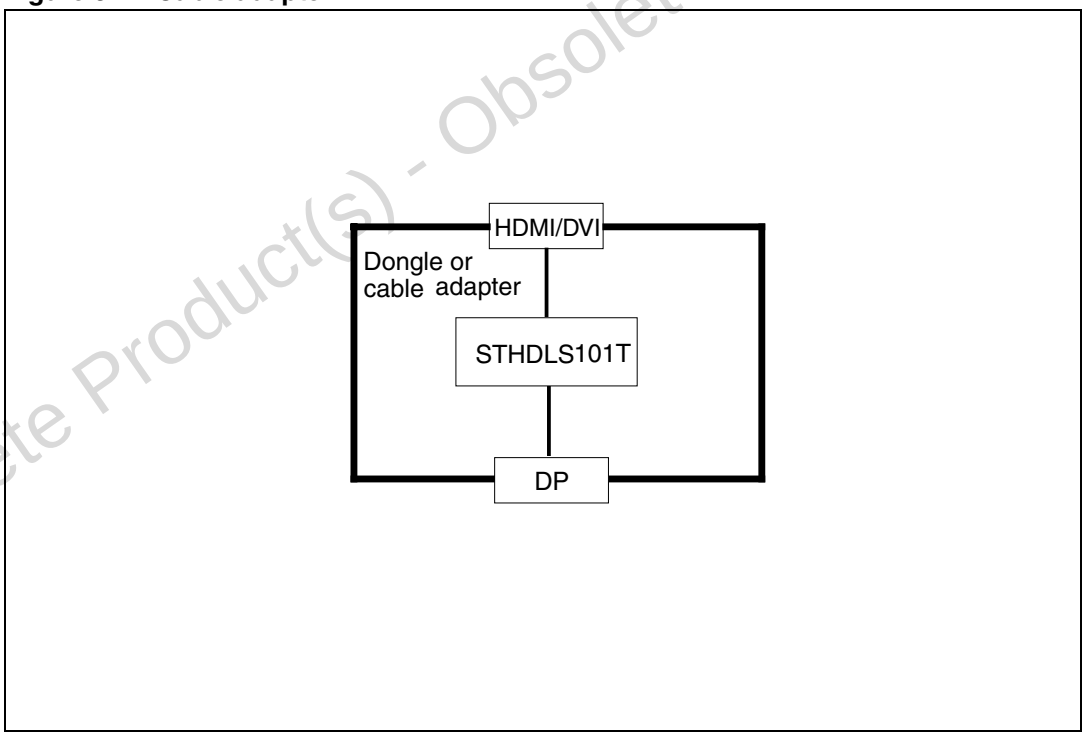
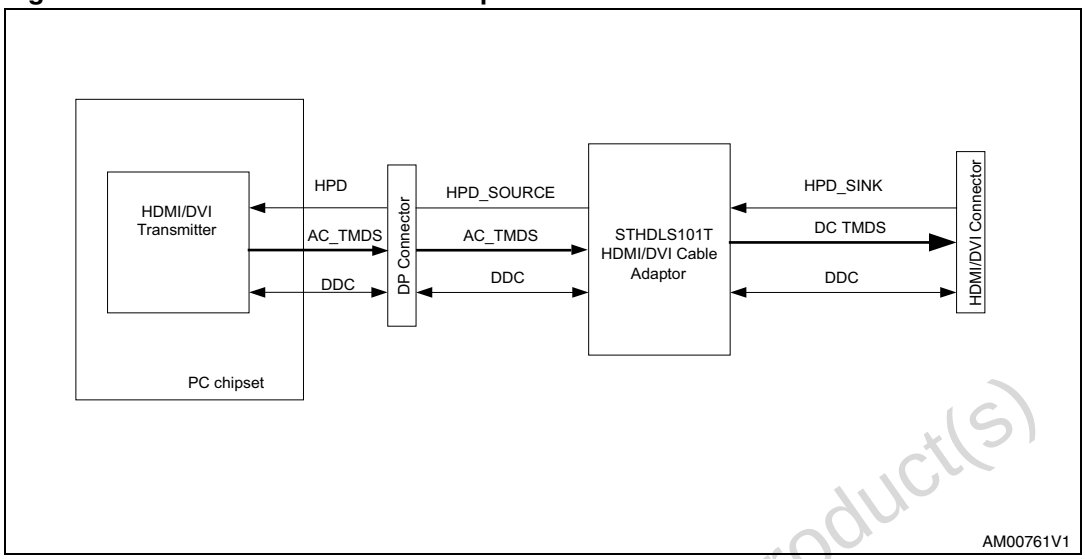
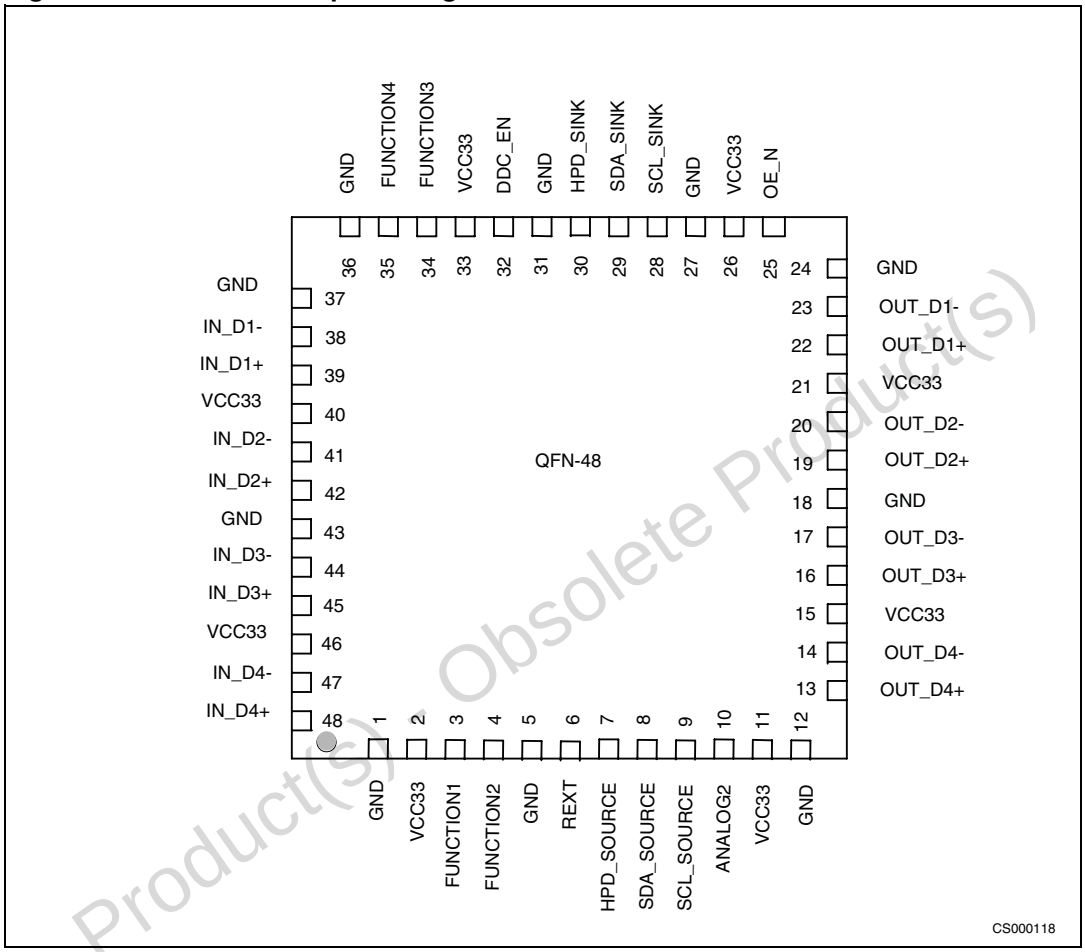


Figure 4. DP to HDMI/DVI cable adapter



3 Pin configuration

Figure 5. STHDLS101T pin configuration



3.1 Pin description

Table 2. Pin description

Pin number	Name	Type	Function		
1	GND	Power	Ground		
2	VCC33	Power	3.3V±10% DC supply		
3	FUNCTION1	Vendor-specific control or test pins	Function pins are to enable vendor-specific features or test modes. For normal operation, these pins are tied to GND or VCC33. For consistent interoperability, GND is the preferred default connection for these signals		
4	FUNCTION2	Vendor-specific control or test pins	Function pins are to enable vendor-specific features or test modes. For normal operation, these pins are tied to GND or VCC33. For consistent interoperability, GND is the preferred default connection for these signals		
5	GND	Power	Ground		
6	REXT	Analog	Connection to external resistor. Resistor value specified by device manufacturer. Acceptable connections to this pin are: - Resistor to GND - Resistor to 3.3V; - NC (direct connections to V_{CC} or GND are through a 0-Ù resistor for layout compatibility		
7	HPD_SOURCE	Output	Buffer from the 0 V to 5 V input signal. The output buffer stage is configurable based on the FUNCTION3 pin settings as desribed in the table below:		
			FUNCTION3	**HPD_SINK**	**HPD_SOURCE**
			0	Low	Open-drain, connected an external pull up to the desired supply (normally 1 V)
			0	High (5 V)	Low (0 V)
			1	Low (0 V)	Low (0 V)
			1	High (5 V)	High (3 V)
8	SDA_SOURCE	I/O	3.3 V DDC data I/O. Pulled-up by external termination to 3.3 V. Connected to SDA_SINK through voltage-limiting integrated NMOS pass-gate		
9	SCL_SOURCE	Input	3.3 V DDC clock I/O. Pulled-up by external termination to 3.3 V. Connected to SCL_SINK through voltage-limiting integrated NMOS pass-gate		

Table 2. Pin description (continued)

Pin number	Name	Type	Function
10	ANALOG2	Analog	Analog connection determined by vendor. Acceptable connections to this pin are: - Resistor or capacitor to GND - Resistor or capacitor to 3.3 V - Short to 3.3 V or to GND - NC
11	VCC33	Power	3.3 V ±10% DC supply
12	GND	Power	Ground
13	OUT_D4+	Output	HDMI 1.3 compliant TMDS output. OUT_D4+ makes a differential output signal with OUT_D4-.
14	OUT_D4-	Output	HDMI 1.3 compliant TMDS output. OUT_D4- makes a differential output signal with OUT_D4+.
15	VCC33	Power	3.3 V±10% DC supply
16	OUT_D3+	Output	HDMI 1.3 compliant TMDS output. OUT_D3+ makes a differential output signal with OUT_D3-.
17	OUT_D3-	Output	HDMI 1.3 compliant TMDS output. OUT_D3- makes a differential output signal with OUT_D3+.
18	GND	Power	Ground
19	OUT_D2+	Output	HDMI 1.3 compliant TMDS output. OUT_D2+ makes a differential output signal with OUT_D2-.
20	OUT_D2-	Output	HDMI 1.3 compliant TMDS output. OUT_D2- makes a differential output signal with OUT_D2+.
21	VCC33	Power	3.3 V±10% DC supply
22	OUT_D1+	Output	HDMI 1.3 compliant TMDS output. OUT_D1+ makes a differential output signal with OUT_D1-.
23	OUT_D1-	Output	HDMI 1.3 compliant TMDS output. OUT_D1- makes a differential output signal with OUT_D1+.
24	GND	Power	Ground
25	OE_N	Input	Enable for level shifter path. 3.3 V tolerant low-voltage single-ended input. Internal pull-down enables chip when unconnected.
			OE_N / **IN_D termination** / **OUT_D Outputs**
			1 / High-Z / High-Z
			0 / 50 Ω / Active
26	VCC33	Power	3.3 V±10% DC supply

Table 2. Pin description (continued)

Pin number	Name	Type	Function
27	GND	Power	Ground
28	SCL_SINK	Output	5 V DDC Clock I/O. Pulled-up by external termination to 5 V. Connected to SCL_SOURCE through voltage-limiting integrated NMOS pass-gate
29	SDA_SINK	I/O	5V DDC Data I/O. Pulled-up by external termination to 5V. Connected to SDA_SOURCE through voltage-limiting integrated NMOS pass-gate
30	HPD_SINK	Input	Low-frequency, 0V to 5V (nominal) input signal. This signal comes from the HDMI connector. Voltage high indicates “plugged” state; voltage low indicates “unplugged” state. HPD_SINK is pulled down by an integrated 160KΩ pull-down resistor.
31	GND	Power	Ground
32	DDC_EN	Input	Enables bias voltage to the DDC pass-gate level shifter gates. (May be implemented as a bias voltage connection to the DDC pass-gate themselves).
			DDC_EN / **Pass-gate**
			0 V / Disabled
			3.3 V / Enabled
33	VCC33	Power	3.3V±10% DC supply
34	FUNCTION3	Input	Used for polarity control of the HPD_SOURCE output. When L, the HPD_SOURCE is an open-drain output sand when H, the HPD_SOURCE is a buffered output (O V to V_{CC})
35	FUNCTION4	Vendor-specific control or test pins	Function pins are to enable vendor-specific features or test modes. For normal operation, these pins are tied to GND or VCC33. For consistent interoperability, GND is the preferred default connection for these signals
36	GND	Power	Ground
37	GND	Power	Ground
38	IN_D1-	Input	Low-swing differential input from GMCH PCIE outputs. IN_D1- makes a differential pair with IN_D1+.
39	IN_D1+	Input	Low-swing differential input from GMCH PCIE outputs. IN_D1+ makes a differential pair with IN_D1-.
40	VCC33	Power	3.3 V±10% DC supply
41	IN_D2-	Input	Low-swing differential input from GMCH PCIE outputs. IN_D2- makes a differential pair with IN_D2+.
42	IN_D2+	Input	Low-swing differential input from GMCH PCIE outputs. IN_D2+ makes a differential pair with IN_D2-.

Table 2. Pin description (continued)

Pin number	Name	Type	Function
43	GND	Power	Ground
44	IN_D3-	Input	Low-swing differential input from GMCH PCIE outputs. IN_D3- makes a differential pair with IN_D3+.
45	IN_D3+	Input	Low-swing differential input from GMCH PCIE outputs. IN_D3+ makes a differential pair with IN_D3-.
46	VCC33	Power	3.3 V±10% DC supply
47	IN_D4-	Input	Low-swing differential input from GMCH PCIE outputs. IN_D4- makes a differential pair with IN_D4+.
48	IN_D4+	Input	Low-swing differential input from GMCH PCIE outputs. IN_D4+ makes a differential pair with IN_D4-.

4 Functional description

The section describes the basic functionality of the STHDLS101T device.

Power supply

The STHDLS101T is powered by a single DC power supply of 3.3 V ± 10%.

Clocking

This device does not retime any data. The device contains no state machines. No inputs or outputs of the device are latched or clocked.

Reset

This device acts as a level shifter, reset is not required.

OE_N function

When OE_N is asserted (low level), the IN_D and OUT_D signals are fully functional. Input termina-tion resistors are enabled and any internal bias circuits are turned on.

OE_N pin has an internal pull-down that enables the chip if left unconnected.

When OE_N is de-asserted (high level), the OUT_D outputs are in high impedance state. The IN_D input buffers are disabled and the IN_D termination resistors are disabled. Internal bias circuits for the differential inputs and outputs are turned off. Power consumption of the chip is minimized.

The HPD_SINK input and HPD_SOURCE output are not affected by OE_N. The SCL and SDA pass-gates are not affected by OE_N.

Table 3. OE_N description

OE_N	Device state	Comments
Asserted (low level) or unconnected	Differential input buffers and output buffers enabled. Input impedance = 50Ù	Normal functioning state for IN_D to OUT_D level shifting function.
De-asserted (high level)	Low-power state. Differential input buffers and terminations are disabled. Differential input buffers are in high-impedance state. OUT_D level shifting outputs are disabled. OUT_D level shifting outputs are in a high-impedance state. Internal bias currents are turned off.	Intended for lowest power condition when: • No display is plugged in or • The level shifted data path is disabled HPD_SINK input and HPD_SOURCE output are not affected by OE_N. SCL_SOURCE, SCL_SINK, SDA_SOURCE and SDA_SINK signals and functions are not affected by OE_N.

Table 4. OE_N function

OE_N	IN_Dx	OUT_Dx (TMDS outputs)	Notes
De-asserted (high level)	High-Z	High-Z	Device disabled. Low power state. Internal bias currents are disabled.
Asserted or unconnected (low level)	50 Ω termination	Enabled	Level shifting mode enabled.

5 Maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 5. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage to ground potential		-0.5 to +4.0	V
V_I	DC input voltage (TMDS and PCIe ports)		-0.5 to +4.0	V
	Control pins		-0.5 to +4.0	V
	SDA_SINK, SCL_SINK, HPD_SINK pins		-0.5 to +6	V
I_O	DC output current		120	mA
P_D	Power dissipation		1	W
T_{STG}	Storage temperature		-65 to +150	°C
T_L	Lead temperature (10 sec)		300	°C
V_{ESD}	Electrostatic discharge voltage on IOs(1)	Human body model	±6	kV

1. In accordance with the MIL standard 883 method 3015

Table 6. Thermal data

Symbol	Parameter	QFN-48	Unit
θ_{JA}	Junction-ambient thermal coefficient	48	°C/W

5.1 Recommended operating conditions

5.1.1 Power supply and temperature range

Table 7. Power supply and temperature range

Symbol	Parameter	Comments	Min	Typ	Max	Unit
V_{CC33}	3.3 V power supply		3.0	3.3	3.6	V
I_{CC}	Maximum power supply current	Total current from V_{CC} 3.3 V power supply			100	mA
T	Operating temperature range		-40		85	°C

5.1.2 Differential inputs (IN_D signals)

Table 8. Differential input characteristics for IN_D signals

Symbol	Parameter	Comments	Min	Typ	Max	Unit
Tbit	Unit interval	Tbit is determined by the display mode. Nominal bit rate ranges from 250 Mbps to 2.5 Gbps per lane. Nominal Tbit at 2.5 Gbps = 400 ps. 360 ps = 400 ps – 10%	360			ps
$V_{RX-DIFFp-p}$	Differential input peak to peak voltage	$V_{RX-DIFFp-p}$=2*|V_{RX-D+} - V_{RX-D-}|. Applies to IN_D signals.	0.175		1.2	V
T_{RX-EYE}	Minimum eye width at IN_D input pair	The level shifter may add a maximum of 0.02UI jitter	0.8			Tbit
$V_{CM-AC-pp}$	AC peak common mode input voltage	VCM-AC-pp=|VRX-D+ + VRX-D-|/2 – VRX-CM-DC. VRX-CM-DC=DC(avg) of |VRX-D+ + VRX-D-|/2 VCM-AC-pp includes all frequencies above 30 kHz.			100	mV
Z_{RX-DC}	DC single-ended input impedance	Applies to IN_D+ as well as IN_D- pins (50 Ω ± 20% tolerance)	40	50	60	Ω
$V_{RX-Bias}$	RX input termination voltage	Intended to limit power-up stress on chipset's PCIE output buffers	0		2	V
$Z_{RX-HIGH-Z}$	Single-ended input resistance for IN_Dx when inputs are in high-Z state	Differential inputs must be in a high impedance state	100			KΩ

5.2 TMDS outputs (OUT_D signals)

The level shifter's TMDS outputs are required to meet the HDMI 1.3 specifications. The HDMI 1.3 specification is assumed to be the correct reference in instances where this document conflicts with the HDMI 1.3 specification.

Table 9. Differential output characteristics for TMDS OUT_D signals

Symbol	Parameter	Comments	Min	Typ	Max	Unit
V_H	Single-ended high level output voltage	AV_{CC} is the DC termination voltage in the HDMI or DVI sink. AV_{CC} is nominally 3.3 V	AV_{CC}-10 mV	AV_{CC}	AV_{CC}+10 mV	V
V_L	Single-ended low level output voltage	The open-drain output pulls down form AV_{CC}	AV_{CC}- 600 mV	AV_{CC}- 500 mV	AV_{CC}- 400 mV	V
V_{SWING}	Single-ended output swing voltage	Swing down from TMDS termination voltage (3.3 V ±10%)	400 mV	500 mV	600 mV	V
I_{OFF}	Single-ended current in high-Z state	Measured with TMDS outputs pulled up to AV_{CC} max (3.6 V) through 50 Ω resistors			10	µA
T_R	Rise time	Maximum rise/fall time at 2.7 Gbps = 148ps. 125ps = 148 – 15%	125 ps		0.4 Tbit	ps
T_F	Fall time	Maximum rise/fall time at 2.7 Gbps = 148 ps. 125ps = 148 – 15%	125 ps		0.4 Tbit	ps
$T_{SKEW-INTRA}$	Intra-pair differential skew	This differential skew budget is in addition to the skew presented between D+ and D- paired input pins.			10	ps
$T_{SKEW-INTER}$	Inter-pair lane to lane output skew	This lane to lane skew budget is in addition to the skew between differential input pairs.			250	ps
T_{JIT}	Jitter added to TMDS signals	Jitter budget for TMDS signals as they pass through the level shifter. 7.4 ps = 0.02 Tbit at 2.7 Gbps			7.4	ps

5.3 HPD input and output characteristics

Table 10. HPD_SINK input and HPS_SOURCE output

Symbol	Parameter	Comment	Min	Typ	Max	Unit
$V_{IH\text{-}HPD\_SINK}$	HPD_SINK input high level	Low speed input changes state on cable plug/unplug	2	5.0	5.3	V
$V_{IL\text{-}HPD\_SINK}$	HPD_SINK input low level		0		0.8	V
$I_{IN\text{-}HPD\_SINK}$	HPD_SINK input leakage current	Measured with HPD_SINK at $V_{IH\text{-}HPD}$ max and $V_{IL\text{-}HPD}$ min			50	µA
$V_{OH\text{-}HPD\_SOURCE}$ (INV)	HPD_SOURCE output high level when FUNCTION3 = L	V_{CC} = 3.3 V ±10% Based on external pull-up resistor; output is open drain.				
$V_{OL\text{-}HPD\_SOURCE}$	HPD_SOURCE output low level when FUNCTION3 = H	V_{CC} = 3.3 V ±10%	2.5		V_{CC}	V
$V_{OH\text{-}HPD\_SOURCE}$ (INV)	HPD_SOURCE output high level when FUNCTION3 = L	V_{CC} = 3.3 V ±10% I_{OL} = 1 mA	0		0.2	V
$V_{OL\text{-}HPD\_SOURCE}$	HPD_SOURCE output low level when FUNCTION3 = H	V_{CC} = 3.3 V ±10%	0		0.2	V
T_{HPD}	HPD_SINK to HPD_SOURCE propagation delay	Time from HPD_SINK changing state to HPD_SOURCE changing state. Includes HPD_SOURCE rise/fall time C_L=10 pF			200	ns
$T_{RF\text{-}HPD}$	HPD_SOURCE rise/fall time	Time required to transition from $V_{OH\text{-}HPD\_SOURCE}$ to $V_{OL\text{-}HPD\_SOURCE}$ or from $V_{OL\text{-}HPD\_SOURCE}$ to $V_{OH\text{-}HPD\_SOURCE}$ C_L=10 pF	1		20	ns

5.4 DDC input and output chatacteristics

Table 11. SDA_SOURCE, SCL_SOURCE and SDA_SINK, SCL_SINK characteristics

Symbol	Parameter	Comment	Min	Typ	Max	Unit
V_I	Input voltage on SDA_SINK, SCL_SINK pins	Voltage on the DDC pins on connector end	0		5.5	V
I_{LKG}	Input leakage current on SDA_SINK, SCL_SINK pins	V_{CC} = 3.3 V V_I =0.1V_{DD} to 0.9 V_{DD} to isolated DDC inputs V_{DD} = external pull-up resistor voltage on SDA_SINK and SCL_SINK inputs (maximum of 5.5 V)	-10		10	µA
I_{OFF}	Power-down leakage current on SDA_SINK, SCL_SINK pins	V_{CC} = 0.0 V V_I = 0.1 V_{DD} to 0.9 V_{DD} to DDC sink inputs V_{DD} = external pull-up resistor voltage on SDA_SINK and SCL_SINK inputs (maximum of 5.5 V) SDA_SOURCE, SCL_SOURCE = 0.0 V	-10		10	µA
$C_{I/O}$	Input/output capacitance (switch off)	$V_{I(pp)}$=1 V, 100 KHz V_{CC}=3.3 V, T=25C		5		pF
$C_{I/O}$	Input/output capacitance (switch on)	$V_{I(pp)}$=1 V, 100KHz V_{CC} = 3.3 V, T= 25 ° C			10	pF
R_{ON}	Switch resistance	I_O=3 mA, V_O = 0.4 V V_{CC} = 3.3 V		27	40	Ω
T_{PD}	DDC_SINK to DDC_SOURCE propagation delay	Time from DDC_SINK changing state to DDC_SOURCE changing state while the pass gate is enabled. C_L=10 pF R_{PU}=1.5 K (min), 2.0 K (max)		8	15	ns
T_{SX}	Switch time from DDC_EN to the valid state on DDC_SOURCE	C_L = 10 pF R_{PU} = 1.5 K (min), 2.0 K (max)		8	15	ns

5.5 OE_ input characteristics

Table 12. OE_N input characteristics

Symbol	Parameter	Comment	Min	Typ	Max	Unit
V_{IH-OE_N}	Input high level		2		VCC33	V
V_{IL-OE_N}	Input low level		0		0.8	V
I_{IN-OE_N}	Input leakage current	Measured with OE_N at VIH-OE_N max and VIL-OE_N mix			200	µA

5.6 HPD input resistor

Table 13. HDP input resistor

Symbol	Parameter	Comment	Min	Typ	Max	Unit
R_{HPD}	HPD_SINK input pull-down resistor	Guarantees HPD_SINK is LOW when no display is plugged in	130 K	160 K	190 K	Ω

5.7 ESD performance

Table 14. ESD performance

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
ESD	MIL STD 883 method 3015 (all pins)	Human Body Model (HBM)	-6		+6	kV

6 Application information

6.1 Power supply sequencing

Proper power-supply sequencing is advised for all CMOS devices. It is recommended to always apply V_{CC} before applying any signals to the input/output or control pins.

6.2 Supply bypassing

Bypass each of the V_{CC} pins with 0.1 µF and 1nF capacitors in parallel as close to the device as possible, with the smaller-valued capacitor as close to the V_{CC} pin of the device as possible.

6.3 Differential traces

The high-speed inputs and TMDS outputs are the most critical parts for the device. There are several considerations to minimize discontinuities on these transmission lines between the connectors and the device.

(a) Maintain 100 Ω differential transmission line impedance into and out of the device.

(b) Keep an uninterrupted ground plane below the high-speed I/Os.

(c) Keep the ground-path vias to the device as close as possible to allow the shortest return current path.

(d) Layout of the TMDS differential outputs should be with the shortest stubs from the connectors.

Output trace characteristics affect the performance of the STHDLS101T. Use controlled impedance traces to match trace impedance to both the transmission medium impedance and termination resistor. Run the differential traces close together to minimize the effects of the noise. Reduce skew by matching the electrical length of the traces. Avoid discontinuities in the differential trace layout. Avoid 90 degree turns and minimize the number of vias to further prevent impedance discontinuities.

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 6. QFN-48 (7 x 7 mm) package outline

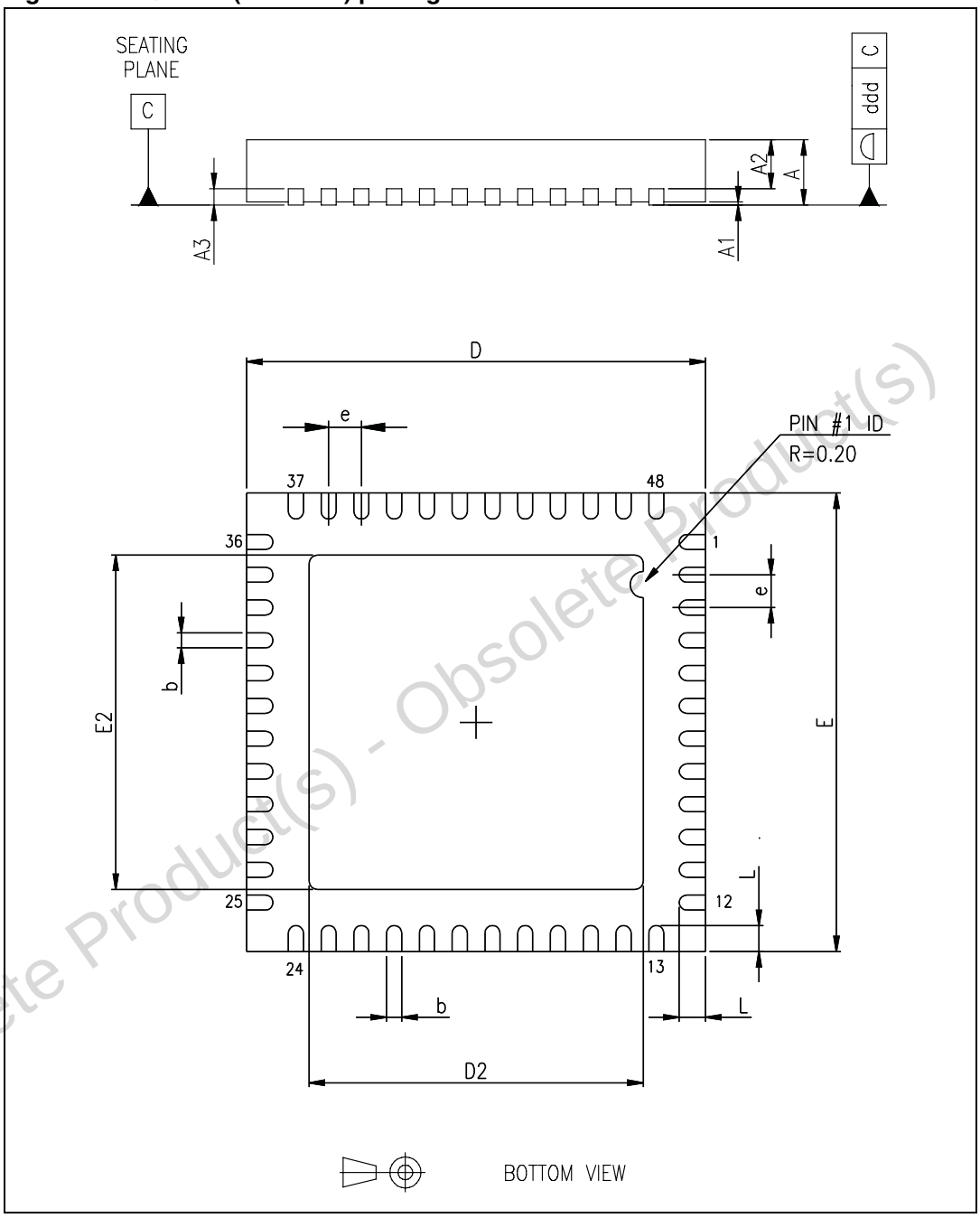


Table 15. QFN-48 (7 x 7 mm) package mechanical data

Symbol	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	0.80	0.85	1.00
A1		0.02	0.05		0.01	0.05
A2		0.65	1.00		0.65	
A3		0.25			0.20	
b	0.18	0.23	0.30	0.18	0.23	0.30
D	6.85	7.00	7.15	6.90	7.00	7.10
D2	2.25	4.70	5.25	SEE EXPOSED PAD VARIATIONS		
E	6.85	7.00	7.15	6.90	7.00	7.10
E2	2.25	4.70	5.25	SEE EXPOSED PAD VARIATIONS		
e	0.45	0.50	0.55	0.45	0.50	0.55
L	0.30	0.40	0.50	0.30	0.40	0.50
ddd			0.08			0.08

Figure 7. QFN-48 tape and reel information

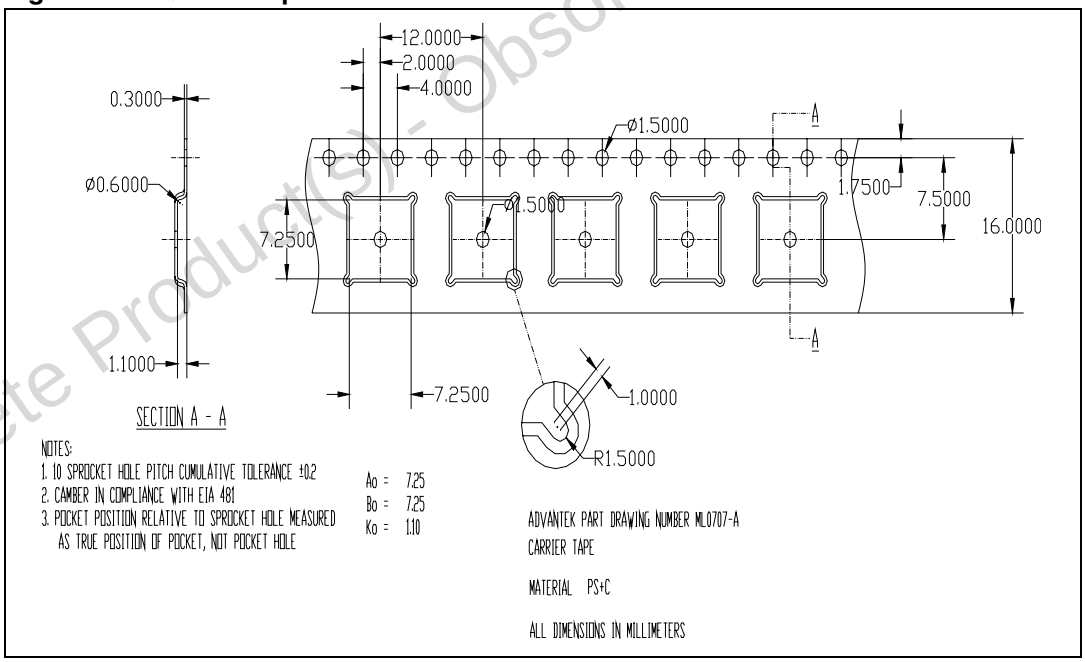


Figure 8. Reel information

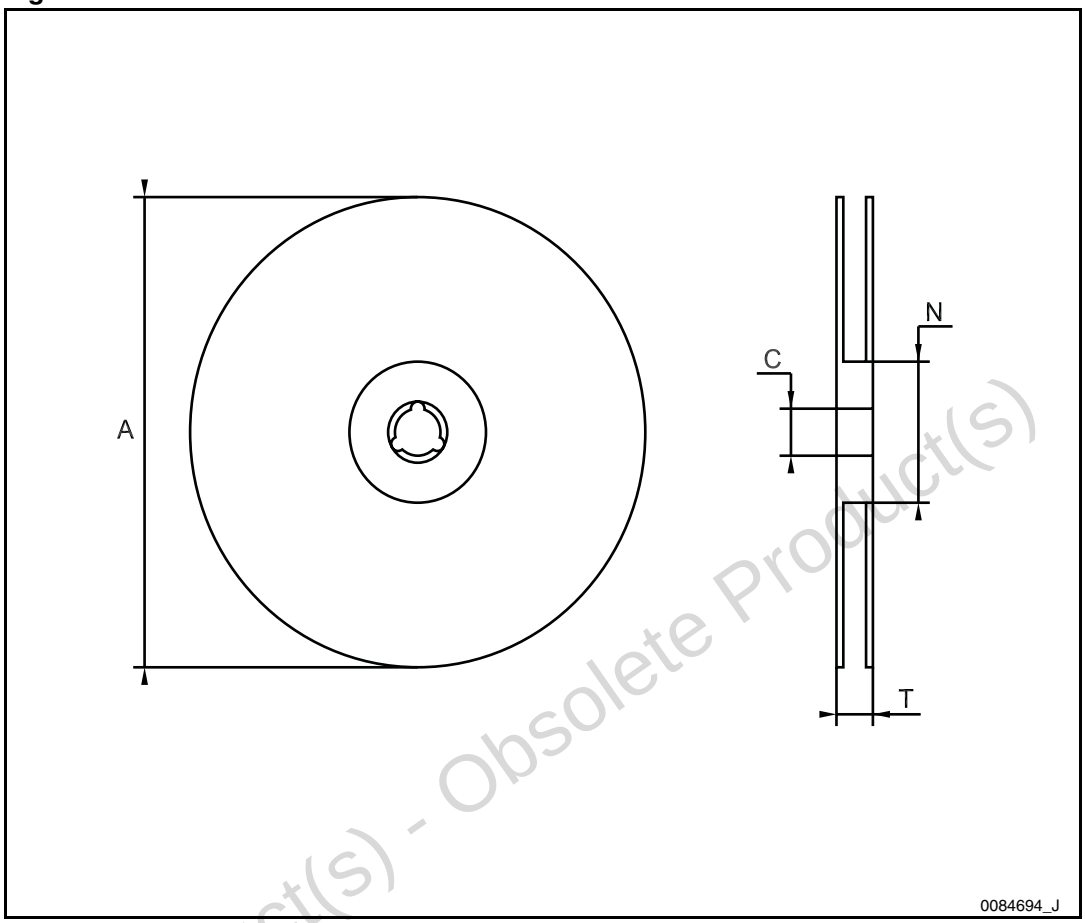


Table 16. Reel mechanical data (dimensions in mm)

A	C	N	T
330.2	13 ±0.25	100	16.4

8 Revision history

Table 17. Document revision history

Date	Revision	Changes
30-Jun-2008	1	Initial release.
24-Sep-2008	2	Document status promoted from preliminary data to datasheet. Modified: features section, *Table 2: Pin description on page 8* and *Section 4: Functional description*.
01-Dec-2008	3	Updated: Features section and*Chapter 5: Maximum ratings* Added: *Figure 3: Cable adapter on page 5* , *Figure 4: DP to HDMI/DVI cable adapter on page 6*, *Figure 8: Reel information on page 24* and *Table 16: Reel mechanical data (dimensions in mm) on page 24*