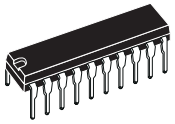
L6204

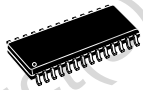
DMOS DUAL FULL BRIDGE DRIVER

- SUPPLY VOLTAGE UP TO 48V
- $R_{DS(ON)}$ 1.2Ω L6204 (25°C)
- CROSS CONDUCTION PROTECTION
- THERMAL SHUTDOWN
- 0.5A DC CURRENT
- TTL/CMOS COMPATIBLE DRIVER
- HIGH EFFICIENCY CHOPPING
- MULTIPOWER BCD TECHNOLOGY

MULTOPOWER BCD TECHNOLOGY



Powerdip 16+2+2



SO 24+2+2

ORDERING NUMBERS:

L6204 **L6204D**

DESCRIPTION

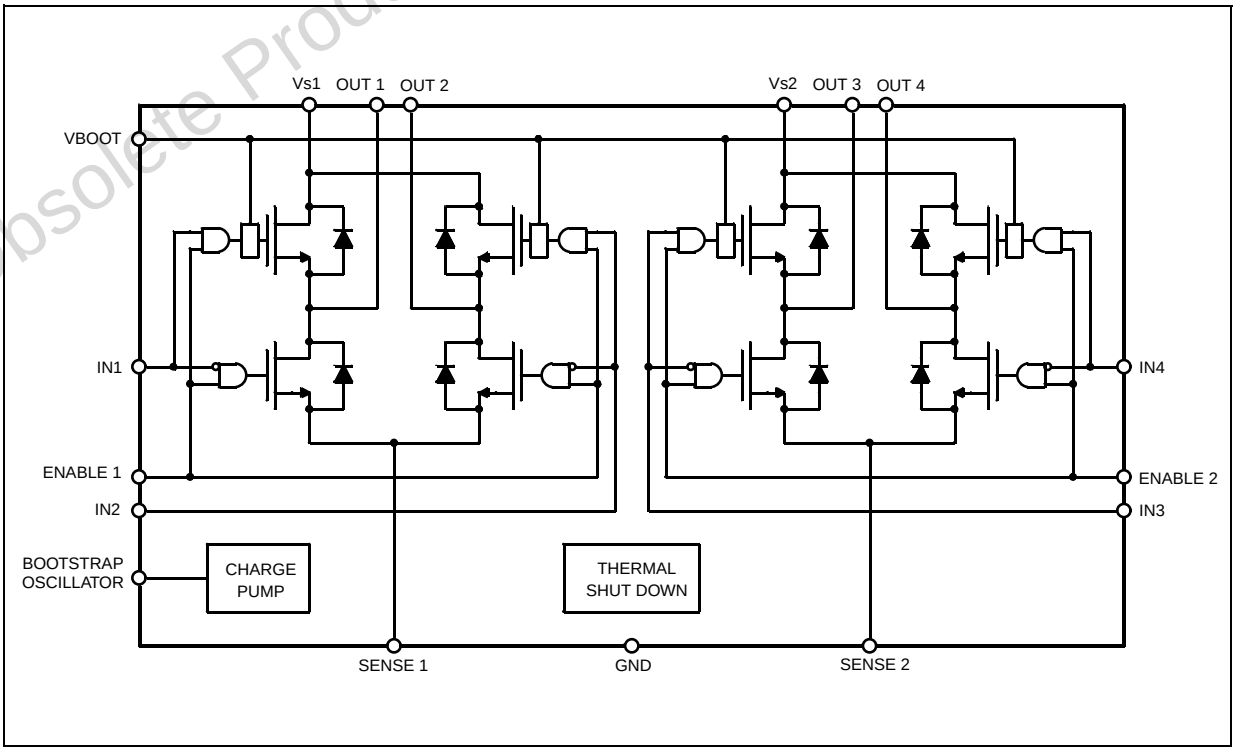
The L6204 is a dual full bridge driver for motor control applications realized in BCD technology which combines isolated DMOS power transistors with CMOS and Bipolar circuits on the same chip. By using mixed technology it has been possible to optimize the logic circuitry and the power stage to achieve the best possible performance.

The logic inputs are TTL/CMOS compatible. Both channels are controlled by a separate Enable.

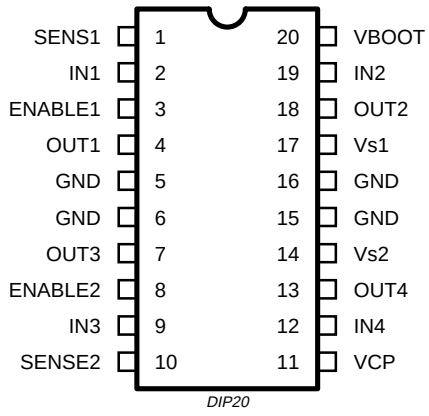
Each bridge has a sense resistor to control the currenrt level.

The L6204 is mounted in an 20-lead Powerdip and SO 24+2+2 packages and the four center pins are used to conduct heat to the PCB. At normal operating temperatures no external heatsink is required.

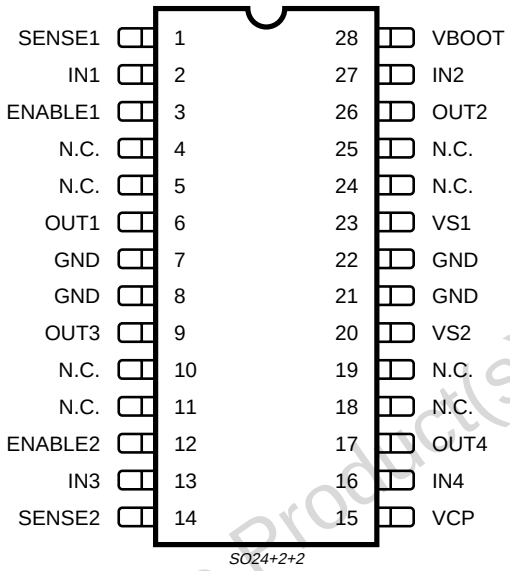
BLOCK DIAGRAM



PIN CONNECTIONS



DIP16+2+2



SO24+2+2

PIN DESCRIPTION

SO Pin (*)	DIP Pin	Symbols	Functions
1	1	SENSE 1	Sense resistor to provide the feedback for motor current control of the bridge A
2	2	IN1	Digital input from the motor controller (bridge A)
3	3	ENABLE 1	A logic level low on this pin disable the bridge A
6	4	OUT 1	Output of one half bridge of the bridge A
7	5	GND	Common Power Ground
8	6	GND	Common Power Ground
9	7	OUT 3	Ouput of one half bridge of the bridge B
12	8	ENABLE 2	A logic level low on this pin disable the bridge B
13	9	IN 3	Digital input from the motor controller (bridge B)
14	10	SENSE 2	Sense resistor to provide the feedback for motor current control of the bridge B
15	11	BOOSTRAP OSC. VCP	Oscillator output for the external charge pump
16	12	IN 4	Digital input from the motor controller (bridge B)
17	13	OUT 4	Output of one half bridge of the bridge B
20	14	V_{S2}	Supply voltage bridge B
21	15	GND	Common Power Ground
22	16	GND	Common Power Ground
23	17	V_{S1}	Supply Voltage bridge A
26	18	OUT 2	Output of one half bridge of the bridge A
27	19	IN 2	Digital input from the motor controller (bridge A)
28	20	VBOOT	Overvoltage input for driving of the upper DMOS

(*) For SO package the pins 4, 5, 10, 11, 18, 19, 24 and 25 are not connected.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	50	V
V_{IN}, V_{EN}	Input or Enable Voltage Range	-0.3 to +7	V
I_o	Pulsed Output Current	3	A
V_{SENSE}	Sensing Voltage	-1 to 4	V
V_{BOOT}	Bootstrap Supply	60	V
P_{tot}	Total power dissipation: (T_{pins} = 80°C) (T_{amb} = 70°C no copper area on PCB) (T_{amb} = 70°C 8cm_2 copper area on PCB)	5 1.23 2	W W W
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

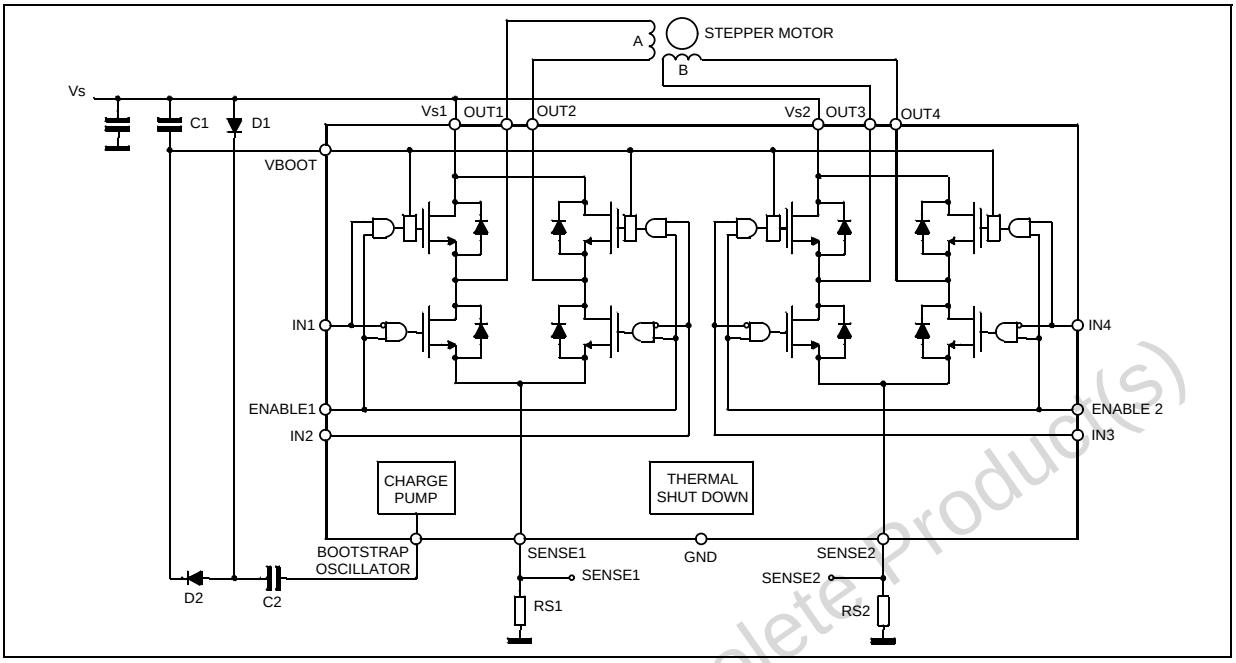
THERMAL DATA

Symbol	Parameter		SO	DIP	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	16	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	73	65	°C/W

ELECTRICAL CHARACTERISTCS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		12		48	V
I_S	Total Quiescent Current	EN1=EN2=H; IN1=IN2=IN3=IN4=L EN1 = EN2 = L			10 10	mA mA
f_C	Commutation Frequency			20		KHz
T_J	Thermal Shutdown			150		°C
T_d	Dead Time Protection			500		ns
TRANSISTORS						
I_{DSS}	Leakage Current	OFF		1		mA
R_{DS}	On Resistance	ON		1.2		Ω
LOGIC LEVELS						
V_{INL}, V_{ENL}	Input Low Voltage		-0.3		0.8	V
V_{INH}, V_{ENH}	Input High Voltage		2		7	V
I_{INL}, I_{ENL}	Input Low Current	IN1 = IN2 = IN3 = IN4 = EN1 = EN2 = L			-10	µA
I_{INH}, I_{ENH}	Input High Current	IN1 = IN2 = IN3 = IN4 = EN1 = EN2 = H		50		µA

APPLICATION DIAGRAM



CIRCUIT DESCRIPTION

L6204 is a dual full bridge IC designed to drive DC motors, stepper motors and other inductive loads. Each bridge has 4 power DMOS transistor with R_{DSon} = 1.2Ω and the relative protection and control circuitry. (see fig. 3)

The 4 half bridges can be controlled independently by means of the 4 inputs IN!, IN2, IN3, IN4 and 2 enable inputs ENABLE1 and ENABLE2.

External connections are provided so that sensing resistors can be added for constant current chopper applications.

LOGIC DRIVE (*)

INPUTS			OUTPUT MOSFETS
	IN1	**IN2**	
	IN3	**IN4**	
EN1=EN2=H	L	L	Sink 1, Sink 2
	L	H	Sink 1, Source 2
	H	L	Source 1, Sink 2
	H	H	Source 1, Source 2
EN1=EN2=L	X	X	All transistor turned OFF

L = Low H = High X = Don't care
(*) True table for the two full bridges

CROSS CONDUCTION

Although the device guarantees the absence of cross-conduction, the presence of the intrinsic diodes in the POWER DMOS structure causes the generation of current spikes on the sensing terminals.

This is due to charge-discharge phenomena in the capacitors C1 & C2 associated with the drain source junctions (fig. 1). When the output switches from high to low, a current spike is generated associated with the capacitor C1. On the low-to-high transition a spike of the same polarity is generated by C2, preceded by a spike of the opposite polarity due to the charging of the input capacity of the lower POWER DMOS transistor (see fig. 2).

Figure 1. Intrinsic Structures in the POWER MOS Transistors

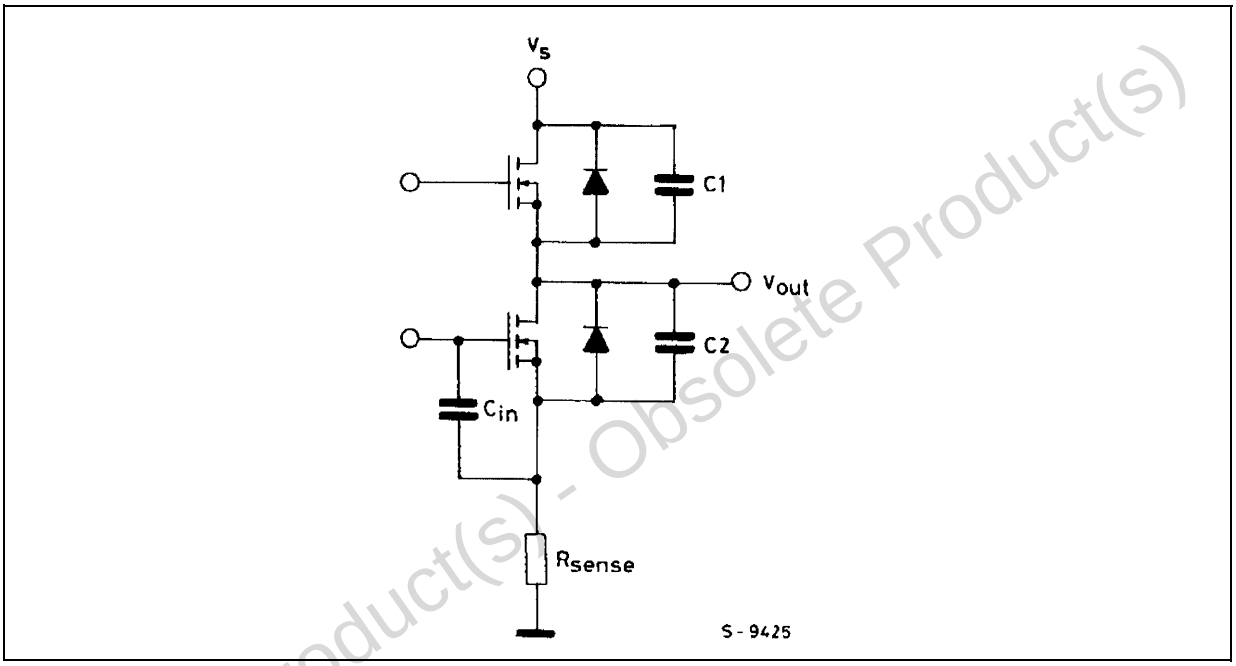
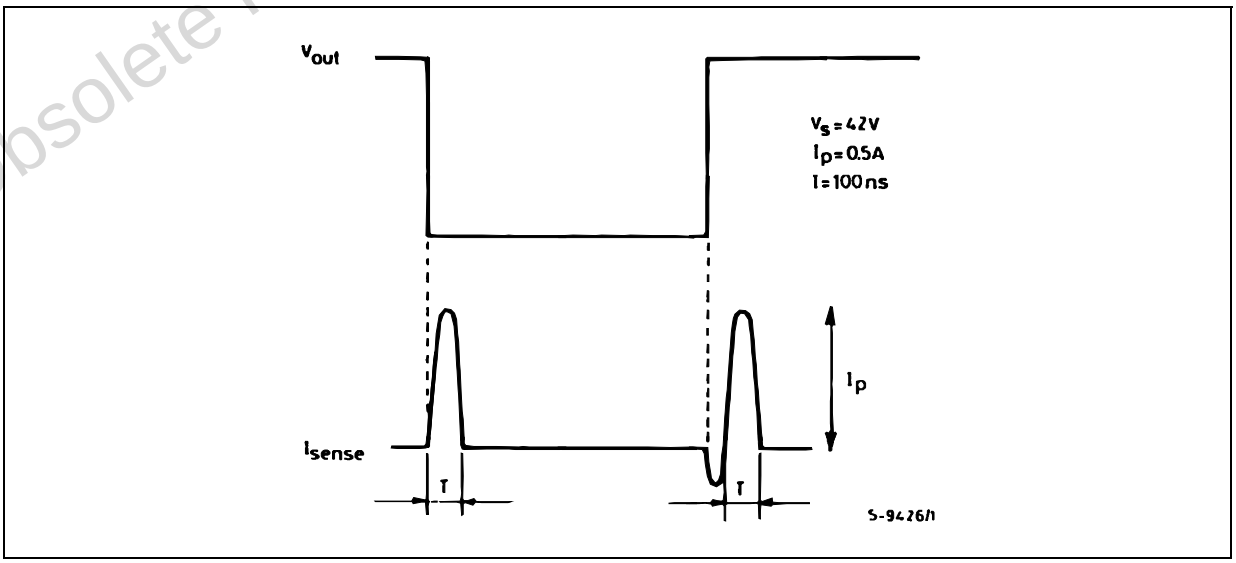


Figure 2. Current Typical Spikes on the Sensing Pin



TRANSISTOR OPERATION

ON STATE

When one of the POWER DMOS transistors is ON it can be considered as a resistor $R_{DS(ON)}$ = 1.2Ω at a junction temperature of 25°C.

In this condition the dissipated power is given by :

$$P_{ON} = R_{DS(ON)} \cdot I_{DS}^2$$

The low $R_{DS(ON)}$ of the Multipower-BCD process can provide high currents with low power dissipation.

OFF STATE

When one of the POWER DMOS transistor is OFF the VDS voltage is equal to the supply voltage and only the leakage current IDSS flows. The power dissipation during this period is given by :

$$P_{OFF} = V_S \cdot I_{DSS}$$

TRANSITIONS

Like all MOS power transistors the DMOS POWER transistors have as intrinsic diode between their source and drain that can operate as a fast freewheeling diode in switched mode applications.

During recirculation with the ENABLE input high, the voltage drop across the transistor is RDS(ON) . ID and when the voltage reaches the diode voltage it is clamped to its characteristic.

When the ENABLE input is low, the POWER MOS is OFF and the diode carries all of the recirculation current. The power dissipated in the transitional times in the cycle depends upon the voltage and current waveforms in the application.

$$P_{trans} = I_{DS}(t) \times V_{DS}(t)$$

BOOTSTRAP CAPACITORS

To ensure the correct driving of high side drivers a voltage higher than V_S is supplied on pin 20 (V_{boot}). This bootstrap voltage is not needed for the lower power DMOS transistor because their sources are grounded. To produce this voltage a charge pump method is used and mAde by two external capacitors and two diodes. It can supply the 4 driving blocks of the high side drivers. Using an external capacitor the turn-on speed of the high side driver is very high; furthermore with different capacitance values it is possible to adapt the device to different switching frequencies. It is also possible to operate two or more L6204s using only 2 diodes and 2 capacitance for all the ICs; all the Vboot pins are connected to the Cstore capacitance while the pin 11 (VCP) of just one L6204 is connect to C_{pump}, obviously all the L6204 ICs have to be connected to the same V_S. (see fig. 6)

Figure 3. Two Phase Chopping

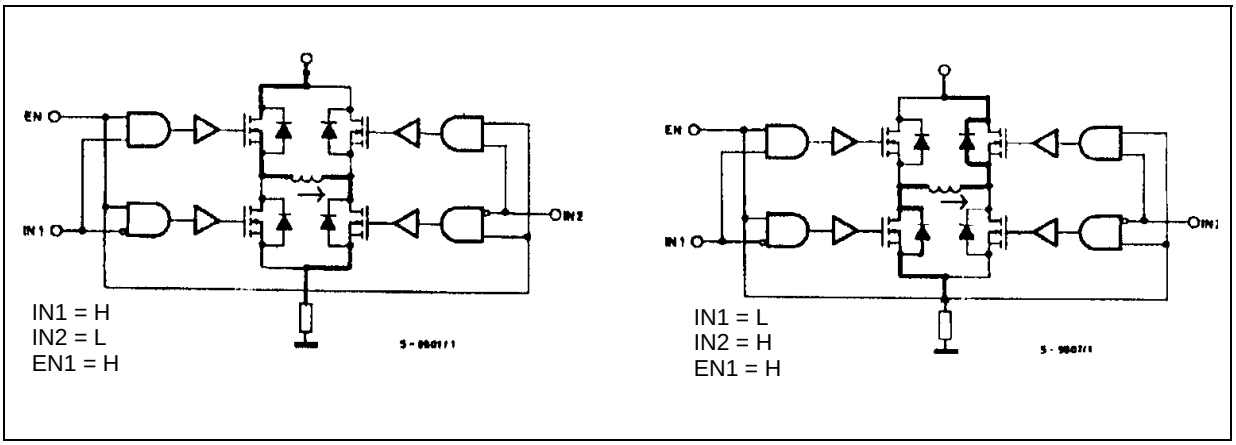


Figure 4. One Phase Chopping

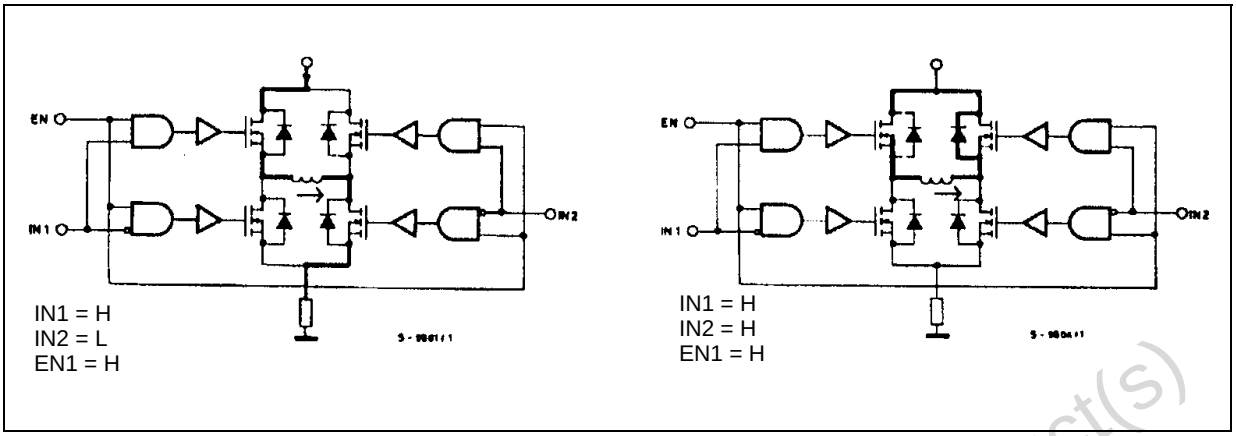


Figure 5. Enable Chopping

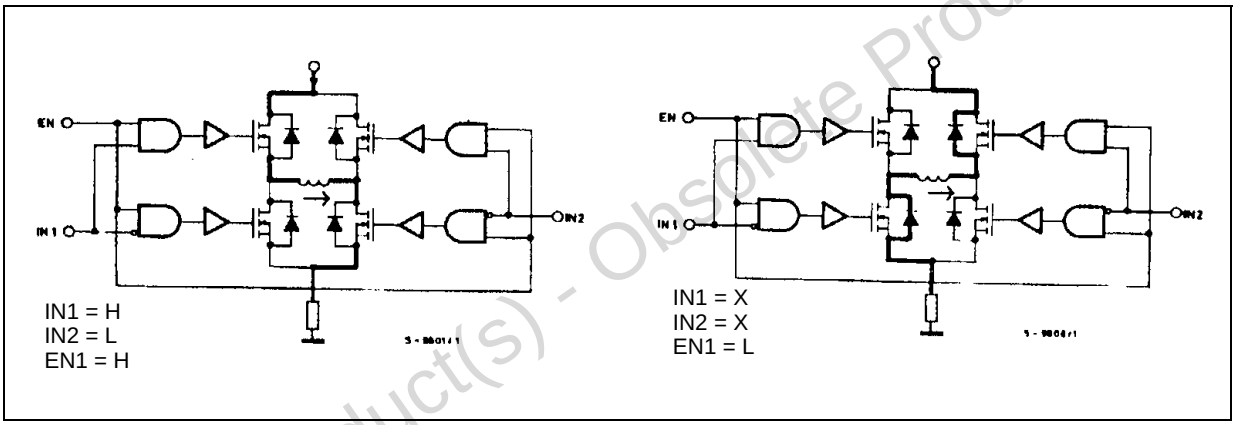
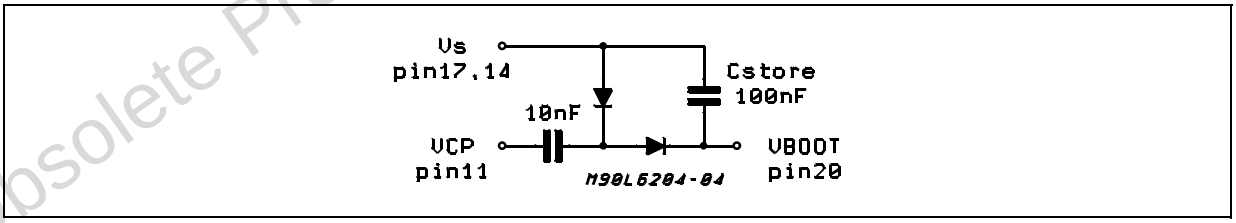


Figure 6.



DEAD TIME

To protect the device against simultaneous conduction in both arms of the bridge and the resulting rail-to-rail short, the logic circuits provide a dead time.

THERMAL PROTECTION

A thermal protection circuit has been included that will disable the device if the junction temperature reaches 150 °C. When the temperature has fallen to a safe level the device restarts under the control of the input and enable signals.

APPLICATION INFORMATION

RECIRCULATION

During recirculation with the ENABLE input high, the voltage drop across the transistor is $R_{DS(ON)}$. I_L for voltages less than 0.7 V and is clamped at a voltage depending on the characteristics of the source-drain diode for greater voltages. Although the device is protected against cross conduction, current spikes can appear on the current sense pin due to charge/discharge phenomena in the intrinsic source drain capacitances. In the application this does not cause any problems because the voltage created across the sense resistor is usually much less than the peak value, although a small RC filter can be added if necessary.

POWER DISSIPATION (each bridge)

In order to achieve the high performance provided by the L6204 some attention must be paid to ensure that it has an adequate PCB area to dissipate the heat. The first stage of any thermal design is to calculate the dissipated power in the appl ication, for this example the half step operation shown in figure 7 is considered.

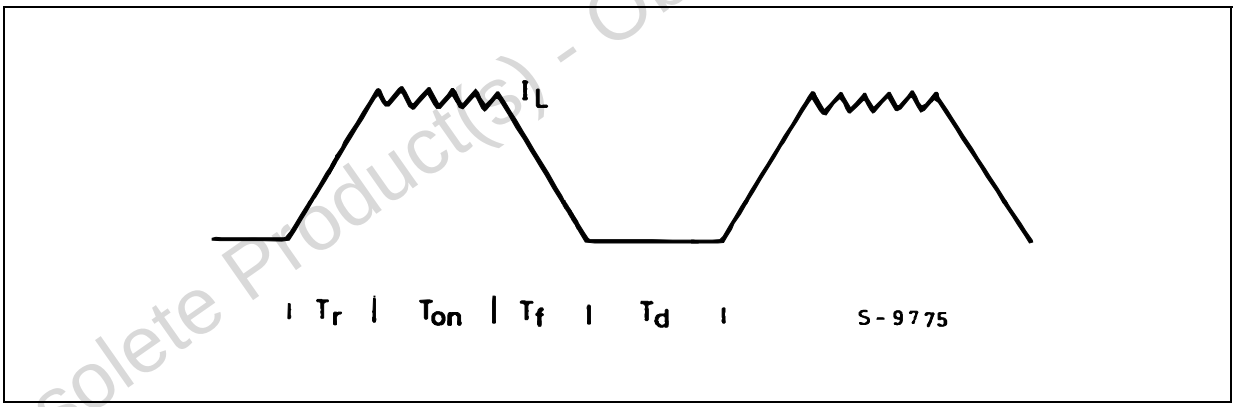
RISE TIME T_r

When an arm of the half bridge is turned on current begins to flow in the inductive load until the maximum current I_L is reached after a time T_r.

The dissipated energy $E_{OFF/ON}$ is in this case :

$$E_{OFF/ON} = [R_{DS(ON)} \cdot I_L^2 \cdot T_r] \cdot 2/3$$

Figure 7.



ON TIME T_{ON}

During this time the energy dissipated is due to the ON resistance of the transistors E_{ON} and the commutation E_{COM}. As two of the POWER DMOS transistors are ON E_{ON} is given by :

$$E_{ON} = I_L^2 \cdot R_{DS(ON)} \cdot 2 \cdot T_{ON}$$

In the commutation the energy dissipated is :

$$E_{COM} = V_S \cdot I_L \cdot T_{COM} \cdot f_{SWITCH} \cdot T_{ON}$$

Where :

T_{COM} = Commutation Time and it is assumed that ;

$T_{COM} = T_{TURN-ON} = T_{TURN-OFF}$ = 100 ns

f_{SWITCH} = Chopper frequency

FALL TIME T_f

For this example it is assumed that the energy dissipated in this part of the cycle takes the same form as that shown for the rise time :

$$E_{ON/OFF} = [R_{DS(ON)} \cdot I_L \cdot T_f] \cdot 2/3$$

QUIESCENT ENERGY

The last contribution to the energy dissipation is due to the quiescent supply current and is given by :

$$E_{QUIESCENT} = I_{QUIESCENT} \cdot V_S \cdot T$$

TOTAL ENERGY PER CYCLE

$$E_{TOT} = (E_{OFF/ON} + E_{ON} + E_{COM} + E_{ON/OFF})\ \text{bridge 1} + (E_{OFF/ON} + E_{ON} + E_{COM} + E_{ON/OFF})\text{bridge 2} + + E_{QUIESCENT}$$

The Total Power Dissipation PDIS is simply :

$$P_{DIS} = E_{TOT}/T$$

T_r = Rise time

T_{ON} = ON time

T_f = Fall Time

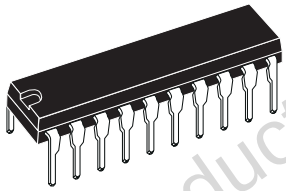
T_d = Dead time

T = Period

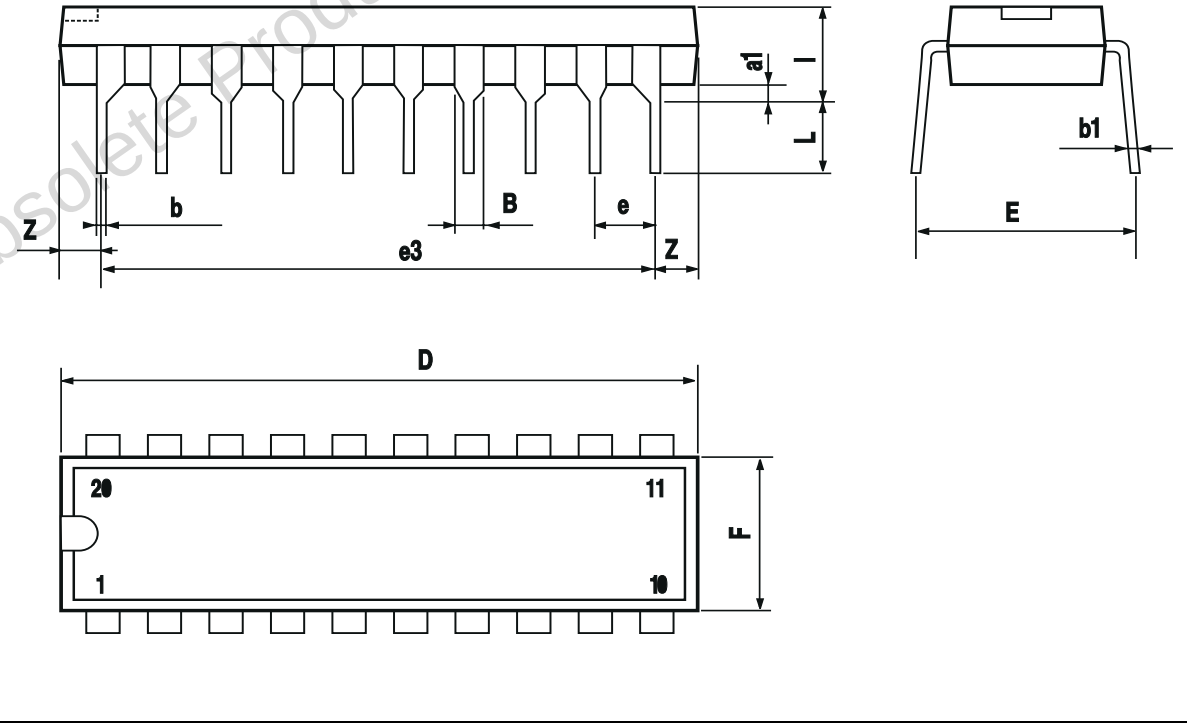
$$T = T_r + T_{ON} + T_f + T_d$$

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
E		8.80			0.346	
e		2.54			0.100	
e3		22.86			0.900	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050

OUTLINE AND MECHANICAL DATA

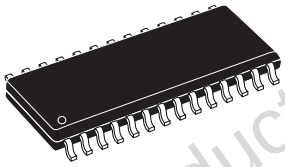


Powerdip 20



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8 ° (max.)					

OUTLINE AND MECHANICAL DATA



SO28