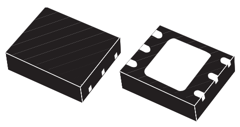
ST1L02

Very low quiescent current BiCMOS voltage regulator

Datasheet - production data



DFN6 (3x3 mm)

Features

- Fixed output voltages: 1.8 V, 2.5 V, 3.3 V (1.5 V, upon customer request)
- Output voltage tolerance: ± 2% at 25 °C
- Output current capability: 1 A minimum
- Very low quiescent current: max. 500 µA overtemperature range
- Typical dropout voltage 0.7 V (@ I_O = 1 A)
- Stable with low ESR ceramic capacitors
- Thermal shutdown protection with hysteresis
- Overcurrent protection
- Operating junction temperature range: from 0 to 125 °C

Description

The ST1L02 is a low drop linear voltage regulator, which supplies up to 1 A output current.

It is available in several fixed output voltage versions. Thanks to BiCMOS technology, quiescent current is well-controlled and maintained below 650 µA over the whole allowed junction temperature range.

The ST1L02 is stable with low ESR output ceramic capacitors.

Internal protection circuitry includes thermal protection with hysteresis and overcurrent limiting.

The ST1L02 is suitable for data storage applications such as HDDs, where it can be used to supply the read channel and memory chips requiring 3.3 V.

The regulator is available in the small and thin DFN6 (3x3 mm) package.

Table 1. Device summary

Order code	Package
ST1L02PU18R	DFN6 (3x3 mm)
ST1L02PU33R	DFN6 (3x3 mm)

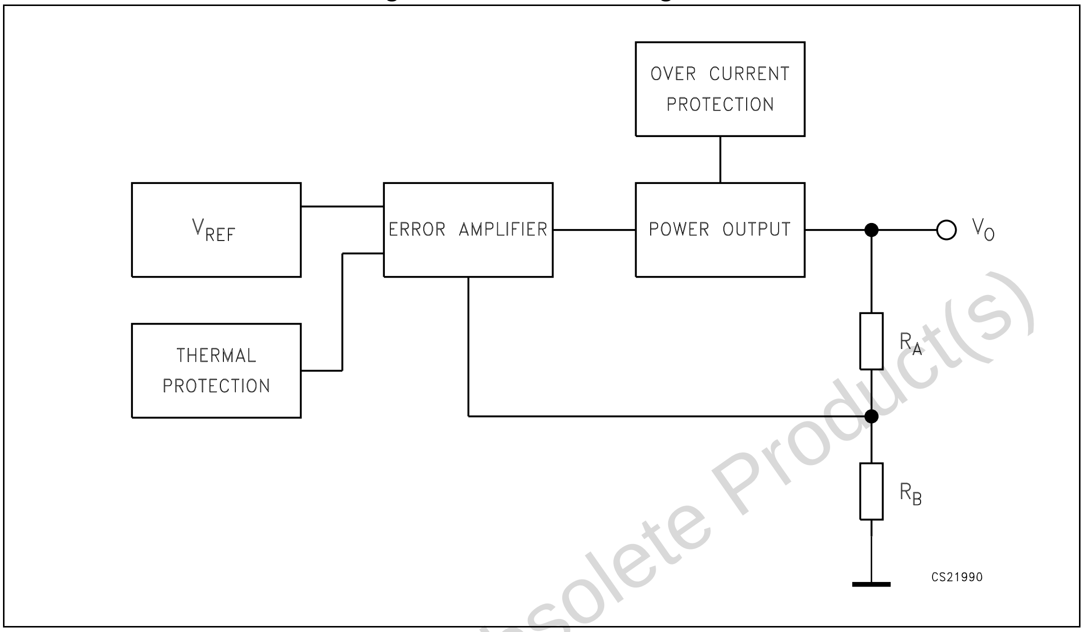
This is information on a product in full production. www.st.com

Contents

List of figures

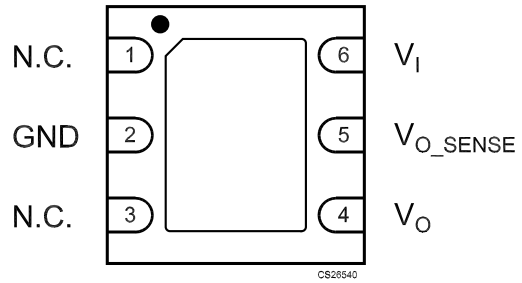
1 Diagram

Figure 1. Schematic diagram



2 Pin configuration

Figure 2. Pin connection (top view)



ST1L02

Table 2. Pin description

Pin	Symbol	Function
1, 3	N.C.	Not connected
2	GND	Ground. The exposed metallic pad of the package is connected to GND
4	V_O	Output voltage pin. Bypass with a 4.7 µF capacitor to GND
5	V_{O_SENSE}	Sense output voltage pin, to be connected to pin 4
6	V_I	Supply voltage input pin. Bypass with a 4.7 µF capacitor to GND

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_I	DC supply voltage	10	V
P_{TOT}	Power dissipation	Internally limited	W
I_O	Output current	Internally limited	A
T_{OP}	Operating junction temperature range	0 to 150	°C
T_{STG}	Storage temperature range(1)	-65 to 150	°C
T_{LEAD}	Lead temperature (soldering) 10 seconds	260	°C

1. Storage temperature >125 °C is acceptable only if the regulator is soldered to a PCBA.

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case	10	°C/W
R_{thJA}	Thermal resistance junction-ambient	55	°C/W

4 Electrical characteristics

Refer to the typical application schematic, V_I = 4.5 V to 7 V, I_O = 5 mA to 1 A, C_I = 4.7 µF, C_O = 4.7 µF, T_J = 0 to 125 °C unless otherwise specified. Intended typical values are T_J = 25 °C unless otherwise specified.

Table 5. ST1L02PU18R electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_I = 4.75 V to 5.25 V, T = 25 °C	1.764	1.8	1.836	V
V_O	Output voltage	V_I = 4.75 V to 5.25 V	1.746	1.8	1.854	V
ΔV_O	Line regulation	V_I = 4.75 V to 5.25 V			15	mV
ΔV_O	Load regulation	V_I = 4.75 V, I_O = 10 mA to 1 A			10	mV
I_S	Output current limit	V_I = 5.5 V	1.0			A
I_{OMIN}	Minimum output current for regulation				2	mA
V_d	Dropout voltage(1)	I_O = 0.8 A			1.6	V
		I_O = 1 A			1.6	V
I_Q	Quiescent current	V_I = 5 V, I_O = 2 mA to 1 A, T = 25 °C			500	µA
I_Q	Quiescent current	V_I = 7 V, I_O = 2 mA to 1 A			650	µA
SVR	Supply voltage rejection(2)	V_I = 5 ± 0.5 V, I_O = 5 mA, f = 120 Hz	50	75		dB
eN	RMS output noise(2)	B = 10 Hz to 10 kHz, V_I = 5 V, I_O = 5 mA		0.003		$\%V_O$
$\Delta V_O/\Delta I_O$	Load transient (rising)(3)	V_I = 5 V, any 200 mA step from 100 mA to 1 A, $t_R \geq 1$ µs			5	$\%V_O$
T_{SH}	Thermal shutdown trip point (3)	V_I = 5 V		165		°C

1. See minimum start-up voltage, V_I = 3.3 V.
2. Guaranteed by design. Not tested in production.
3. C_I = 10 µF, C_O = 10 µF, X7R ceramic capacitors.

Refer to the typical application schematic, V_I = 4.5 V to 7 V, I_O = 5 mA to 1 A, C_I = 4.7 µF, C_O = 4.7 µF, T_J = 0 to 125 °C, unless otherwise specified. Intended typical values are T_J = 25 °C unless otherwise specified.

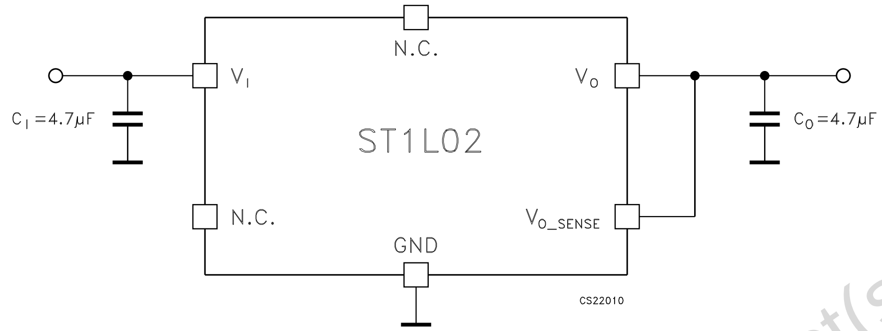
Table 6. ST1L02PU33 electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_I = 4.75 V to 5.25 V, T = 25 °C	3.234	3.3	3.366	V
V_O	Output voltage	V_I = 4.75 V to 5.25 V	3.2175	3.3	3.3825	V
ΔV_O	Line regulation	V_I = 4.75 V to 5.25 V			15	mV
ΔV_O	Load regulation	V_I = 4.75 V, I_O = 10 mA to 1 A			10	mV
I_S	Output current limit	V_I = 5.5 V	1.0			A
I_{OMIN}	Minimum output current for regulation				2	mA
V_d	Dropout voltage	I_O = 0.8 A		0.6	1.0	V
		I_O = 1 A		0.7	1.1	V
I_Q	Quiescent current	V_I = 5 V, I_O = 2 mA to 1 A, T = 25 °C			500	µA
I_Q	Quiescent current	V_I = 7 V, I_O = 2 mA to 1 A			650	µA
SVR	Supply voltage rejection(2)	V_I = 5 ± 0.5 V, I_O = 5 mA, f = 120 Hz	50	75		dB
eN	RMS output noise(2)	B = 10 Hz to 10 kHz, V_I = 5 V, I_O = 5 mA		0.003		%V_O
$\Delta V_O/\Delta I_O$	Load transient (rising)(1)	V_I = 5 V, any 200 mA step from 100 mA to 1 A, $t_R \geq$ 1 µs			5	%V_O
T_{SH}	Thermal shutdown trip point (2)	V_I = 5 V		165		°C

1. C_I = 10 µF, C_O = 10 µF, X7R ceramic capacitors.
2. Guaranteed by design. Not tested in production.

5 Typical application

Figure 3. ST1L02 application schematic



Note: The regulator is stable both with tantalum and ceramic capacitors on the input and the output. The expected values of the input and output ceramic capacitors are from 1 µF to 22 µF with 4.7 µF typical. The input capacitor has to be connected within 1 cm from V_I terminal. The output capacitor has also to be connected within 1 cm from output pin. There is not any upper limit to the value of the input capacitor.

6 Typical characteristics

Figure 4. Output voltage vs temperature

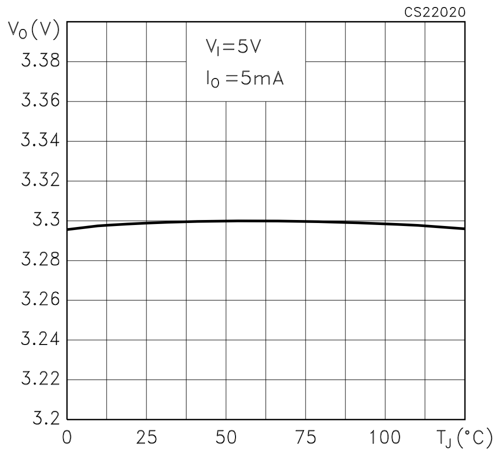


Figure 5. Line regulation vs temperature I_O = 5 mA

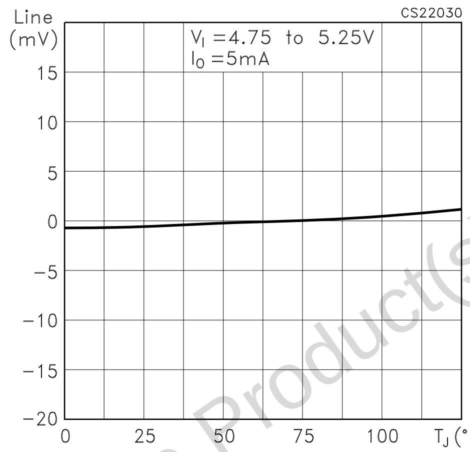


Figure 6. Line regulation vs temperature I_O = 1 A

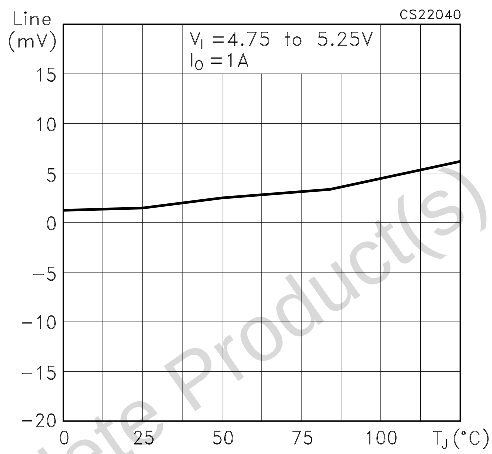


Figure 7. Load regulation vs temperature

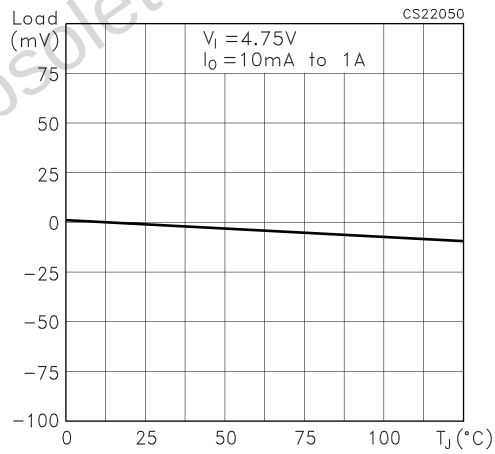


Figure 8. Dropout voltage vs temperature

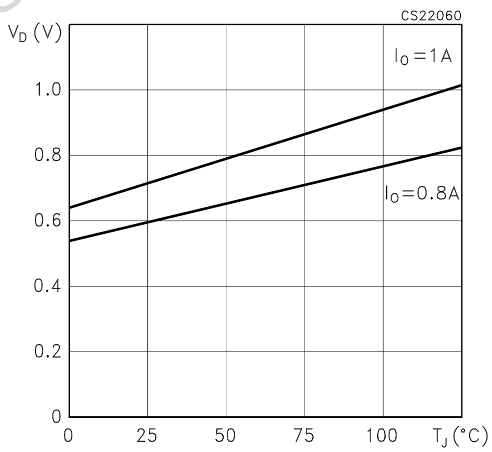


Figure 9. Quiescent current vs temperature I_O = 1 A

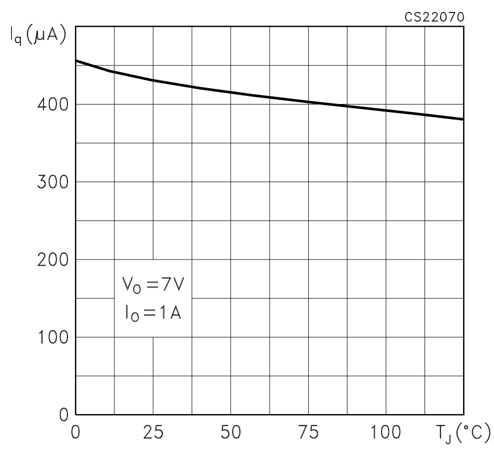


Figure 10. Quiescent current vs temperature no load

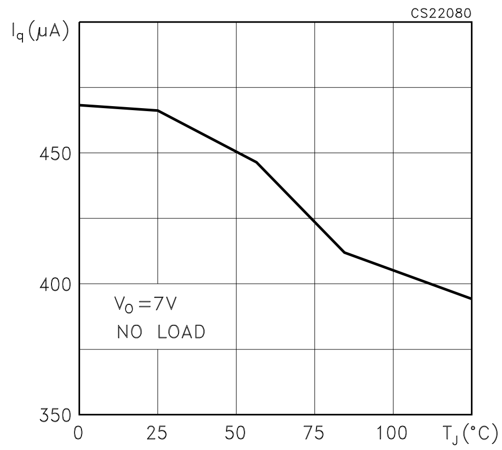


Figure 11. Quiescent current vs temperature I_O = 500 mA

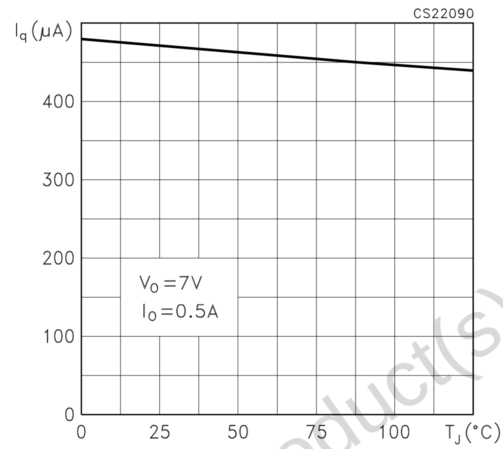


Figure 12. Quiescent current vs temperature I_O = 5 mA

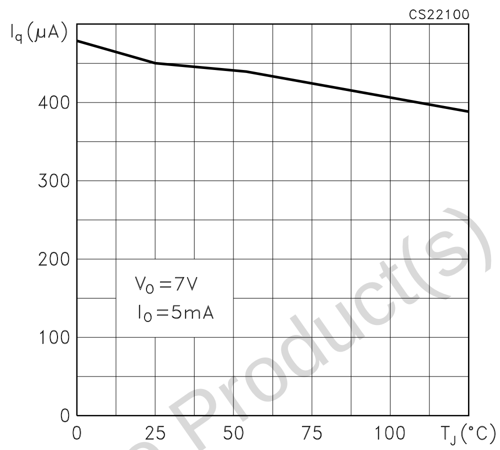


Figure 13. Quiescent current vs output current

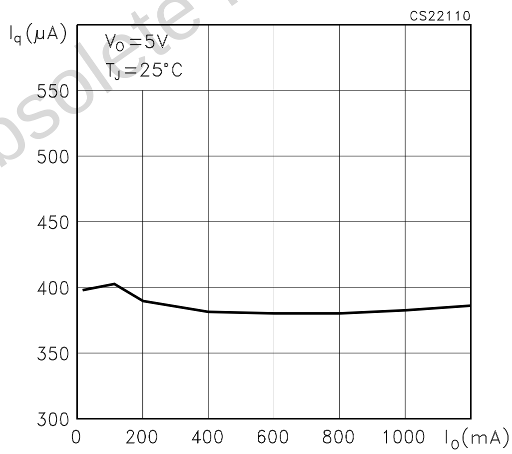


Figure 14. Supply voltage rejection vs temperature

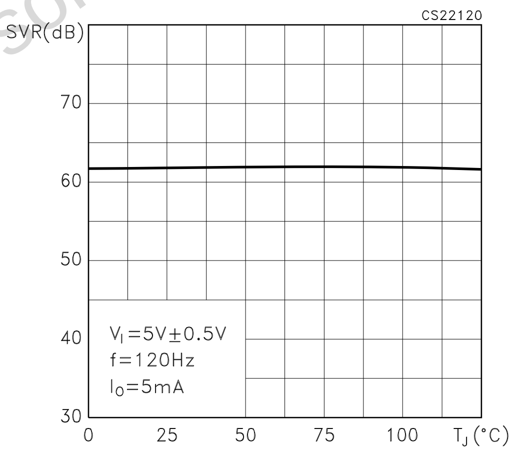


Figure 15. Supply voltage rejection vs frequency

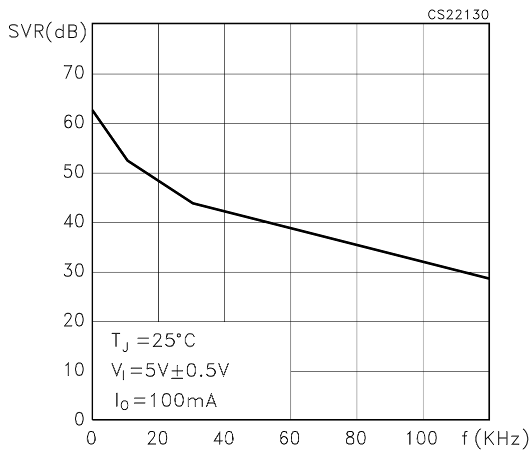


Figure 16. Output noise vs frequency

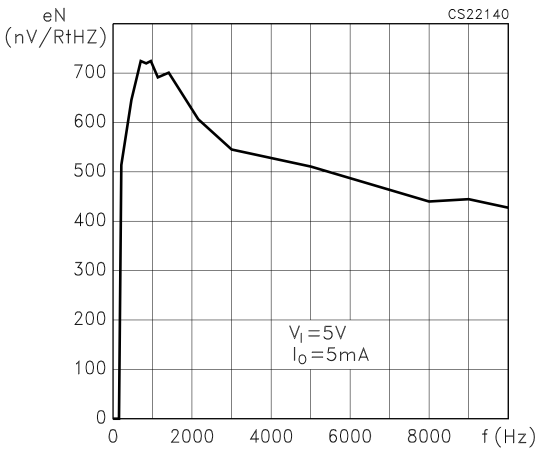
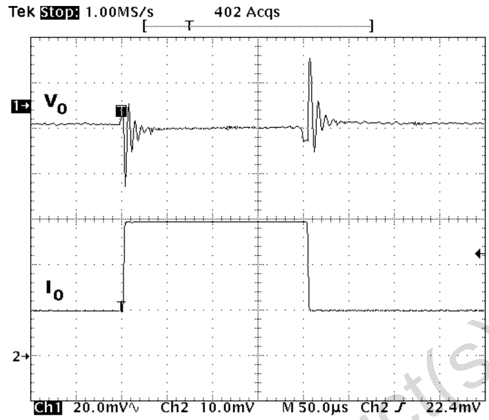
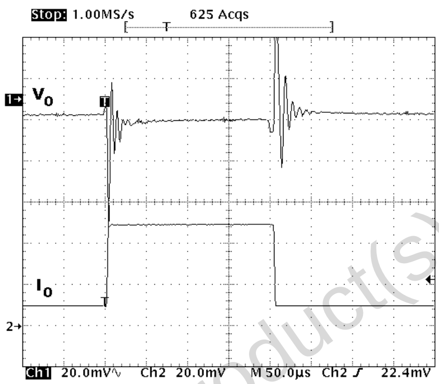


Figure 17. V_O change with step load change I_O = 100 to 300 mA



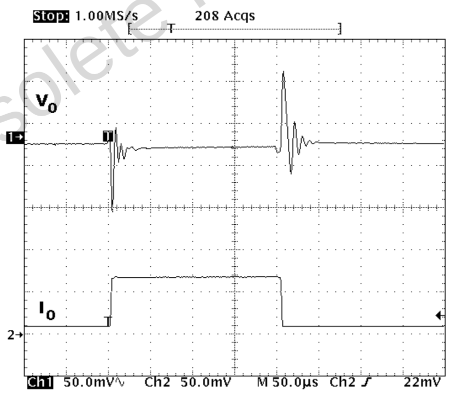
V_I=5V, I_O=100mA to 300mA, C_O=10µF, C_I=10µF, t_{RISE}≥1µs

Figure 18. V_O change with step load change I_O = 300 to 500 mA



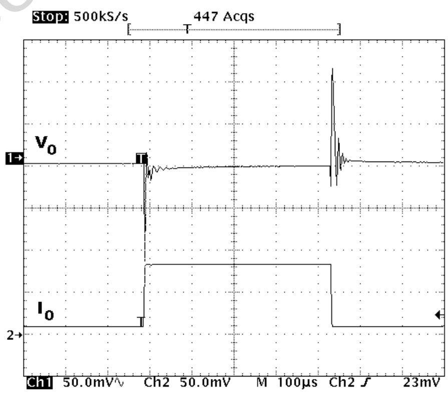
V_I=5V, I_O=300mA to 500mA, C_O=10µF, C_I=10µF, t_{RISE}≥1µs

Figure 19. V_O change with step load change I_O = 500 to 700 mA



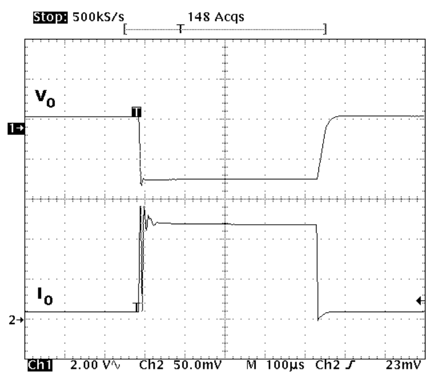
V_I=5V, I_O = 500mA to 700mA, C_O=10µF, C_I=10µF, t_{RISE} ≥ 1µs, T_J= 25°C

Figure 20. V_O change with step load change I_O = 700 to 900 mA



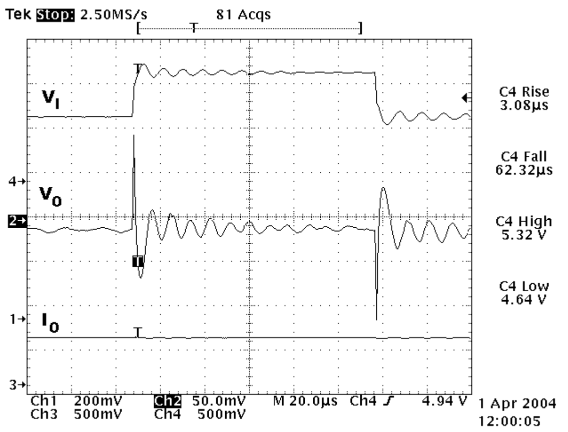
V_I=5V, I_O=700mA to 900mA, C_O=10µF, C_I=10µF, t_{RISE}≥1µs, T_J=25°C

Figure 21. V_O change with step load change I_O = 10 mA to short-circuit



V_I=5V, I_O=10mA to short-circuit, C_O=10µF, C_I=10µF, t_{RISE}≥1µs T_J=25°C

Figure 22. Line transient



V_I = 4.75 V to 5.25 V, I_O = 500 mA, C_O=10 µF, C_I = 2.2 µF, $t_{RISE} \geq 1$ µs

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 23. DFN6 (3x3 mm) drawings

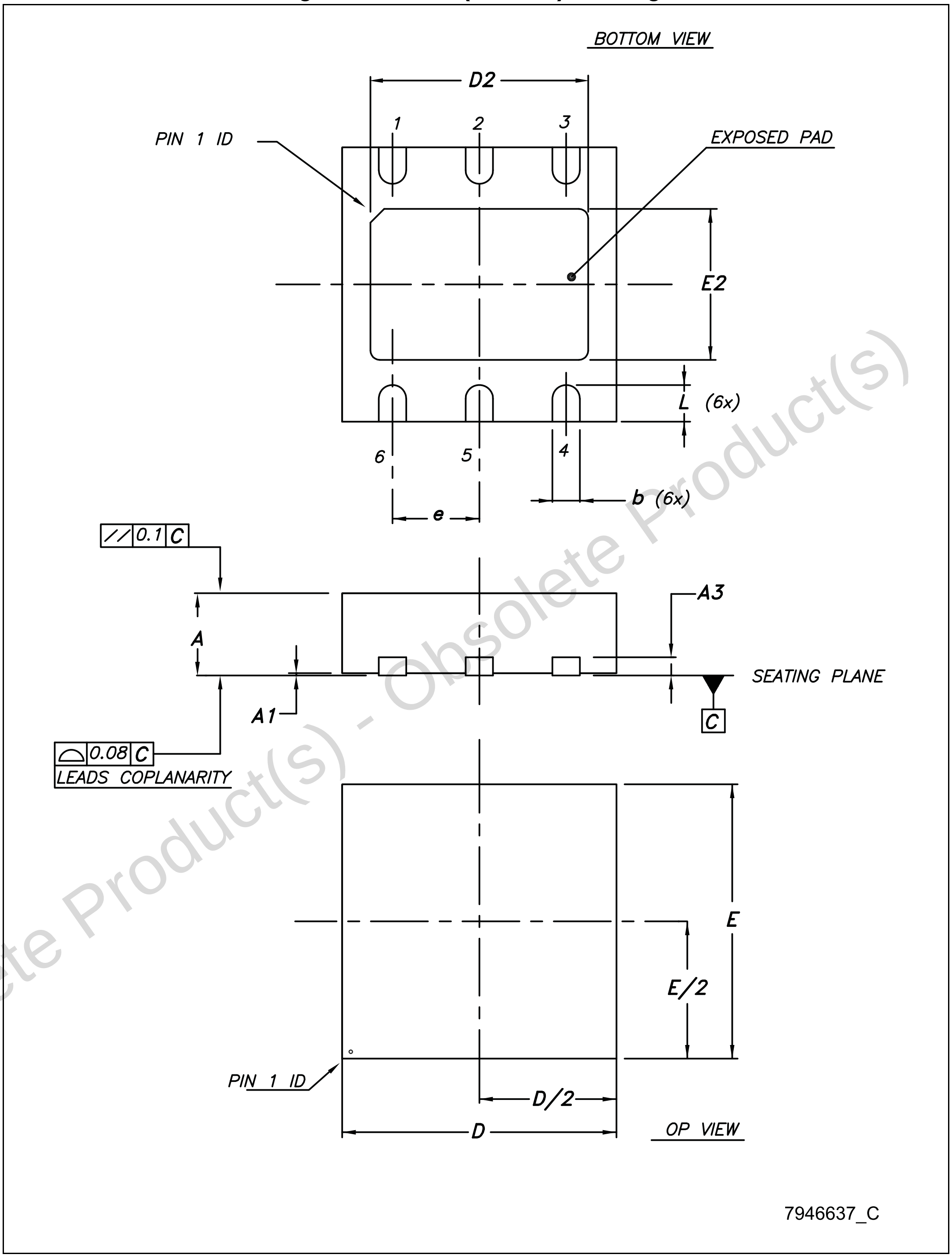
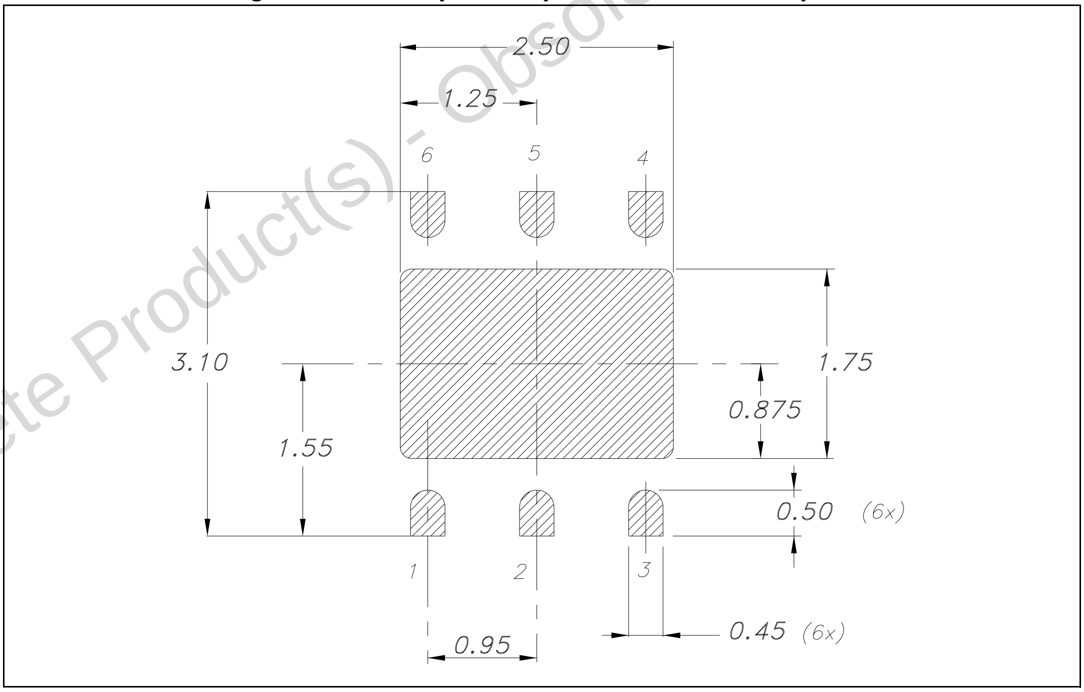


Table 7. DFN6 (3x3 mm) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1
A1	0	0.02	0.05
A3		0.20	
b	0.23		0.45
D	2.90	3	3.10
D2	2.23		2.50
E	2.90	3	3.10
E2	1.50		1.75
		0.95	
L	0.30	0.40	0.50

Figure 24. DFN6 (3x3 mm) recommended footprint



8 Packaging information

Figure 25. DFN6 (3x3 mm) tape

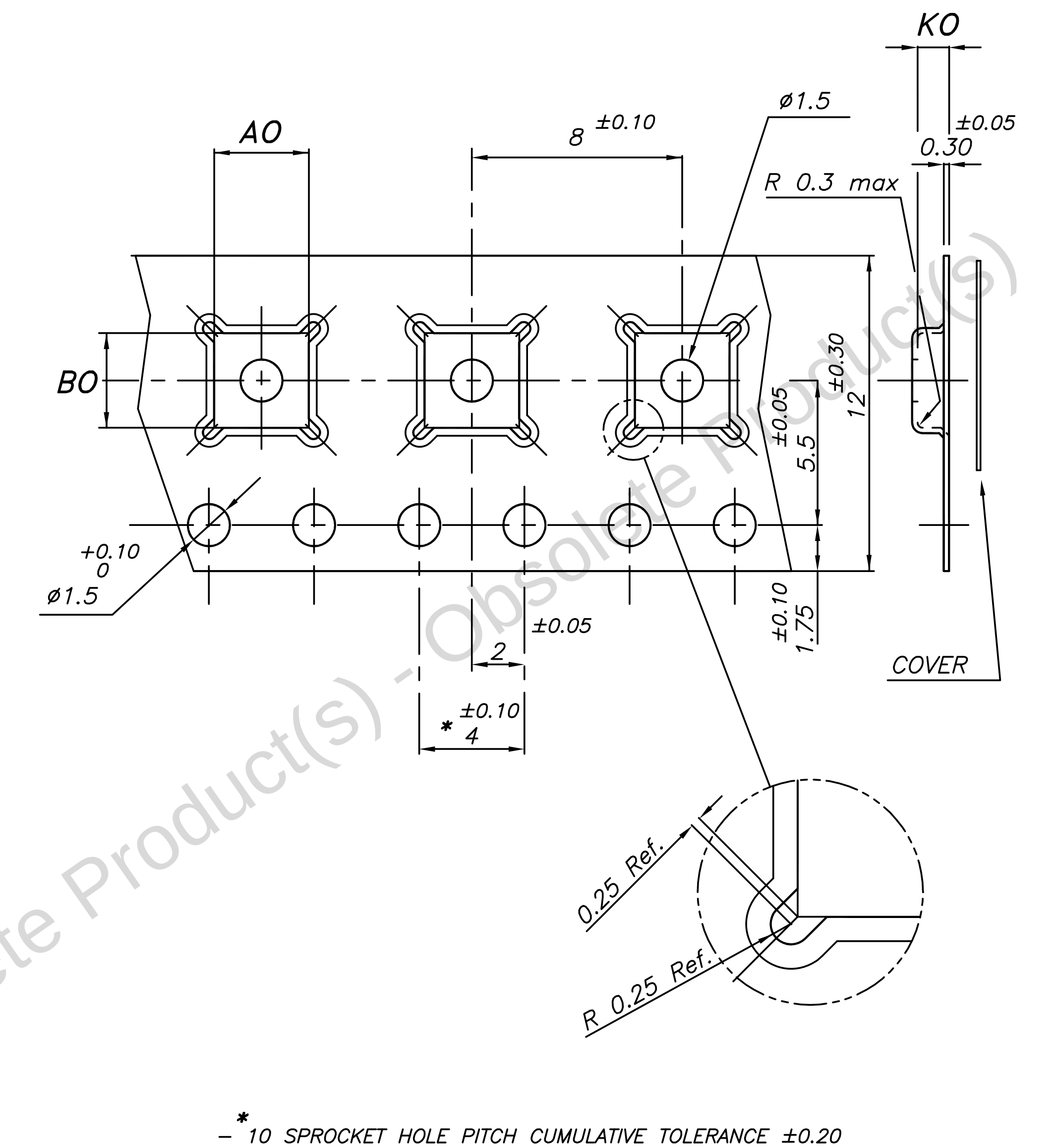


Figure 26. DFN6 (3x3 mm) reel

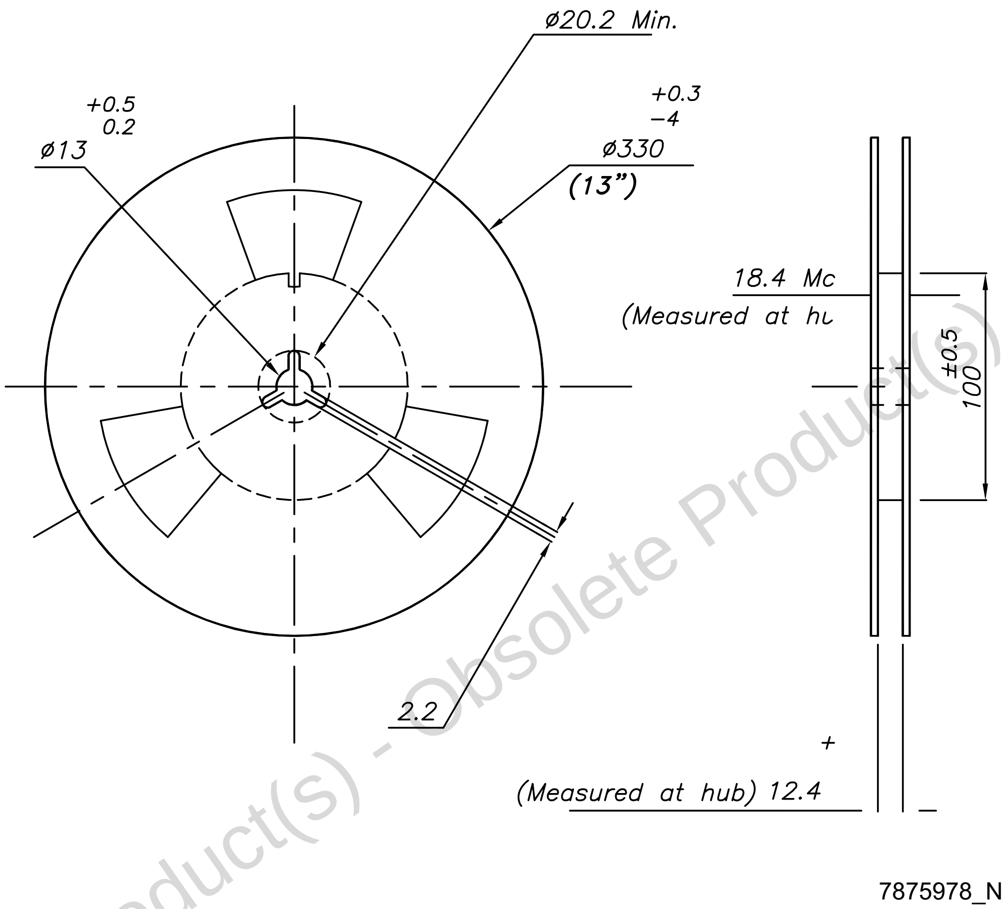


Table 8. DFN6 (3x3 mm) tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A0	3.20	3.30	3.40
B0	3.20	3.30	3.40
K0	1	1.10	1.20

9 Revision history

Table 9. Document revision history

Date	Revision	Changes
25-Feb-2005	1	First release.
10-Jan-2006	2	Add new order codes and tables of the electrical characteristics.
16-May-2006	3	General feature has been updated and add note 3 in table 6.
05-Jul-2006	4	Updated mechanical data DFN6 (3x3).
22-Feb-2007	5	Add note in *Figure 2* and in order codes.
03-Apr-2007	6	Add order codes and mechanical data DFN6D.
05-Sep-2007	7	Add *Table 1* in cover page.
12-Mar-2008	8	Removed: mechanical data DFN6.
09-Apr-2014	9	Changed the part number ST1L02xx to ST1L02. Changed the title in cover page. Updated *Features* and *Description*. Changed the *Table 1: Device summary*. Updated *Figure 2*, and *Table 2*. Updated *Section 4: Electrical characteristics*. Deleted figure titled: ST1L02PM application schematic. Updated title of: *Figure 5*, *Figure 6*, *Figure 9*, *Figure 10*, *Figure 11*, *Figure 12*, *Figure 17*, *Figure 18*, *Figure 19*, *Figure 20* and *Figure 21*. Updated package mechanical data.

Please Read Carefully: