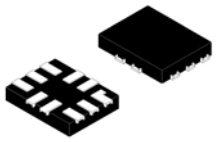
AS21P2THB

Low voltage high bandwidth dual single-pole double-throw analog switch

Datasheet - production data



QFN10
(1.8 x 1.4 mm)

Features

- Ultra low power dissipation:
  - I_{CC} = 1 µA (max.) at T_A = 85 °C
- Low “ON” resistance:
  - R_{ON} = 4.8 Ω (T_A = 25 °C) at V_{CC} = 4.3 V
  - R_{ON} = 5.9 Ω (T_A = 25 °C) at V_{CC} = 3.0 V
- Wide operating voltage range:
  - V_{CC} (opr.) = 1.65 V to 4.3 V
- 4.3 V tolerant and 1.8 V compatible threshold on digital control input at V_{CC} = 2.3 V to 3.0 V
- Typical bandwidth (-3 dB) at 800 MHz on all channels
- USB (2.0) high speed (480 Mbps) signal switching compliant
- Integrated fail safe function
- Interrupt function to indicate to the processor that the device is in dedicated port charging mode
- Latch-up performance exceeds 500 mA per JESD 78, Class II
- ESD performance exceeds JESD22:
  - Dn pins: 4000-V human body model (A114-A)
  - All other pins: 2000-V human body model (A114-A)

Applications

- Wearable
- Sport and fitness
- Portable equipment

Description

The AS21P2THB is a high-speed CMOS low voltage dual analog SPDT (single pole double throw) switch or 2:1 multiplexer/demultiplexer switch fabricated in silicon gate C²MOS technology. It is designed to operate from 1.65 V to 4.3 V, thus making this device the ideal selection for portable applications.

The SEL input is provided to control the switch. The switch nS1 is ON (connected to common ports Dn) when the SEL input is held high and OFF (high impedance state exists between the two ports) when SEL is held low, the switch nS2 is ON (it is connected to common port Dn) when the SEL input is held low and OFF (high impedance state exists between the two ports) when SEL is held high. AS21P2THB has an integrated fail safe function to withstand over-voltage condition when the device is powered off.

The AS21P2THB also has an interrupt pin which sends a signal to the processor when the device is in dedicated port charging mode. Additional key features are fast switching speed, break-before-make-delay time and ultralow power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

Table 1. Device summary

Order code	Package	Packaging
AS21P2THB	QFN10 (1.8 x 1.4 mm)	Tape and reel

Contents

1 Pin settings

Figure 1. Pin connection (top through view)

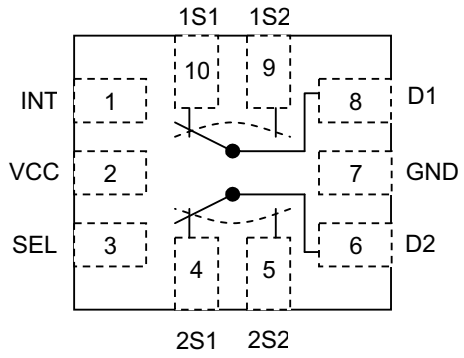


Table 2. Pin description

Pin number	Symbol	Name and function
1	INT	Interrupt
2	VCC	Positive supply voltage
3	SEL	Control
4	2S1	Independent channel for switch 2
5	2S2	Independent channel for switch 2
6	D2	Common channel for switch 2
7	GND	Ground (0 V)
8	D1	Common channel for switch 1
9	1S2	Independent channel for switch 1
10	1S1	Independent channel for switch 1

2 Logic diagram

Figure 2. Logic block diagram

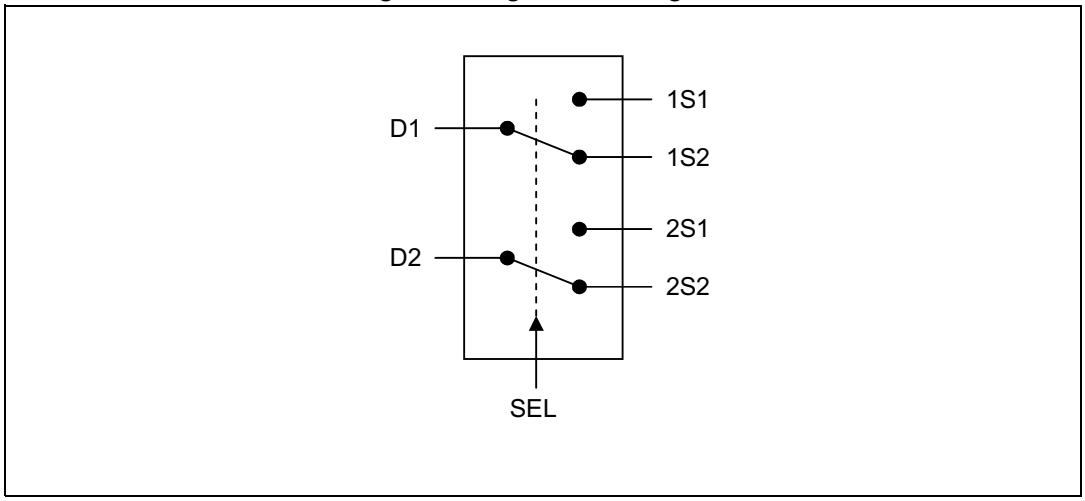


Figure 3. Logic equivalent circuit

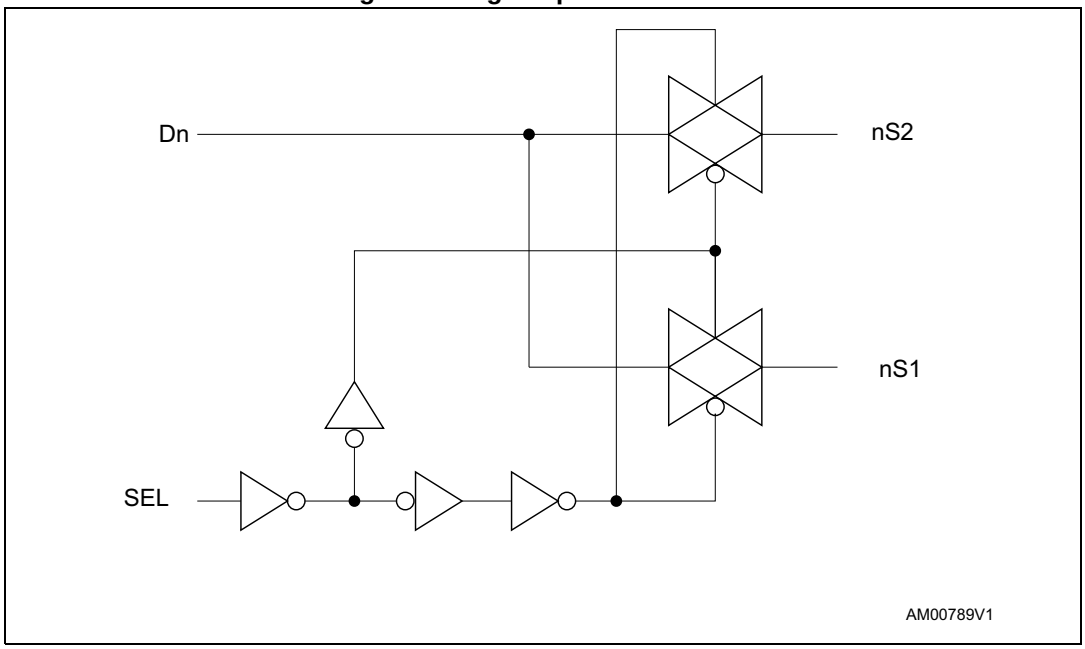


Table 3. Truth table

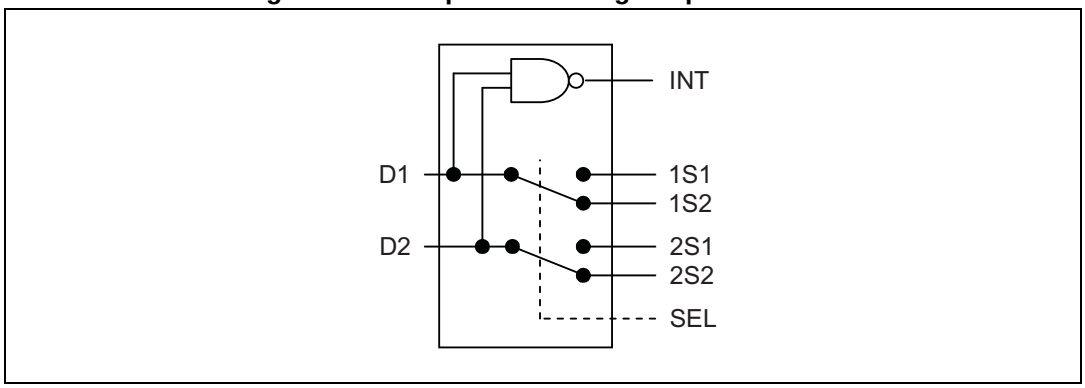
SEL	Switch nS1	Switch nS2
H	ON	OFF(1)
L	OFF(1)	ON

1. High impedance.

3 Dedicated port charging detection

The AS21P2THB has a built-in dedicated port charging detection circuit to detect the condition when the USB D+/D- lines are both in high state. When this occurs, the device sends an interrupt signal to the processor to indicate that the connected USB device is in dedicated port charging mode.

Figure 4. Interrupt function logic representation



4 Maximum rating

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to 5.5	V
V_I	DC input voltage	-0.5 to V_{CC} + 0.5	V
V_{IC}	DC control input voltage	-0.5 to 5.5	V
V_O	DC output voltage	-0.5 to V_{CC} + 0.5	V
I_{IKC}	DC input diode current on control pin (V_{SEL} < 0V)	-50	mA
I_{IK}	DC input diode current (V_{SEL} < 0V)	±50	mA
I_{OK}	DC output diode current	±20	mA
I_O	DC output current	±128	mA
I_{OP}	DC output current peak (pulse at 1ms, 10% duty cycle)	±300	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	±100	mA
P_D	Power dissipation at T_A = 70 °C (1)	1120	mW
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec)	300	°C

1. Derate above 70 °C by 18.5 mW/°C.

4.1 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		1.65 to 4.3	V
V_I	Input voltage		0 to V_{CC}	V
V_{IC}	Control input voltage		0 to 4.3	V
V_O	Output voltage		0 to V_{CC}	V
T_{op}	Operating temperature		-40 to 85	°C
dt/dv	Input rise and fall time control input	V_L = 1.65 V to 2.7 V	0 to 20	ns/V
		V_L = 3.0 to 4.3 V	0 to 10	

5 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	V_{CC} (V)	Test condition	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
V_{IH}	High level input voltage	1.65 – 1.95	–	0.65 V_{CC}	–	–	0.65V_{CC}	–	V
		2.3 – 2.5		1.2	–	–	1.2	–	
		2.7 – 3.0		1.3	–	–	1.3	–	
		3.3 – 3.6		1.4	–	–	1.4	–	
		4.3		1.6	–	–	1.6	–	
V_{IL}	Low level input voltage	1.65 – 1.95	–	–	–	0.25	–	0.25	V
		2.3 – 2.5		–	–	0.25	–	0.25	
		2.7 – 3.0		–	–	0.25	–	0.25	
		3.3 – 3.6		–	–	0.30	–	0.30	
		4.3		–	–	0.40	–	0.40	
V_{IH-INT}	High level input voltage for INT	4.3	–	2.4	–	–	2.4	–	V
V_{IL-INT}	Low level input voltage for INT	4.3	–	–	–	0.9	–	0.9	V
V_{OL-INT}	Low level output voltage for INT	4.3	I_O = 4 mA	–	–	0.40	–	0.50	V
R_{PEAK}	Switch ON peak resistance	1.8	V_S = 0 V to V_{CC} I_S = 8 mA	–	15.1	17.8	–	–	Ω
		2.7		–	6.4	8.0	–	–	
		3.0		–	5.9	7.5	–	–	
		3.7		–	5.0	6.5	–	–	
		4.3		–	4.8	6.1	–	–	
R_{ON}	Switch ON resistance	3.0	V_S = 3 V I_S = 8 mA	–	4.2	5.4	–	–	Ω
		3.0	V_S = 0.4 V I_S = 8 mA	–	5.7	7.0	–	–	

Table 6. DC specifications (continued)

Symbol	Parameter	V_{CC} (V)	Test condition	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
ΔR_{ON}	ON resistance match between channels(1)	1.8	V_S at R_{ON} max I_S = 8 mA	–	–	–	–	–	Ω
		2.7		–	–	–	–	–	
		3.0		–	0.1	–	–	–	
		3.7		–	–	–	–	–	
		4.3		–	–	–	–	–	
R_{FLAT}	ON resistance flatness(2)	1.8	V_S = 0 V to 0.4 V I_S = 8 mA	–	4.5	–	–	–	Ω
		1.8	V_S = 0 V to V_{CC} I_S = 8 mA	–	9.0	–	–	–	
		2.7		–	2.2	–	–	–	
		3.0		–	1.8	–	–	–	
		3.7		–	1.6	–	–	–	
		4.3		–	1.6	–	–	–	
I_{OFF}	OFF state leakage current (Sn), (D)	4.3	V_S = 0.3 or 4 V	-20	–	20	-100	100	nA
I_{IN}	Input leakage current	0 to 4.3	V_{SEL} = 0 to 4.3 V	-0.2	–	0.2	-1.0	1.0	µA
I_{CC}	Quiescent supply current	1.65 to 4.3	V_{SEL} = VCC or GND	-0.2		0.2	-1.0	1.0	µA
I_{CCLV}	Quiescent supply current for low voltage driving	4.3	V_{SEL} = 1.65 V	–	±37	±50	–	±100	µA
			V_{SEL} = 1.80 V	–	±33	±40	–	±50	
			V_{SEL} = 2.60 V	–	±11	±20	–	±30	

1. ΔR_{ON} = max |mSN-nSN|, where m = 1, 2 and n = 1, 2, N = 1, 2
2. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Table 7. AC characteristics (C_L = 35 pf, R_L: 50 Ω, $T_R = T_f \leq 5$ ns)

Symbol	Parameter	V_{CC} (V)	Test conditions	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation delay	1.65 - 1.95	–	–	0.21	–	–	–	ns
		2.3 - 2.7		–	0.15	–	–	–	
		3.0 - 3.3		–	0.14	–	–	–	
		3.6 - 4.3		–	0.13	–	–	–	
t_{ON}	Turn on time	1.65 - 1.95	V_S = 0.8 V	–	34	–	–	–	ns
		2.3 - 2.7	V_S = 1.5 V	–	20	23	–	26	
		3.0 - 3.3		–	15	17	–	20	
		3.6 - 4.3		–	13	15	–	17	
t_{OFF}	Turn off time	1.65 - 1.95	V_S = 0.8 V	–	27	–	–	–	ns
		2.3 - 2.7	V_S = 1.5 V	–	19	22	–	25	
		3.0 - 3.3		–	14	16	–	18	
		3.6 - 4.3		–	11	13	–	14	
t_D	Break-before-make time delay	1.65 - 1.95	C_L = 35 pF R_L = 50 Ω V_S = 1.5 V	–	10	–	–	–	ns
		2.3 - 2.7		–	6	–	–	–	
		3.0 - 3.3		–	4	–	–	–	
		3.6 - 4.3		–	3	–	–	–	

Table 8. AC electrical characteristics (C_L = 5 pF, R_L = 50 Ω, T_A = 25 °C)

Symbol	Parameter	V_{CC} (V)	Test conditions	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
Q	Charge injection	1.65	C_L = 100 pF V_{GEN} = 0 V R_{GEN} = 0 Ω	–	3.9	–	–	–	pC
		2.3		–	4.8	–	–	–	
		3.0		–	5.2	–	–	–	
		4.3		–	6.4	–	–	–	
OIRR	OFF isolation(1)	1.65 – 4.3	V_S = 1V $_{RMS}$, f = 1 MHz Signal = 0 dBm	–	-78	–	–	–	dB
			V_S = 1 V_{RMS}, f = 10 MHz Signal = 0 dBm	–	-57	–	–	–	
Xtalk	Crosstalk	1.65 – 4.3	V_S = 1 V_{RMS}, f = 1 MHz Signal = 0 dBm	–	-78	–	–	–	dB
			V_S = 1V_{RMS}, f = 10 MHz Signal = 0 dBm	–	-58	–	–	–	
BW	-3dB bandwidth	3.0 – 4.3	R_L = 50 Ω Signal = 0 dBm	–	800	–	–	–	MHz
C_{IN}	Control pin input capacitance		V_{CC} = 0 V	–	2	–	–	–	pF
C_{ON}	Sn port capacitance when switch is enabled	3.3	f = 240 MHz	–	6	–	–	–	
C_{OFF}	Sn port capacitance when switch is disabled	3.3	f = 240 MHz	–	2	–	–	–	

1. Off isolation = 20 Log10 (V_D/V_S), V_D = output, V_S = input to off switch.

Table 9. USB related AC electrical characteristics

Symbol	Parameter	V_{CC} (V)	Test conditions	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
$t_{SK(0)}$	Channel-to-channel skew	3.0 - 3.6	C_L = 10 pF	–	26	–	–	–	ps
$t_{SK(P)}$	Skew of opposite transition of the same output	3.0 - 3.6	C_L = 10 pF	–	60	–	–	–	ps
T_J	Total jitter	3.0 - 3.6	R_L = 50 Ω C_L = 10 pF $t_R = t_F$ = 750 ps at 480 Mbps	–	130	–	–	–	ps

6 Test circuit

Figure 5. ON resistance

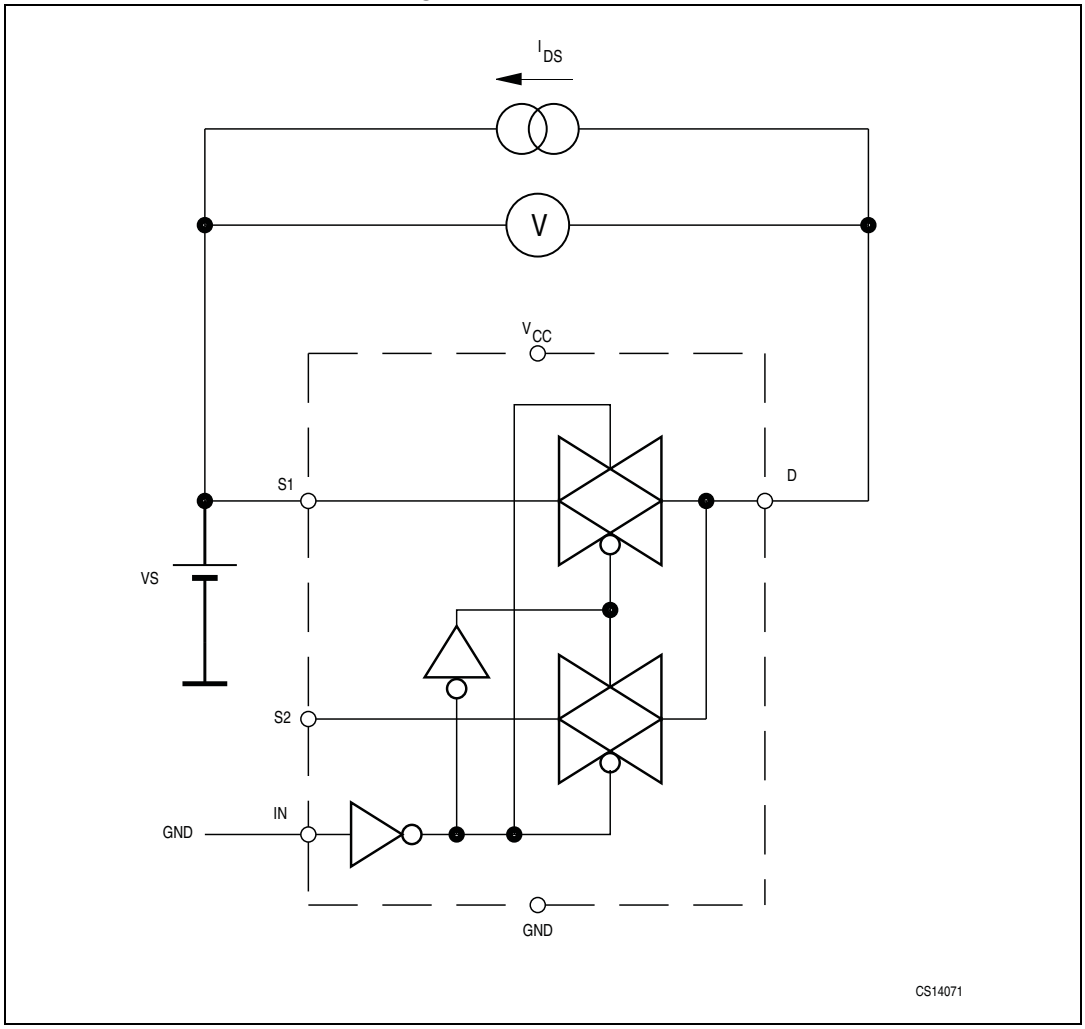


Figure 6. OFF leakage

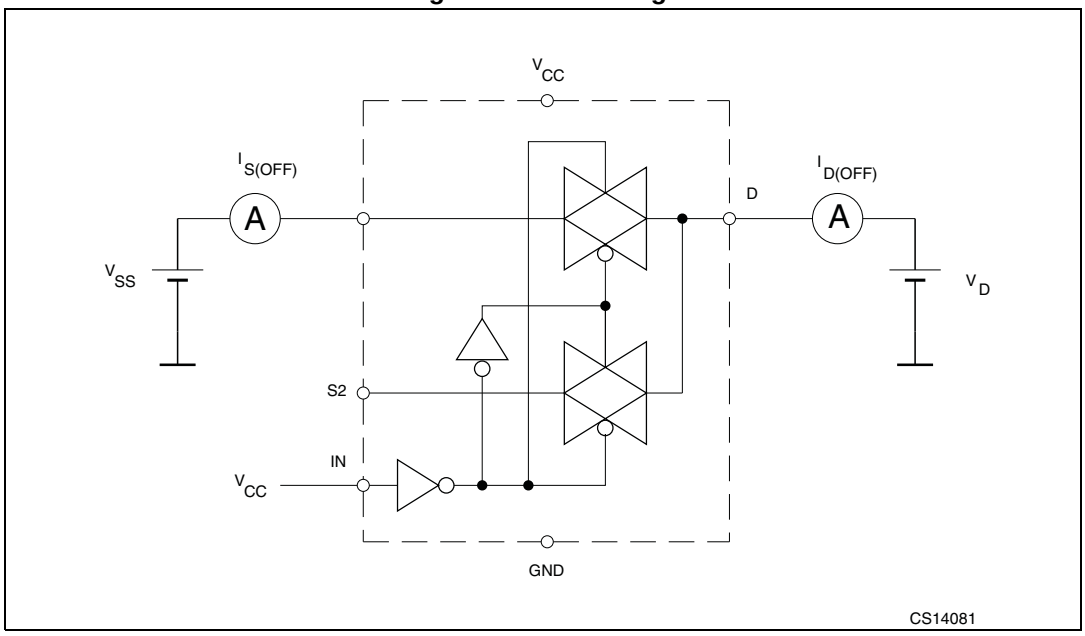


Figure 7. OFF isolation

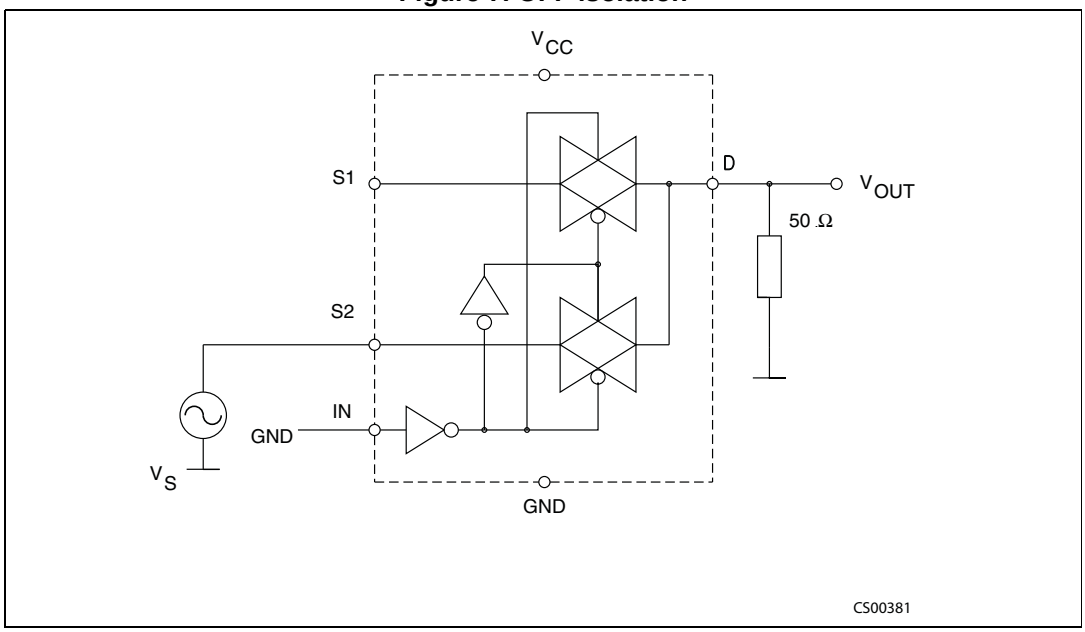


Figure 8. Bandwidth

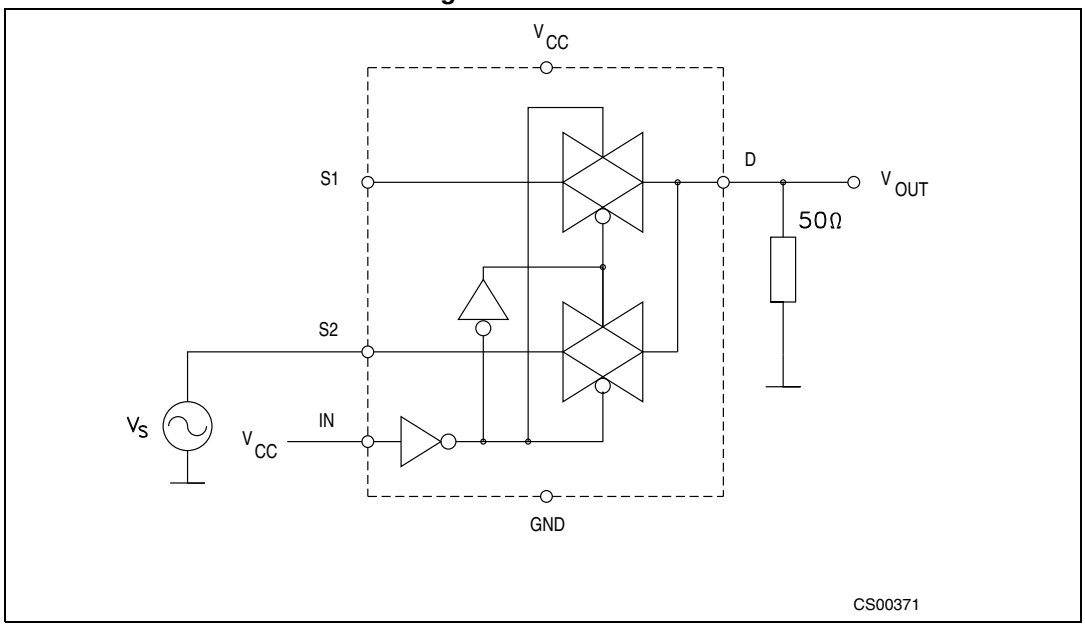


Figure 9. Channel-to-channel crosstalk

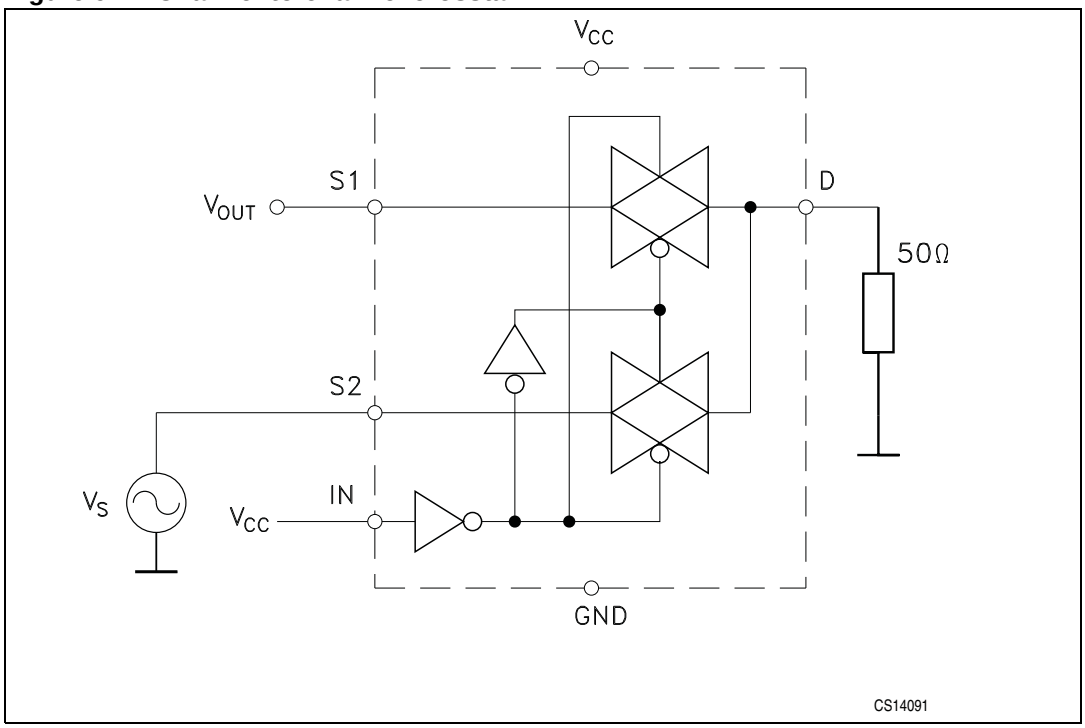
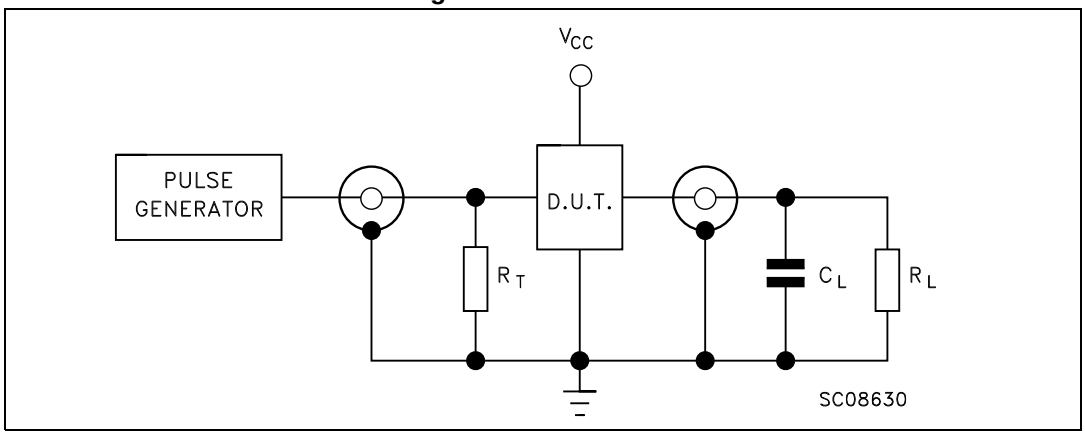


Figure 10. Test circuit



1. C_L = 5/35 pF or equivalent (includes jig and probe capacitance)
2. R_L = 50 Ω or equivalent
3. R_T = Z_{OUT} of pulse generator (typically 50 Ω)

Figure 11. Break-before-make time delay

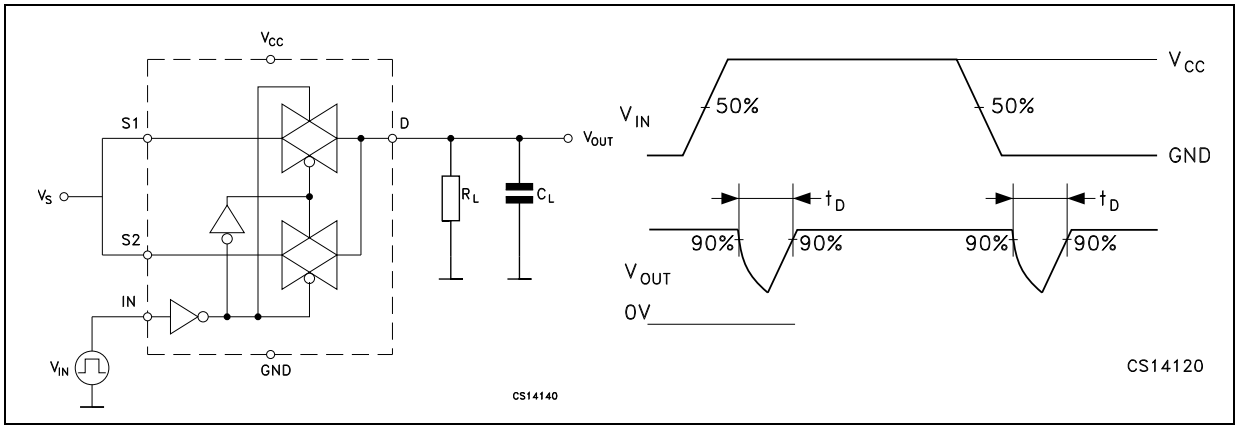


Figure 12. Switching time and charge injection (V_{GEN} = 0 V, R_{GEN} = 0 Ω, R_L = 1 MΩ, C_L = 100 pF)

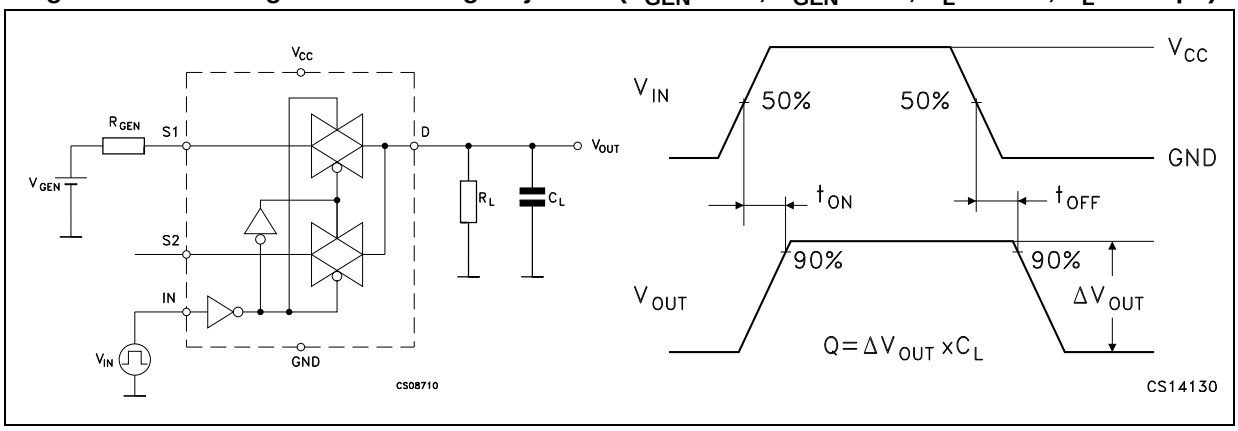
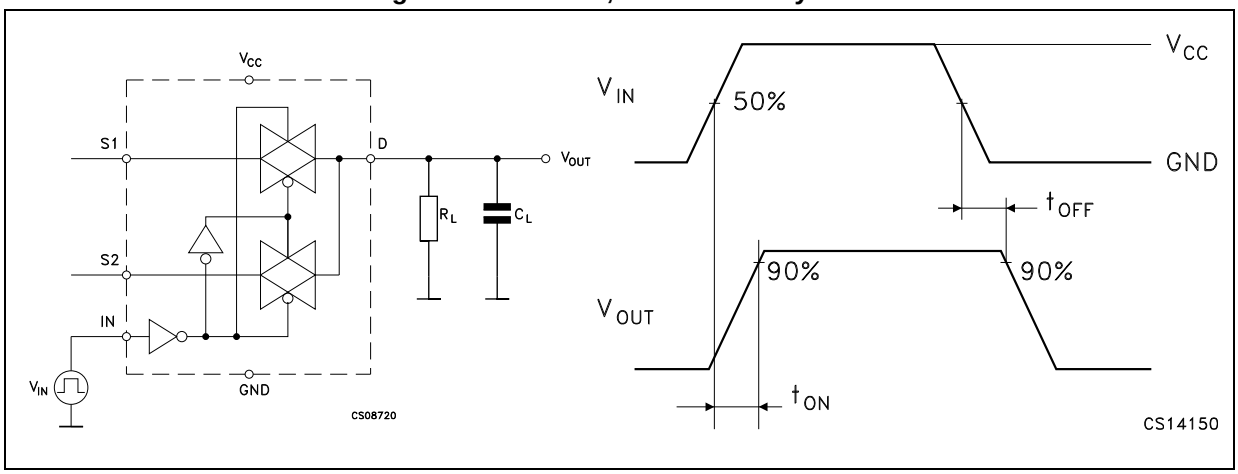


Figure 13. Turn ON, turn OFF delay time



7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 14. Package outline for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.4 mm pitch

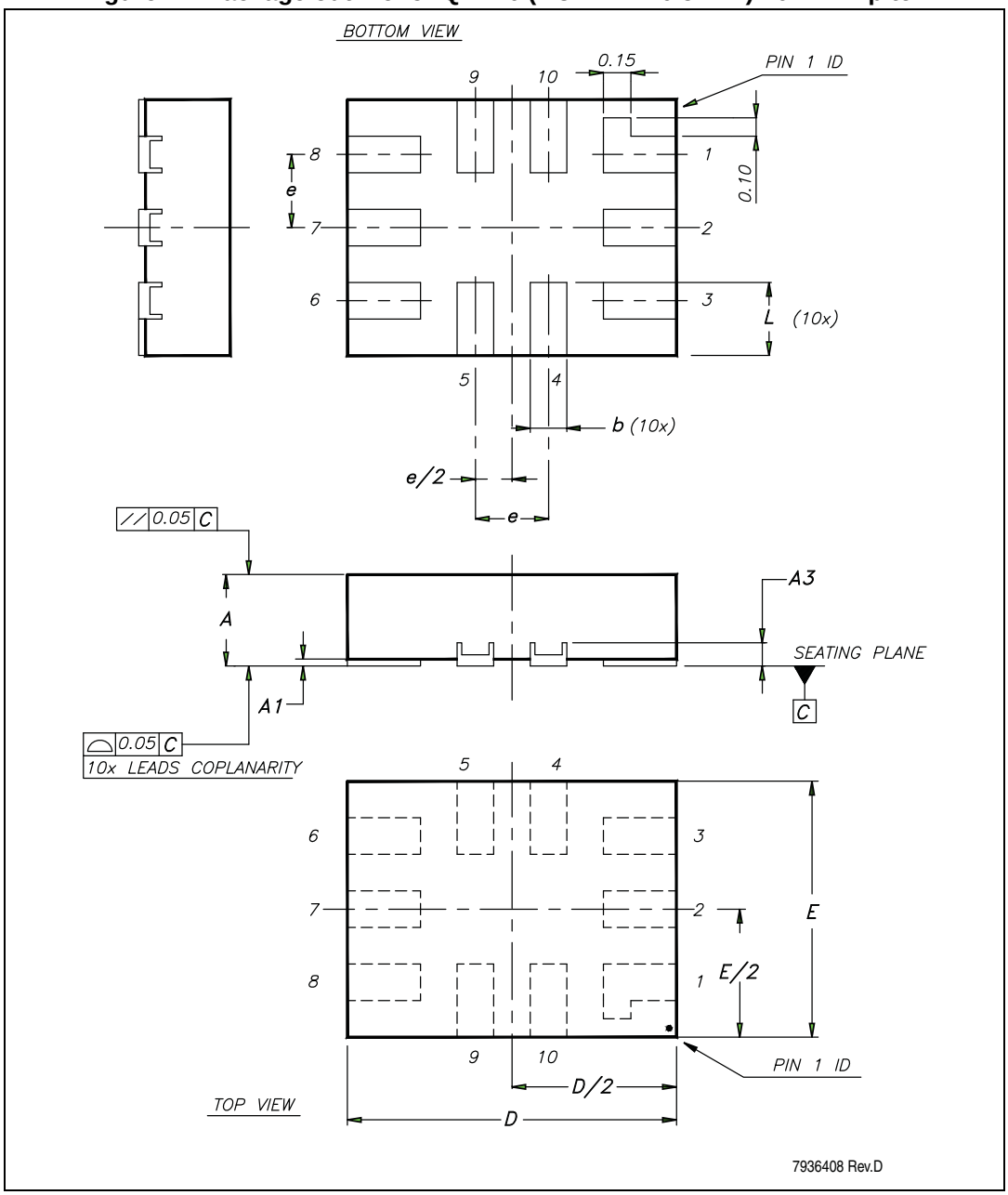


Table 10. QFN10 (1.8 x 1.4 x 0.5 mm) - 0.4 mm pitch

Symbol	Millimeters		
	Min.	Typ.	Max.
A	0.45	0.50	0.55
A1	0	0.02	0.05
A3		0.127	
b	0.15	0.20	0.25
D	1.75	1.80	1.85
E	1.35	1.40	1.45
e		0.40	
L	0.35	0.40	0.45

Figure 15. Footprint recommendations for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.4 mm pitch

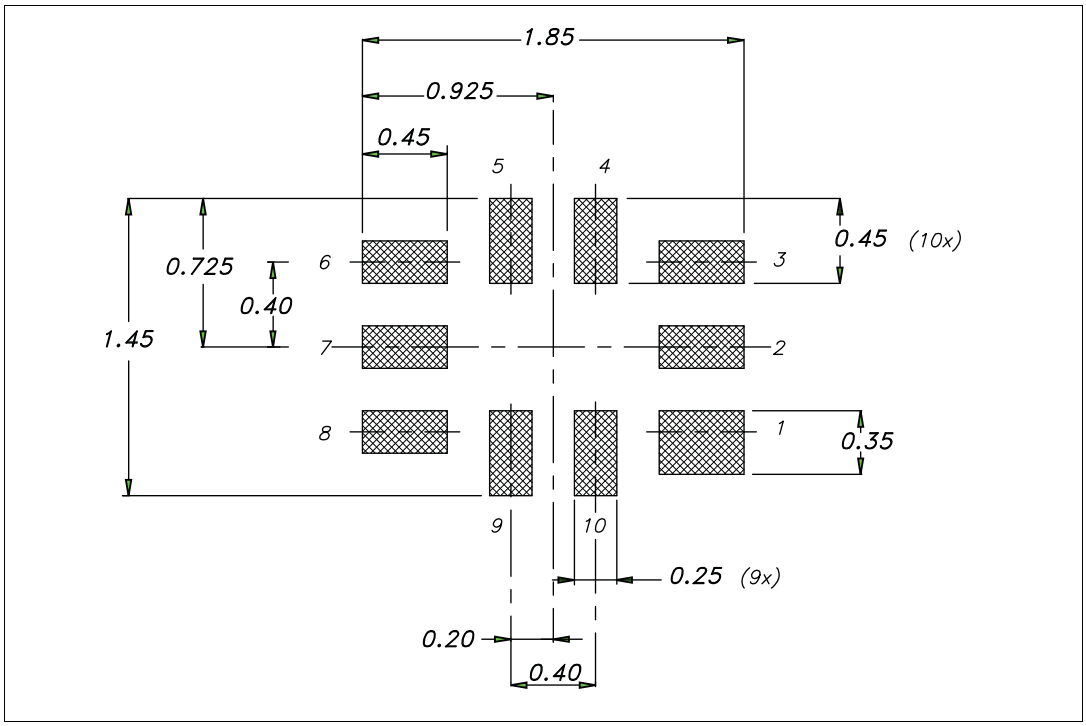


Figure 16. Carrier tape for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.4 mm pitch

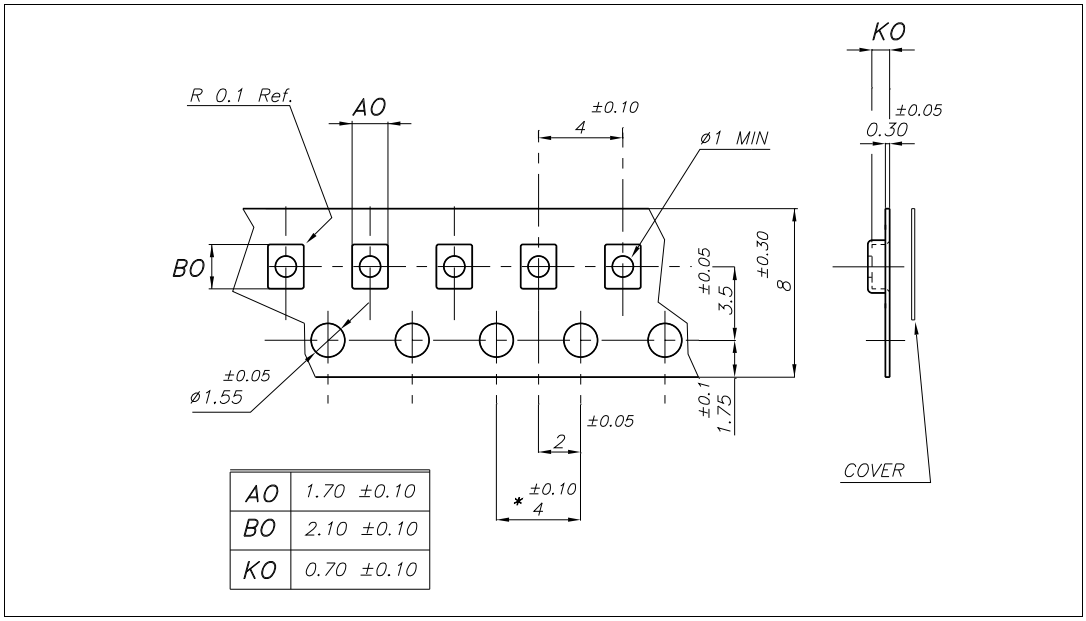


Figure 17. Reel information (front side) for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.4 mm pitch

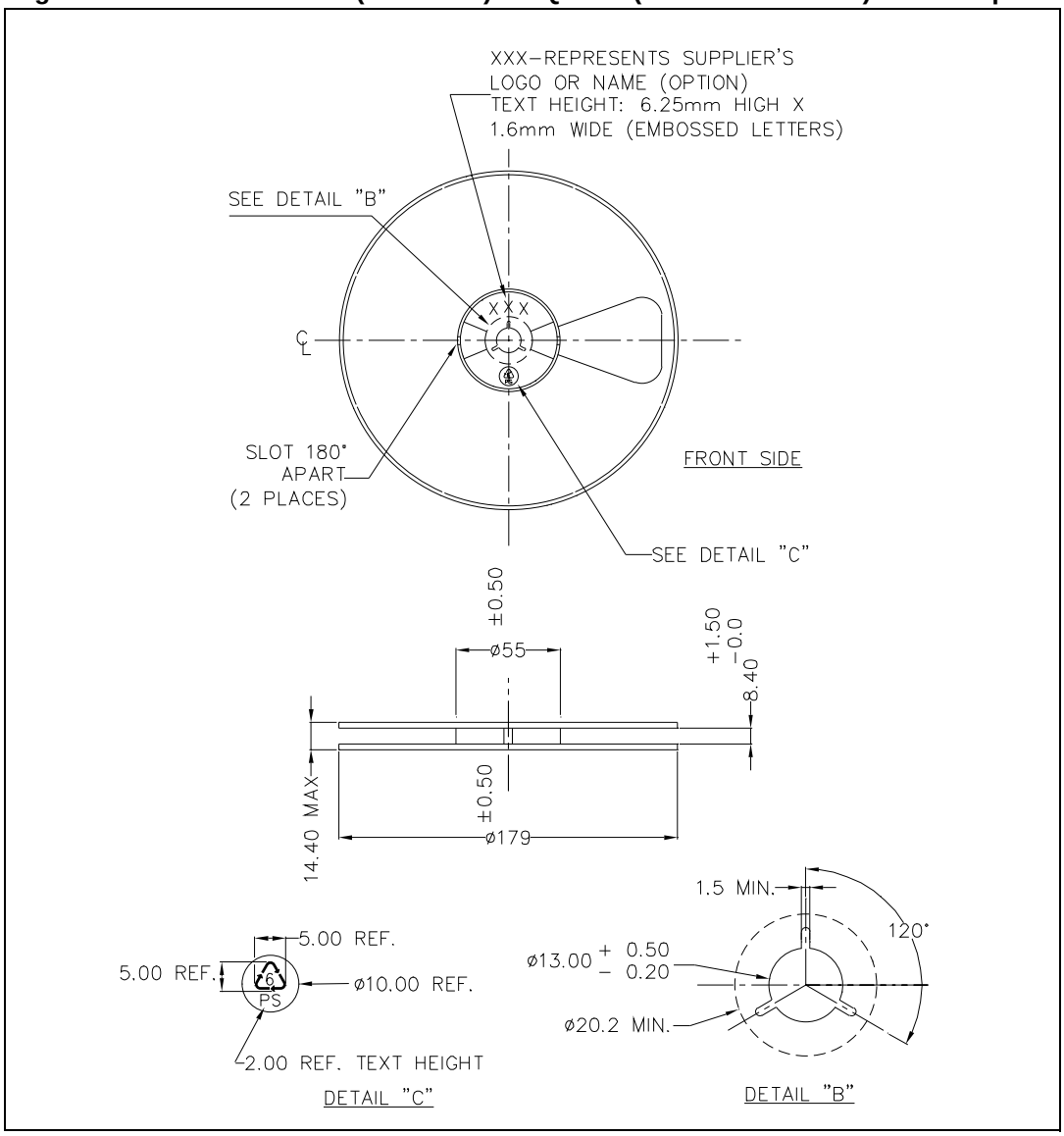
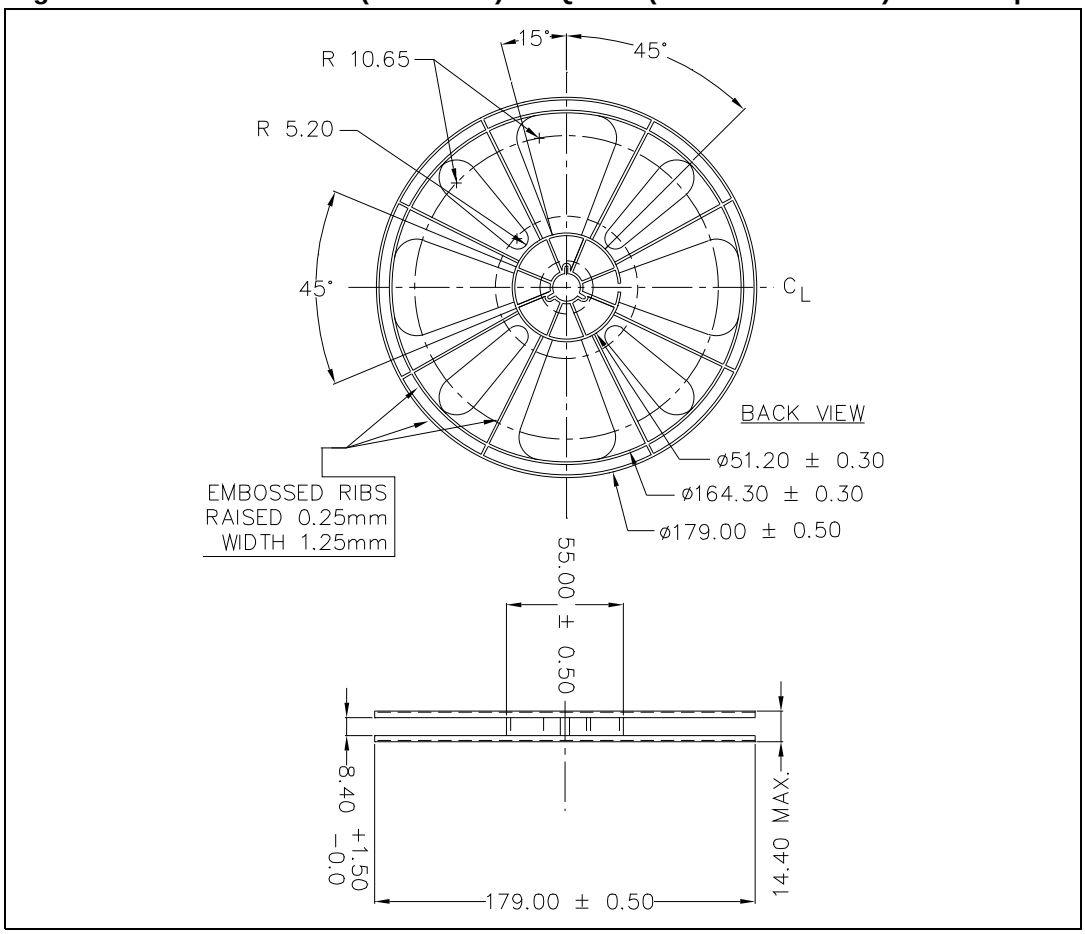


Figure 18. Reel information (back view) for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.4 mm pitch



8 Revision history

Table 11. Document revision history

Date	Revision	Changes
07-Mar-2014	1	Initial release.

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