Secondary-side rectification for LLC resonant converter featuring SRK2000

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Introduction

The EVLSRK2000 is a family of demonstration boards designed for the evaluation of the SRK2000 in LLC resonant converters with synchronous rectification (SR).

The first part of this application note is a brief description of the IC features while the second is dedicated to the board description. Finally, some considerations regarding circuit optimization and performance are given.

This board was realized in four different configurations depending on the mounted SR MOSFETs. Different board codes are shown in *Table 1*:

Table 1. Demonstration board ordering codes

Ordering code	SR MOSFET P/N	MOSFET package	MOSFET $R_{DS(on)}$	MOSFET BV_{DSS}
EVLSRK2000-L-40	STL140N4LLF5	PowerFLAT™	2.75 mΩ	40 V
EVLSRK2000-L-60	STL85N6F3	PowerFLAT™	5.70 mΩ	60 V
EVLSRK2000-D-40	STD95N4F3	DPAK	5.80 mΩ	40 V
EVLSRK2000-S-40	STS15N4LLF3	SO-8	5.00 mΩ	40 V

Figure 1. EVLSRK2000: smart driving control for LLC resonant converter

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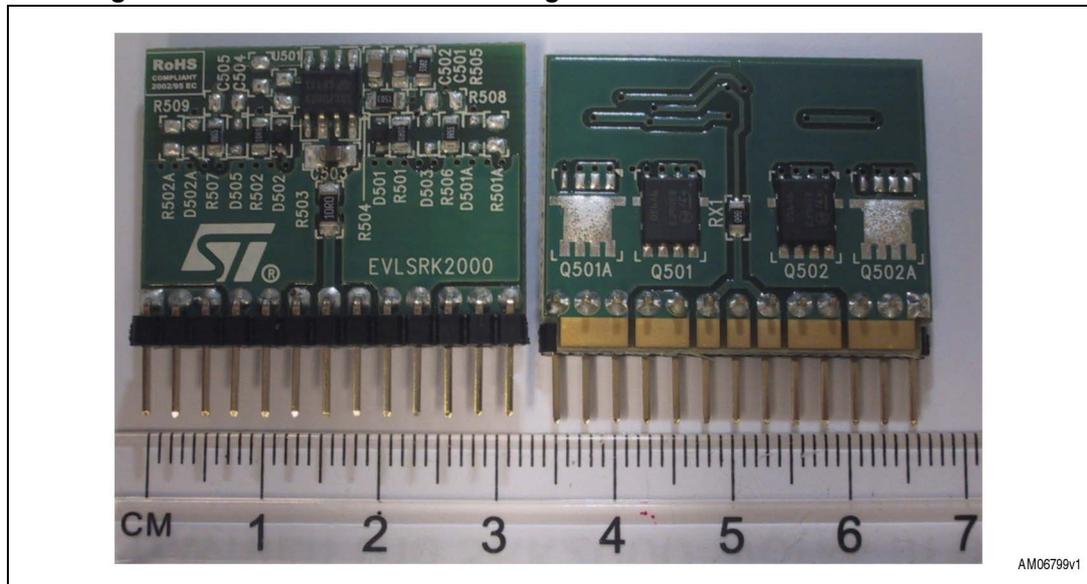
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1   SRK2000 main characteristics

The main features of the SRK2000 are described below. The values of the following parameters are reported in the SRK2000 datasheet (see *1* in *Section 8: References on page 25*).

The SRK2000 implements a control scheme specific for secondary-side synchronous rectification in an LLC resonant converter that uses a transformer with center-tap secondary winding for full-wave rectification. It provides two high-current gate-drive outputs, each capable of driving one or more N-channel power MOSFETs in parallel. Each gate driver is controlled separately and an interlocking logic circuit prevents the two synchronous rectifier MOSFETs from conducting simultaneously.

Figure 2. Block diagram of LLC converter with synchronous rectification
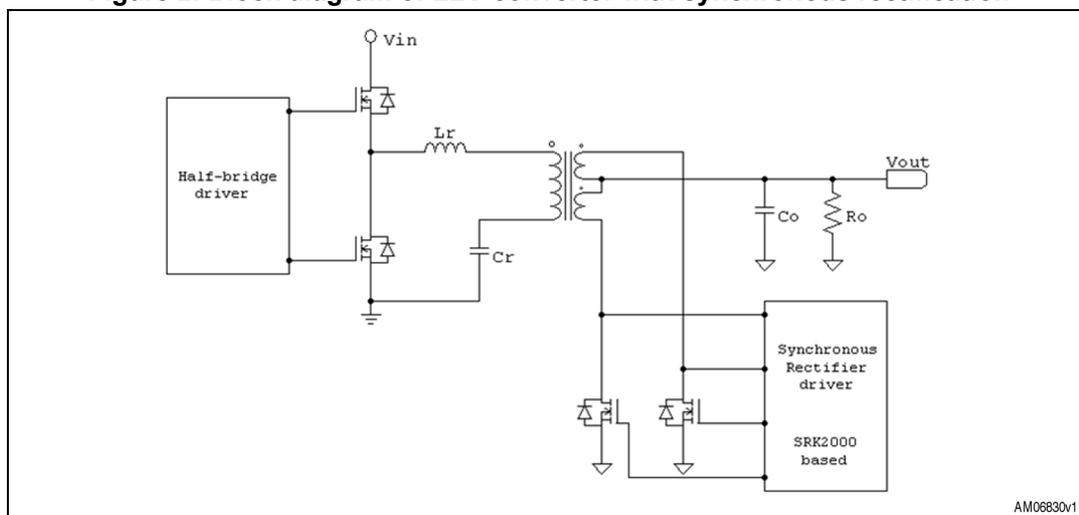
1.1   Drain MOSFET sensing and driving logic

The core function of the IC is to switch on each synchronous rectifier MOSFET whenever the corresponding transformer half-winding starts conducting (i.e. when the MOSFET body diode starts conducting) and then to switch it off when the flowing current approaches zero. For this purpose, the IC is provided with two pins (DVS1 and DVS2) able to sense the power MOSFET drain voltage level. Because each power MOSFET is turned on when its body diode is conducting, zero voltage turn-on is achieved.

Device operations described below refer to *Figure 3*.

    a)   When the current ISR1 starts flowing through the body diode, the voltage across the power MOSFET drain-source becomes negative; as it reaches the negative threshold $V_{TH.ON}$, the power MOSFET is switched on.

           The threshold at which the power MOSFET turns on can be set by *Equation 1*:

Equation 1

$$V_{THON} = R_D \cdot I_{DVS1,2ON} + V_{DVS1,2\underline{T}H}$$

where $I_{DVS1,2.on}$ is the current sourced out of the DVS1,2 pins (50 µA typ.) and $V_{DVS1,2\_TH}$ is the lower clamp voltage of the DVS1,2 pins (-0.2 V typ.).

This may enable the ON threshold to be set according to the SR power MOSFET body diode V_F chosen for the application or the external diode connected in parallel to the power MOSFET drain-source (e.g. Schottky rectifier).

The current sourcing out of the DVS1,2 pin is enabled after the drain-source voltage experiences a voltage below the pre-triggering level $V_{DVS1,2\_PT}$ (negative going edge) and is disabled once the rectifier is switched on. A debouncing delay (T_{PD_ON}) is introduced after the current generator is activated in order to avoid false triggering of the gate driver.

In some applications, $R_{D1,2}$ is also needed to limit the current that can be injected into the DVS pins when the corresponding SR power MOSFET is off. In fact, when one power MOSFET is off (and the other is conducting) its drain-to-source voltage is slightly higher than twice the output voltage; if this exceeds the voltage rating of the internal clamp (VccZ = 36 V typ.), RD1,2 has to limit the injected current below the maximum rating (25 mA). In addition, the SRK2000 clamping circuit dissipation must be taken into account to avoid device overheating. In this case, *Equation 1* is used to check that the resulting $V_{TH.ON}$ is compatible with the forward drop of the SR power MOSFET body diode (or the parallel external diode).

b) Once the power MOSFET is turned on, its drain-source voltage drops to:

Equation 2

$$V_{DS1,2} = R_{DS(on)} \cdot I_{SR1,2}$$

which is negative because current flows from source to drain. When this voltage reaches (exceeds) the turn-off threshold $V_{DVS1,2\_Off}$, the power MOSFET is switched off. The user can set the turn-off threshold selecting between two different values (see *1* in *Section 8: References on page 25*) by properly biasing the EN pin during the IC startup phase.

c) After the power MOSFET is switched off, the current still flows through its body diode (causing the drain-source voltage to jump negative) until it becomes zero; then the transformer winding voltage reverses and the drain-source voltage starts increasing. As it exceeds the arming voltage $V_{DVS1,2\_A}$ (positive going edge), the gate drive of the second power MOSFET is armed and the operation, described above, now applies to this rectifier.

Figure 3. Power MOSFET drain voltage sensing and typical waveforms
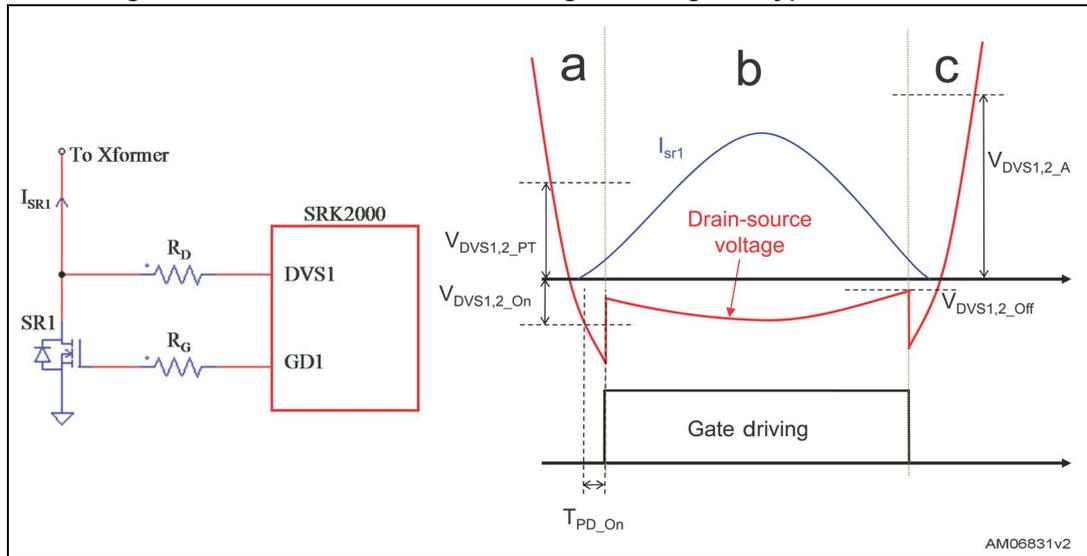
Power losses are certainly much higher during phases a) and c), when the secondary current flows through the SR power MOSFET body diode, than during phase b), when the current flows through the power MOSFET channel. Therefore, minimizing phase a) and c) duration is a good way to optimize the efficiency. In the following section, the reason circuit parasitic elements play a fundamental role in this is described.

1.2 Drain sensing optimization

Drain voltage sensing must be very accurate to avoid disturbances and minimize the parasitic elements that can affect it. The most important of these are shown in *Figure 4*.

Figure 4. Parasitic elements model
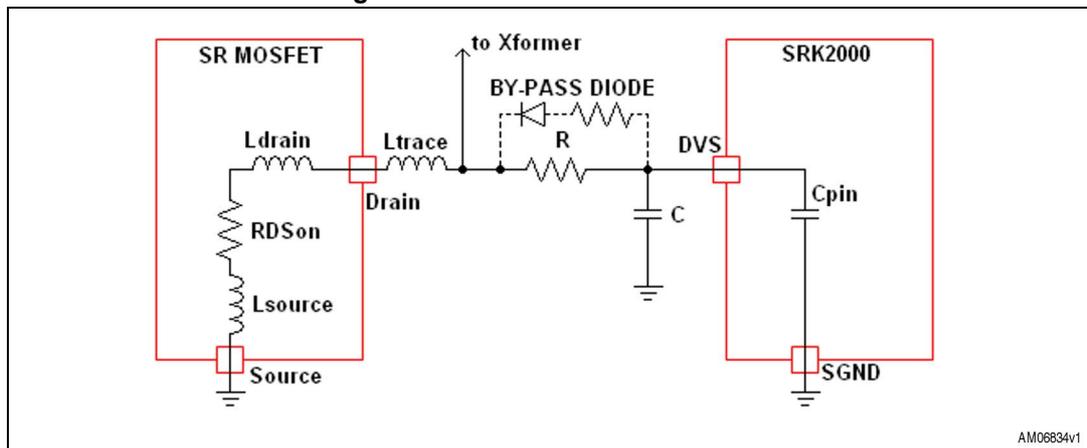
The stray inductance of the power MOSFET leads, internal bonding (L_{source}, L_{drain}) and PCB trace (L_{trace}) connecting the power MOSFET to the sensing trace, introduces a discrepancy between the sensed voltage and the actual voltage drop across $R_{DS(on)}$ in the effective drain voltage sensing. The contribution of L_{trace} can be minimized by connecting the sensing trace as close as possible to the power MOSFET but L_{drain} and L_{source} are power MOSFET parameters and cannot be modified externally. As shown on the left-hand

side of *Figure 5*, this error causes an early power MOSFET turn-off. This anticipation is partially compensated by the RC formed by the sensing resistor R and the DVS pin capacitance, but it may be necessary to add an external capacitance; in particular when using power MOSFET packages with a high associated stray inductance, such as the TO-220.

In several cases it can be advantageous to over-compensate with the external capacitor, therefore introducing an additional delay to the power MOSFET turn-off. This solution, shown on the right-hand side of *Figure 5*, reduces the current flowing through the power MOSFET body diode increasing the efficiency. Power MOSFET turn-off fine tuning must be handled carefully because, if the power MOSFET is turned off after the drain-source voltage becomes positive, the current reverses and begins flowing from drain-to-source with consequent converter malfunctioning.

Figure 5. Effect of parasitic elements on power MOSFET turn-off
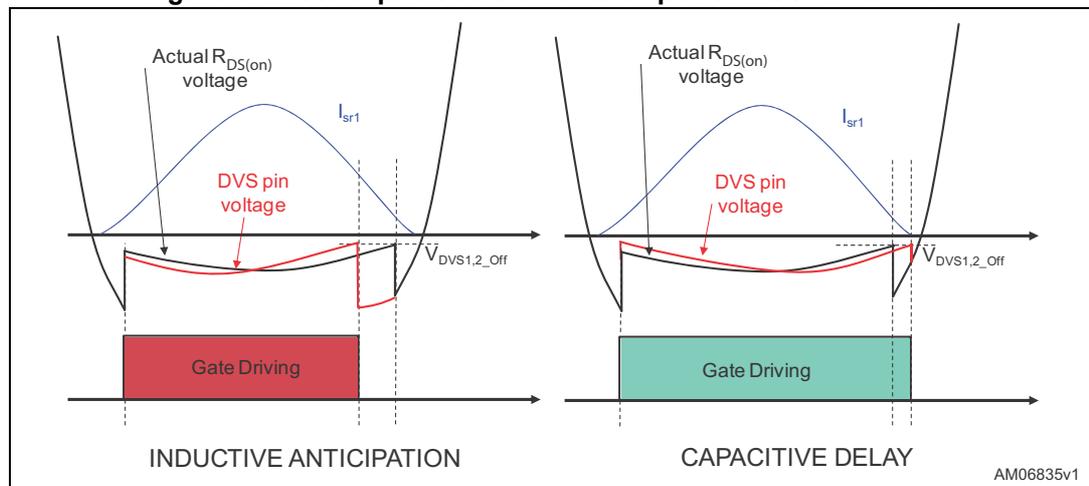
A second effect associated to the parasitic elements is related to the power MOSFET turn-on. Before turn-on, at the half-bridge inversion, the corresponding drain voltage starts decreasing; the DVS voltage also drops but the RC formed by the parasitic capacitance of the DVS pin (about 10 pF) and the sensing resistors introduces a time constant that slows down the sensed signal. During this phase the power MOSFET stray inductance does not contribute because there is no current flowing through it. As illustrated in *Figure 6*, this results in a late power MOSFET turn-on which adversely affects efficiency.

This turn-on delay, which is negligible if the sensing resistor value is indicatively below 1 kΩ, becomes significant in a case where the resistor value is high and, obviously, further increases if an external capacitor is mounted between the pin and ground as previously indicated. To avoid this effect, a bypass diode can be mounted in parallel to the sensing resistor. In this way, the parasitic capacitance is discharged through the diode dynamic resistance instead of the sense resistor. A 100-200 Ω resistor in series to the bypass diode is recommended to limit the current sourced from the DVS pins in case SR power MOSFET drain voltage goes excessively below ground.

Figure 6. Effect of parasitic elements on power MOSFET turn-on
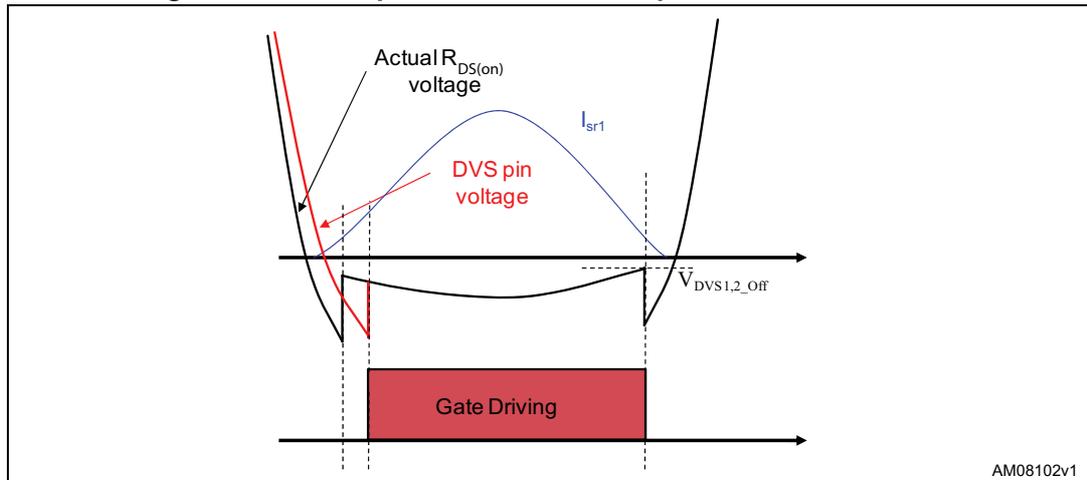
1.3   Blanking time

One peculiarity of resonant converters and in particular of LLCs which differentiate them from hard switching topologies, like flyback or forward, is that secondary currents have a sinusoidal shape. This requires handling of the SR with a dedicated logic scheme: as shown in *Figure 7*, the secondary current is not monotonic and consequently the same current level is crossed twice each half-cycle and the DVS voltage also crosses the turn-off threshold twice.

Figure 7. Blanking time
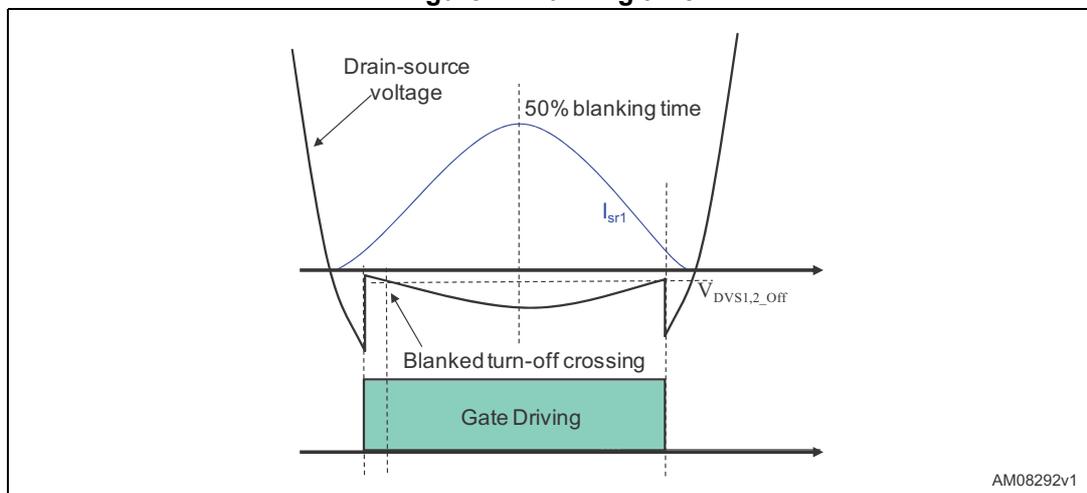
To avoid switch-off after the first crossing, a blanking time is introduced. It is important to point out that this blanking time must be related to the switching period, because the operating frequency can change considerably depending on the converter design and the operating point. In the SRK2000, this blanking time is set to 50% of each half-cycle.

There is a peculiar condition that needs highlighting. In many cases, except for some unusual designs operating well below resonance, the secondary current peak value is achieved after 50% of the half-cycle. Depending on the converter design and on the power MOSFET $R_{DS(on)}$, at the light load the turn-off threshold may happen to be very close to the

peak current and, consequently, the turn-off point may jump from one half-cycle to the next between the 50% limit imposed by the blanking time and the desired turn-off point. The result is a sort of sub-harmonic oscillation in the duty cycle of the SR power MOSFET. This has no significant effect as long as the oscillation amplitude is limited but could cause instability in the case of wider oscillation. For this reason the SRK2000 sets the blanking time in track with the switching period, therefore, keep it as close as possible to the peak current.

Figure 8. Duty cycle oscillation when V$_{DVS}$ at 50% cycle almost equals V$_{DVS1,2}$ $_{Off}$
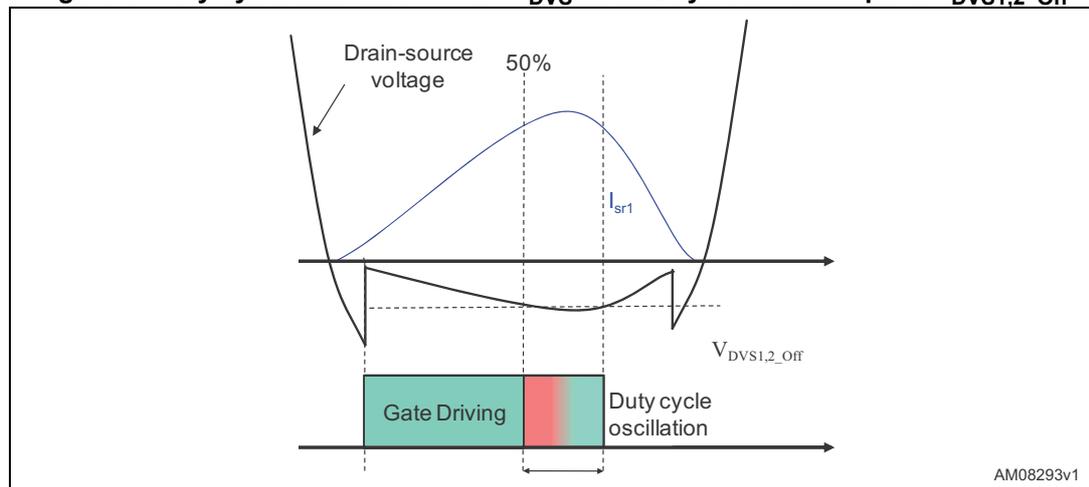
1.4 Light load operation and sleep mode

A unique feature of the SRK2000 is its intelligent automatic sleep mode. The internal logic circuitry is able to detect a light load condition of the converter and stop gate driving, reducing also IC's quiescent consumption. This improves converter efficiency at the light load, where the power losses on the rectification body diodes become lower than the power losses in the power MOSFETs and those related to their driving.

The IC is also able to detect an increase of the converter's load and automatically restart gate driving.

The automatic sleep mode detection is performed by comparing the duration of a half-cycle to the SR power MOSFET conduction time. The duration of a half-cycle is measured by generating a clock signal each time the half-bridge voltage reverts. The IC enters sleep mode when the conduction time of the two SR power MOSFETs falls below 40% of the measured half-period. *Figure 9* shows details of time measuring for sleep mode entering. To avoid erroneous decisions, this sleep mode condition must be confirmed on at least one of the two sections for 16 consecutive resonant converter switching cycles.

Figure 9. Conduction time sensing during normal operation
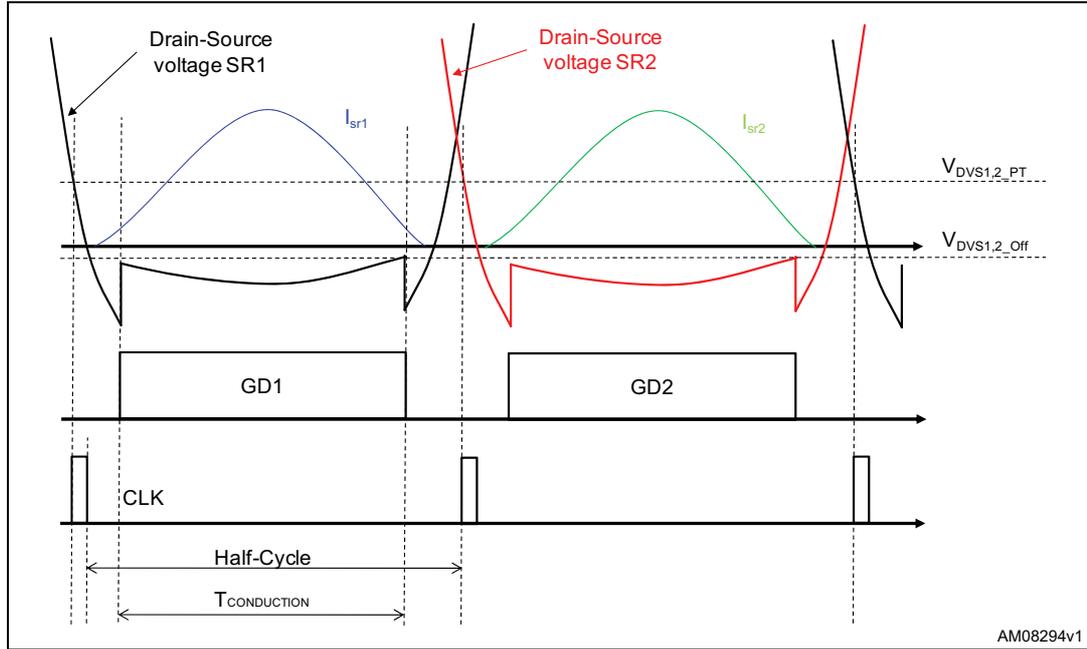
Once in sleep mode, gate driving is re-enabled when body diode conduction time of both MOSFETs exceeds 60% of the half-cycle. *Figure 10* shows details of time measuring for sleep mode exiting.

Figure 10. Conduction time sensing under sleep mode
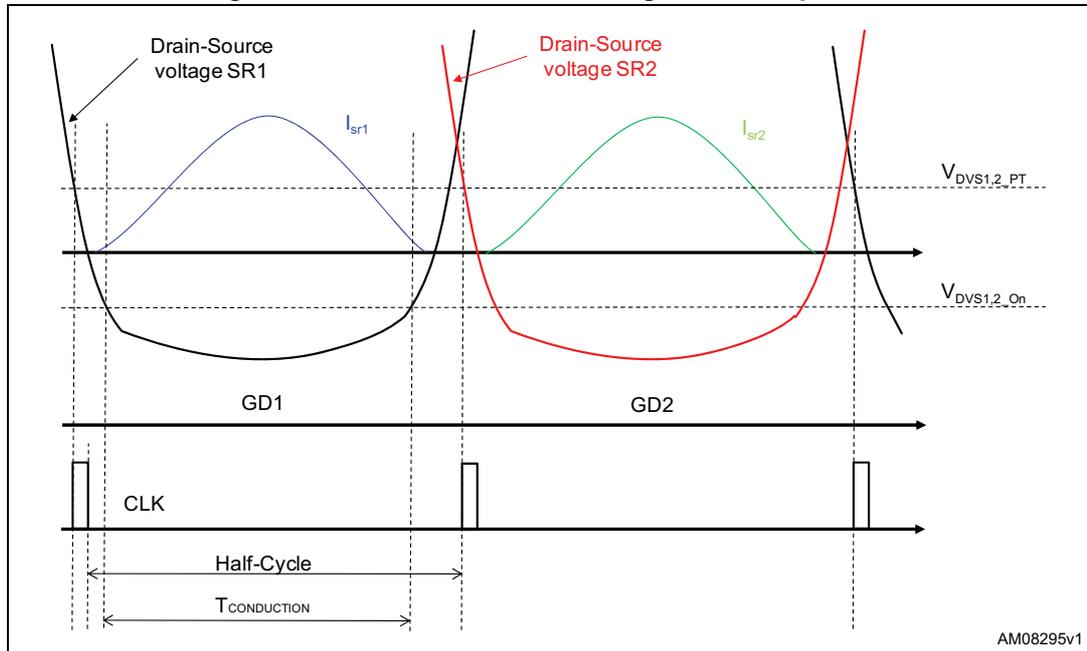
Also in this case the decision is made considering the measurement on eight consecutive switching cycles (considering both sections).

Furthermore, after each sleep mode entering/exiting transition, the timing is ignored for a certain number of cycles, to let the resulting transient in the output current fade out. The

number of ignored resonant converter switching cycles is 128 after entering sleep mode and 256 after exiting sleep mode. If by the end of the ignored cycles the condition to enter or exit the sleep mode is already met for the required number of cycles, the state will be changed immediately; otherwise the controller (after the ignored cycles) will wait until that condition is satisfied.

Figure 11 shows some examples of operation mode transition.

Figure 11. Operation mode transitions
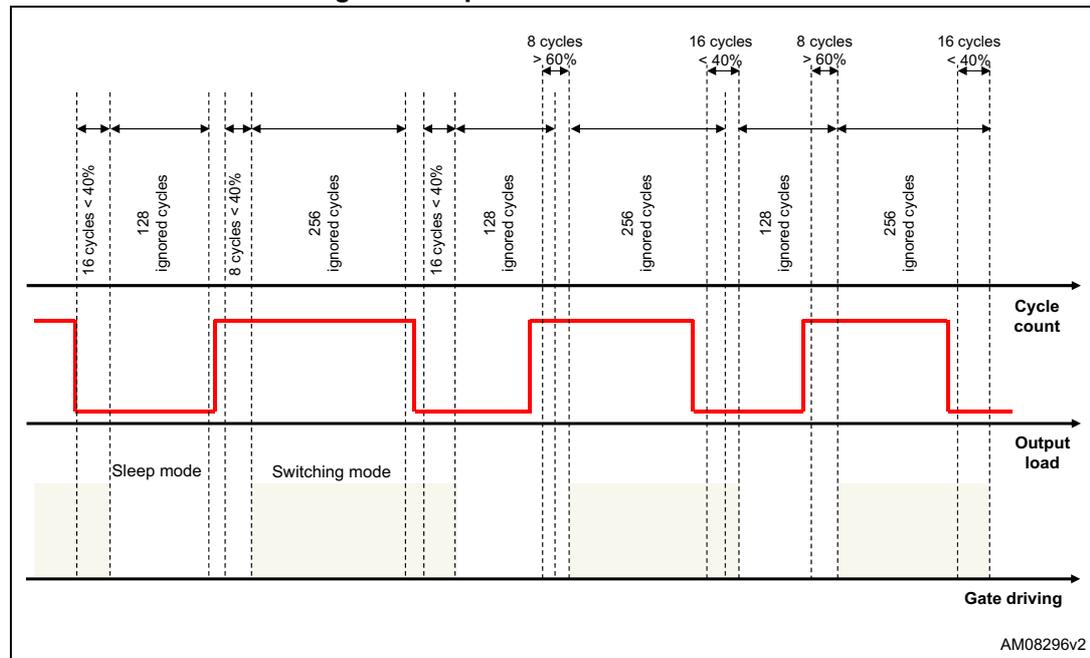
1.5 Enable pin

The EN pin can be used to remotely enable or disable power MOSFET driving. A voltage above 1.8 V enables the IC outputs which are otherwise inhibited.

By connecting the EN pin to Vcc through a resistor divider, the minimum Vcc voltage, at which the IC starts driving power MOSFETs, can be precisely set. If the SR power MOSFETs are logic level, the IC can start driving as soon as Vcc reaches the turn-on threshold (4.5 V), but if the SR power MOSFETs are standard level, it is better to keep the IC inhibited until the Vcc achieves the voltage necessary to properly drive the power MOSFETs (i.e. 10 V).

The EN pin has an additional function which allows setting the SR power MOSFETs turn-off threshold. It is set before the IC starts operating, when Vcc ramps up from 0 V to 4.5 V (VccOn). During this time window, if the voltage on the pin EN is below 0.36 V (typ.), the turn-off threshold is set to -25 mV, if it is above VEN-Th, the threshold is set to -12.5 mV. This function gives the possibility to change the turn-off threshold according to the SR power MOSFET $R_{DS(on)}$ and to the converter operation. Details of divider resistor calculation can be found in the SRK2000 datasheet.

2   Electrical diagram description

The board schematic is shown in *Figure 12*. Components were dimensioned supposing an implementation of the SR on a 12 V output converter and using the converter output as supply bus for the SRK2000. If the board is used with a different supply voltage, some components should be modified accordingly.

The C502 is a bypass capacitor mounted between Vcc and the SGND pin, as close as possible to the IC pin, in order to obtain a clean supply voltage for the internal circuitry. The C503 is another bypass capacitor from Vcc to PGND working as an energy buffer for the pulsed gate-drive currents. The R503, together with the C502 and C503, forms an RC filter and smoothes eventual disturbances from the 12 V supply. The R504 and R505 polarize the EN pin setting the Vcc enable voltage to 10 V (see *1* in *Section 8: References on page 25*). They are dimensioned to set the SR power MOSFET turn-off to -12.5 mV. The EN pin is externally accessible through the board connector pins #6 and #8 and can be used to force the IC disable.

The R506 and R507 connect the power MOSFET drains to DVS1,2 pins and set the turn-on threshold as previously described.

The D503 and D505 bypass the R506 and R507 before the power MOSFET turn-on. In this case they are not mounted because the R506 and R507 value is quite low and turn-on delay is negligible.

The C504 and C505 are intended to introduce an additional delay between the signals on the power MOSFET drain and on the sensing pin itself. In this case they are not mounted because they are not strictly necessary but their contribution is analyzed in *Section 3*.

The R501A, D501A, Q501A, R502A, D502A, and Q502A are optional and they are present only in case paralleled power MOSFETs are used (EVLSRK2000-S-40).

Figure 12. Electrical diagram

3 Sensing optimization by waveform check

The board has been tested on a 150 W 12 V LLC converter (see *2* in *Section 8: References on page 25*). The following assertions refer to the EVLSRK2000-L-40 but similar considerations can be made for all the configurations of the EVLSRK2000-x-xx.

Note that current and voltage probes can affect the IC sensing leading to malfunctioning. Signal probing must be accomplished carefully and with minimal modification with respect to the original circuit.

Figure 13 and *14* show key signals of the SRK2000: each SR power MOSFET is switched on and off according to its drain-source voltage which, during conduction time, is the voltage image of the current flowing through the power MOSFET. The measurement resolution is not sufficient to appreciate the turn-off threshold voltage on power MOSFET drain but the voltage step changes, corresponding to the power MOSFET turn-on and turn-off, can be noted.

Figure 13. Full load operation	Figure 14. Full load operation - detail
CH1: SR FET drain CH2: SR FET gate CH3: SR FET current CH4: primary current	CH1: SR FET drain CH2: SR FET gate CH3: SR FET current CH4: primary current
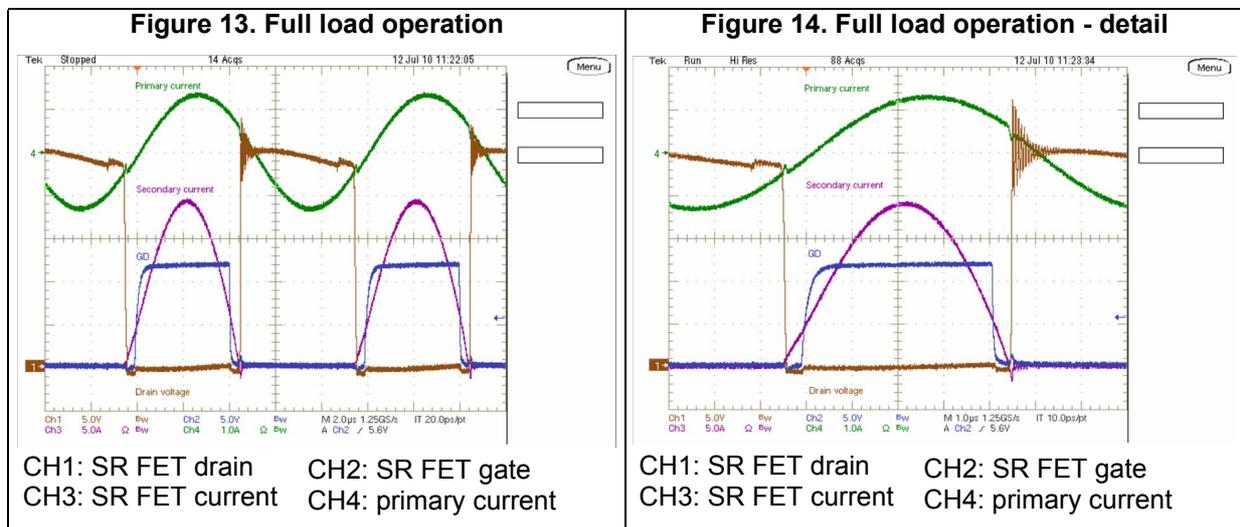
3.1 Power MOSFET turn-off compensation

Considering the SR power MOSFET $R_{DS(on)}$ and the SRK2000 turn-off threshold, turn-off current can be approximately calculated as follows:

Equation 3

$$I_{OFF} = \frac{V_{DVS1,2OFF}}{R_{DS(on)}}$$

Actually, this calculation neglects many other factors like the IC driver propagation delay and the $R_{DS(on)}$ deviation due to operative temperature. Furthermore, as previously discussed, turn-off timing is heavily influenced by parasitic elements.

Because it is quite difficult to accurately estimate all these parameters, it is better to confront this issue from a practical point of view. As seen in *Figure 14*, the power MOSFET turns off when significant current is still flowing through it, which is diverted to the MOSFET body diode. It can be worth delaying the turn-off to increase efficiency. This can be easily

performed by adding a capacitor on each DVS pin, as indicated before in *Section 1.2 on page 7*. In *Figure 15* and *16*, IC behavior corresponding to different values of RC sensing circuit is shown.

Figure 15. SR MOSFET turn-off	Figure 16. SR MOSFET turn-off - detail

CH3: SR FET current   CH2: SR FET gate
CH4: primary current

CH3: SR FET current   CH2: SR FET gate
CH4: primary current
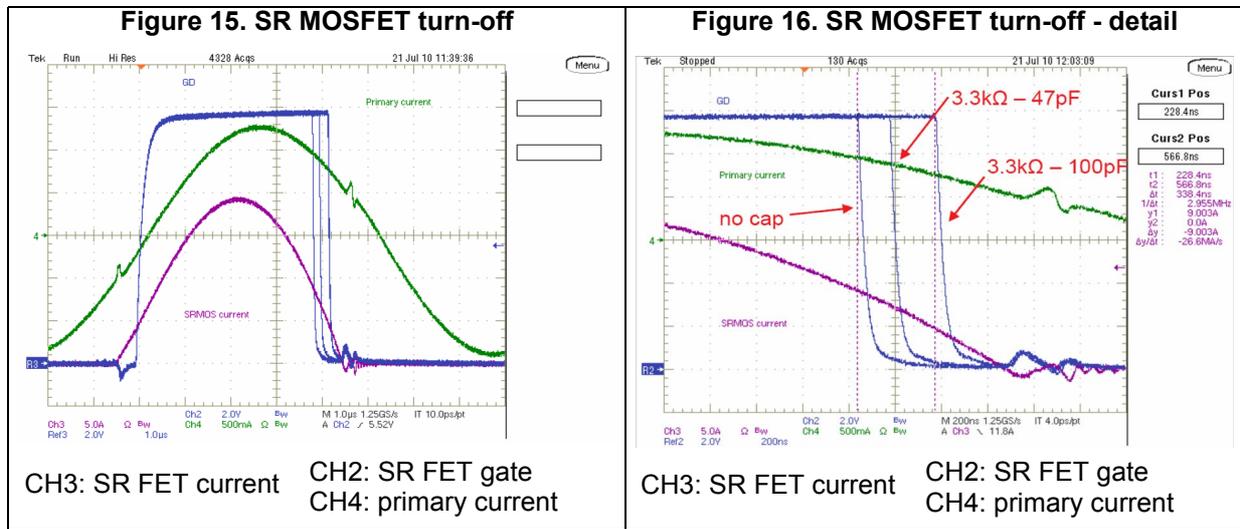
It is important to point out that this fine tuning must be done at the maximum operating temperature because the $R_{DS(on)}$ increases significantly with temperature, moving the corresponding turn-off forward. An over-delayed turn-off must be avoided because, if the MOSFET is turned off after the drain current goes to zero, the resulting current reversal produces a series of possible adverse effects, ranging from an efficiency drop to the converter's catastrophic failure. A good rule of thumb is to keep at least a 50/100 nS margin before the zero current point, because it has negligible impact on efficiency and it is a safe margin in the case of abrupt load changes or other disturbances.

Figure 17 shows the case of operation above resonance. Note how the current flowing through the MOSFET exhibits a very steep edge while decreasing down to zero. In this case, no external capacitors are implemented because a further delay could cause a current reversal.

Figure 17. Operation above resonance frequency

CH3: SR FET current   CH2: SR FET gate
CH4: primary current
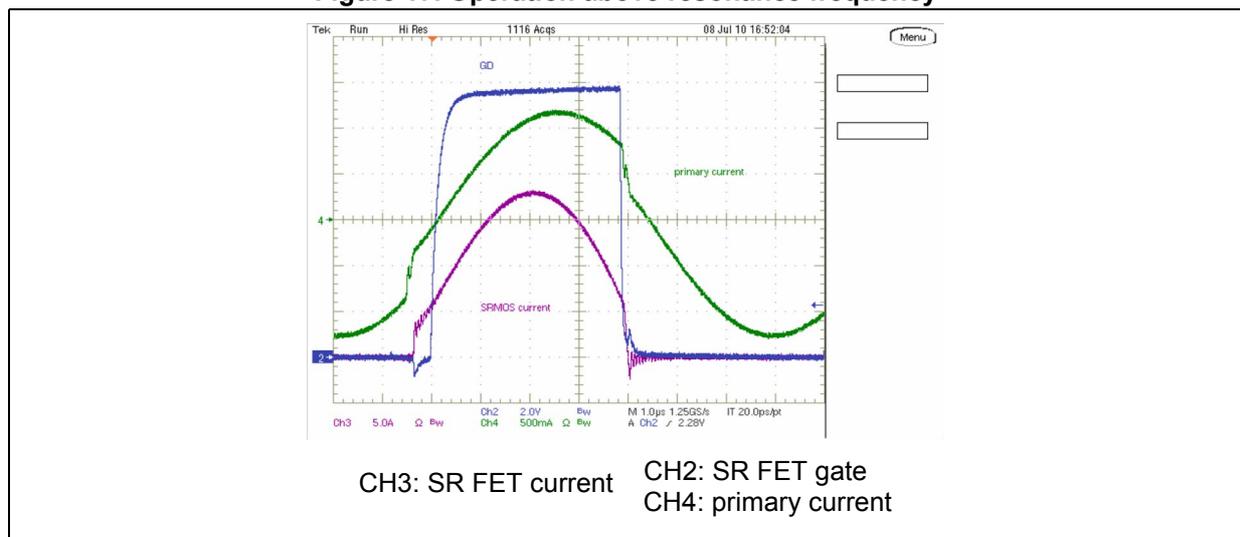
3.2 MOSFET turn-on delay compensation

As discussed in *Section 1.2 on page 7*, the RC circuit added to fine tune the turn-off timing has the side effect of also delaying the turn-on. It was stated that to avoid this effect, a bypass diode plus a series resistor can be mounted in parallel to the sensing resistor. *Figure 18* and *19* below show the turn-on delay improvement using this solution.

Figure 18. SR MOSFET turn-on

CH3: SR FET current
CH2: SR FET gate
CH4: primary current

Figure 19. SR MOSFET turn-on - detail

CH3: SR FET current
CH2: SR FET gate
CH4: primary current
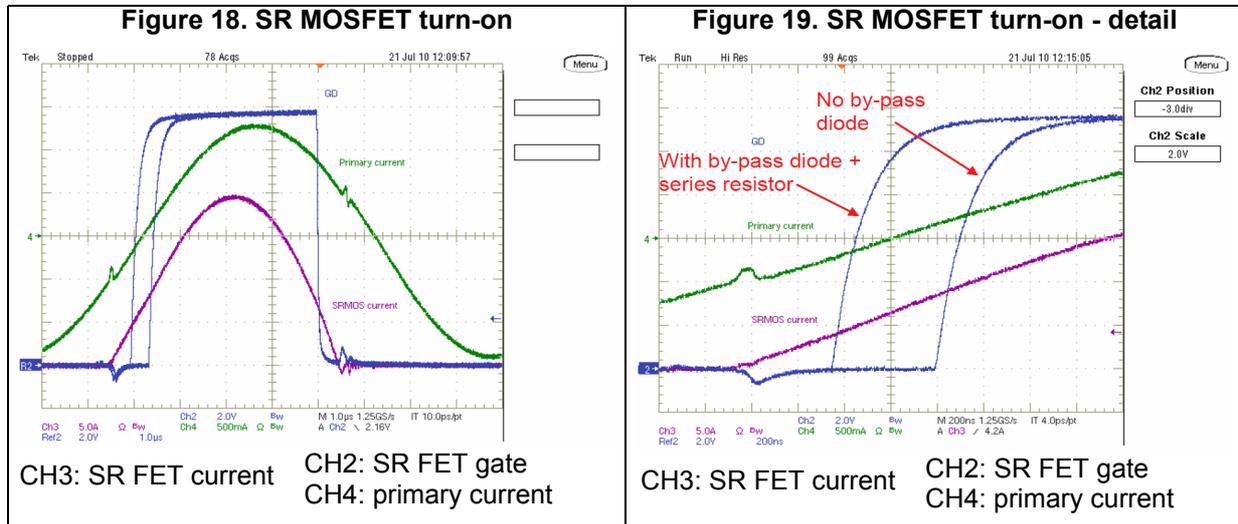
3.3 Sub-harmonic oscillation

Figure 20 shows the behavior described in *Section 1.3 on page 9*. At the light load the turn-off threshold (in terms of current) is quite close to the peak current value. This causes a duty cycle oscillation around the current peak. This duty oscillation causes the secondary current to fluctuate, therefore amplifying the phenomenon. The 50% blanking time implemented in the SRK2000 limits the oscillation width, which would otherwise further increase causing output instability.

Figure 20. Duty cycle oscillation
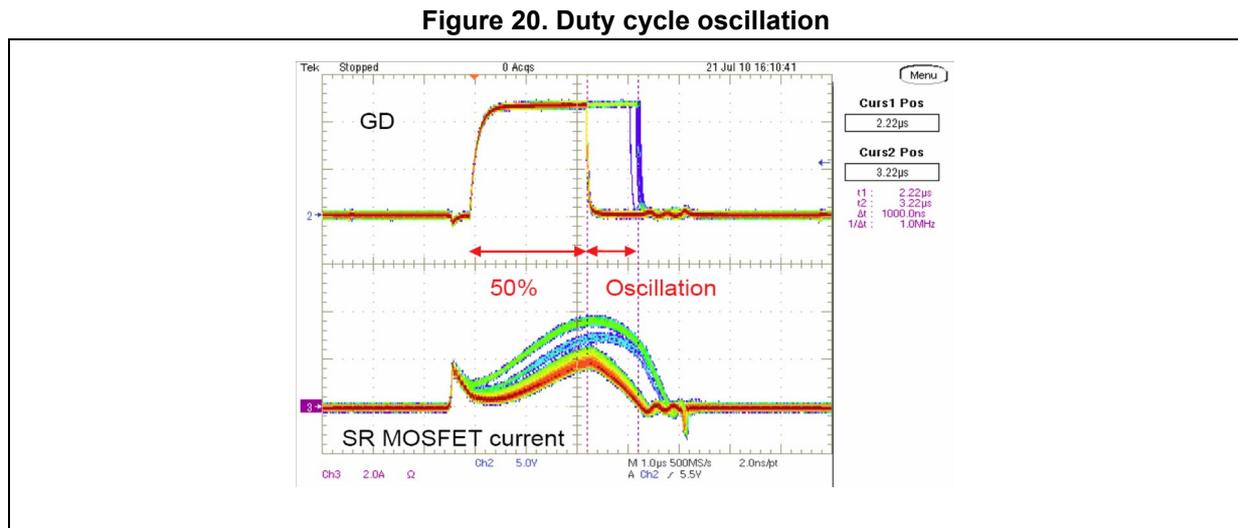
4 How to implement the board in the converter

The demonstration board is intended to implement synchronous rectification in an LLC resonant converter with center-tap secondary winding. If the converter implements diode rectification, rectifiers must be removed and the board must be connected as indicated in *Figure 21*. Connect the transformer center-tap to the converter output. Tie the other two secondary outputs respectively to pins 1, 2, 3 and to pins 11, 12, 13; bond pins 4, 5, 9, and 10 to secondary ground. The central pin 7 is for supplying the SRK2000 and can be connected to the converter output. Pins 6 and 8 are connected to the EN pin and can be used to inhibit the IC remotely. The board connector pinout is perfectly symmetrical and, if necessary for mechanical issues, the board tie to the converter can be rotated by 180°.

Figure 21. How to implement the board on an existing converter
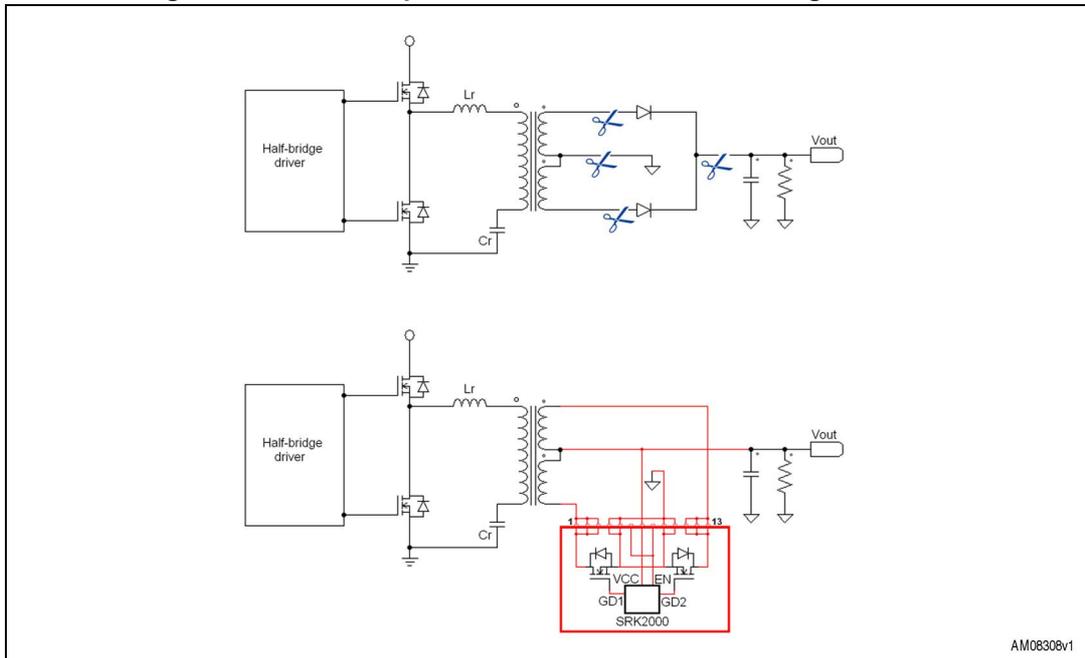
5 Power losses and thermal design

The SR dramatically reduces output rectification power losses enabling the design of more efficient power supplies and, even more significant, with a considerable reduction of converter secondary side size.

To get a better idea of the improvement obtained by implementing the SR with the SRK2000, the power loss calculation in a 12 V - 150 W application (see *2* in *Section 8: References on page 25*) is illustrated below.

5.1 Power losses calculation

The average output current of a 12 V - 150 W power supply at the nominal load is:

Equation 4

$$I_0 = \frac{P_0}{V_0} = 12.50\,A$$

The average current flowing through each output rectifier is:

Equation 5

$$I_{avg} = \frac{I_0}{2} = 6.25\,A$$

and the RMS current is approximately:

Equation 6

$$I_{RMS} = \frac{\pi}{4}I_0 = 9.82\,A$$

To evaluate power losses, a suitable diode and MOSFET part numbers were selected.

In the case of diode rectification the STPS20L45C was selected (see *3* in *Section 8*). The power losses associated to each rectifier can be calculated using the formula indicated in the STPS20L45C datasheet:

Equation 7

$$P_{Diode} = 0.28 \cdot I_{avg} + 0.022 \cdot I_{RMS^2} = 3.87\,W$$

In the case of SR, the selected MOSFET is the STL140N4LLF5, which is actually mounted on theEVLSRK2000-L-40.

Capacitive losses associated to the MOSFET turn-on are negligible because each MOSFET is turned on after its body diode starts conducting. Also losses at turn-off are of minor concern because, after the MOSFET is turned off, the current goes on flowing through the diode.

Supposing the MOSFET turn-on and turn-off timing are optimized as described in *Section 3 on page 14*, losses associated to the current flowing through the body diodes can be neglected too. Most SR MOSFET losses can be summarized into conduction losses:

Equation 8

$$P_{MOS} = R_{DS(on)} \cdot I_{RMS^2} = 265 \text{ mW}$$

In addition, the power consumption of the SRK2000 must be taken into account: for a rough estimate, consider the IC quiescent current indicated in the SRK2000 datasheet (I_q) and the energy required for SR MOSFET driving (E_{ZVS}).

Equation 9

$$E_{ZVS} = \frac{1}{2(V_{GS} - V_M)} [(2V_{GS^2} + V_{M^2})(Q_g - Q_{gd}) - V_{GS}(2V_{GS} + V_M)Q_{gs}] = 765 \text{ n}$$

Where V_{GS} is the gate driver high level, V_M is the MOSFET turn-on threshold, and Q_g, Q_{gd}, and Q_{gs} are the charges associated to MOSFET gate driving and are specified in the SRK2000 datasheet.

A detailed explanation on the calculating energy required to drive MOSFETs in ZVS is reported in *Appendix A* of the AN2644 application note (see *5* in *Section 8: References on page 25*).

Equation 10

$$P_{SRK2000} = (I_q \cdot Vcc) + (2 \cdot E_{ZVS} \cdot f_{sw}) = 159 \text{ mW}$$

Finally, at the full load, the total power saving obtained by implementing SR with respect to diode rectification is calculated as follows:

Equation 11

$$\Delta P = 2 \cdot P_{Diode} - (2 \cdot P_{MOS} + P_{SRK2000}) = 7.05 \text{ W}$$

A power saving of 7.05 W corresponds to a 4.7% efficiency boost on a 150 W converter.

5.2 Thermal design consideration

The improvement in efficiency obtained by implementing SR allows dramatic squeezing of the converter secondary side. This becomes evident when comparing the heatsink required in case of diode rectification with that required if SR is employed.

Considering the diode rectification, the maximum junction temperature of the selected diode is 150 °C. Consider 125 °C as the maximum tolerable temperature keeping some margin to improve system reliability. Supposing an ambient temperature of 60 °C, the maximum allowed thermal rise is 65 °C. Considering the power dissipation per diode calculated in *Equation 7*, the maximum junction to ambient thermal resistance allowed is:

Equation 12

$$R_{th(j-amb)} = \frac{65°C}{P_{Diode}} = 17°C/W$$

It is possible to assume that the thermal resistance between the TO-220FP case and the heatsink is $R_{th(c-hs)} = 1$ °C/W. As a consequence, each diode rectifier needs a heatsink with a thermal resistance of:

Equation 13

$$R_{th(hs-amb)} = R_{th(j-amb)} - R_{th(j-c)} - R_{th(c-hs)} = 15°C/W$$

Considering now the case with SR: again the thermal rise is 65 °C. Based on the power dissipation per MOSFET calculated in *Equation 8*, the maximum junction to ambient thermal resistance allowed is:

Equation 14

$$R_{th(j-amb)} = \frac{65°C}{P_{MOS}} = 245°C/W$$

That means that a heatsink is not required, just some copper area is needed, calculated according to the SRK2000 datasheet indication.

The same is true for the SRK2000:

Equation 15

$$R_{th(j-amb)} = \frac{65°C}{P_{SRK2000}} = 409°C/W$$

This is higher than the controller junction to ambient thermal resistance (150 °C/W).

6   Layout considerations

The IC is designed with two ground pins, SGND and PGND. The SGND is used as the ground reference for all the internal high precision analog blocks. The PGND, on the other hand, is the ground reference for all the digital blocks, as well as the current return for the gate drivers.

Listed below are the main recommendations that should be taken into account when designing the PCB:

- Close the output current loop as short as possible by connecting the SR MOSFET drains as close as possible to the transformer termination.

- Route the connection between the two MOSFET drains and transformer terminals symmetrically to each other.

- Connect the MOSFET sources close to the output capacitor ground terminals.

- Route the trace that connects MOSFET sources to the SRK2000 PGND pin as short as possible and separately from the load current return path.

- Keep the source terminals of both SR MOSFETs as close as possible to one another.

- Design the PCB as geometrically symmetrical as possible to help make the circuit operation as electrically symmetrical as possible.

- The SGND pin must be directly connected to the PGND pin using a path as short as possible (under the device body).

- Connect the drain voltage sensing resistor as physically close to the drain terminals as possible: any stray inductance involved by the load current that is in the drain-to-source voltage sensing circuit may significantly alter the current reading, leading to a premature turn-off of the SR MOSFET.

- Use bypass ceramic capacitors between Vcc and both SGND and PGND. They should be located as close to the IC pins as possible. Sometimes, a series resistor (in the ten) between the converter's output voltage and the Vcc pin, forming an RC filter along with the bypass capacitor, is useful to get a cleaner Vcc voltage.

Figure 22. Board layout
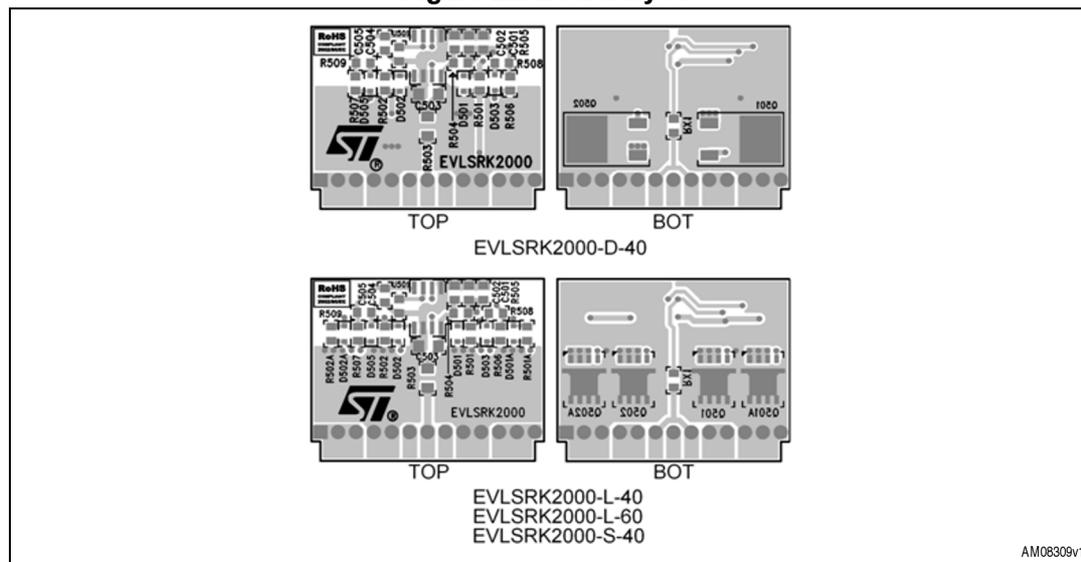
7 Bill of materials

Table 2. EVLSRK2000-L-40 bill of materials

Ref	Value/PN	Description	Supplier	Case
C501	4.7 nF	50 V CERCAP X7R - general purpose	BCcomponents	0805
C502	100 nF	50 V CERCAP X7R - general purpose	BCcomponents	0805
C503	1 µF	50 V CERCAP X7R - general purpose	BCcomponents	0805
D501	BAS316	Fast switching signal diode	VISHAY	SOD-323
D502	BAS316	Fast switching signal diode	VISHAY	SOD-323
JP501	HEADER 13	Strip connector	-	-
Q501	STL140N4LLF5	N-channel power MOSFET	STMicroelectronics	PowerFLAT™
Q502	STL140N4LLF5	N-channel power MOSFET	STMicroelectronics	PowerFLAT™
R501	10 Ω	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	0805
R502	10 Ω	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	0805
R503	10 Ω	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	1206
R504	150 kΩ	SMD std. film. res .- 1/8 W - 1% - 100 ppm/°C	BCcomponents	0805
R505	33 kΩ	SMD std. film. res. - 1/8 W - 1% - 100 ppm/°C	BCcomponents	0805
R506	330 Ω	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	0805
R507	330 Ω	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	0805
RX1	0	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	0805
U501	SRK2000D	SR driver for LLC resonant converter	STMicroelectronics	SO-8

Table 3. EVLSRK2000-L-60 bill of materials

Ref	Value/PN	Description	Supplier	Case
C501	4.7 nF	50 V CERCAP X7R - general purpose	BCcomponents	0805
C502	100 nF	50 V CERCAP X7R - general purpose	BCcomponents	0805
C503	1 µF	50 V CERCAP X7R - general purpose	BCcomponents	0805
D501	BAS316	Fast switching signal diode	VISHAY	SOD-323
D502	BAS316	Fast switching signal diode	VISHAY	SOD-323
JP501	HEADER 13	Strip connector	-	-
Q501	STL85N6F3	N-channel power MOSFET	STMicroelectronics	PowerFLAT™
Q502	STL85N6F3	N-channel power MOSFET	STMicroelectronics	PowerFLAT™
R501	10 Ω	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	0805
R502	10 Ω	SMD std. film. res. - 1/8W - 5% - 200 ppm/°C	BCcomponents	0805
R503	10 Ω	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	1206
R504	150 kΩ	SMD std. film. res. - 1/8 W - 1% - 100 ppm/°C	BCcomponents	0805

Table 3. EVLSRK2000-L-60 bill of materials (continued)

Ref	Value/PN	Description	Supplier	Case
R505	33 kΩ	SMD std. film. res. - 1/8 W - 1% - 100 ppm/°C	BCcomponents	0805
R506	330 Ω	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	0805
R507	330 μ	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	0805
RX1	0	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	0805
U501	SRK2000D	SR driver for LLC resonant converter	STMicroelectronics	SO-8

Table 4. EVLSRK2000-S-40 bill of materials

Ref	Value/PN	Description	Supplier	Case
C501	4.7 nF	50 V CERCAP X7R - general purpose	BCcomponents	0805
C502	100 nF	50 V CERCAP X7R - general purpose	BCcomponents	0805
C503	1 μF	50 V CERCAP X7R - general purpose	BCcomponents	0805
D501	BAS316	Fast switching signal diode	VISHAY	SOD-323
D501A	BAS316	Fast switching signal diode	VISHAY	SOD-323
D502	BAS316	Fast switching signal diode	VISHAY	SOD-323
D502A	BAS316	Fast switching signal diode	VISHAY	SOD-323
JP501	HEADER 13	Strip connector	-	-
Q501	STS15N4LLF3	N-channel power MOSFET	STMicroelectronics	SO-8
Q501A	STS15N4LLF3	N-channel power MOSFET	STMicroelectronics	SO-8
Q502	STS15N4LLF3	N-channel power MOSFET	STMicroelectronics	SO-8
Q502A	STS15N4LLF3	N-channel power MOSFET	STMicroelectronics	SO-8
R501	10 Ω	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	0805
R501A	10 Ω	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	0805
R502	10 Ω	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	0805
R502A	10 Ω	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	0805
R503	10 Ω	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	1206
R504	150 kΩ	SMD std. film. res. - 1/8 W - 1% - 100 ppm/°C	BCcomponents	0805
R505	33 kΩ	SMD std. film. res. - 1/8 W - 1% - 100 ppm/°C	BCcomponents	0805
R506	330 Ω	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	0805
R507	330 Ω	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	0805
RX1	0	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	0805
U501	SRK2000D	SR driver for LLC resonant converter	STMicroelectronics	SO-8

Table 5. EVLSRK2000-D-40 bill of materials

Ref	Value/PN	Description	Supplier	Case
C501	4.7 nF	50 V CERCAP X7R - general purpose	BCcomponents	0805
C502	100 nF	50 V CERCAP X7R - general purpose	BCcomponents	0805
C503	1 µF	50 V CERCAP X7R - general purpose	BCcomponents	0805
D501	BAS316	Fast switching signal diode	VISHAY	SOD-323
D502	BAS316	Fast switching signal diode	VISHAY	SOD-323
JP501	HEADER 13	Strip connector	-	-
Q501	STD95N4F3	N-channel power MOSFET	STMicroelectronics	D-PAK
Q502	STD95N4F3	N-channel power MOSFET	STMicroelectronics	D-PAK
R501	10 Ω	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	0805
R502	10 Ω	SMD std. film. res.- 1/8 W - 5% - 200 ppm/°C	BCcomponents	0805
R503	10 Ω	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	1206
R504	150 kΩ	SMD std. film. res. - 1/8 W - 1% - 100 ppm/°C	BCcomponents	0805
R505	33 kΩ	SMD std. film. res. - 1/8 W - 1% - 100 ppm/°C	BCcomponents	0805
R506	330 Ω	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	0805
R507	330 Ω	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	0805
RX1	0	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	BCcomponents	0805
U501	SRK2000D	SR driver for LLC resonant converter	STMicroelectronics	SO-8

8 References

1. SRK2000 datasheet
2. AN3233 application note
3. STPS20L45C datasheet
4. STL140N4LLF5 datasheet
5. AN2644 application note

9 Revision history

Table 6. Document revision history

Date	Revision	Changes
20-Jan-2011	1	Initial release.
16-Sep-2011	2	Updated *Figure 12 on page 13*.
20-Mar-2017	3	Updated *Figure 3 on page 7* (replaced by new figure). Updated *Section 1.4 on page 10* (removed "of at least one"). Minor modifications throughout document.
05-May-2017	4	Updated *Section 1.4 on page 10* (updated text, replaced *Figure 11 on page 12* by new figure). Minor modifications throughout document.

IMPORTANT NOTICE – PLEASE READ CAREFULLY