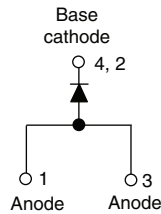


## Schottky Rectifier, 10 A


**D-PAK (TO-252AA)**


### FEATURES

- Popular D-PAK outline
- Small foot print, surface mountable
- Low forward voltage drop
- High frequency operation
- Guard ring for enhanced ruggedness and long term reliability
- Compliant to RoHS Directive 2002/95/EC
- Meets MSL level 1, per J-STD-020, LF maximum peak of 260 °C


**RoHS  
COMPLIANT**

### PRODUCT SUMMARY

Package	D-PAK (TO-252AA)
$I_{F(AV)}$	10 A
$V_R$	45 V
$V_F$ at $I_F$	0.53 V
$I_{RM}$	15 mA at 125 °C
$T_J$ max.	175 °C
Diode variation	Single die
$E_{AS}$	20 mJ

### DESCRIPTION

The VS-10WQ045FN surface mount Schottky rectifier has been designed for applications requiring low forward drop and small foot prints on PC board. Typical applications are in disk drives, switching power supplies, converters, freewheeling diodes, battery charging, and reverse battery protection.

### MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{F(AV)}$	Rectangular waveform	10	A
$V_{RRM}$		45	V
$I_{FSM}$	$t_p = 5 \mu s$ sine	400	A
$V_F$	10 Apk, $T_J = 125 \text{ °C}$	0.53	V
$T_J$	Range	- 40 to 175	°C

### VOLTAGE RATINGS

PARAMETER	SYMBOL	VS-10WQ045FNPbF	UNITS
Maximum DC reverse voltage	$V_R$	45	V
Maximum working peak reverse voltage	$V_{RWM}$		

### ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum average forward current See fig. 5	$I_{F(AV)}$	50 % duty cycle at $T_C = 157 \text{ °C}$ , rectangular waveform	10	A
Maximum peak one cycle non-repetitive surge current See fig. 7	$I_{FSM}$	5 $\mu s$ sine or 3 $\mu s$ rect. pulse	400	A
		10 ms sine or 6 ms rect. pulse		
Non-repetitive avalanche energy	$E_{AS}$	$T_J = 25 \text{ °C}$ , $I_{AS} = 3 \text{ A}$ , $L = 4.4 \text{ mH}$	20	mJ
Repetitive avalanche current	$I_{AR}$	Current decaying linearly to zero in 1 $\mu s$ Frequency limited by $T_J$ maximum $V_A = 1.5 \times V_R$ typical	3.0	A

ELECTRICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum forward voltage drop See fig. 1	$V_{FM}^{(1)}$	10 A	$T_J = 25\text{ }^\circ\text{C}$	0.63	V
		20 A		0.80	
		10 A	$T_J = 125\text{ }^\circ\text{C}$	0.53	
		20 A		0.71	
Maximum reverse leakage current See fig. 2	$I_{RM}^{(1)}$	$T_J = 25\text{ }^\circ\text{C}$	$V_R = \text{Rated } V_R$	1	mA
		$T_J = 125\text{ }^\circ\text{C}$		15	
Threshold voltage	$V_{F(TO)}$	$T_J = T_J \text{ maximum}$		0.255	V
Forward slope resistance	$r_t$			22	m $\Omega$
Typical junction capacitance	$C_T$	$V_R = 5 V_{DC}$ (test signal range 100 kHz to 1 MHz), 25 $^\circ\text{C}$		760	pF
Typical series inductance	$L_S$	Measured lead to lead 5 mm from package body		5.0	nH

**Note**

(1) Pulse width < 300  $\mu\text{s}$ , duty cycle < 2 %

THERMAL - MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum junction and storage temperature range	$T_J^{(1)}, T_{Stg}$			- 40 to 175	$^\circ\text{C}$
Maximum thermal resistance, junction to case	$R_{thJC}$	DC operation See fig. 4		2.0	$^\circ\text{C}/\text{W}$
Maximum thermal resistance, junction to ambient	$R_{thJA}$			50	
Approximate weight				0.3	g
				0.01	oz.
Marking device		Case style D-PAK (similar to TO-252AA)		10WQ045FN	

**Note**

(1)  $\frac{dP_{tot}}{dT_J} < \frac{1}{R_{thJA}}$  thermal runaway condition for a diode on its own heatsink

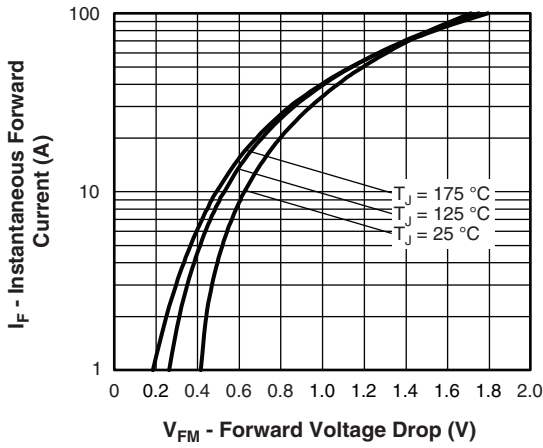


Fig. 1 - Maximum Forward Voltage Drop Characteristics

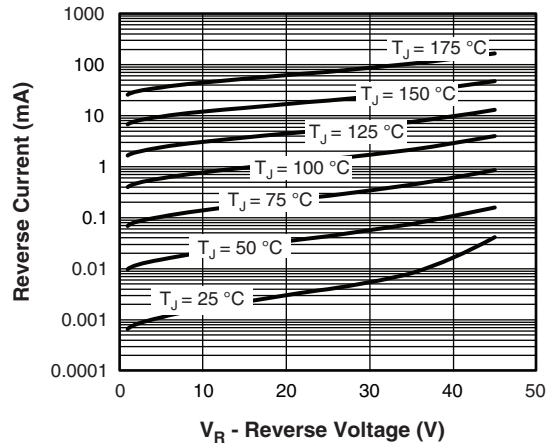


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

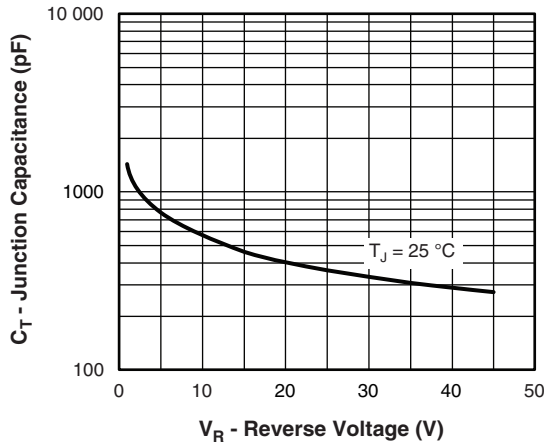


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

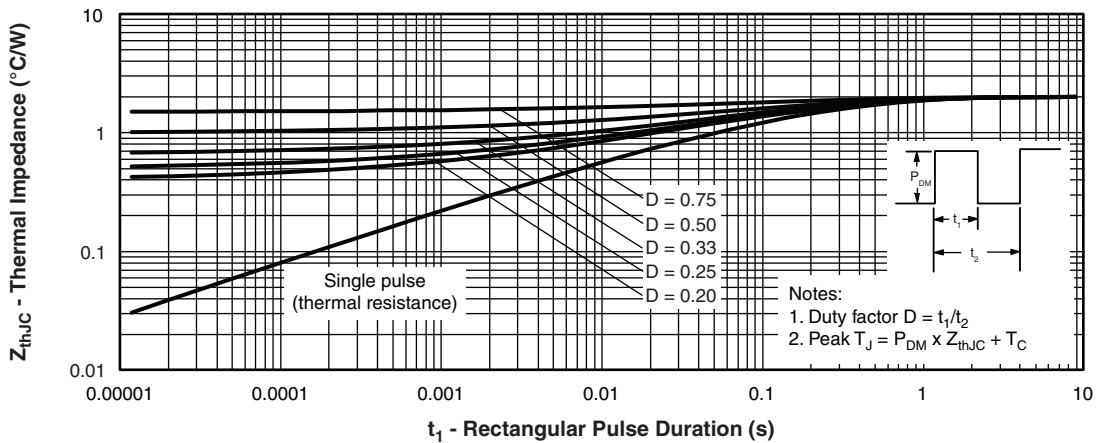


Fig. 4 - Maximum Thermal Impedance  $Z_{thJC}$  Characteristics

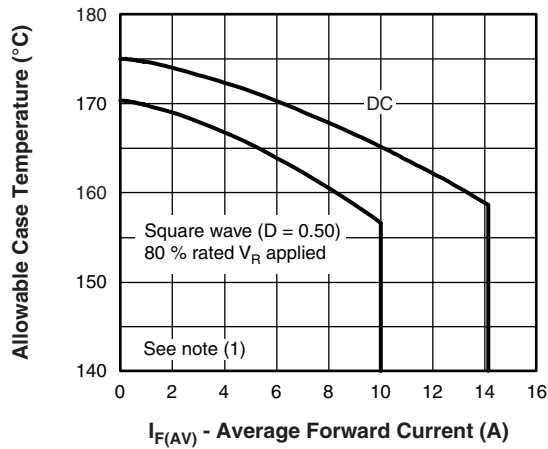


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current

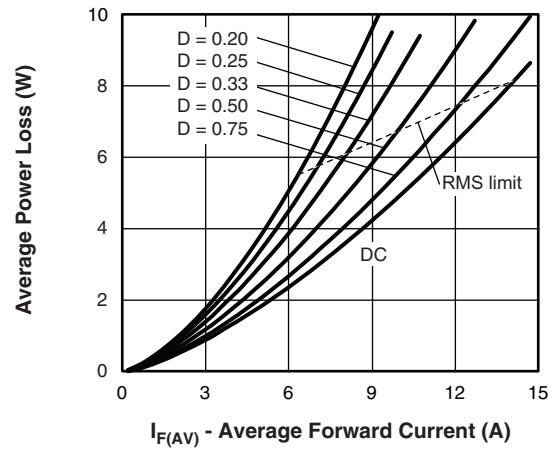


Fig. 6 - Forward Power Loss Characteristics

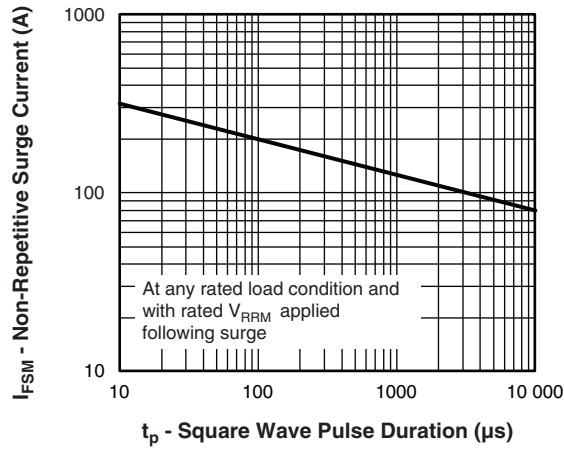


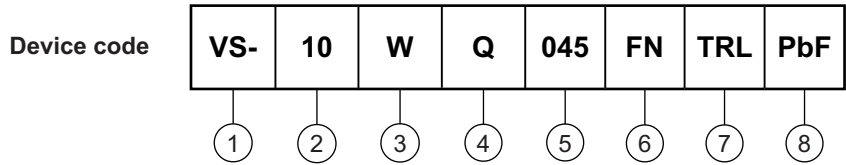
Fig. 7 - Maximum Non-Repetitive Surge Current

**Note**

- (1) Formula used:  $T_C = T_J - (P_d + P_{d_{REV}}) \times R_{thJC}$ ;  
 $P_d$  = Forward power loss =  $I_{F(AV)} \times V_{FM}$  at  $(I_{F(AV)}/D)$  (see fig. 6);  
 $P_{d_{REV}}$  = Inverse power loss =  $V_{R1} \times I_R (1 - D)$ ;  $I_R$  at  $V_{R1} = 80\%$  rated  $V_R$



**ORDERING INFORMATION TABLE**

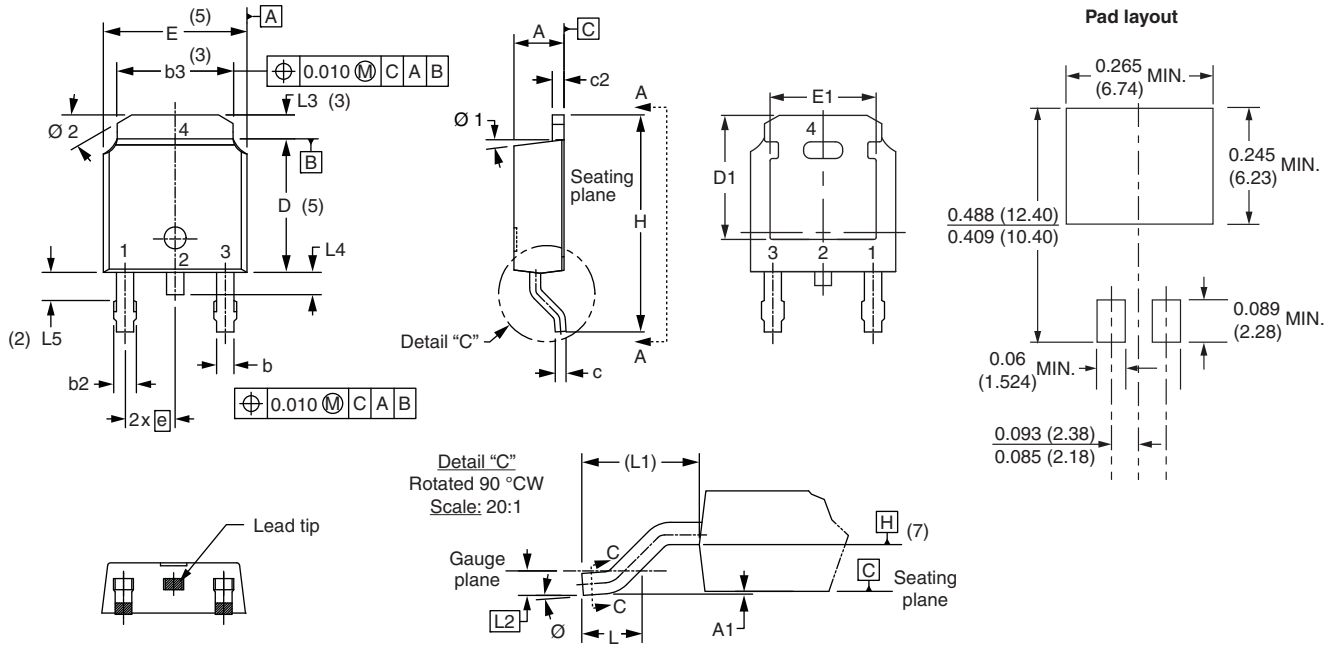


- 1** - Vishay Semiconductors product
- 2** - Current rating (10 A)
- 3** - Package identifier:  
W = D-PAK
- 4** - Schottky "Q" series
- 5** - Voltage rating (045 = 45 V)
- 6** - FN = TO-252AA (D-PAK)
- 7** -
  - None = Tube (50 pieces)
  - TR = Tape and reel
  - TRL = Tape and reel (left oriented)
  - TRR = Tape and reel (right oriented)
- 8** - PbF = Lead (Pb)-free

LINKS TO RELATED DOCUMENTS	
Dimensions	<a href="http://www.vishay.com/doc?95016">www.vishay.com/doc?95016</a>
Part marking information	<a href="http://www.vishay.com/doc?95059">www.vishay.com/doc?95059</a>
Packaging information	<a href="http://www.vishay.com/doc?95033">www.vishay.com/doc?95033</a>

## D-PAK (TO-252AA)

**DIMENSIONS** in millimeters and inches



SYMBOL	MILLIMETERS		INCHES		NOTES	SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.			MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	0.094		e	2.29 BSC		0.090 BSC		
A1	-	0.13	-	0.005		H	9.40	10.41	0.370	0.410	
b	0.64	0.89	0.025	0.035		L	1.40	1.78	0.055	0.070	
b2	0.76	1.14	0.030	0.045		L1	2.74 BSC		0.108 REF.		
b3	4.95	5.46	0.195	0.215	3	L2	0.51 BSC		0.020 BSC		
c	0.46	0.61	0.018	0.024		L3	0.89	1.27	0.035	0.050	3
c2	0.46	0.89	0.018	0.035		L4	-	1.02	-	0.040	
D	5.97	6.22	0.235	0.245	5	L5	1.14	1.52	0.045	0.060	2
D1	5.21	-	0.205	-	3	Ø	0°	10°	0°	10°	
E	6.35	6.73	0.250	0.265	5	Ø1	0°	15°	0°	15°	
E1	4.32	-	0.170	-	3	Ø2	25°	35°	25°	35°	

**Notes**

- (1) Dimensioning and tolerancing as per ASME Y14.5M-1994
- (2) Lead dimension uncontrolled in L5
- (3) Dimension D1, E1, L3 and b3 establish a minimum mounting surface for thermal pad
- (4) Section C - C dimension apply to the flat section of the lead between 0.13 and 0.25 mm (0.005 and 0.10") from the lead tip
- (5) Dimension D, and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (6) Dimension b1 and c1 applied to base metal only
- (7) Datum A and B to be determined at datum plane H
- (8) Outline conforms to JEDEC outline TO-252AA



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