

N-Channel 80-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
80	0.013 at V _{GS} = 10 V	17.3	35 nC

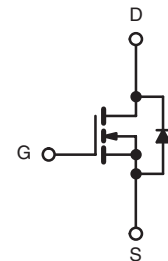
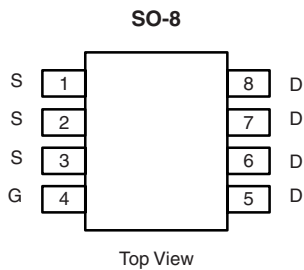
FEATURES

- Halogen-free
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested



APPLICATIONS

- Primary Side Switch
- Half Bridge
- Intermediate Bus Converter



Ordering Information: Si4110DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	80	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	17.3	A
		T _C = 70 °C	13.9	
		T _A = 25 °C	11.7 ^{b, c}	
		T _A = 70 °C	9.4 ^{b, c}	
Pulsed Drain Current	I _{DM}	60		
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	6.5	
		T _A = 25 °C	3 ^{b, c}	
Single Pulse Avalanche Current	I _{AS}	35		
Single Pulse Avalanche Energy	E _{AS}	61.3	mJ	
Maximum Power Dissipation	P _D	T _C = 25 °C	7.8	W
		T _C = 70 °C	5	
		T _A = 25 °C	3.6 ^{b, c}	
		T _A = 70 °C	2.3 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature)		260		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	29	35	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	13	16	

Notes:

- Based on T_C = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under Steady State conditions is 80 °C/W.



SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	80			V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		84		mV/ $^\circ\text{C}$	
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-9.8			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2		4	V	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$			1	μA	
		$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10		
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 10\text{ V}, V_{GS} = 10\text{ V}$	20			A	
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 11.7\text{ A}$		0.0108	0.0130	Ω	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 11.7\text{ A}$		23		S	
Dynamic^b							
Input Capacitance	C_{iss}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		2205		pF	
Output Capacitance	C_{oss}				260		
Reverse Transfer Capacitance	C_{rss}				78		
Total Gate Charge	Q_g	$V_{DS} = 40\text{ V}, V_{GS} = 10\text{ V}, I_D = 11.7\text{ A}$		35	53	nC	
Gate-Source Charge	Q_{gs}			12.5			
Gate-Drain Charge	Q_{gd}			8			
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.22	1.1	2.2	Ω	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 40\text{ V}, R_L = 4.3\text{ }\Omega$ $I_D \cong 9.4\text{ A}, V_{GEN} = 8\text{ V}, R_g = 1\text{ }\Omega$		18	27	ns	
Rise Time	t_r			10	18		
Turn-Off Delay Time	$t_{d(off)}$			22	33		
Fall Time	t_f			8	16		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 40\text{ V}, R_L = 4.3\text{ }\Omega$ $I_D \cong 9.4\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		15	23		
Rise Time	t_r			9	18		
Turn-Off Delay Time	$t_{d(off)}$			22	33		
Fall Time	t_f			7	14		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			6.5	A	
Pulse Diode Forward Current ^a	I_{SM}				60		
Body Diode Voltage	V_{SD}	$I_S = 9.4\text{ A}$		0.80	1.2	V	
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 9.4\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		45	68	ns	
Body Diode Reverse Recovery Charge	Q_{rr}				82	123	nC
Reverse Recovery Fall Time	t_a				34		ns
Reverse Recovery Rise Time	t_b				11		

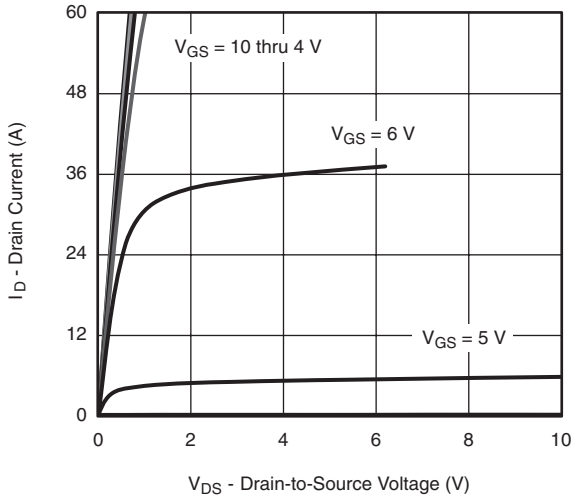
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing.

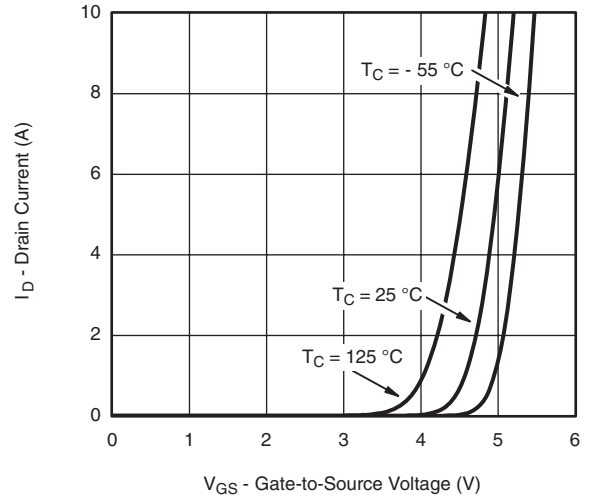
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



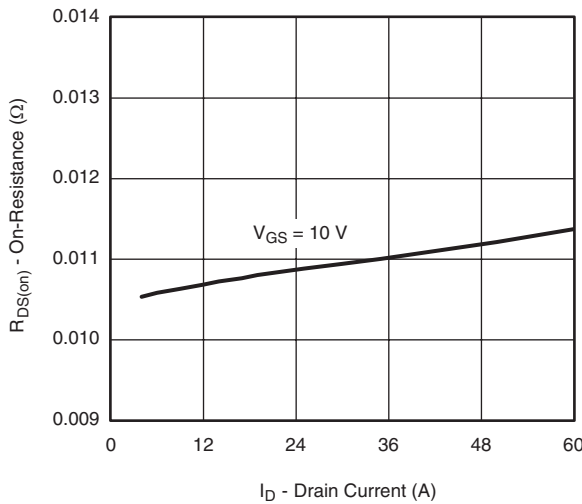
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



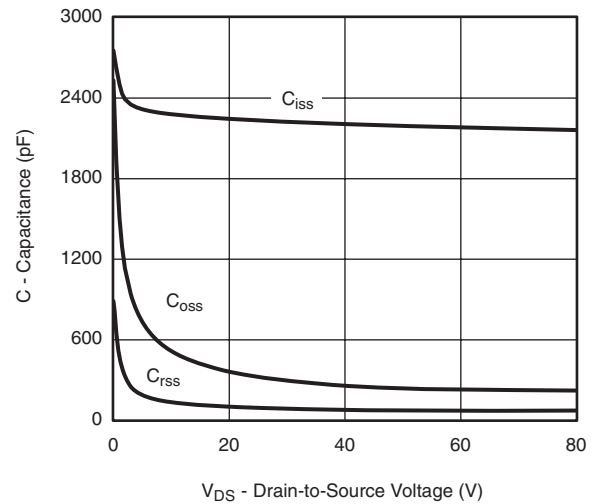
Output Characteristics



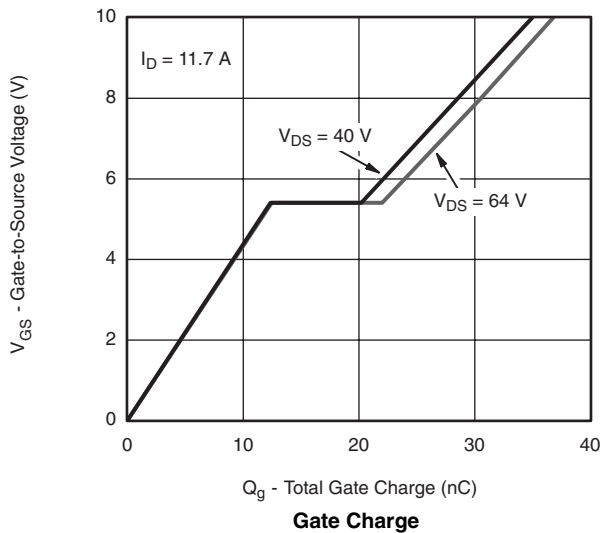
Transfer Characteristics



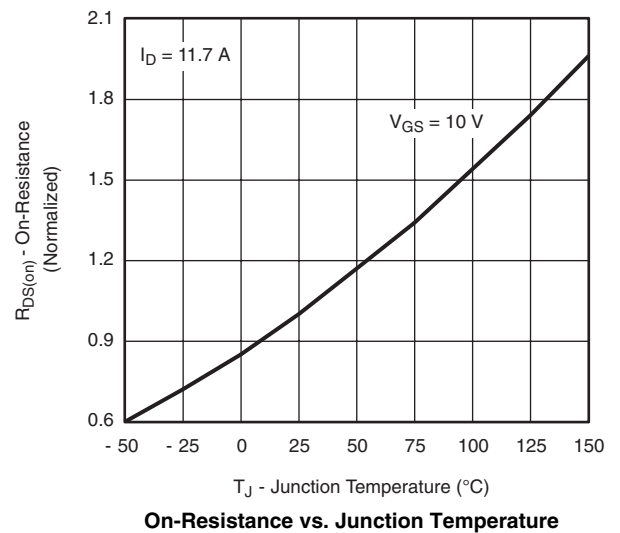
On-Resistance vs. Drain Current



Capacitance



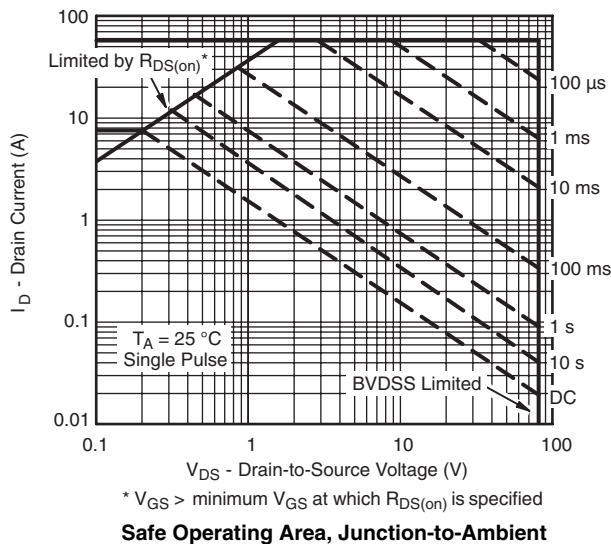
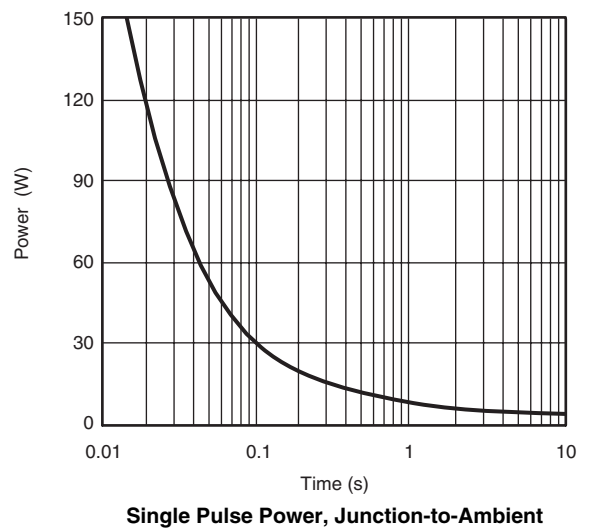
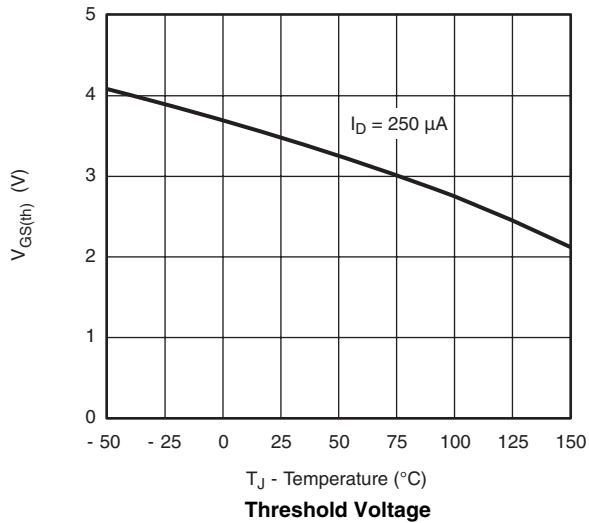
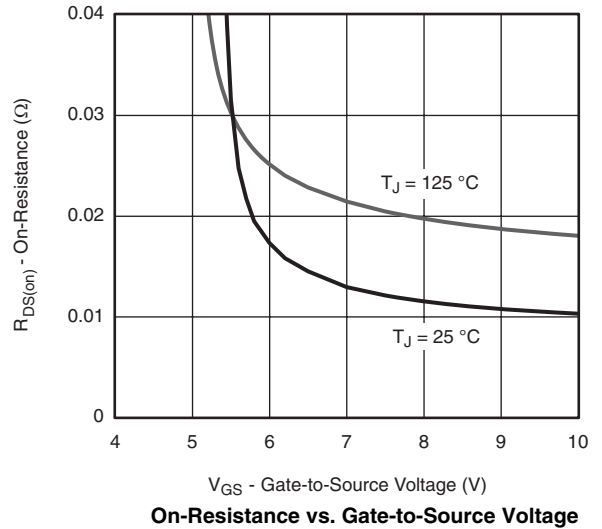
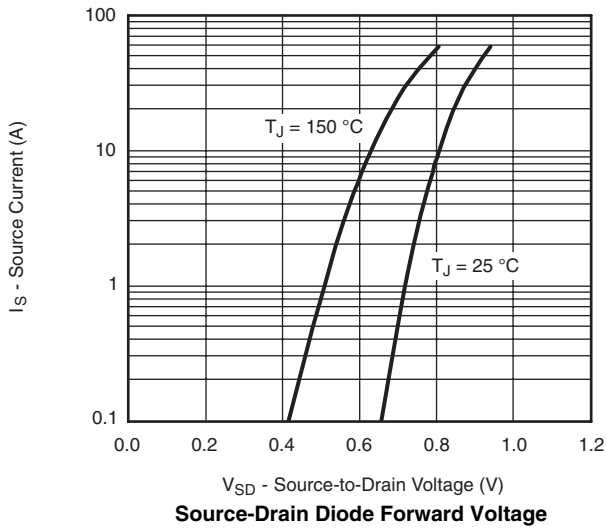
Gate Charge



On-Resistance vs. Junction Temperature

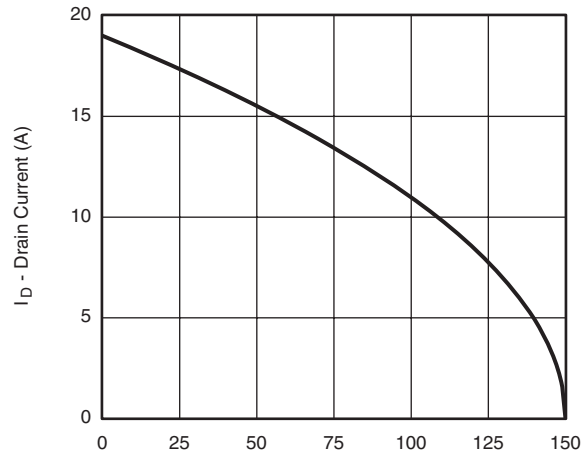


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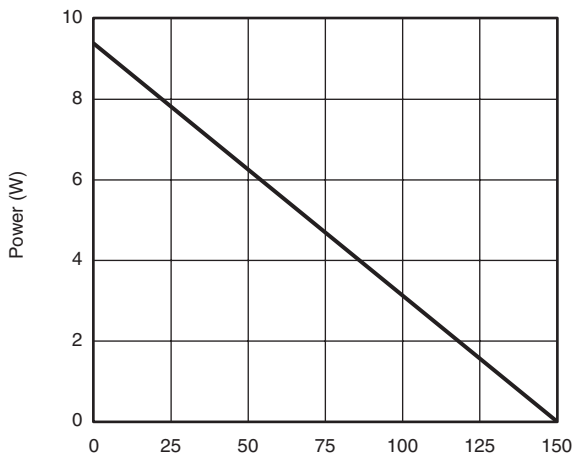




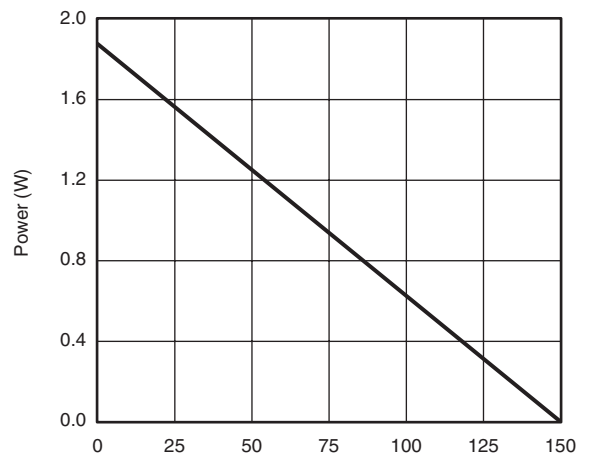
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T_C - Case Temperature (°C)
Current Derating*



T_C - Case Temperature (°C)
Power, Junction-to-Case

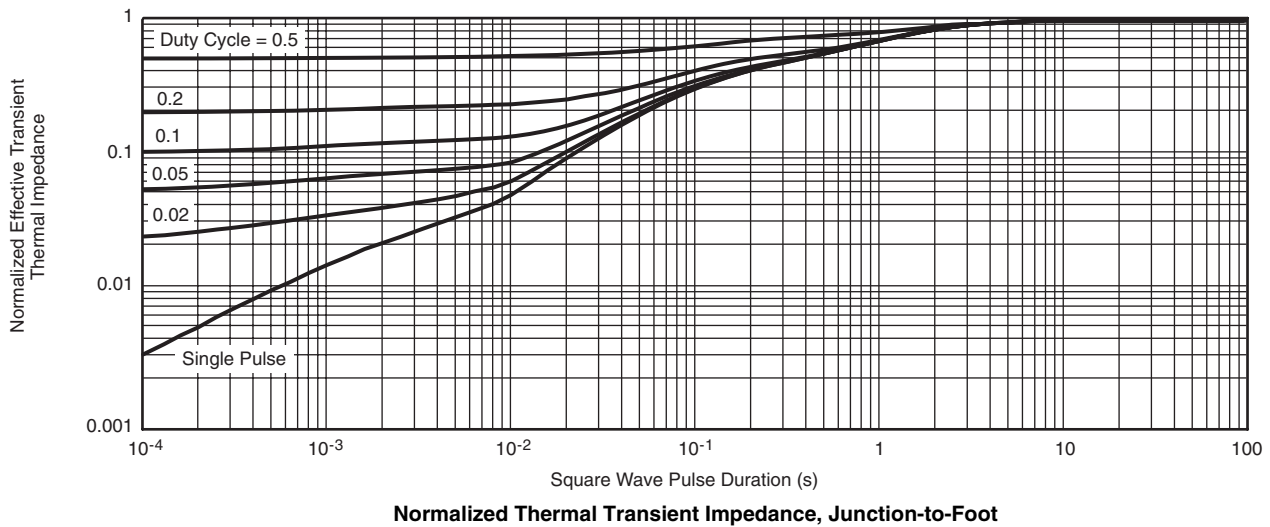
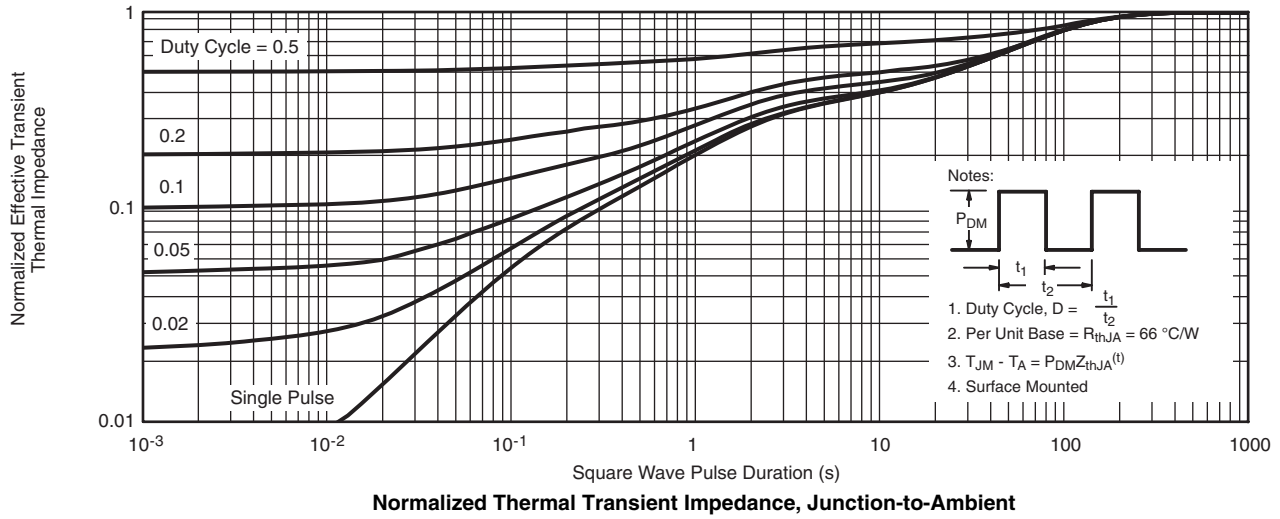


T_A - Ambient Temperature (°C)
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



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