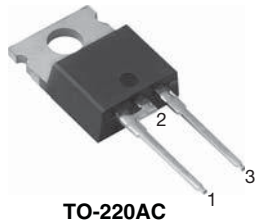
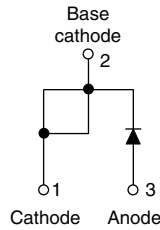




## High Voltage, Input Rectifier Diode, 10 A



TO-220AC



### FEATURES

- Very low forward voltage drop
- 150 °C max. operating junction temperature
- Glass passivated pellet chip junction
- Designed and qualified according to JEDEC®-JESD 47
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
**HALOGEN**  
**FREE**  
Available

PRODUCT SUMMARY	
Package	TO-220AC
$I_{F(AV)}$	10 A
$V_R$	800 V to 1200 V
$V_F$ at $I_F$	1.1 V
$I_{FSM}$	160 A
$T_J$ max.	150 °C
Diode variation	Single die

### APPLICATIONS

- Input rectification
- Vishay Semiconductors switches and output rectifiers which are available in identical package outlines

### DESCRIPTION

High voltage rectifiers optimized for very low forward voltage drop with moderate leakage.

These devices are intended for use in main rectification (single or three phase bridge).

OUTPUT CURRENT IN TYPICAL APPLICATIONS			
APPLICATIONS	SINGLE-PHASE BRIDGE	THREE-PHASE BRIDGE	UNITS
Capacitive input filter $T_A = 55$ °C, $T_J = 125$ °C common heatsink of 1 °C/W	12.0	16.0	A

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{F(AV)}$	Sinusoidal waveform	10	A
$V_{RRM}$		800/1200	V
$I_{FSM}$		160	A
$V_F$	10 A, $T_J = 25$ °C	1.1	V
$T_J$		-40 to +150	°C

VOLTAGE RATINGS			
PART NUMBER	$V_{RRM}$ , MAXIMUM PEAK REVERSE VOLTAGE V	$V_{RSM}$ , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	$I_{RRM}$ AT 150 °C mA
VS-10ETS08PbF, VS-10ETS08-M3	800	900	0.5
VS-10ETS12PbF, VS-10ETS12-M3	1200	1300	



ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum average forward current	$I_{F(AV)}$	$T_C = 105\text{ }^\circ\text{C}$ , 180° conduction half sine wave	10	A
Maximum peak one cycle non-repetitive surge current	$I_{FSM}$	10 ms sine pulse, rated $V_{RRM}$ applied	135	
		10 ms sine pulse, no voltage reapplied	160	
Maximum $I^2t$ for fusing	$I^2t$	10 ms sine pulse, rated $V_{RRM}$ applied	91	A <sup>2</sup> s
		10 ms sine pulse, no voltage reapplied	130	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	$t = 0.1\text{ ms to }10\text{ ms}$ , no voltage reapplied	1300	A <sup>2</sup> √s

ELECTRICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum forward voltage drop	$V_{FM}$	10 A, $T_J = 25\text{ }^\circ\text{C}$	1.1	V
Forward slope resistance	$r_t$	$T_J = 150\text{ }^\circ\text{C}$	20	mΩ
Threshold voltage	$V_{F(TO)}$		0.82	V
Maximum reverse leakage current	$I_{RM}$	$T_J = 25\text{ }^\circ\text{C}$	0.05	mA
		$T_J = 150\text{ }^\circ\text{C}$		

THERMAL - MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range	$T_J, T_{Stg}$		-40 to +150	°C
Maximum thermal resistance, junction to case	$R_{thJC}$	DC operation	2.5	°C/W
Maximum thermal resistance, junction to ambient (PCB mount)	$R_{thJA}$		62	
Soldering temperature	$T_S$		240	°C
Approximate weight			2	g
			0.07	oz.
Marking device		Case style TO-220AC	10ETS08	
			10ETS12	

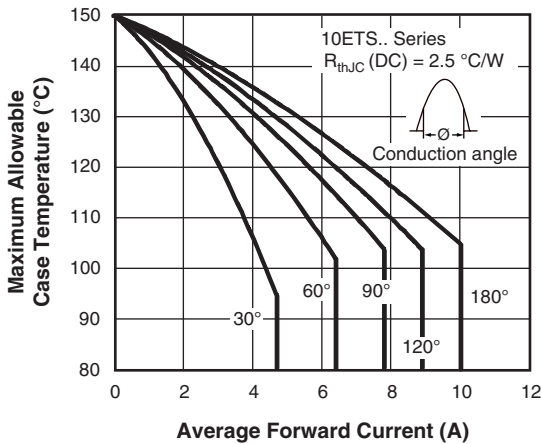


Fig. 1 - Current Rating Characteristics

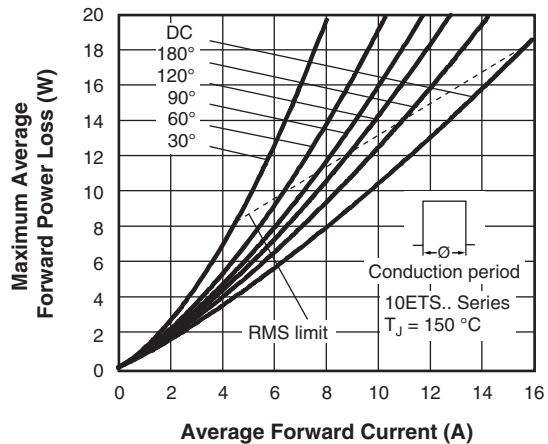


Fig. 4 - Forward Power Loss Characteristics

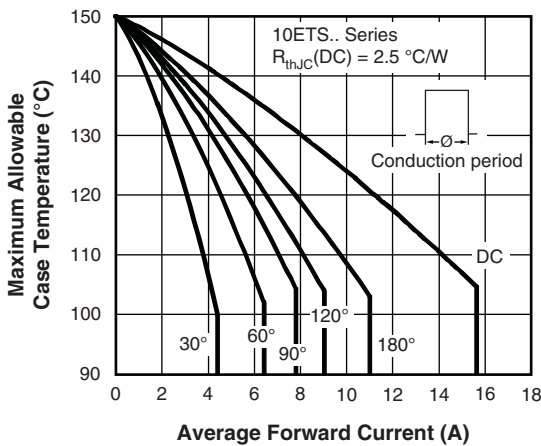


Fig. 2 - Current Rating Characteristics

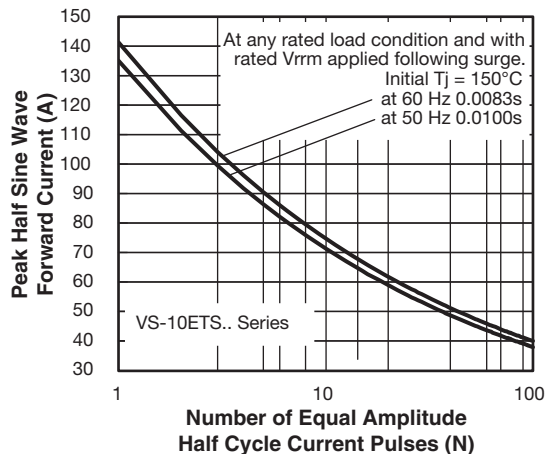


Fig. 5 - Maximum Non-Repetitive Surge Current

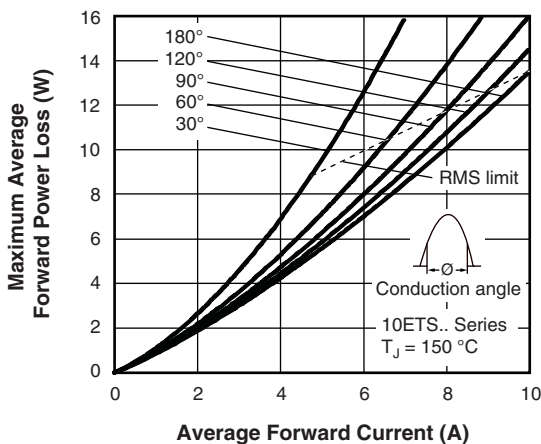


Fig. 3 - Forward Power Loss Characteristics

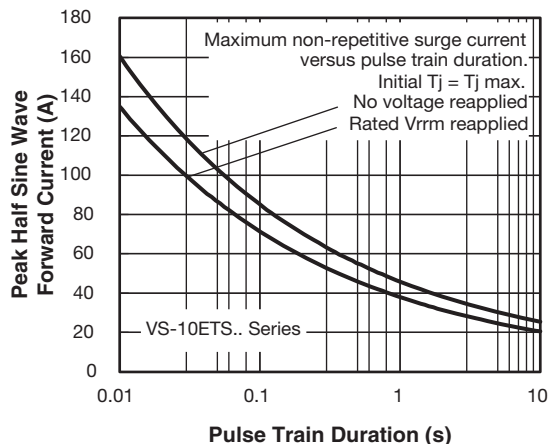


Fig. 6 - Maximum Non-Repetitive Surge Current

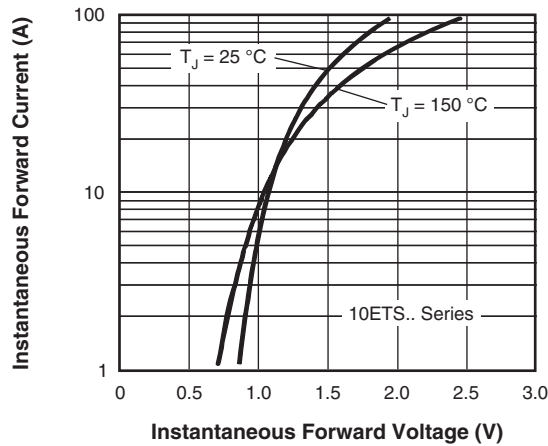


Fig. 7 - Forward Voltage Drop Characteristics

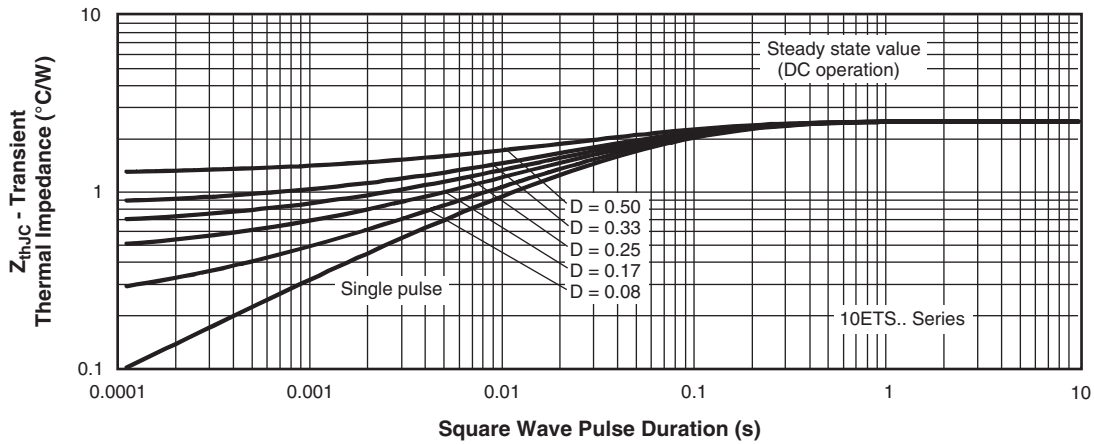
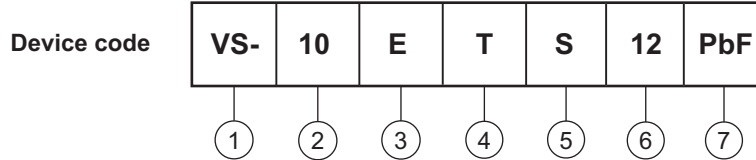


Fig. 8 - Thermal Impedance  $Z_{thJC}$  Characteristics



## ORDERING INFORMATION TABLE



- 1** - Vishay Semiconductors product
- 2** - Current rating (10 = 10 A)
- 3** - Circuit configuration:  
E = single diode
- 4** - Package:  
T = TO-220AC
- 5** - Type of silicon:  
S = standard recovery rectifier
- 6** - Voltage code x 100 =  $V_{RRM}$ 

08 = 800 V
12 = 1200 V
- 7** - Environmental digit:  
PbF = lead (Pb)-free and RoHS-compliant  
-M3 = halogen-free, RoHS-compliant, and terminations lead (Pb)-free

ORDERING INFORMATION (Example)			
PREFERRED P/N	QUANTITY PER T/R	MINIMUM ORDER QUANTITY	PACKAGING DESCRIPTION
VS-10ETS08PbF	50	1000	Antistatic plastic tubes
VS-10ETS08-M3	50	1000	Antistatic plastic tubes
VS-10ETS12PbF	50	1000	Antistatic plastic tubes
VS-10ETS12-M3	50	1000	Antistatic plastic tubes

LINKS TO RELATED DOCUMENTS	
Dimensions	<a href="http://www.vishay.com/doc?95221">www.vishay.com/doc?95221</a>
Part marking information	TO-220AC PbF <a href="http://www.vishay.com/doc?95224">www.vishay.com/doc?95224</a>
	TO-220AC -M3 <a href="http://www.vishay.com/doc?95068">www.vishay.com/doc?95068</a>

## TO-220AC

**DIMENSIONS** in millimeters and inches



SYMBOL	MILLIMETERS		INCHES		NOTES	SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.			MIN.	MAX.	MIN.	MAX.	
A	4.25	4.65	0.167	0.183		E1	6.86	8.89	0.270	0.350	6
A1	1.14	1.40	0.045	0.055		E2	-	0.76	-	0.030	7
A2	2.56	2.92	0.101	0.115		e	2.41	2.67	0.095	0.105	
b	0.69	1.01	0.027	0.040		e1	4.88	5.28	0.192	0.208	
b1	0.38	0.97	0.015	0.038	4	H1	6.09	6.48	0.240	0.255	6, 7
b2	1.20	1.73	0.047	0.068		L	13.52	14.02	0.532	0.552	
b3	1.14	1.73	0.045	0.068	4	L1	3.32	3.82	0.131	0.150	2
c	0.36	0.61	0.014	0.024		L3	1.78	2.13	0.070	0.084	
c1	0.36	0.56	0.014	0.022	4	L4	0.76	1.27	0.030	0.050	2
D	14.85	15.25	0.585	0.600	3	Ø P	3.54	3.73	0.139	0.147	
D1	8.38	9.02	0.330	0.355		Q	2.60	3.00	0.102	0.118	
D2	11.68	12.88	0.460	0.507	6	θ	90° to 93°		90° to 93°		
E	10.11	10.51	0.398	0.414	3, 6						

**Notes**

- (1) Dimensioning and tolerancing as per ASME Y14.5M-1994
- (2) Lead dimension and finish uncontrolled in L1
- (3) Dimension D, D1 and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Dimension b1, b3 and c1 apply to base metal only
- (5) Controlling dimension: inches
- (6) Thermal pad contour optional within dimensions E, H1, D2 and E1
- (7) Dimension E2 x H1 define a zone where stamping and singulation irregularities are allowed
- (8) Outline conforms to JEDEC TO-220, D2 (minimum) where dimensions are derived from the actual package outline



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