



Low-Voltage Single SPDT Analog Switch

DESCRIPTION

The DG9461 is a single-pole/double-throw monolithic CMOS analog device designed for high performance switching of analog signals. Combining low power, high speed (t_{ON} : 35 ns, t_{OFF} : 20 ns), low on-resistance ($r_{DS(on)}$: 40 Ω) and small physical size (TSOP-6), the DG9461 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG9461 is built on Vishay Siliconix's low voltage BCD-15 process. Minimum ESD protection, per Method 3015.7, is 2000 V. An epitaxial layer prevents latchup. Break-before-make is guaranteed for DG9461.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FEATURES

- Low Voltage Operation (+ 2.7 to + 5 V)
- Low On-Resistance $r_{DS(on)}$: 40 Ω
- Fast Switching t_{ON}: 35 ns, t_{OFF}: 20 ns
- Low Leakage I_{COM(on)}: 200 pA max
- Low Charge Injection Q_{IN.J}: 1 pC
- Low Power Consumption
- TTL/CMOS Compatible
- ESD Protection > 2000 V (Method 3015.7)
- Available in TSOP-6 and SOIC-8

BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space (TSOP-6)

APPLICATIONS

- · Battery Operated Systems
- Portable Test Equipment
- Sample and Hold Circuits
- Cellular Phones
- Communication Systems
- Military Radio

TRUTH TABLE

Logic

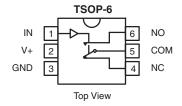
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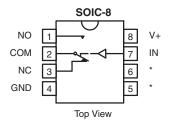
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Logic "0" ≤ 0.8 V Logic "1" ≥ 2.4 V

PBX, PABX Guidance and Control Systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION





*Not Connected

ORDERING INFORMATION					
Temp Range	Package	Part Number			
- 40 to 85 °C	TSOP-6	DG9461DV-T1 DG9461DV-T1-E3			
	SOIC-8	DG9461DY-T1			

NC

ON

OFF

NO

OFF

ON

DG9461DY-T1-E3

^{*} Pb containing terminations are not RoHS compliant, exemptions may apply

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ABSOLUTE MAXIMUM RATINGS						
Parameter		Limit	Unit			
Reference V+ to GND	V+ to GND - 0.3 to + 13					
IN, COM, NC, NO ^a		- 0.3 V to (V+ + 0.3 V)	V			
Continuous Current (Any terminal)		± 20	mA			
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 40	- IIIA			
ESD (Method 3015.7)		> 2000	V			
Storage Temperature (D Suffix)		- 65 to 125	°C			
Power Dissipation (Packages) ^b	8-Pin Narrow Body SOIC ^c	400	mW			

Notes:

- a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings. b. All leads welded or soldered to PC Board. c. Derate 6.5 mW/°C above 75 °C.

SPECIFICATIONS (V+ = 3 V)							
		Test Conditions Unless Otherwise Specified		D Suffix - 40 to 85 °C			
Parameter	Symbol	$V+ = 3 V, \pm 10 \%, V_{IN} = 0.4 \text{ or } 2.4 V^{e}$	Temp ^a	Min ^c	Typ ^b	Max ^c	Unit
Analog Switch							
Analog Signal Range ^d	V_{ANALOG}		Full	0		3	V
Drain-Source On-Resistance	r _{DS(on)}	V_{NO} or $V_{NC} = 1.5 \text{ V}$, $V_{+} = 2.7 \text{ V}$ $I_{COM} = 5 \text{ mA}$	Room Full		50	80 140	
r _{DS(on)} Match ^d	$\Delta r_{DS(on)}$	V_{NO} or $V_{NC} = 1.5 \text{ V}$	Room		0.4	2	Ω
r _{DS(on)} Flatness ^f	r _{DS(on)} Flatness	V_{NO} or $V_{NC} = 1$ and 2 V	Room		4	8	
NO or NC Off Leakage Current ^g	I _{NO/NC(off)}	V_{NO} or V_{NC} = 1 V/2 V, V_{COM} = 2 V/1 V	Room Full	- 100 - 5000	5	100 5000	
COM Off Leakage Current ^g	I _{COM(off)}	$V_{COM} = 1 \text{ V/2 V}, V_{NO} \text{ or } V_{NC} = 2 \text{ V/1 V}$	Room Full	- 100 - 5000	5	100 5000	pА
Channel-On Leakage Current ^g	I _{COM(on)}	$V_{COM} = V_{NO}$ or $V_{NC} = 1 \text{ V/2 V}$	Room Full	- 200 - 10000	10	200 10000	
Digital Control							
Input Current	I _{INL} or I _{INH}		Full		1		μΑ
Dynamic Characteristics							
Turn-On Time	t _{ON}		Room Full		50	120 200	
Turn-Off Time	t _{OFF}	V_{NO} or $V_{NC} = 1.5 \text{ V}$	Room Full		20	50 120	ns
Break-Before-Make Time	t _d		Room	3	20		
Charge Injection	Q_{INJ}	C_L = 1 nF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room		1	5	рС
Off-Isolation	OIRR	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$	Room		- 74		dB
Source Off Capacitance	C _{S(off)}	f = 1 MHz	Room		7		pF
Channel-On Capacitance	C _{D(on)}		Room		32		Pi
Power Supply							
Power Supply Range	V+			2.7	•	12	V
Power Supply Current	l+	$V+ = 3.3 \text{ V}, V_{IN} = 0 \text{ or } 3.3 \text{ V}$				1	μΑ





SPECIFICATIONS (V+ = 5 V)							
		Test Conditions Unless Otherwise Specified		D Suffix - 40 to 85 °C			
Parameter	Symbol	$V+ = 5 V$, $\pm 10 \%$, $V_{IN} = 0.8 \text{ or } 2.4 V^e$	Temp ^a	Min ^c	Typ ^b	Max ^c	Unit
Analog Switch							
Analog Signal Range ^d	V _{ANALOG}		Full	0		5	٧
Drain-Source On-Resistance	r _{DS(on)}	V_{NO} or $V_{NC} = 3.5 \text{ V}$, $V_{+} = 4.5 \text{ V}$ $I_{COM} = 5 \text{ mA}$	Room Full		30	60 75	
r _{DS(on)} Match ^d	$\Delta r_{DS(on)}$	V _{NO} or V _{NC} = 1.5 V	Room		0.4	2	Ω
r _{DS(on)} Flatness ^f	r _{DS(on)} Flatness	V_{NO} or $V_{NC} = 1,2$ and 3 V	Room		2	6	-
NO or NC Off Leakage Current	I _{NO/NC(off)}	V_{NO} or V_{NC} = 1 V/4 V, V_{COM} = 4 V/1 V	Room Full	- 100 - 5000	10	100 5000	
COM Off Leakage Current	I _{COM(off)}	$V_{COM} = 1 \text{ V/4 V}, V_{NO} \text{ or } V_{NC} = 4 \text{ V/1 V}$	Room Full	- 100 - 5000	10	100 5000	pА
Channel-On Leakage Current	I _{COM(on)}	$V_{COM} = V_{NO}$ or $V_{NC} = 1 \text{ V/4 V}$	Room Full	- 200 - 10000		200 10000	
Digital Control			•			•	
Input Current	I _{INL} or I _{INH}		Full		1		μΑ
Dynamic Characteristics							
Turn-On Time	t _{ON}		Room Full		35	75 150	
Turn-Off Time	t _{OFF}	V_{NO} or $V_{NC} = 3.0 \text{ V}$	Room Full		20	50 100	ns
Break-Before-Make Time	t _d		Room	3	10		
Charge Injection	Q _{INJ}	$C_L = 1 \text{ nF, } V_{gen} = 0 \text{ V, } R_{gen} = 0 \Omega$	Room		2	5	рC
Off-Isolation	OIRR	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$	Room		- 74		dB
NC and NO Capacitance	C _(off)	f = 1 MHz	Room		- 7		pF
Channel-On Capacitance	C _{D(on)}		Room		32		Pi
Power Supply							
Power Supply Range	V+			2.7		12	V
Power Supply Current	I+	$V+ = 5.5 V$, $V_{IN} = 0 \text{ or } 5.5 V$				1	μΑ

Notes:

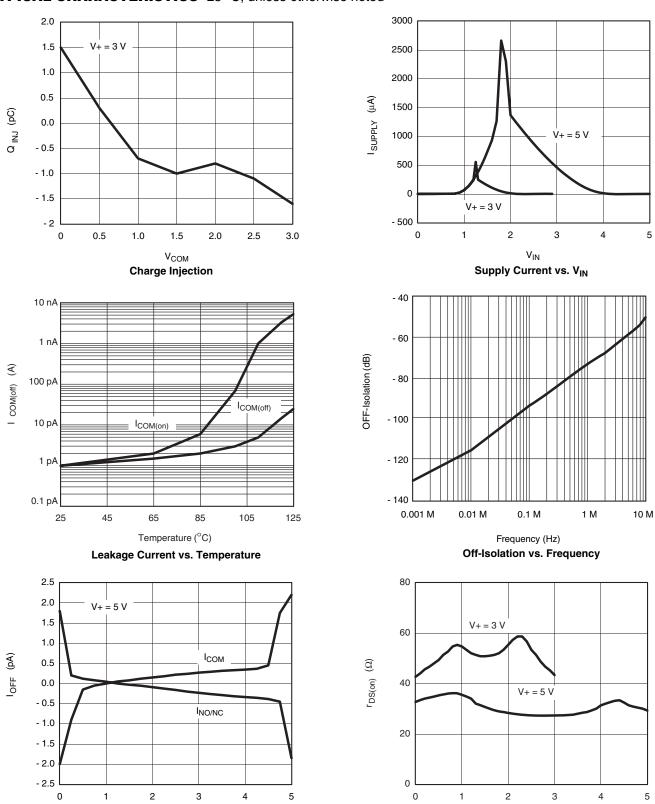
- a. Room = 25 $^{\circ}$ C, Full = as determined by the operating suffix.
- b. Typical values are for design aid only, not guaranteed nor subject to production testing.
- c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- d. Guarantee by design, nor subjected to production test.
- e. V_{IN} = input voltage to perform proper function.
- f. Difference of min and max values.
- g. Guraranteed by 5 V leakage testing, not production tested.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



 V_{COM}

Off-Leakage vs. Voltage at 25 °C

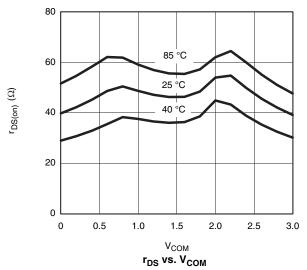
 $\begin{array}{c} v_{\text{COM}} \\ r_{\text{DS}} \text{ vs. } V_{\text{COM}} \end{array}$

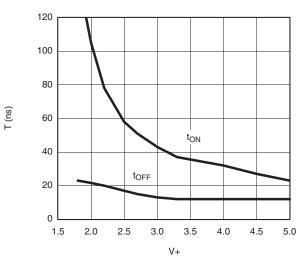




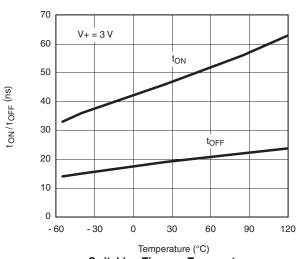


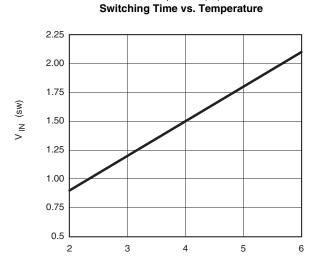
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted







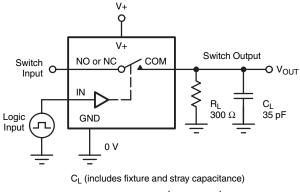


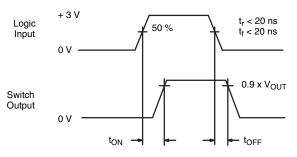


Input Switching Point vs. Power Supply Voltage

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TEST CIRCUITS





$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$

Logic "1" = Switch On Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time

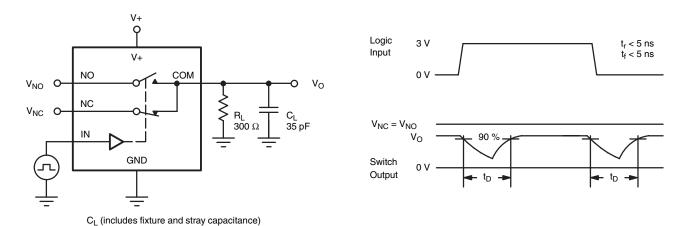


Figure 2. Break-Before-Make Interval

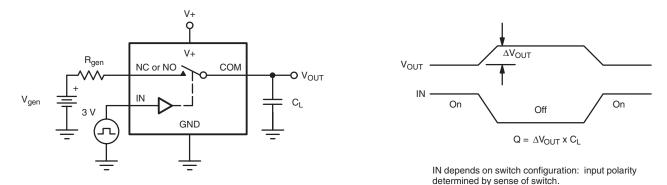


Figure 3. Charge Injection



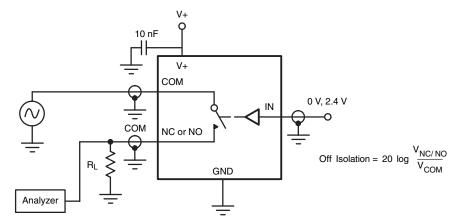


Figure 4. Off-Isolation

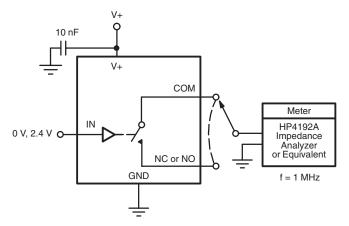


Figure 5. Channel Off/On Capacitance

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