

Low-Voltage Dual SPST Analog Switch

DESCRIPTION

The DG9232, 9233 is a single-pole/single-throw monolithic CMOS analog device designed for high performance switching of analog signals. Combining low power, high speed (t_{ON} : 35 ns, t_{OFF} : 20 ns), low on-resistance ($R_{DS(on)}$: 20 Ω) and small physical size, the DG9232, 9233 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG9232, 9233 is built on Vishay Siliconix's low voltage BCD-15 process. Minimum ESD protection, per method 3015.7 is 2000 V. An epitaxial layer prevents latchup. Break-before-make is guaranteed for DG9232, 9233.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

BENEFITS

- Reduced power consumption
- Simple logic interface
- High accuracy
- Reduce board space

FEATURES

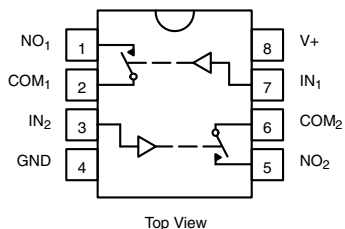
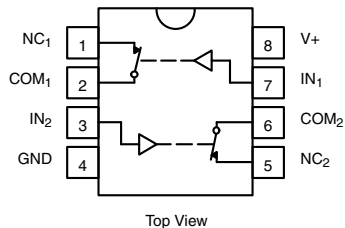
- Low voltage operation (+ 2.7 V to + 5 V)
- Low on-resistance - $R_{DS(on)}$: 20 Ω
- Fast switching - t_{ON} : 35 ns, t_{OFF} : 20 ns
- Low leakage - $I_{COM(on)}$: 200 pA max.
- Low charge injection - Q_{INJ} : 1 pC
- Low power consumption
- TTL/CMOS compatible
- ESD protection > 2000 V (method 3015.7)
- Available in MSOP-8 and SOIC-8
- **Compliant to RoHS Directive 2002/95/EC**


RoHS*
COMPLIANT

APPLICATIONS

- Battery operated systems
- Portable test equipment
- Sample and hold circuits
- Cellular phones
- Communication systems
- Military radio
- PBX, PABX guidance and control systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION


TRUTH TABLE - DG9232

Logic	Switch
0	On
1	Off

 Logic "0" \leq 0.8 V
 Logic "1" \geq 2.4 V

TRUTH TABLE - DG9233

Logic	Switch
0	Off
1	On

 Logic "0" \leq 0.8 V
 Logic "1" \geq 2.4 V

ORDERING INFORMATION

Temp Range	Package	Part Number
- 40 °C to 85 °C	SOIC-8	DG9232DY
		DG9232DY-E3
		DG9232DY-T1
		DG9232DY-T1-E3
	MSOP-8	DG9233DY
		DG9233DY-E3
		DG9233DY-T1
		DG9233DY-T1-E3
		DG9232DQ-T1-E3
		DG9233DQ-T1-E3

* Pb containing terminations are not RoHS compliant, exemptions may apply

ABSOLUTE MAXIMUM RATINGS			
Parameter		Limit	Unit
Reference V+ to GND		- 0.3 to + 13	V
IN, COM, NC, NO ^a		- 0.3 to (V+ + 0.3)	
Continuous Current (Any terminal)		± 20	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 40	
ESD (Method 3015.7)		> 2000	V
Storage Temperature	D suffix	- 65 to 125	°C
Power Dissipation (Packages) ^b	8-pin narrow body SOIC ^c	400	mW

Notes:

- a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 6.5 mW/°C above 70 °C.

SPECIFICATIONS (V+ = 3 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, V _{IN} = 0.8 V or 2.4 V ^e	Temp. ^a	D Suffix - 40 °C to 85 °C			Unit
				Min. ^c	Typ. ^b	Max. ^c	
Analog Switch							
Analog Signal Range ^d	V _{ANALOG}		Full	0		3	V
Drain-Source On-Resistance	R _{DS(on)}	V _{NO} or V _{NC} = 1.5 V, V+ = 2.7 V I _{COM} = 5 mA	Room Full		30	50 80	Ω
R _{DS(on)} Match ^d	ΔR _{DS(on)}	V _{NO} or V _{NC} = 1.5 V	Room		0.4	2	
R _{DS(on)} Flatness ^d	R _{DS(on)} Flatness	V _{NO} or V _{NC} = 1 and 2 V	Room		4	8	
NO or NC Off Leakage Current ^g	I _{NO/NC(off)}	V _{NO} or V _{NC} = 1 V/2 V, V _{COM} = 2 V/1 V	Room Full	- 100 - 5000	5	100 5000	pA
COM Off Leakage Current ^g	I _{COM(off)}	V _{COM} = 1 V/2 V, V _{NO} or V _{NC} = 2 V/1 V	Room Full	- 100 - 5000	5	100 5000	
Channel-On Leakage Current ^g	I _{COM(on)}	V _{COM} = V _{NO} or V _{NC} = 1 V/2 V	Room Full	- 200 - 10000	10	200 10000	
Digital Control							
Input Current	I _{INL} or I _{INH}		Full		1		μA
Dynamic Characteristics							
Turn-On Time	t _{ON}	V _{NO} or V _{NC} = 1.5 V	Room Full		50	120 200	ns
Turn-Off Time	t _{OFF}		Room Full		20	50 120	
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _{GEN} = 0 V, R _{GEN} = 0 Ω	Room		1	5	pC
Off-Isolation	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room		- 74		dB
Crosstalk	X _{TALK}		Room		- 90		
NC and NO Capacitance	C _{S(off)}	f = 1 MHz	Room		7		pF
Channel-On Capacitance	C _{COM(on)}		Room		20		
COM-Off Capacitance	C _{COM(off)}		Room		13		
Power Supply							
Positive Supply Range	V+			2.7		12	V
Power Supply Current	I+	V+ = 3.3 V, V _{IN} = 0 or 3.3 V				1	μA

Notes:

- a. Room = 25 °C, Full = as determined by the operating suffix.
- b. Typical values are for design aid only, not guaranteed nor subject to production testing.
- c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
- d. Guarantee by design, nor subjected to production test.
- e. V_{IN} = input voltage to perform proper function.
- f. Difference of min and max values.
- g. Guaranteed by 5 V leakage tests, not production tested.



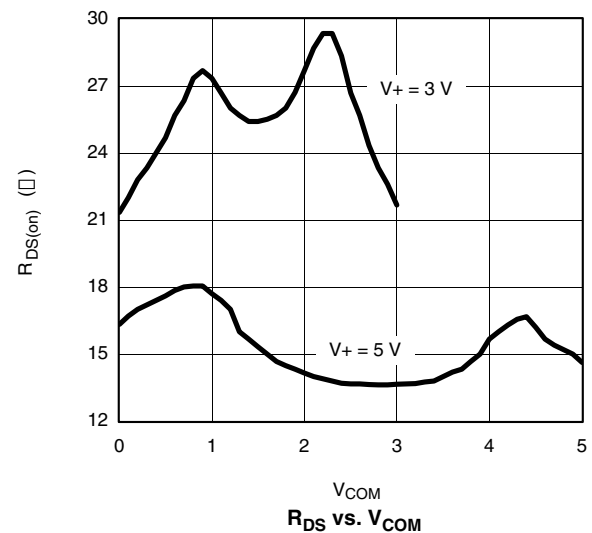
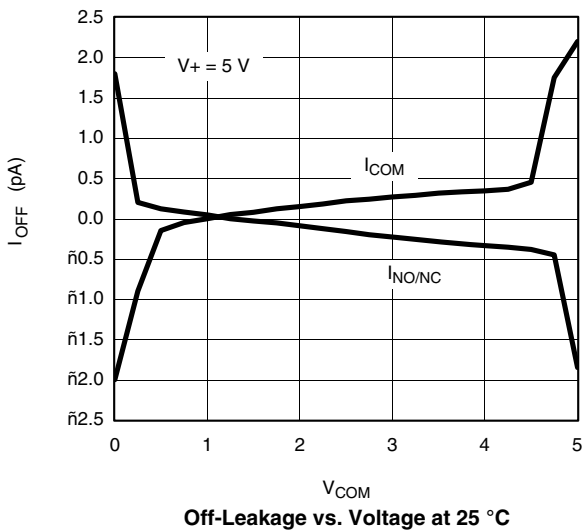
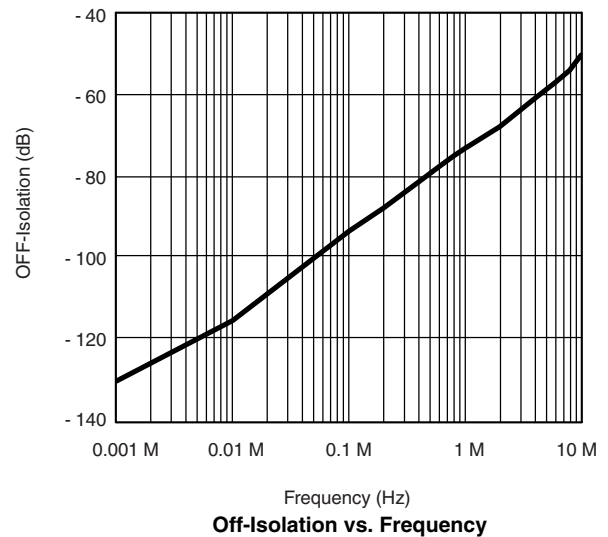
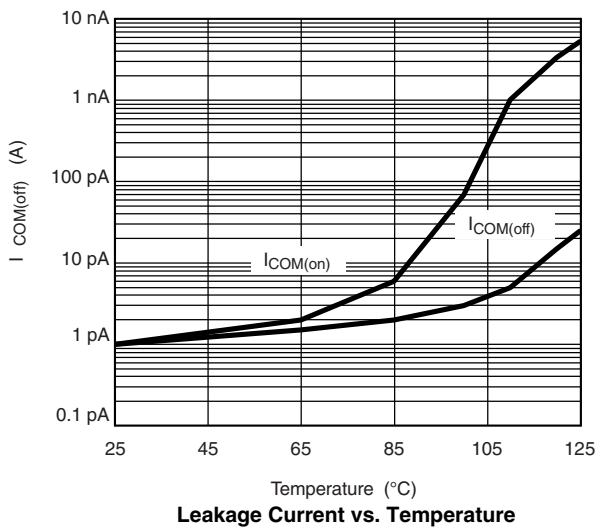
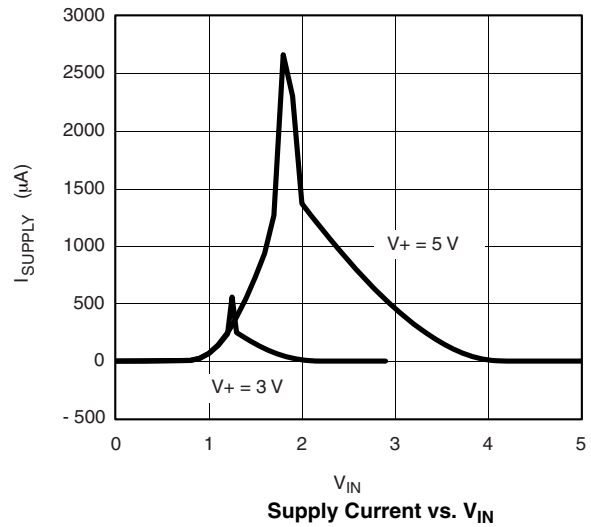
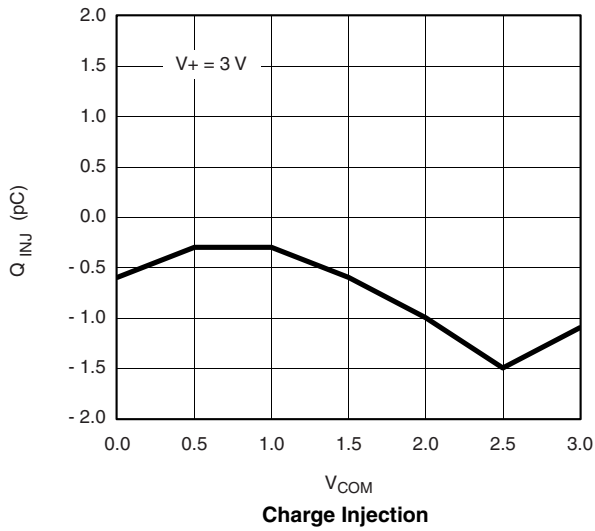
SPECIFICATIONS (V+ = 5 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ± 10 %, VIN = 0.8 V or 2.4 V ^e	Temp. ^a	D Suffix - 40 °C to 85°C			Unit
				Min. ^c	Typ. ^b	Max. ^c	
Analog Switch							
Analog Signal Range ^d	V _{ANALOG}		Full	0		5	V
Drain-Source On-Resistance	R _{DS(on)}	V _{NO} or V _{NC} = 3.5 V, V+ = 4.5 V I _{COM} = 5 mA	Room Full		20	30 50	Ω
R _{DS(on)} Match ^d	ΔR _{DS(on)}	V _{NO} or V _{NC} = 3.5 V	Room		0.4	2	
R _{DS(on)} Flatness ^d	R _{DS(on)} Flatness	V _{NO} or V _{NC} = 1, 2 and 3 V	Room		2	6	
NO or NC Off Leakage Current ^g	I _{NO/NC(off)}	V _{NO} or V _{NC} = 1 V/4 V, V _{COM} = 4 V/1 V	Room Full	- 100 - 5000	10	100 5000	pA
COM Off Leakage Current	I _{COM(off)}	V _{COM} = 1 V/4 V, V _{NO} or V _{NC} = 4 V/1 V	Room Full	- 100 - 5000	10	100 5000	
Channel-On Leakage Current	I _{COM(on)}	V _{COM} = V _{NO} or V _{NC} = 1 V/4 V	Room Full	- 200 - 10000		200 10000	
Digital Control							
Input Current	I _{INL} or I _{INH}		Full		1		μA
Dynamic Characteristics							
Turn-On Time	t _{ON}	V _{NO} or V _{NC} = 3.0 V	Room Full		35	75 150	ns
Turn-Off Time	t _{OFF}		Room Full		20	50 100	
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _{GEN} = 0 V, R _{GEN} = 0 Ω	Room		2	5	pC
Off-Isolation	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room		- 74		dB
Crosstalk	X _{TALK}		Room		- 90		
NC and NO Capacitance	C _(off)		f = 1 MHz	Room		7	
Channel-On Capacitance	C _{D(on)}	Room			20		
COM-Off Capacitance	C _{D(off)}	Room			13		
Power Supply							
Positive Supply Range	V+			2.7		12	V
Power Supply Current	I+	V+ = 5.5 V, V _{IN} = 0 or 5.5 V				1	μA

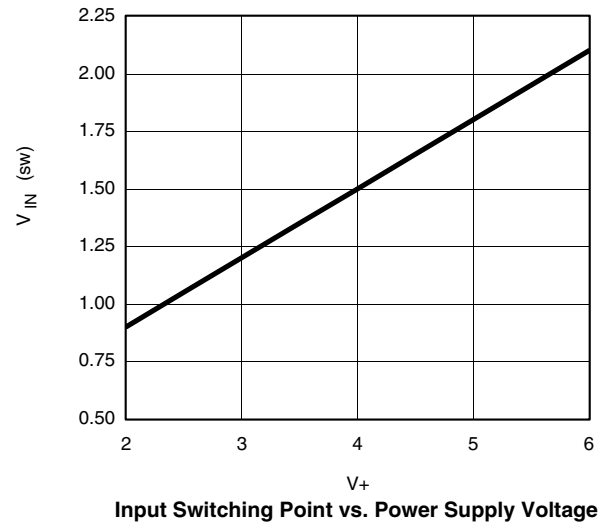
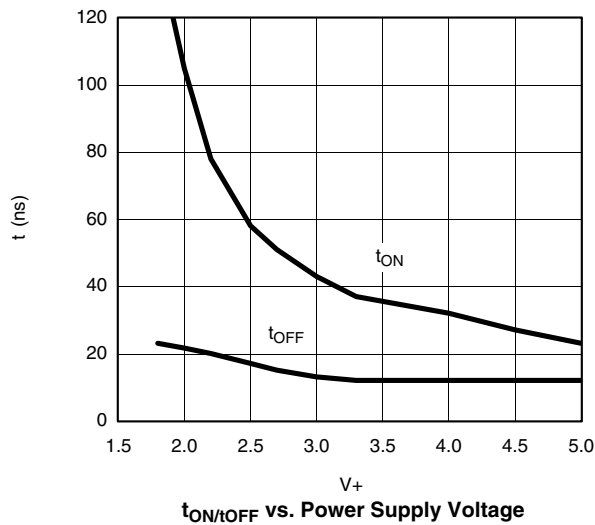
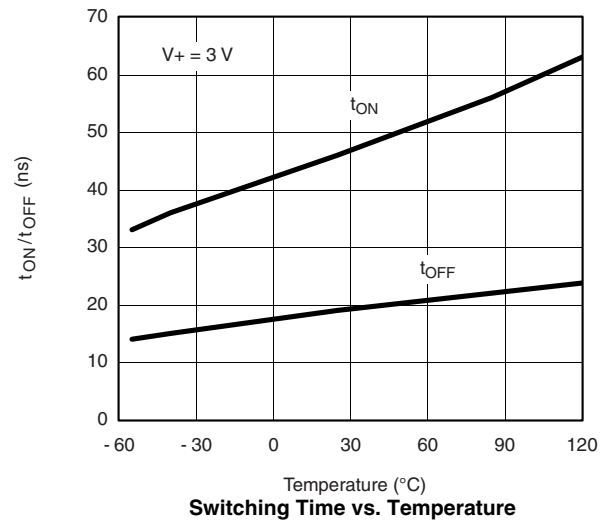
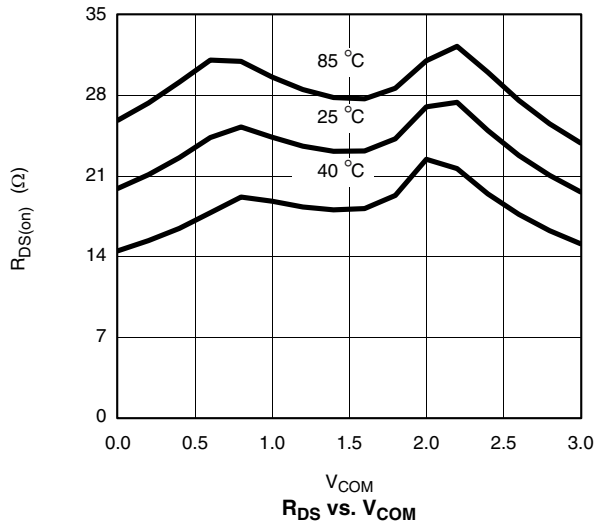
Notes:

- a. Room = 25 °C, Full = as determined by the operating suffix.
- b. Typical values are for design aid only, not guaranteed nor subject to production testing.
- c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
- d. Guarantee by design, nor subjected to production test.
- e. V_{IN} = input voltage to perform proper function.
- f. Difference of min and max values.

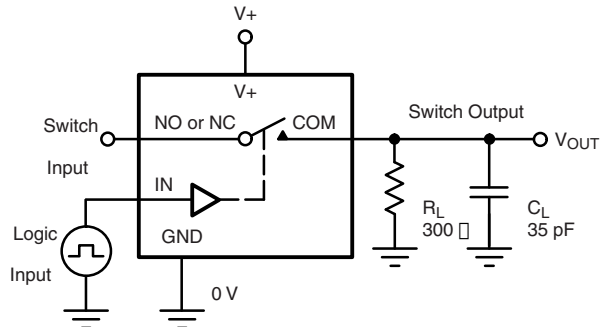
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted



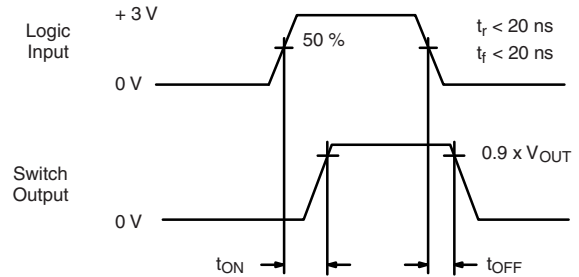
TYPICAL CHARACTERISTICS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted


TEST CIRCUITS



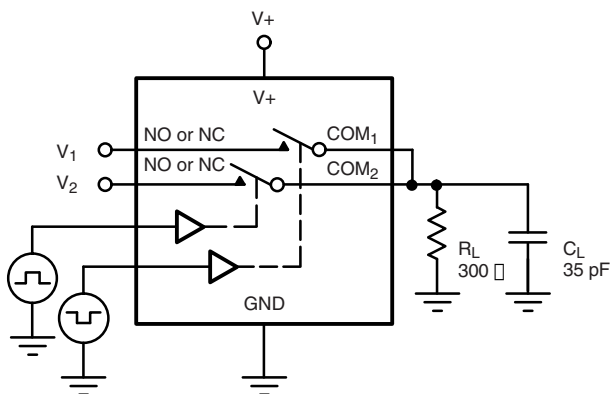
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

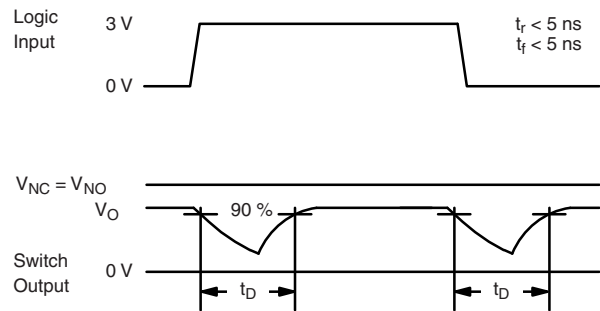
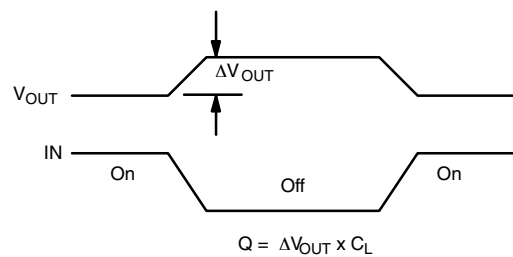
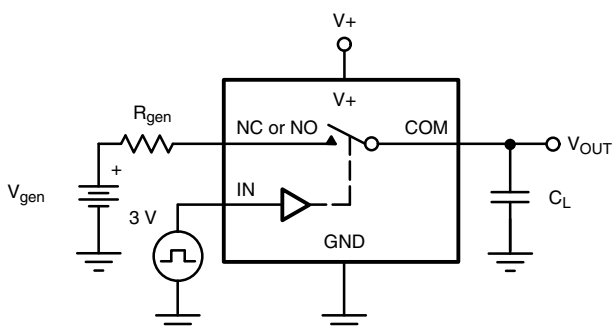


Figure 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

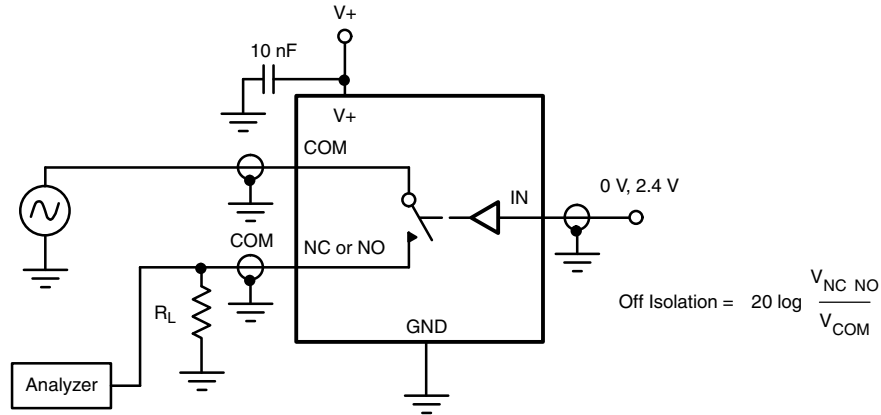


Figure 4. Off-Isolation

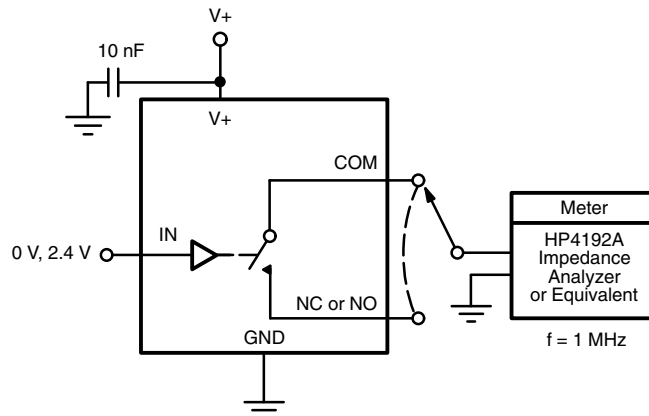


Figure 5. Channel Off/On Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?70837>.

SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012

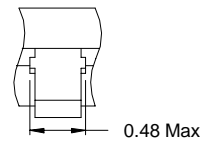
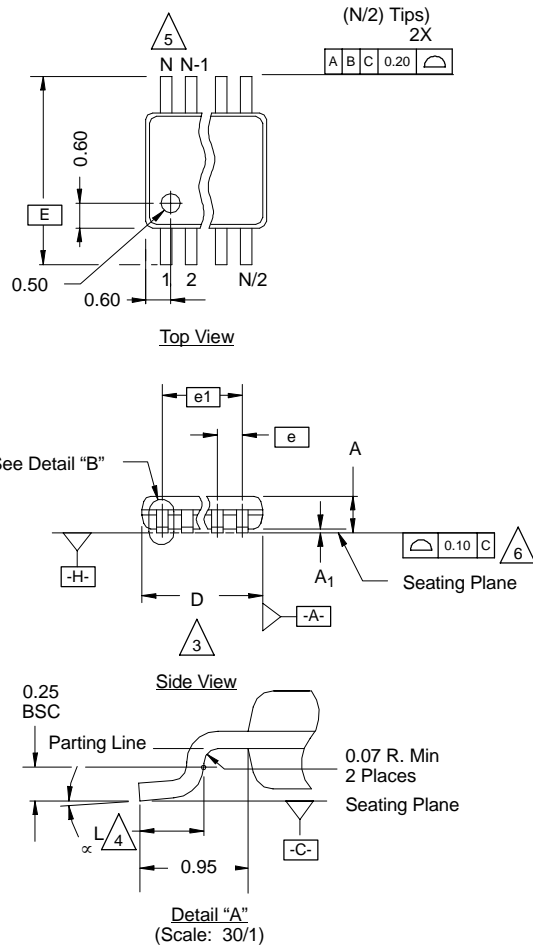


DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

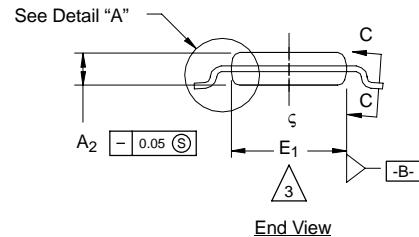
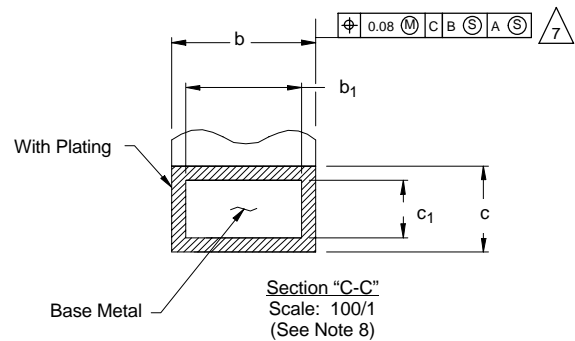


MSOP: 8-LEADS

JEDEC Part Number: MO-187, (Variation AA and BA)



Detail "B"
 (Scale: 30/1)
 Dambar Protrusion



NOTES:

- Die thickness allowable is 0.203 ± 0.0127 .
- Dimensioning and tolerances per ANSI.Y14.5M-1994.
- Dimensions "D" and "E₁" do not include mold flash or protrusions, and are measured at Datum plane [-H-], mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimension is the length of terminal for soldering to a substrate.
- Terminal positions are shown for reference only.
- Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
- The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
- Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
- Controlling dimension: millimeters.
- This part is compliant with JEDEC registration MO-187, variation AA and BA.
- Datums [-A-] and [-B-] to be determined Datum plane [-H-].
- Exposed pad area in bottom side is the same as teh leadframe pad size.

N = 8L

Dim	MILLIMETERS			Note
	Min	Nom	Max	
A	-	-	1.10	
A ₁	0.05	0.10	0.15	
A ₂	0.75	0.85	0.95	
b	0.25	-	0.38	8
b ₁	0.25	0.30	0.33	8
c	0.13	-	0.23	
c ₁	0.13	0.15	0.18	
D	3.00 BSC			3
E	4.90 BSC			
E ₁	2.90	3.00	3.10	3
e	0.65 BSC			
e ₁	1.95 BSC			
L	0.40	0.55	0.70	4
N	8			5
α	0°	4°	6°	

ECN: T-02080—Rev. C, 15-Jul-02
 DWG: 5867

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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