

Monolithic Dual SPST CMOS Analog Switch

FEATURES

- ± 15 V Input Signal Range
- 44-V Maximum Supply Ranges
- On-Resistance: 45Ω
- TTL and CMOS Compatibility

BENEFITS

- Wide Dynamic Range
- Simple Interfacing
- Reduced External Component Count

APPLICATIONS

- Servo Control Switching
- Programmable Gain Amplifiers
- Audio Switching
- Programmable Filters

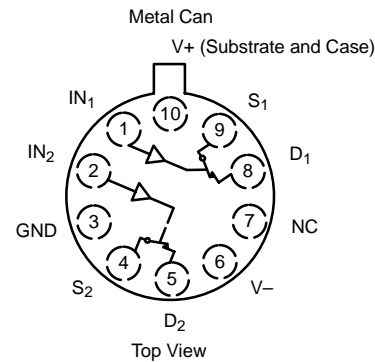
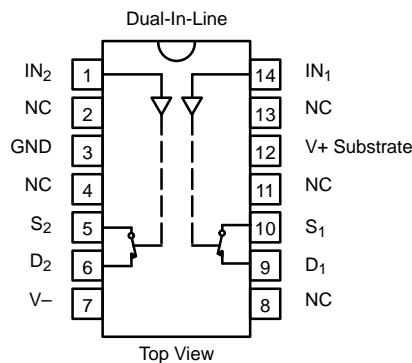
DESCRIPTION

The DG200A_MIL is a dual, single-pole, single-throw analog switch designed to provide general purpose switching of analog signals. This device is ideally suited for designs requiring a wide analog voltage range coupled with low on-resistance.

Each switch conducts equally well in both directions when on, and blocks up to 30 V peak-to-peak when off. In the on condition, this bi-directional switch introduces no offset voltage of its own.

The DG200A_MIL is designed on Vishay Siliconix' improved PLUS-40 CMOS process. An epitaxial layer prevents latchup.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE	
Logic	Switch
0	ON
1	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION		
Temp Range	Package	Part Number
-55 to 125°C	14-Pin CerDIP	DG200AAK
		DG200AAK/883, JM38510/12301BCA, 5962-9562901QCA
	10-Pin Metal Can	DG200AAA
		DG200AAA/883, JM38510/12301BIC
14-Pin Sidebrazed	JM38510/12301BCC	

ABSOLUTE MAXIMUM RATINGS

V+ to V-	44 V
GND to V-	25 V
Digital Inputs ^a , V _S , V _D	(V-) -2 V to (V+) +2 V or 30 mA, whichever occurs first
Current (Any Terminal) Continuous	30 mA
Current S or D (Pulsed at 1 ms, 10% Duty Cycle Max)	100 mA
Storage Temperature	-65 to 150°C

Power Dissipation (Package) ^b	
10-Pin Metal Can ^c	450 mW
14-Pin CerDIP ^d	825 mW

- Notes:
- Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
 - All leads welded or soldered to PC Board.
 - Derate 6 mW/°C above 75°C
 - Derate 11 mW/°C above 75°C

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

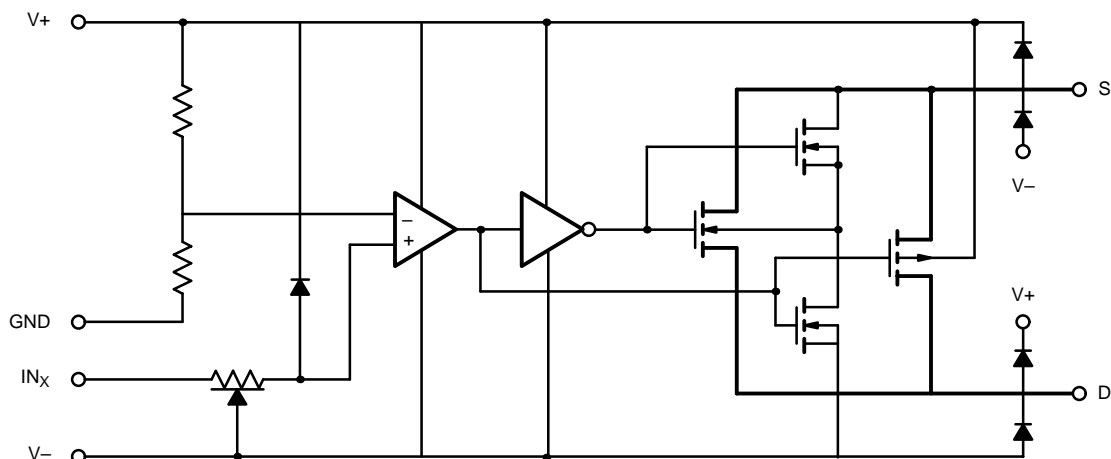


FIGURE 1.

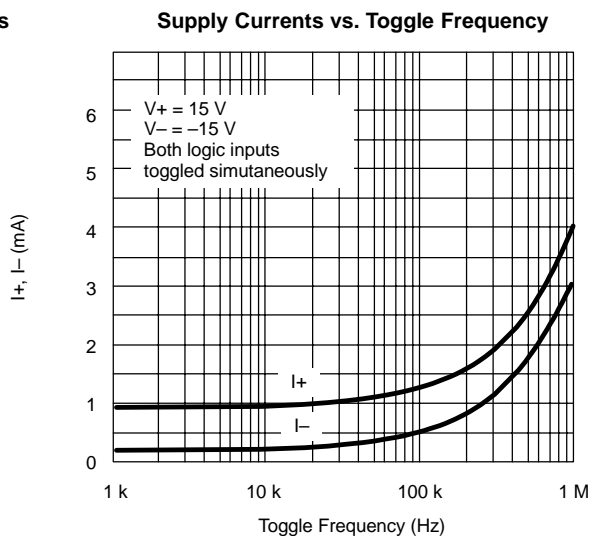
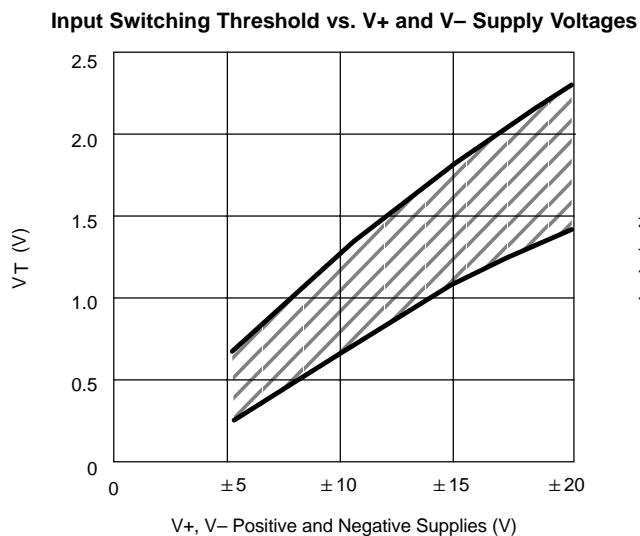
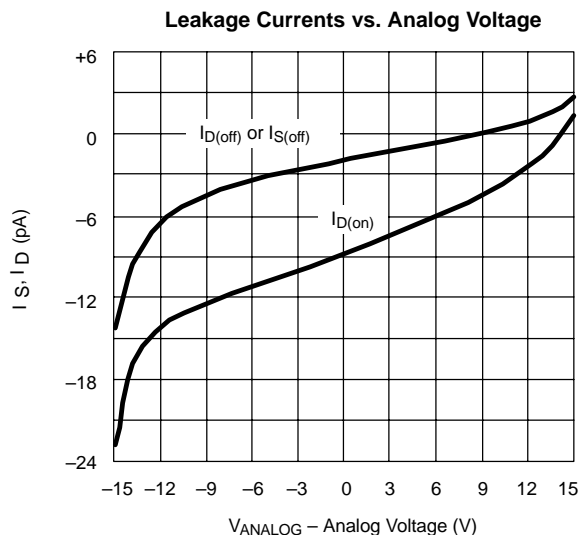
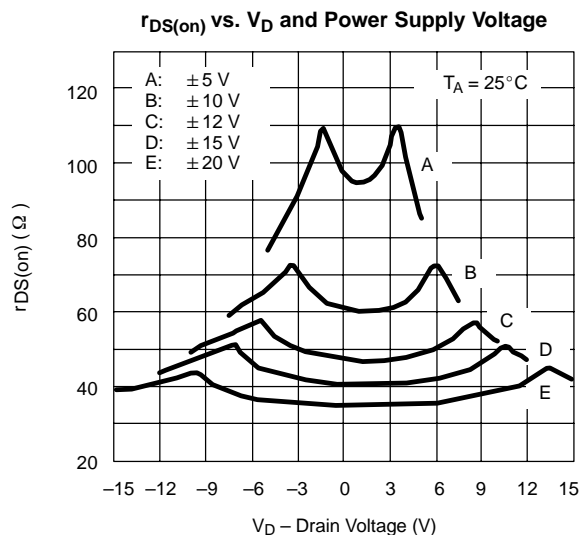


SPECIFICATIONS ^a							
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp ^b	Limits -55 to 125°C			Unit
				Min ^c	Typ ^d	Max ^c	
Analog Switch							
Analog Signal Range ^e	V_{ANALOG}		Full	-15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_D = \pm 10\text{ V}, I_S = -1\text{ mA}$	Room Full		45	70 100	Ω
Source Off Leakage Current	$I_{S(off)}$	$V_S = \pm 14\text{ V}, V_D = \mp 14\text{ V}$	Room Full	-2 -100	± 0.01	2 100	nA
Drain Off Leakage Current	$I_{D(off)}$	$V_D = \pm 14\text{ V}, V_S = \mp 14\text{ V}$	Room Full	-2 -100	± 0.01	2 100	
Channel On Leakage Current ^f	$I_{D(on)}$	$V_S = V_D = \pm 14\text{ V}$	Room Full	-2 -200	± 0.1	2 200	
Digital Control							
Input Current with Input Voltage High	I_{INH}	$V_{IN} = 2.4\text{ V}$	Room Full	-0.5 -1	0.0009		μA
		$V_{IN} = 15\text{ V}$	Room Full		0.005	0.5 1	
Input Current with Input Voltage Low	I_{INL}	$V_{IN} = 0\text{ V}$	Room Full	-0.5 -1	-0.0015		
Dynamic Characteristics							
Turn-On Time	t_{ON}	See Switching Time Test Circuit	Room		440	1000	ns
Turn-Off Time	t_{OFF}		Room		340	425	
Charge Injection	Q	$C_L = 1000\text{ pF}, V_g = 0\text{ V}$ $R_g = 0\ \Omega$	Room		-10		pC
Source-Off Capacitance	$C_{S(off)}$	f = 140 kHz $V_{IN} = 5\text{ V}$	Room		9		pF
Drain-Off Capacitance	$C_{D(off)}$		Room		9		
Channel-On Capacitance	$C_{D(on)} + C_{S(on)}$	$V_D = V_S = 0\text{ V}, V_{IN} = 0\text{ V}$	Room		25		
Off Isolation	OIRR	$V_{IN} = 5\text{ V}, R_L = 75\ \Omega$ $V_S = 2\text{ V}, f = 1\text{ MHz}$	Room		75		dB
Crosstalk (Channel-to-Channel)	X_{TALK}		Room		90		
Power Supplies							
Positive Supply Current	I+	Both Channels On or Off $V_{IN} = 0\text{ V and } 2.4\text{ V}$	Room		0.8	2	mA
Negative Supply Current	I-		Room	-1	-0.23		

Notes:

- Refer to PROCESS OPTION FLOWCHART.
- Room = 25°C, Full = as determined by the operating temperature suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



TEST CIRCUITS

V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

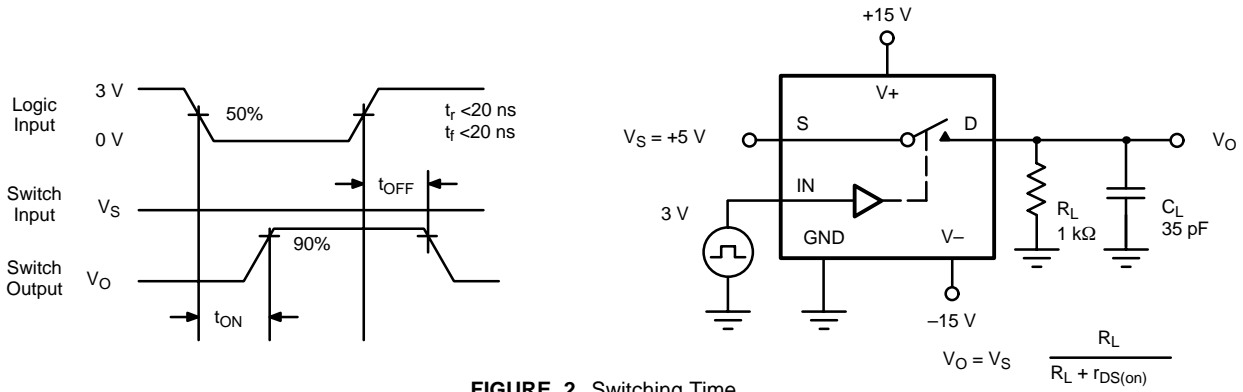


FIGURE 2. Switching Time

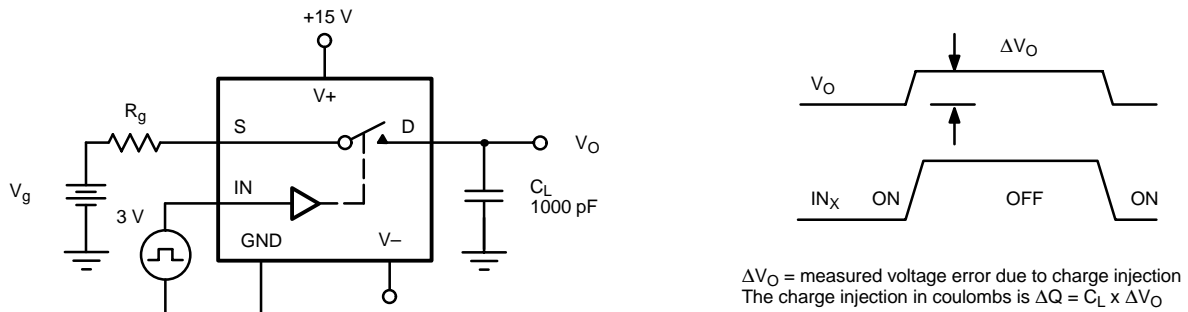


FIGURE 3. Charge Injection

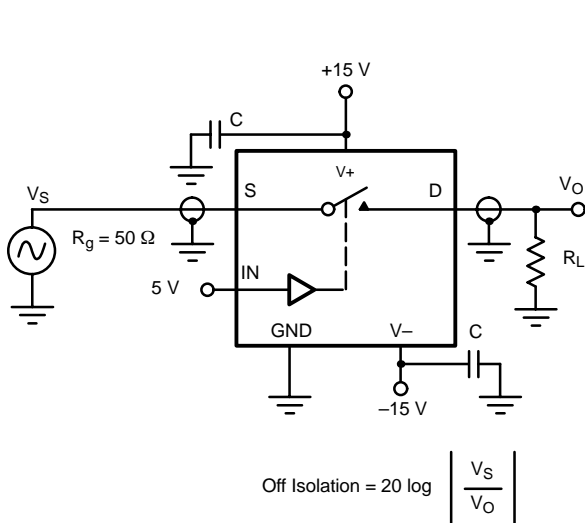


FIGURE 4. Off Isolation

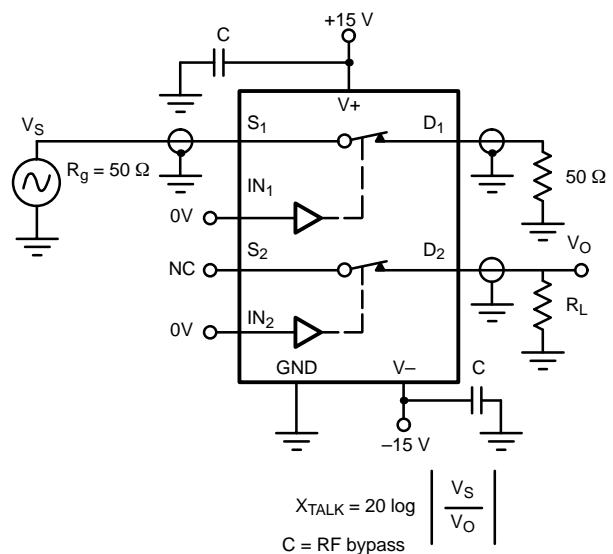


FIGURE 5. Channel-to-Channel Crosstalk



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