24-bit, 192kHz Stereo ADC

DESCRIPTION

The WM8786 is a stereo audio ADC with differential inputs designed for high performance recordable media applications. Data is provided as a PCM output.

Stereo 24-bit multi-bit sigma-delta ADCs are used with digital audio output word lengths of 16 to 32 bits, and sampling rates from 8kHz to 192kHz. The device also has a high pass filter to remove residual DC offsets.

The device is hardware controlled. Pin programming provides access to all features including oversampling rate, audio format, powerdown, master/slave control and digital signal manipulation. The device is supplied in a 20-lead SSOP package.

FEATURES

- SNR 111dB ('A' weighted @ 48kHz)
- THD -102dB (at -0.1dB)
- Sampling Frequency: 8 – 192kHz
- Hardware Control Interface
- Master or Slave Clocking Mode
- Programmable Audio Data Interface Modes
  - I²S, Left, Right Justified or DSP
  - 24-Bit Word Length
- Supply Voltages
  - Analogue 4.5 to 5.5V
  - Digital core: 2.7V to 3.6V
- 20-lead SSOP package

APPLICATIONS

- Recordable DVD Players
- Personal Video Recorders
- High End Sound Cards
- Studio Audio Processing Equipment

BLOCK DIAGRAM

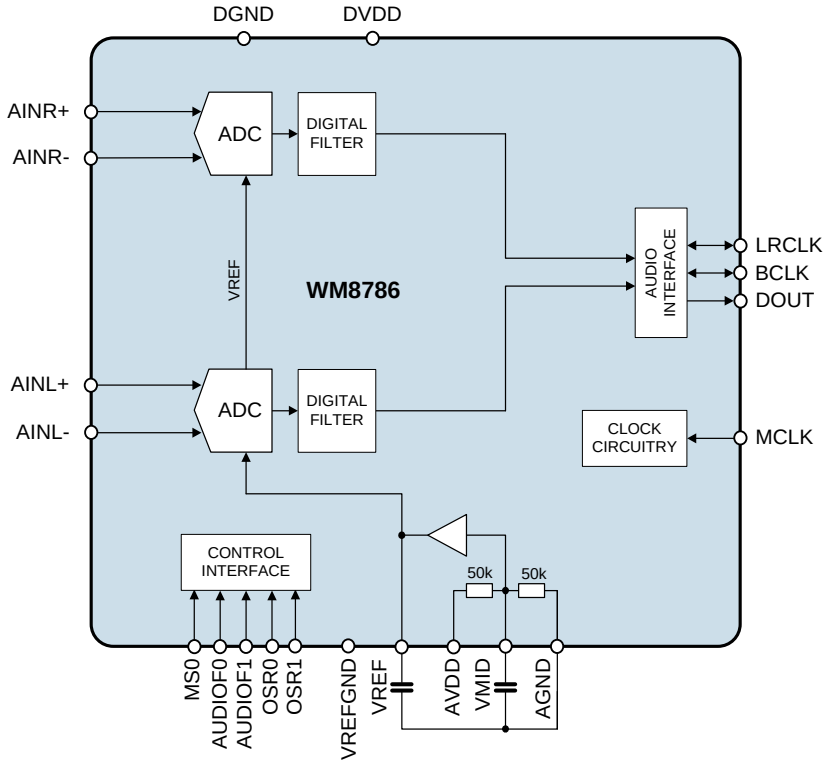
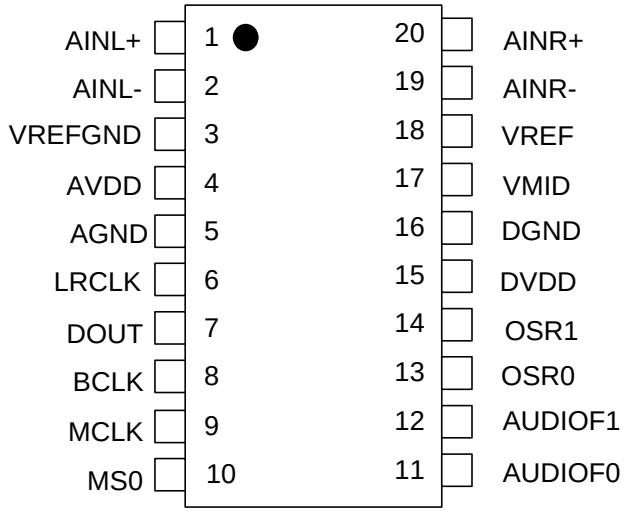


TABLE OF CONTENTS

PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8786GEDS/V	-40°C to +85°C	20-lead SSOP (Pb-free)	MSL3	260ºC
WM8786GEDS/RV	-40°C to +85°C	20-lead SSOP, (Pb-free, tape and reel)	MSL3	260ºC

Note:

Reel quantity = 2,000

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	AINL+	Analogue Input	Left Channel Positive Input
2	AINL-	Analogue Input	Left Channel Negative Input
3	VREFGND	Analogue Reference	Negative Reference Connection
4	AVDD	Supply	Analogue Supply
5	AGND	Supply	Analogue Ground (return path for AVDD)
6	LRCLK	Digital Input / Output	Audio Interface Left / Right Clock
7	DOUT	Digital Output	ADC Digital Audio Data
8	BCLK	Digital Input / Output	Audio Interface Bit Clock
9	MCLK	Digital Input	Master Clock
10	MS0 (pull down pad)	Digital Input	Master/Slave Control 0 = Slave Mode Audio Interface 1 = Master Mode Audio Interface @ 256fs (or @128fs in quad rate)
11	AUDIOF0	Digital Input	Audio Format Selection 00 = 24 bit right justified audio data format 01 = 24 bit left audio data format 10 = I^2S audio data format 11 = DSP audio data format
12	AUDIOF1	Digital Input	
13	OSR0 (pull down pad)	Digital Input	Oversampling Rate Control 00 = Single rate (48kHz) 01 = Dual rate (96kHz) 10 = Quad rate (192kHz) 11 = Not valid
14	OSR1	Digital Input	
15	DVDD	Supply	Digital Supply
16	DGND	Supply	Digital Ground (return path for DVDD)
17	VMID	Analogue Output	Midrail Voltage Decoupling Capacitor
18	VREF	Analogue Reference	Reference Voltage Decoupling Capacitor
19	AINR-	Analogue Input	Right Channel Negative Input
20	AINR+	Analogue Input	Right Channel Positive Input

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+3.63V
Analogue supply voltage	-0.3V	+7V
Voltage range digital inputs	DGND -0.3V	DVDD + 0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Master Clock Frequency		40MHz
Operating temperature range, T_A	-40°C	+85°C
Storage temperature after soldering	-65°C	+150°C

Notes

1. Analogue and digital grounds must always be within 0.3V of each other.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		2.7		3.6	V
Analogue supply range	AVDD		4.5		5.5	V
Ground	DGND,AGND			0		V

ELECTRICAL CHARACTERISTICS

Test Conditions

DVDD = 3.3V, AVDD = 5.0V, T_A = +25°C,
1kHz signal, A-weighted, fs = 48kHz, MCLK = 256fs, 24-bit audio data, Slave Mode unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Performance						
Full Scale Input Signal Level (for ADC 0dB Input)				2.0		V_{rms}
Input resistance				10		kΩ
Input capacitance				10		pF
Signal to Noise Ratio	SNR	A-weighted, @ fs = 48kHz	102	111		dB
		Unweighted, @ fs = 48kHz		108		
Signal to Noise Ratio	SNR	A-weighted, @ fs = 96kHz		111		dB
		Unweighted, @ fs = 96kHz		108		
Signal to Noise Ratio	SNR	A-weighted, @ fs = 192kHz		111		dB
		Unweighted, @ fs = 192kHz		108		
Total Harmonic Distortion	THD	1kHz, -0.1dB Full Scale @ fs = 48kHz		-102	-92	dB
		1kHz, -0.1dB Full Scale @ fs = 96kHz		-102		
		1kHz, -0.1dB Full Scale @ fs = 192kHz		-102		
Total Harmonic Distortion	THD	1kHz, -0.1dB Full Scale @ fs = 48kHz		0.0008	0.0025	%
		1kHz, -0.1dB Full Scale @ fs = 96kHz		0.0008		
		1kHz, -0.1dB Full Scale @ fs = 192kHz		0.0008		
Dynamic Range	DNR	-60dBFS	102	111		dB
Channel Level Matching		20kHz signal		0.1		dB
Power Supply Rejection Ratio (AVDD, DVDD)	PSRR	100mV (peak-peak) 1kHz		50		dB
		100mV (peak-peak) 20Hz to 20kHz		45		
Digital Logic Levels (CMOS Levels)						
Input LOW level	V_{IL}				0.3 x DVDD	V
Input HIGH level	V_{IH}		0.7 x DVDD			V
Input leakage current			-1	±0.2	+1	µA
Input capacitance				5		pF
Output LOW	V_{OL}	I_{OL}=-1mA			0.1 x DVDD	V
Output HIGH	V_{OH}	I_{OH}= 1mA	0.9 x DVDD			V
Analogue Reference Levels						
Midrail Reference Voltage	VMID	AVDD to VMID and VMID to VREFGND	–3%	AVDD/2	+3%	V
Potential Divider Resistance	R_{VMID}	AVDD to VMID and VMID to GND		50		kΩ
Buffered Reference Voltage	VREF		–3%	0.8 x AVDD	+3%	V

Test Conditions

DVDD = 3.3V, AVDD = 5.0V, T_A = +25°C,
1kHz signal, A-weighted, fs = 48kHz, MCLK = 256fs, 24-bit audio data, Slave Mode unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current						
Analogue supply current				27		mA
Digital supply current				5		mA
Power Down				22		uA

Note:

1. The VMID and VREF pins should be decoupled with a 10µF electrolytic capacitor (ESR < 1.5Ω across all operating temperatures) and a 0.1µF ceramic capacitor. Device operation with other decoupling is not recommended, and may affect performance.

TERMINOLOGY

1. Signal-to-noise ratio (dB) – Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, over a 20Hz to 20kHz bandwidth. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
5. All performance measurements are done with a 20kHz low pass filter, and where noted an A-weight filter, except where noted. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although this is not audible, it may affect dynamic specification values.

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

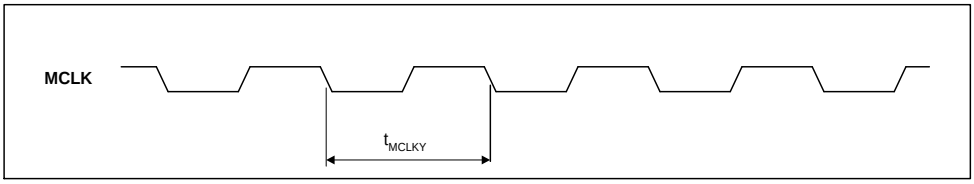


Figure 1 System Clock Timing Requirements

Test Conditions

DVDD = 3.3V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
System Clock Timing Information					
MCLK System clock cycle time	T_{MCLKY}	25			ns
MCLK duty cycle	T_{MCLKDS}	60:40		40:60	

AUDIO INTERFACE TIMING – MASTER MODE, PCM DATA

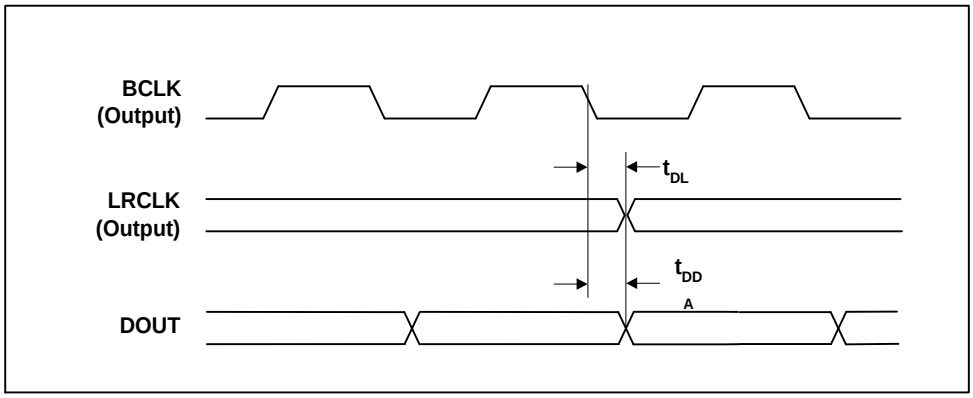


Figure 2 Digital Audio Data Timing – Master Mode (see Control Interface)

Test Conditions

DVDD = 3.3V, DGND = 0V, T_A = +25°C, Master Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
LRCLK propagation delay from BCLK falling edge	t_{DL}	0		10	ns
DOUT propagation delay from BCLK falling edge	t_{DDA}	0		11	ns

AUDIO INTERFACE TIMING – SLAVE MODE, PCM DATA

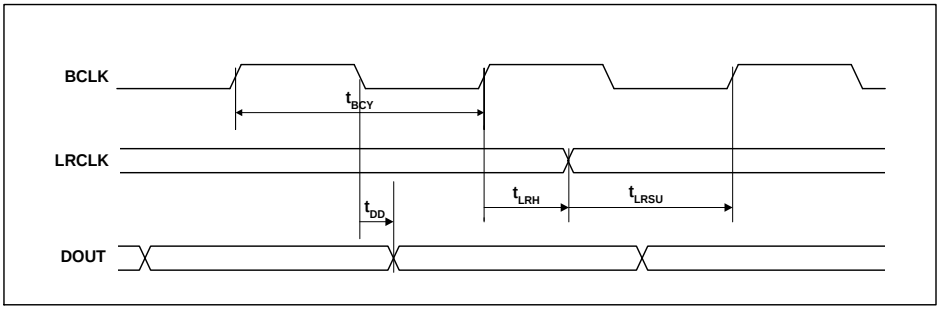


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

DVDD = 3.3V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	t_{BCY}	25			ns
LRCLK set-up time to BCLK rising edge	t_{LRSU}	10			ns
LRCLK hold time from BCLK rising edge	t_{LRH}	10			ns
DOUT propagation delay from BCLK falling edge	t_{DD}	0		11	ns

POWER-ON RESET

The WM8786 has an internal power-on reset circuit. The reset sequence is entered at power-on or power-up (DVDD). Until the internal reset is removed, DOUT is forced to zero. DOUT remains zero for a count equal to 32 sample clocks, after power up. (This count is driven by MCLK and is independent of any external LRCLK).

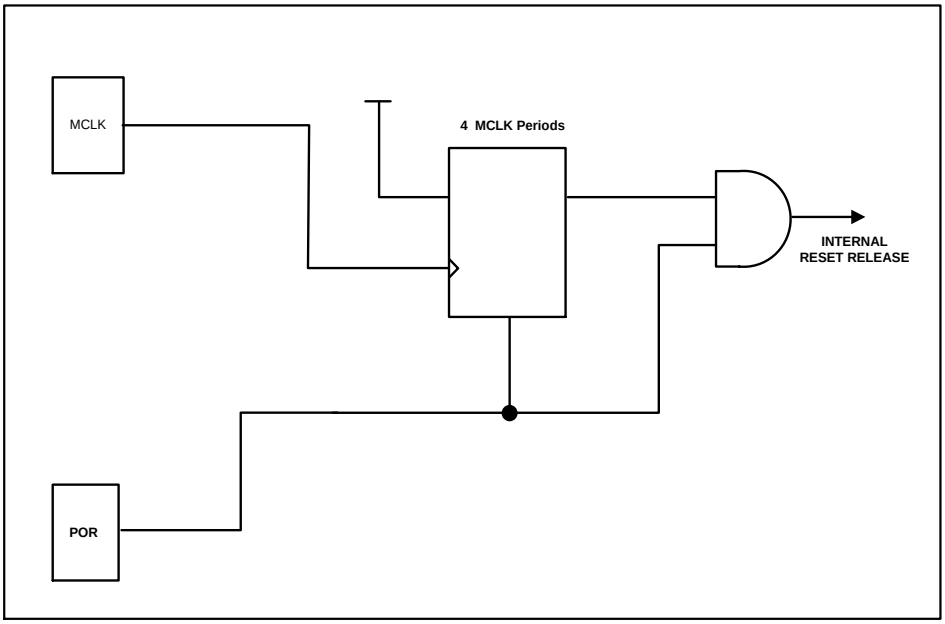


Figure 4 POR Circuit

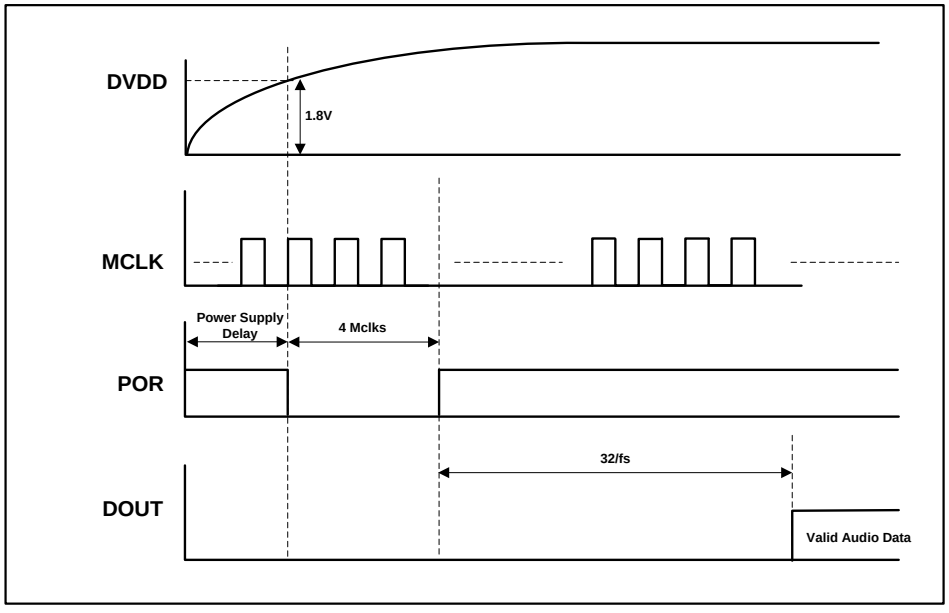


Figure 5 POR Timing

DIGITAL FILTER CHARACTERISTICS

The WM8786 digital filter characteristics scale with sample rate.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Sample Rate (Single Rate - 48Hz typically)					
Passband	+/- 0.005dB	0		0.454fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.005	dB
Stopband		0.546fs			
Stopband Attenuation	f > 0.546fs	-85			dB
Group Delay			32/fs		s
ADC Sample Rate (Dual Rate - 96kHz typically)					
Passband	+/- 0.005dB	0		0.454fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.005	dB
Stopband		0.546fs			
Stopband Attenuation	f > 0.546fs	-85			dB
Group Delay			32/fs		s
ADC Sample Rate (Quad Rate - 192kHz typically)					
Passband	+/- 0.005dB	0		0.25fs	
	-3dB		0.45fs		
	-6dB		0.5fs		
Passband Ripple				+/- 0.005	dB
Stopband		0.75fs			
Stopband Attenuation	f > 0.75fs	-85			dB
Group Delay			10/fs		s
ADC High Pass Filter					
Corner Frequency	-3dB		3.7		Hz
	-0.5dB		10.4		
	-0.1dB		21.6		

Table 1 Digital Filter Characteristics

TERMINOLOGY

1. Stop Band Attenuation (dB) - the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region

HIGH PASS FILTER TRANSFER CHARACTERISTIC

The high pass filter response is defined by the following polynomial:

$$H(z) = \frac{1 - z^{-1}}{1 - (1 - \alpha)z^{-1}}$$

where $\alpha = 2^{-11}$ for single rate (48k) mode

$\alpha = 2^{-12}$ for dual rate (96k) mode

$\alpha = 2^{-13}$ for quad rate (192k) mode

FILTER RESPONSES

SINGLE RATE 48K

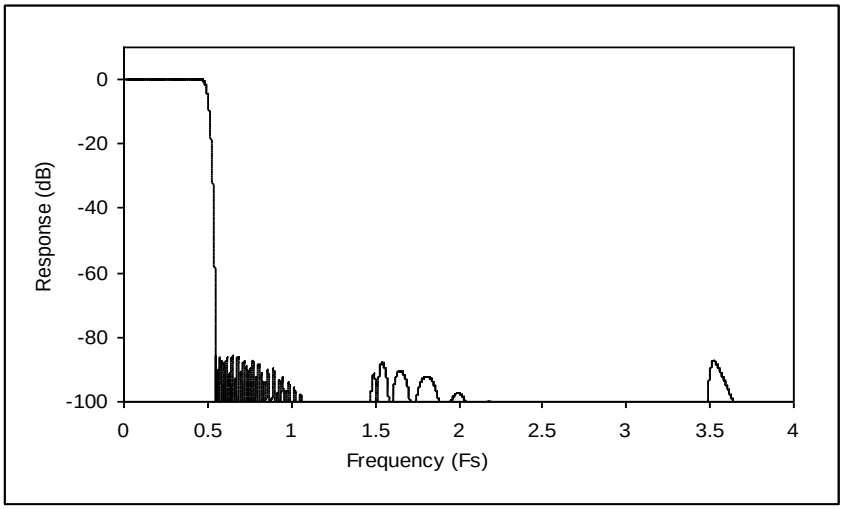


Figure 6 Single Rate 48k Filter Response

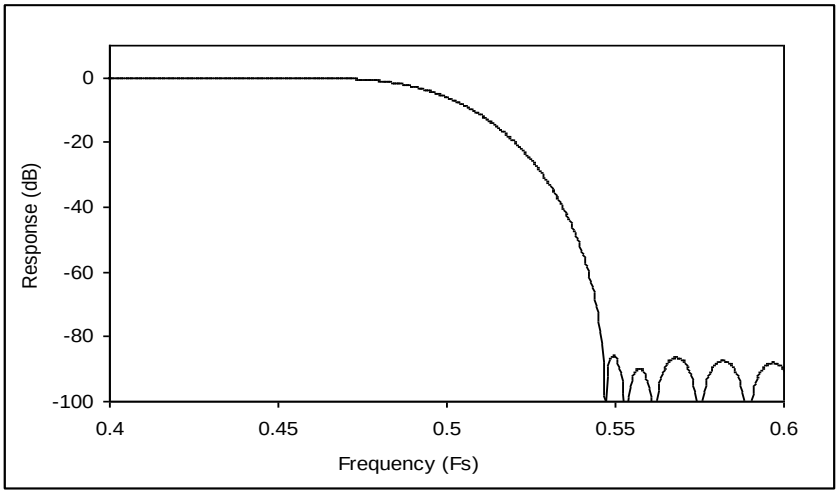


Figure 7 Single Rate 48k Filter Response

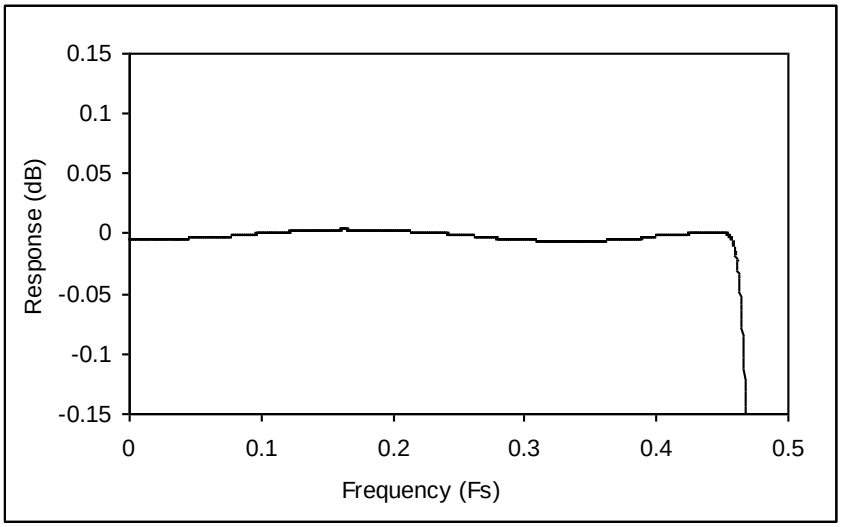


Figure 8 Single Rate 48k Filter Response

DUAL RATE 96K

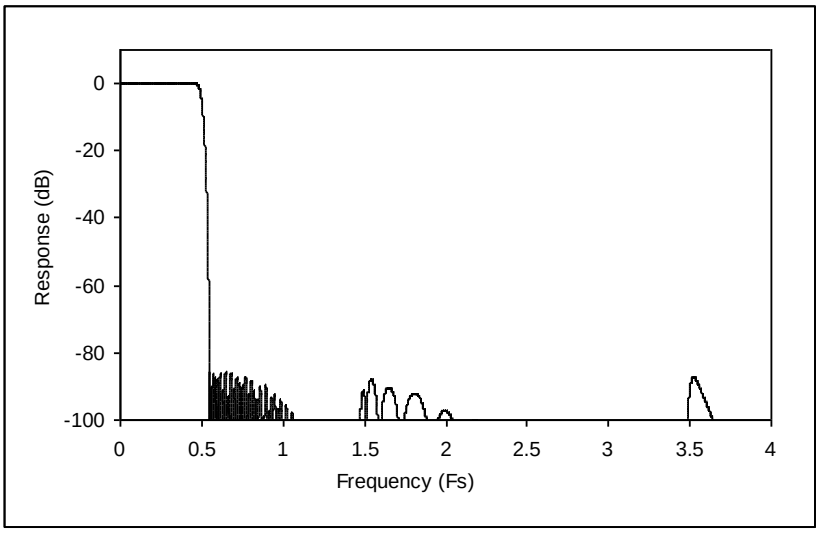


Figure 9 Dual Rate 96k Filter Response

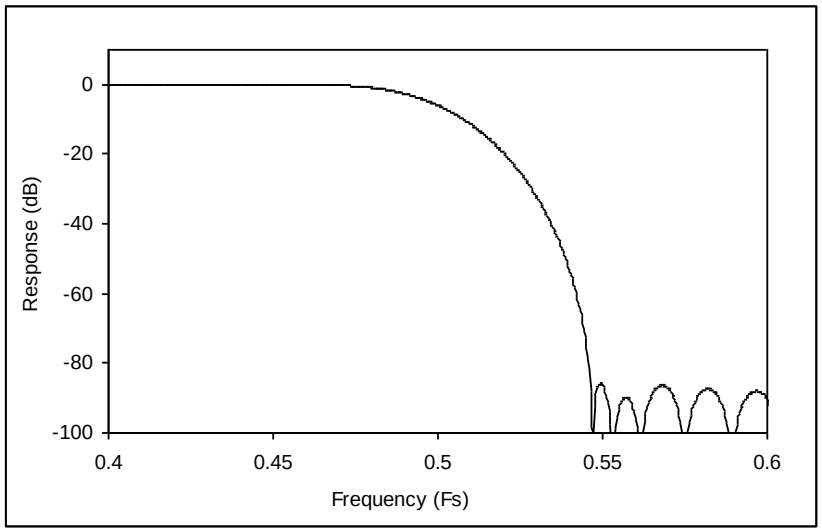


Figure 10 Dual Rate 96k Filter Response

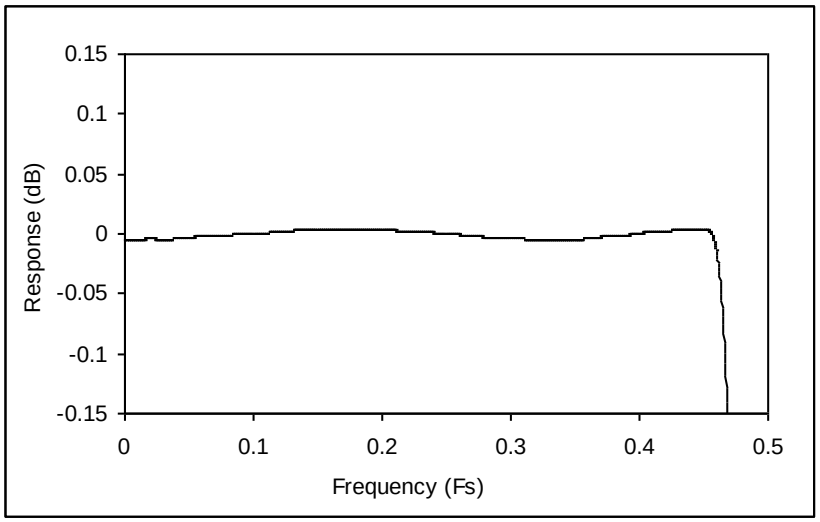


Figure 11 Dual Rate 96k Filter Response

QUAD RATE 192K

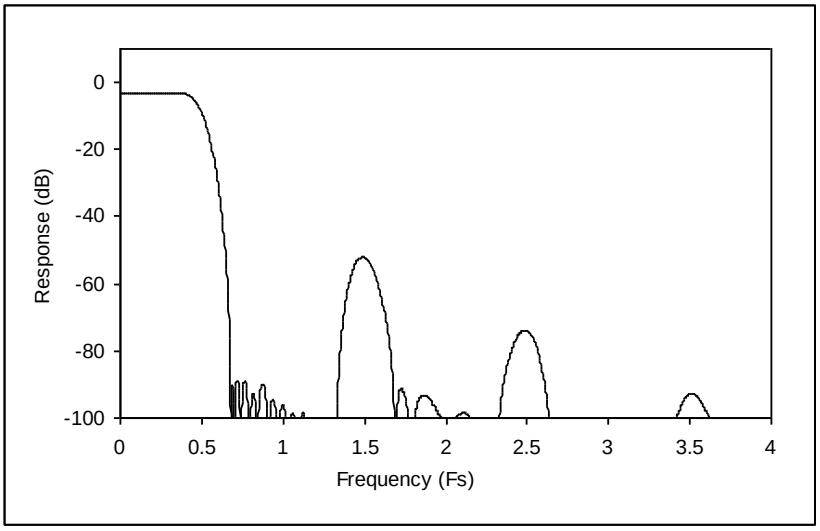


Figure 12 Quad Rate 192k Filter Response

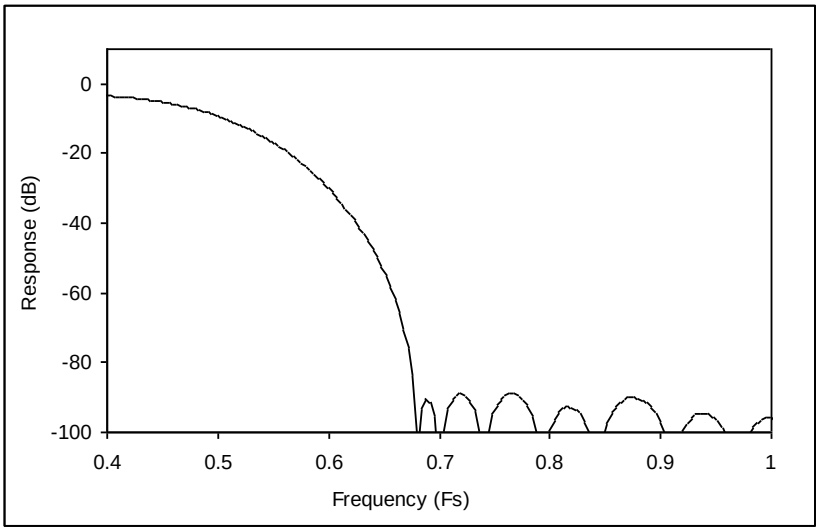


Figure 13 Quad Rate 192k Filter Response

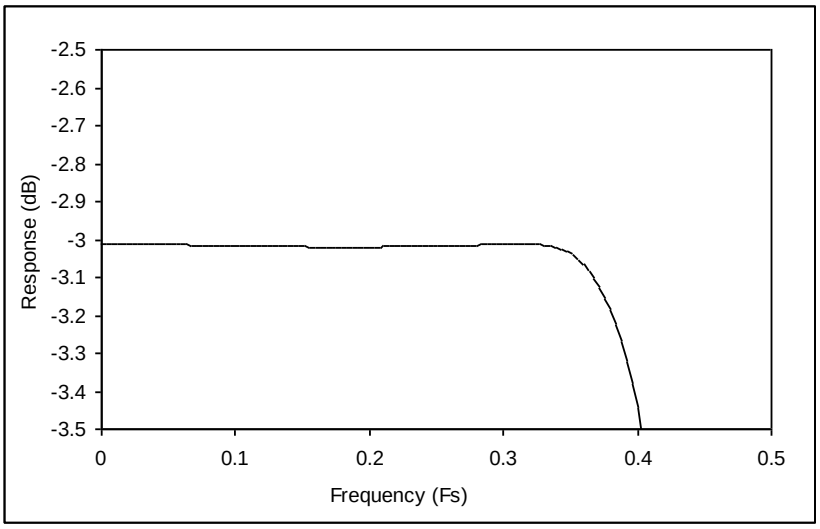


Figure 14 Quad Rate 192k Filter Response

HIGH PASS FILTER

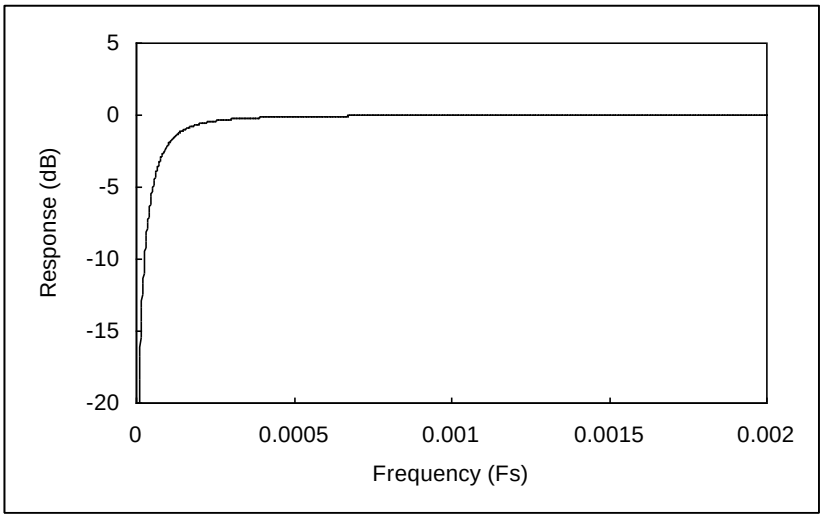


Figure 15 Single Rate 48k High Pass Filter Response

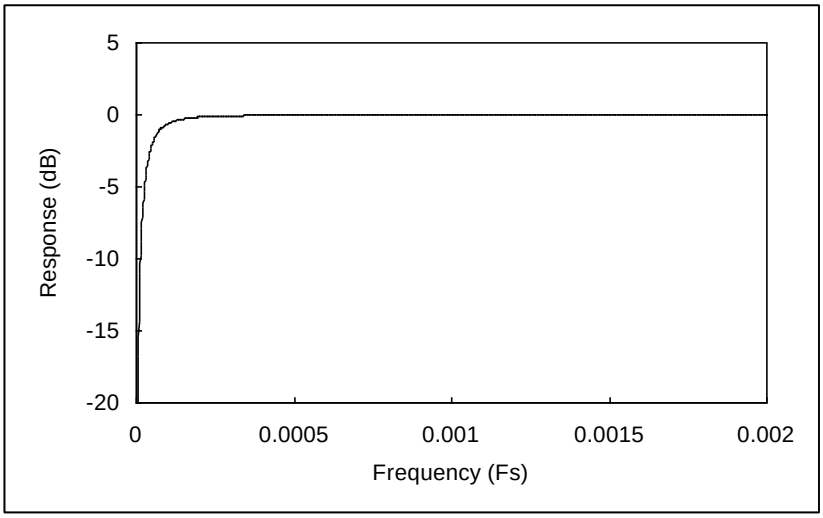


Figure 16 Dual Rate 96k High Pass Filter Response

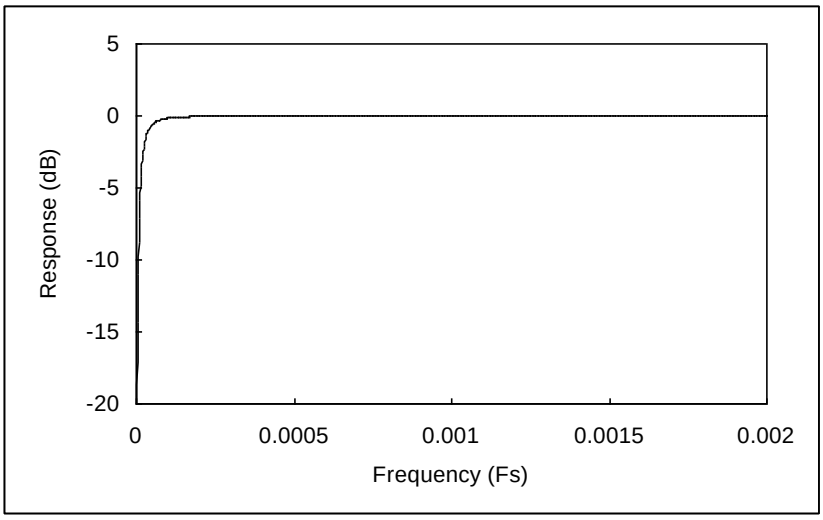


Figure 17 Quad Rate 192k High Pass Filter Response

DEVICE DESCRIPTION

INTRODUCTION

The WM8786 is a high performance stereo audio ADC designed for demanding recording applications such as DVD recorders, studio mixers, PVRs, and AV amplifiers. The WM8786 consists of stereo line level inputs, followed by a sigma-delta modulator and digital filtering.

The WM8786 uses a multi-bit high-order oversampling architecture delivering high SNR operating at oversampling ratios from 128fs to 32fs according to the sample rate. Sample rates from 8kHz to 192kHz are supported. The WM8786 supports master clock rates from 128fs to 768fs.

The digital filter is a high performance linear phase FIR filter. The digital filters are optimised for each sample rate. Also included is a high pass filter to remove residual DC offsets from the input signal.

The output from the ADC is available on a configurable digital audio interface. It supports a number of audio data formats including I^2S, Left justified and Right justified or DSP, and can operate in master or slave modes.

The WM8786 functionality is controlled in hardware via specific pins. It is fully compatible and an ideal partner for a range of industry standard microprocessors, controllers and DSPs.

The WM8786 can be powered down to reduce system power consumption.

DIGITAL AUDIO INTERFACE

The digital audio interface uses three pins:

- DOUT: ADC data output
- LRCLK: ADC data alignment clock
- BCLK: Bit clock, for synchronisation

The digital audio interface takes the data from the internal ADC digital filters and places it on DOUT and LRCLK. DOUT is the formatted digital audio data stream output from the ADC digital filters with left and right channels multiplexed together. LRCLK is an alignment clock that controls whether Left or Right channel data is present on the DOUT line. DOUT and LRCLK are synchronous with the BCLK signal with each data bit transition signified by a BCLK high to low transition. DOUT is always an output. BCLK and LRCLK may be inputs or outputs, depending whether the device is in Master or Slave mode (see Master and Slave Mode Operation, below).

Four different audio data formats are supported:

- Left justified
- Right justified
- I^2S
- DSP

The data formats are described in Audio Data Formats, below. Refer to the Signal Timing Requirements section for timing information.

MASTER AND SLAVE MODE OPERATION

The WM8786 can be configured as either a master or slave mode device. As a master device the WM8786 generates BCLK and LRCLK and thus controls sequencing of the data transfer on DOUT. In slave mode, the WM8786 responds with data to clocks it receives over the digital audio interface. The mode can be selected using the MS0 pin. Master and slave modes are illustrated below.

MS0 PIN STATUS	INTERFACE FORMAT
Low	Slave
High	Master (@256fs in oversampling ratio = single or dual rate)
High	Master (@192fs in oversampling ratio = quad rate)

Table 2 Control Interface Mode Selection

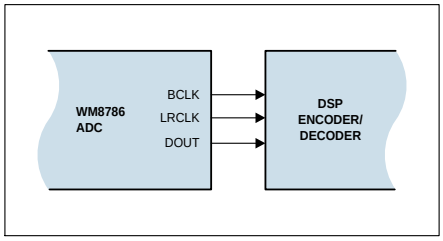


Figure 18a Master Mode

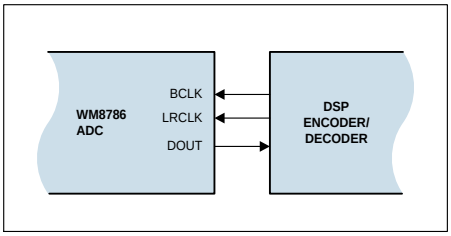


Figure 18b Slave Mode

AUDIO DATA FORMATS

In Left Justified mode, the MSB is available on the first rising edge of BCLK following an LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.

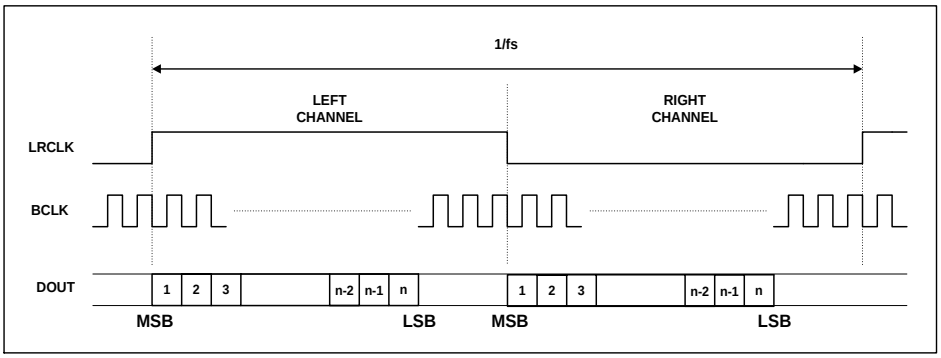


Figure 19 Left Justified Audio Interface (assuming n-bit word length)

In Right Justified mode, the LSB is available on the last rising edge of BCLK before an LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition.

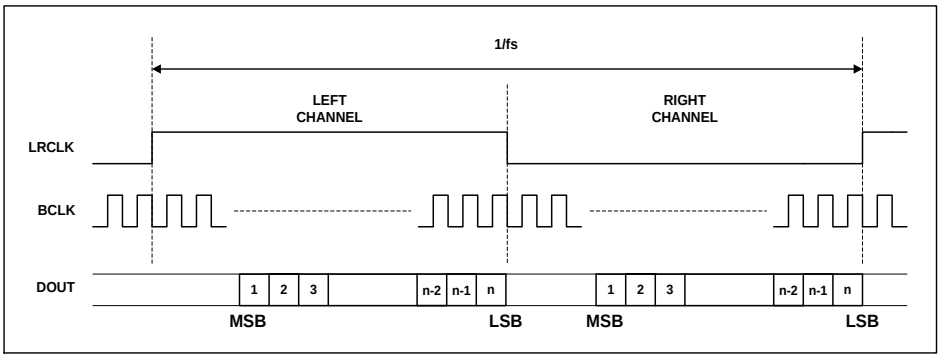


Figure 20 Right Justified Audio Interface (assuming n-bit word length)

In I^2S mode, the MSB is available on the second rising edge of BCLK following an LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

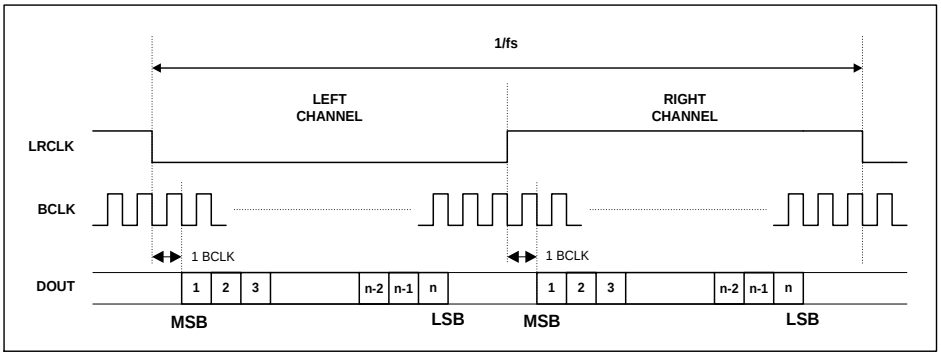


Figure 21 I²S Justified Audio Interface (assuming n-bit word length)

In DSP/PCM mode, the left channel MSB is available on the 2nd rising edge of BCLK following a rising edge of LRC. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In device master mode, the LRC output will resemble the frame pulse shown in Figure 22. In device slave mode, shown in Figure 23 it is possible to use any length of frame pulse less than 1/fs, providing the falling edge of the frame pulse occurs greater than one BCLK period before the rising edge of the next frame pulse.

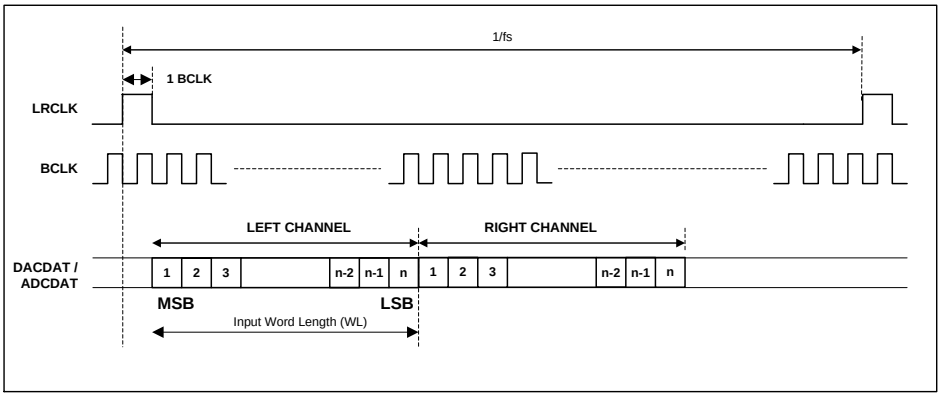


Figure 22 DSP/PCM Mode Audio Interface (mode A, Master)

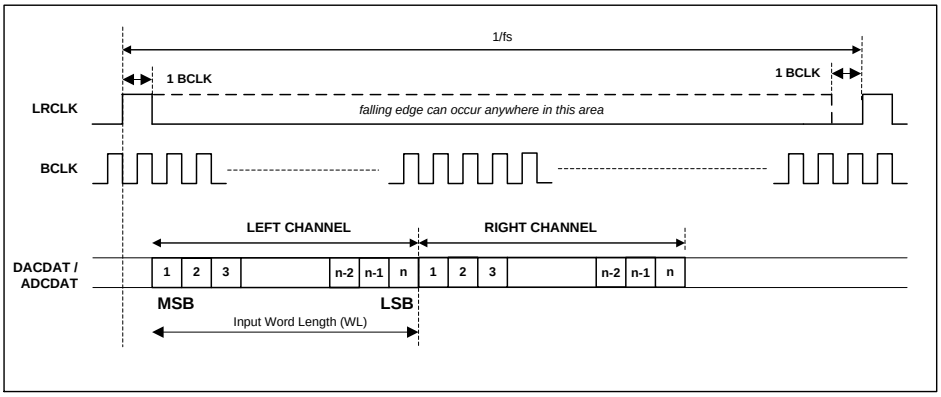


Figure 23 DSP/PCM Mode Audio Interface (mode A, Slave)

AUDIO INTERFACE CONTROL

The audio interface is controlled using the AUDIOF0 and AUDIOF1 pins. Dynamically changing the audio format may cause erroneous operation of the interfaces and is therefore not recommended.

All ADC data is signed 2's complement. The length of the digital audio data is always 24 bits.

AUDIOF1 PIN STATUS	AUDIOF0 PIN STATUS	AUDIO INTERFACE FORMAT
Low	Low	24-bit right justified
Low	High	24-bit left justified
High	Low	24-bit I^2S
High	High	24-bit DSP

Table 3 Audio Interface Format Selection

OVERSAMPLING RATIOS AND SIGMA-DELTA MODULATOR FREQUENCY

For correct operation of the device and optimal performance, the user must select the appropriate ADC modulator oversampling ratio. The oversampling ratio is selected using the OSR0 and OSR1 pins.

OSR1 PIN STATUS	OSR0 PIN STATUS	OVERSAMPLING RATIO CONTROL
Low	Low	Single Rate (128fs)
Low	High	Dual Rate (64fs)
High	Low	Quad Rate (32fs)
High	High	Not Valid

Table 4 Oversampling Ratio Selection

The WM8786 can operate at sample rates from 8kHz to 192kHz. The WM8786 uses a sigma-delta modulator that operates at frequencies between 1.024MHz and 6.144MHz

SAMPLING RATE (LRCLK)	OVERSAMPLING RATIO	SIGMA-DELTA MODULATOR FREQUENCY (MHZ)
8kHz	Single Rate (128fs)	1.024
32kHz	Single Rate (128fs)	4.096
44.1kHz	Single Rate (128fs)	5.6448
48kHz	Single Rate (128fs)	6.144
96kHz	Dual Rate (64fs)	6.144
192kHz	Quad Rate (32fs)	6.144

Table 5 Sigma-delta Modulator Frequency

MASTER CLOCK AND AUDIO SAMPLE RATES

The Master clock (MCLK) is used to operate the digital filters and the noise shaping circuits. The WM8786 supports a wide range of master clock frequencies, and can generate many commonly used audio sample rates directly from the master clock. The following tables show the recommended Master clock frequencies for different sample rates.

In Master Mode, with oversampling ratio = single rate or dual rate, Master clock frequency of 256 is supported.

SAMPLING RATE (LRCLK)	OVERSAMPLING RATIO	MASTER CLOCK FREQUENCY (MHz)
		256fs
32kHz	Single Rate	8.192
44.1kHz	Single Rate	11.2896
48kHz	Single Rate	12.288
96kHz	Dual Rate	24.576

Table 6 Master Mode: Recommended Master Clock Frequency Selection

In Master Mode, with oversampling ratio = quad rate, Master clock frequency of 192 is supported.

SAMPLING RATE (LRCLK)	OVERSAMPLING RATIO	MASTER CLOCK FREQUENCY (MHz)
		128fs
192kHz	Quad Rate	24.576

Table 7 Master Mode: Recommended Master Clock Frequency Selection

In Slave Mode, Master clock frequencies of $128f_s$, $192f_s$, $256f_s$, $384f_s$, $512f_s$ and $768f_s$ are supported. The WM8786 automatically detects the audio sample rate, in slave mode.

SAMPLING RATE (LRCLK)	OVERSAMPLING RATIO	MASTER CLOCK FREQUENCY (MHz)					
		128fs	192fs	256fs	384fs	512fs	768fs
32kHz	Single Rate	-	-	8.192	12.288	16.384	24.576
44.1kHz	Single Rate	-	-	11.2896	16.9344	22.5792	33.8688
48kHz	Single Rate	-	-	12.288	18.432	24.576	36.864
96kHz	Dual Rate	-	-	24.576	36.864	-	-
192kHz	Quad Rate	24.576	36.864	-	-	-	-

Table 8 Slave Mode: Recommended Master Clock Frequency Selection

MLCK AND LRCLK PHASE RELATIONSHIP

The WM8786 does not require a specific phase relationship between MLCK and LRCLK. If the relationship between MCLK and LRCLK changes by more than +/-8 BCLKs in a 64 BLCK frame, the WM8786 will attempt to re-synchronise During re-synchronisation, data samples may be dropped or duplicated.

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

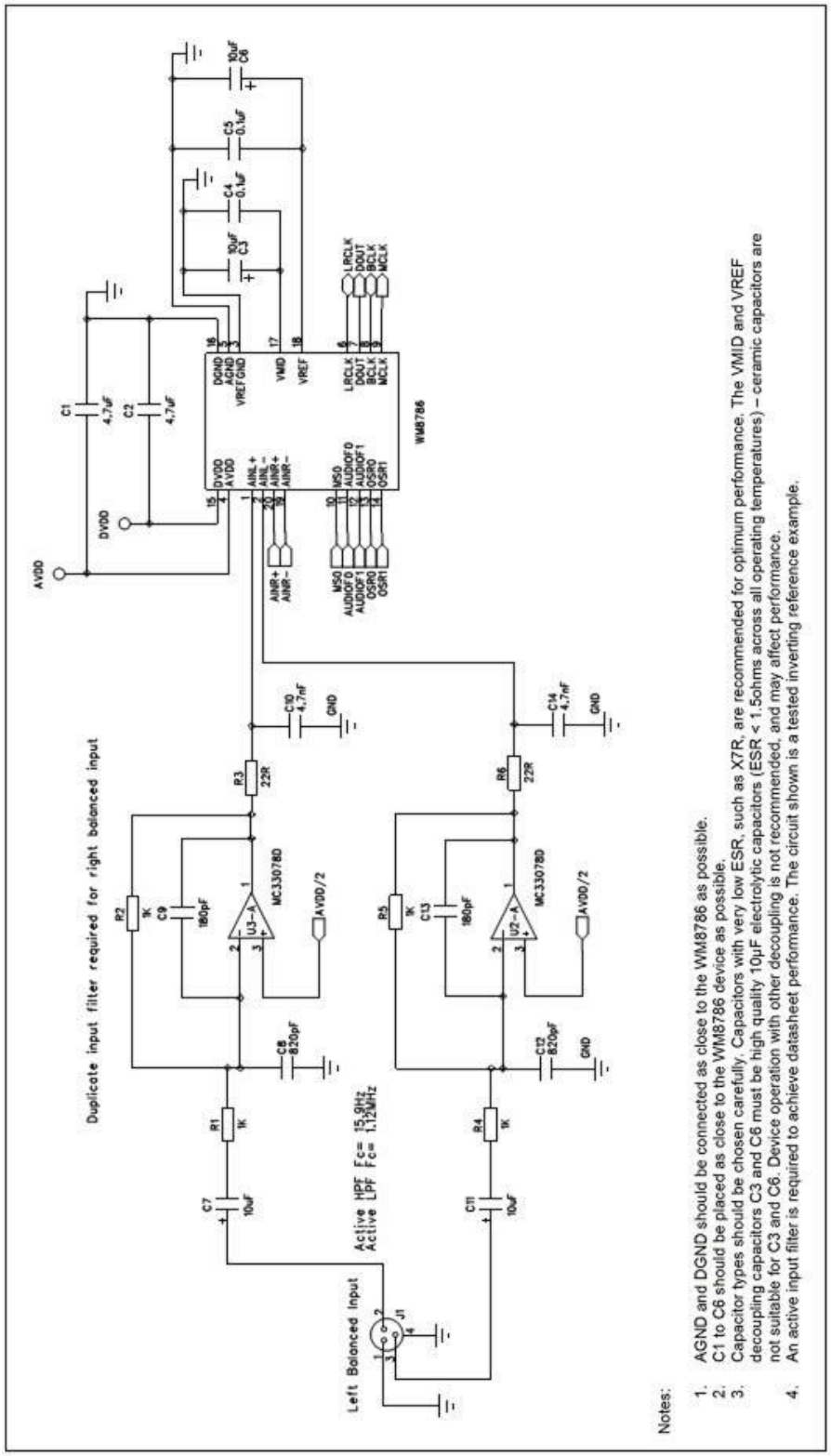


Figure 24 External Component Diagram

RECOMMENDED PCB LAYOUT

The WM8786 is sensitive to the routing of the ground return currents for VREF, VMID, and AVDD; care should be taken to ensure that these currents do not interfere. Figure 25 below shows a recommended PCB layout (with high frequency current paths) for the WM8786 that will demonstrate datasheet performance:

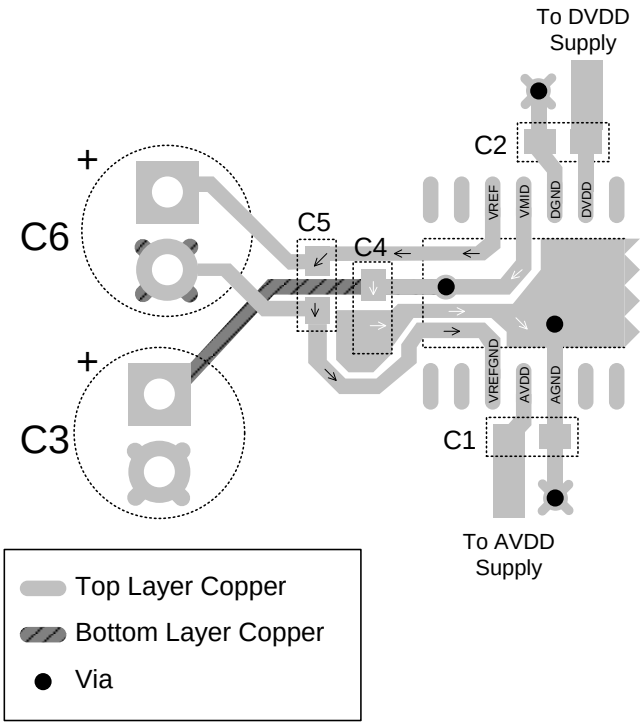


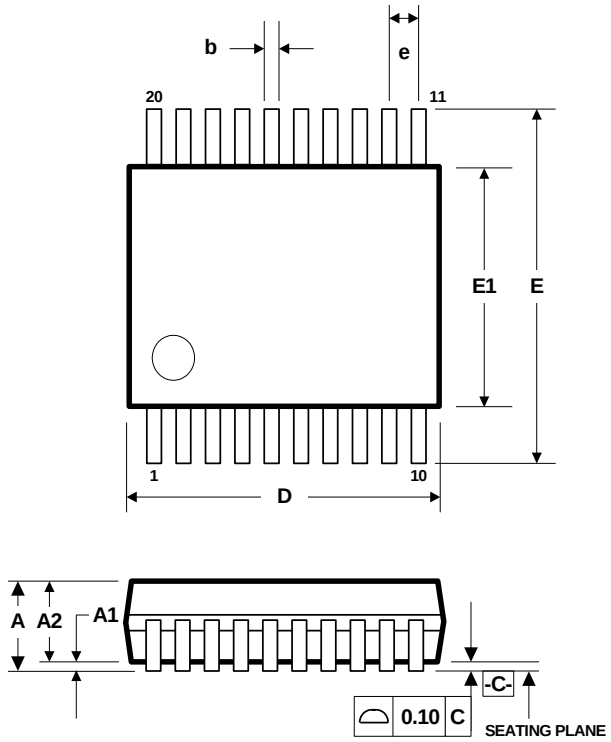
Figure 25 Recommended PCB Layout for VREF, VMID, AVDD and DVDD Decoupling

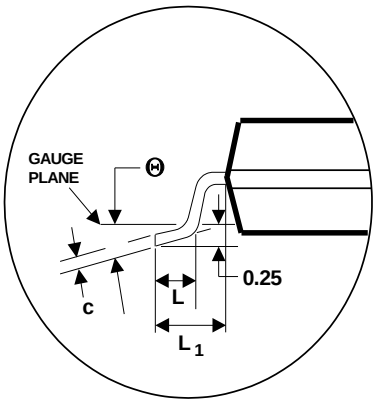
Notes:

1. High frequency noise on VREF is decoupled through C5, and the return path should be directly to VREFGND.
2. The route from the negative terminal of C6 to C5 and then to VREFGND should be made on the top layer only and should not connect to the ground flood on the top layer. This ensures that the VREF return current is returned directly to VREFGND as shown by the black arrows.
3. The negative terminal of C6 should be connected to the ground plane on the underside of the board only.
4. High frequency noise on VMID is decoupled through C4, and the return path should be directly to AGND.
5. Via to bottom layer on VMID used to connect to bottom layer route to positive terminal of C3.
6. The route from C4 to AGND should be made on the top layer only. This ensures that the VMID return current is returned to AGND as shown by the white arrows.
7. AVDD is decoupled to AGND through C1. The ground return currents are not shown in this diagram.
8. DVDD is decoupled to DGND through C2. The ground return currents are not shown in this diagram.
9. DGND should not be connected directly to the ground flood on the top layer under the WM8786. This will ensure that noise in the digital ground does not interfere with the critical routing of VREF and VMID.
10. Bottom layer ground flood not shown for clarity.
11. See the WM8786 Evaluation Board for an example of this layout in use.

PACKAGE DIMENSIONS

DS: 20 PIN SSOP (7.2 x 5.3 x 1.75 mm) **DM0015.C**





Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	2.0
A_1	0.05	-----	-----
A_2	1.65	1.75	1.85
b	0.22	0.30	0.38
c	0.09	-----	0.25
D	6.90	7.20	7.50
e	0.65 BSC		
E	7.40	7.80	8.20
E_1	5.00	5.30	5.60
L	0.55	0.75	0.95
L_1	1.25 REF		
θ	0^o	4^o	8^o
REF:	JEDEC.95, MO-150		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.
D. MEETS JEDEC.95 MO-150, VARIATION = AE. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

IMPORTANT NOTICE

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.

REVISION HISTORY

DATE	REV	DESCRIPTION OF CHANGES	PAGE	CHANGED BY
26/01/15	4.4	Clarifications to external component requirements	7, 23	PH