



Z86193

CMOS Z8[®] MICROCONTROLLER MULTIPLIER/DIVIDER/SEARCH/MERGE

GENERAL DESCRIPTION

The Z86193 is a CMOS ROMless Z8[®] microcontroller enhanced with a hardwired 16-bit x 16-bit multiplier, 32-bit/16-bit divider, three 16-bit counter/timers, search and merge instructions, Evaluation mode and a Bus Request mode. The device is code compatible with other Z8 family devices, yet it offers more powerful mathematical capabilities, data searching capabilities, and bit manipulation. The Z86193 is offered in a 64-pin VQFP package.

The Z86193 provides up to 16 output address lines permitting an address space of up to 64 Kbytes each of Program or Data memory. Eight address outputs are provided by a de-multiplexed 8-bit Address Bus (A7-A0) or by a multiplexed 8-bit Address/Data Bus (AD7-AD0). The remaining eight address lines (A15-A8) can be provided by the software configuration of Port0 to output address.

The Z86193 includes a bus which differs from other Z8 devices. The Z86193 provides bus control signals /RD (Read Strobe), /WR (Write Strobe), and ALE (Address Latch Enable).

There are 464 8-bit registers located on-chip and organized as 444 general-purpose registers, 16 control and status registers, one reserved register, and up to three I/O port registers. The Register File is partitioned into two Register Pages. Page0 contains 208 registers and Page1 contains 208 registers. The 48 other registers are common to both Register Pages. The Register file is also divided into 29 working register groups of 16 registers each. Configuration of the registers in this format allows the use of short format instructions. There are 17 additional registers implemented in the Expanded Register file in Banks D and E. Two of the registers may be used as general-purpose, while the other 15 are used to supply data and control for the multiplier/divider unit and the additional counter/timers.

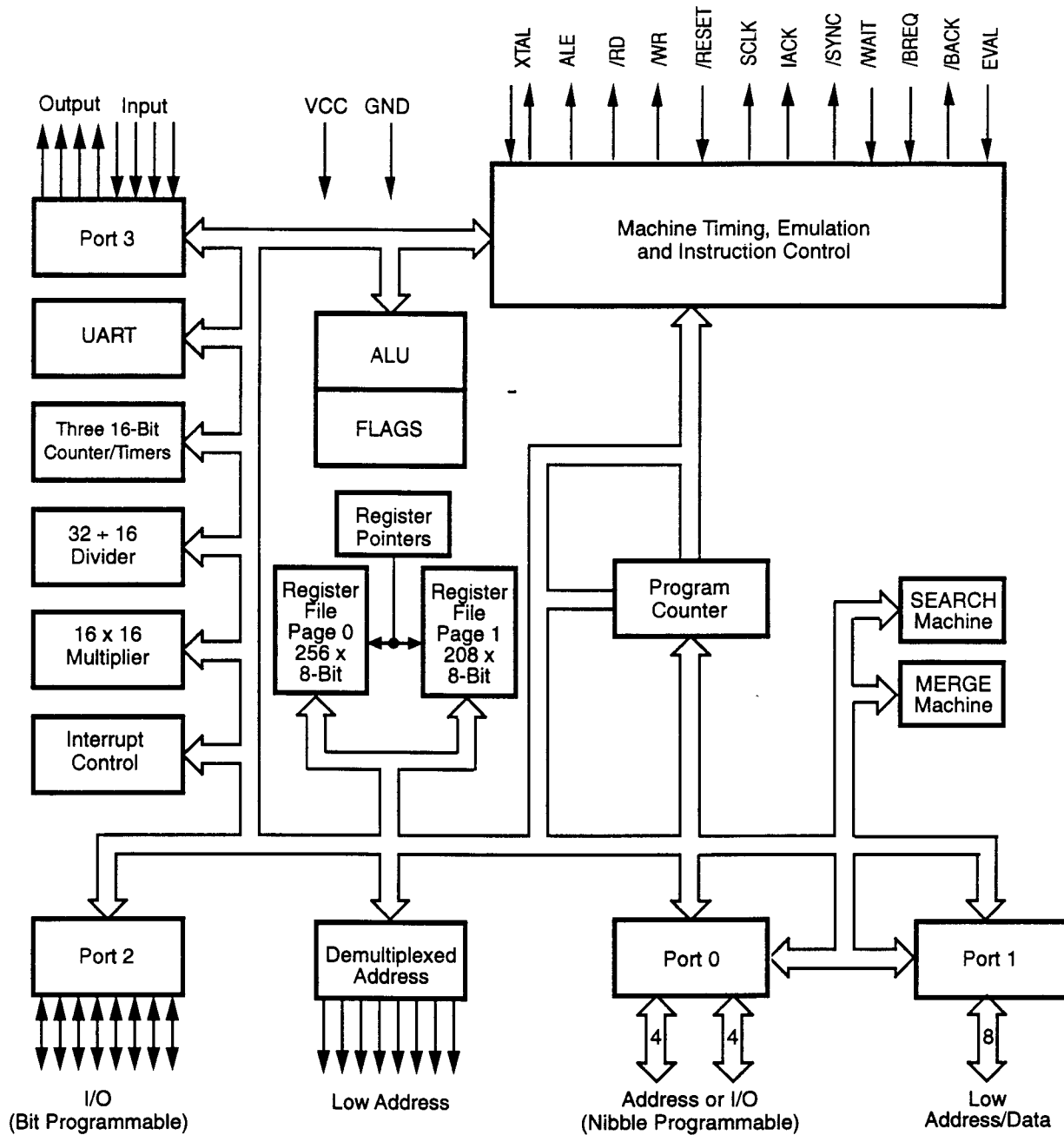
Notes:

All Signals with a preceding front slash, "/", are active Low, e.g.: /B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

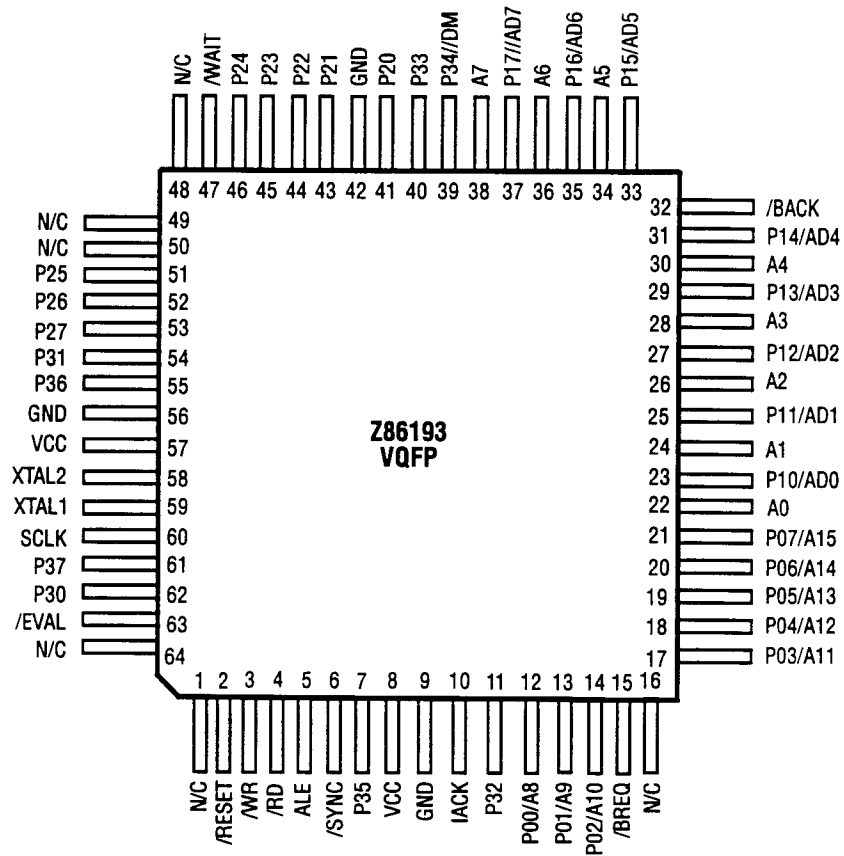
| Connection | Circuit | Device |
|------------|-----------------|-----------------|
| Power | V _{CC} | V _{DD} |
| Ground | GND | V _{SS} |

GENERAL DESCRIPTION (Continued)



Z86193 Functional Block Diagram

PIN CONFIGURATION



64-Pin VQFP Package

ABSOLUTE MAXIMUM RATINGS

| Symbol | Description | Min | Max | Units |
|-----------|-------------------|------|------|-------|
| V_{CC} | Supply Voltage* | -0.3 | +7.0 | V |
| T_{STG} | Storage Temp | -65 | +150 | C |
| T_A | Oper Ambient Temp | † | † | C |

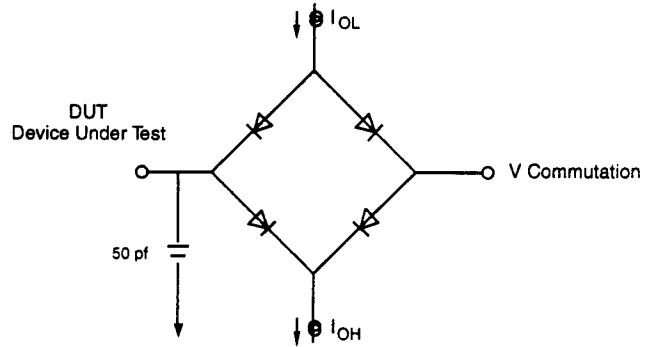
* Voltages on all pins with respect to GND.

† See Ordering Information

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load Diagram).



Test Load Diagram

DC ELECTRICAL CHARACTERISTICS

VCC = 5.0V ± 10%

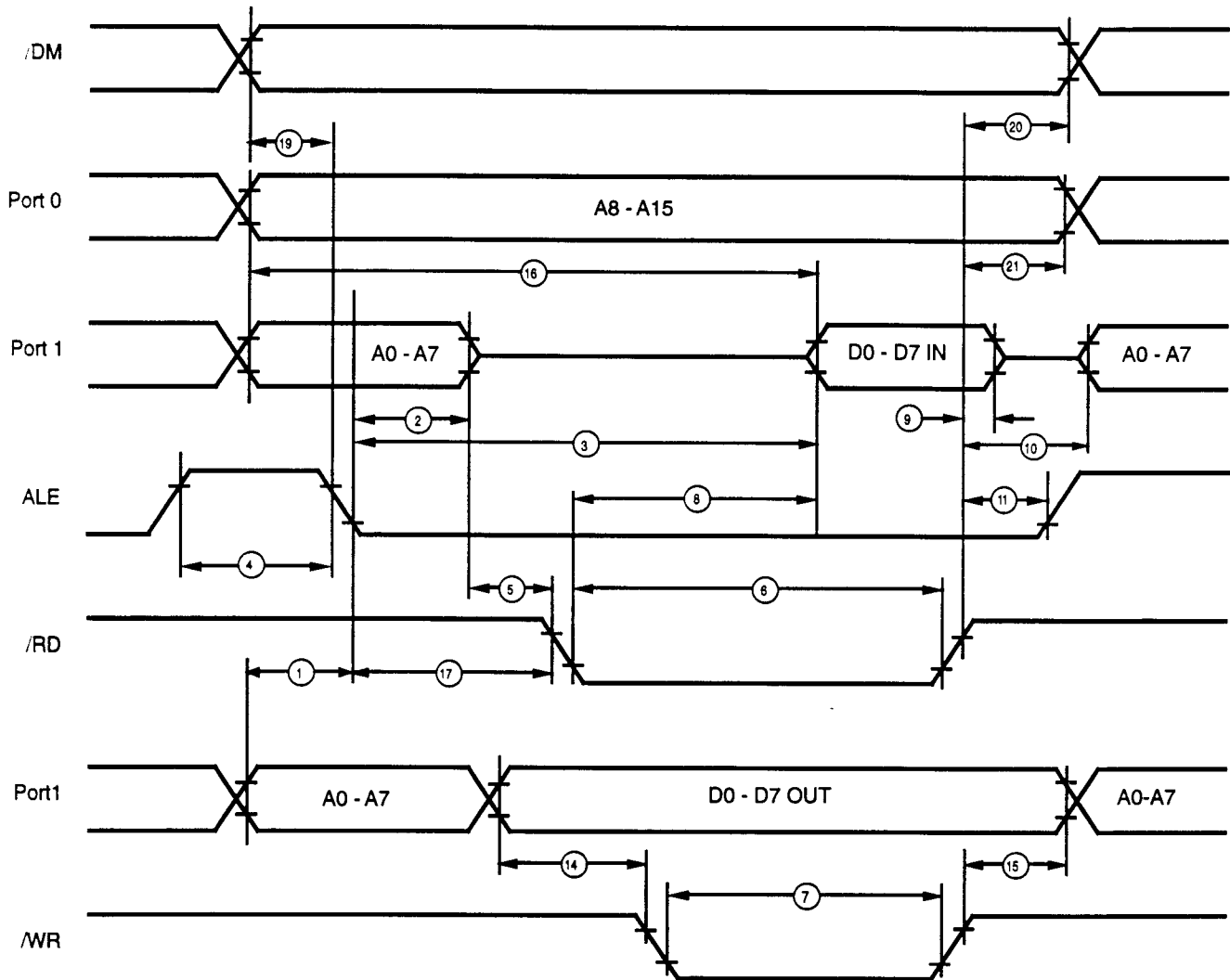
| Sym | Parameter | T | | Typical @ 25 °C | Units | Conditions |
|------------------|-------------------------------|-------------------------|------------------|--------------------|-------|--|
| | | Min ^A | °C to +70 Max | | | |
| | Max Input Voltage | | 7 | | V | I _{IN} 250 µA |
| V _{CH} | Clock Input High Voltage | 3.8 | V _{CC} | | V | Driven by External Clock Generator |
| V _{CL} | Clock Input Low Voltage | -0.03 | 0.8 | | V | Driven by External Clock Generator |
| V _{PH} | Input High Voltage (P0,P1,P2) | 2.0 | V _{CC} | | V | |
| V _{PH} | Input High Voltage (P3) | 2.2 | V _{CC} | | V | |
| V _{PL} | Input Low Voltage | -0.3 | 0.8 | | V | |
| V _{OH} | Output High Voltage | 2.4 | | | V | I _{OH} = -2.0 mA |
| V _{OH} | Output High Voltage | V _{CC} - 100mV | | | V | I _{OH} = -100 µA |
| V _{OL} | Output Low Voltage | | 0.4 | | V | I _{OL} = + 4 mA |
| V _{RH} | Reset Input High Voltage | 3.8 | V _{CC} | | V | |
| V _{RL} | Reset Input Low Voltage | -0.03 | 0.8 | | V | |
| I _{IL} | Input Leakage | -2 | 2 | | µA | Test at 0V, V _{CC} |
| I _{OL} | Output Leakage | -2 | 2 | | µA | Test at 0V, V _{CC} |
| I _{IR} | Reset Input Current | | -180 | | µA | V _{RL} = 0V |
| I _{CC} | Supply Current | | 120 | 70 | mA | @ 40 MHz [1] |
| I _{CC1} | Standby Current (HALT Mode) | | 30 | 20 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 40 MHz [1] |
| I _{CC2} | Standby Current | | 20 | 6 | µA | STOP Mode V _{IN} = 0V, V _{CC} [1] |
| I _{AL} | Auto Latch Current | -16 | 16 | 5 | µA | |

Note:

- [1] All inputs driven to 0V, or V_{CC} and outputs floating.
 [2] Values are preliminary engineering estimates.

AC CHARACTERISTICS

External Memory Read/Write Timing Diagram



External I/O or Memory Read/Write Timing Diagram

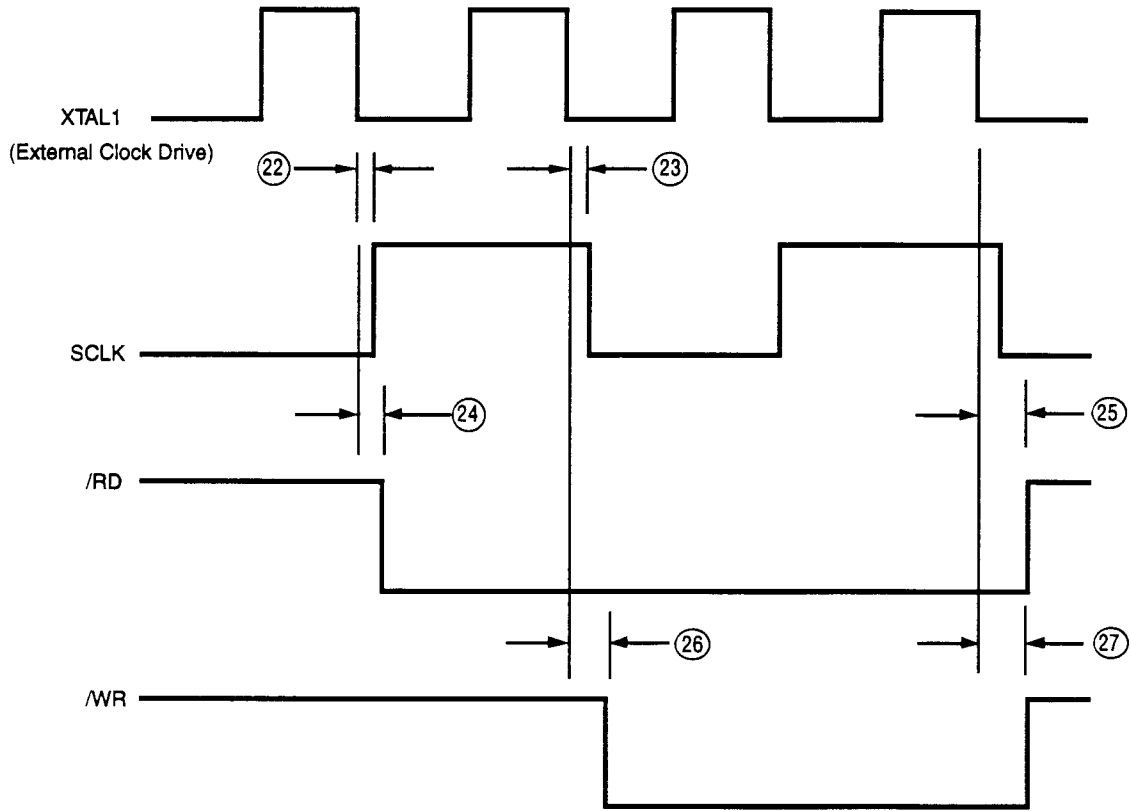
AC CHARACTERISTICS

External I/O or Memory Read/Write Timing Table

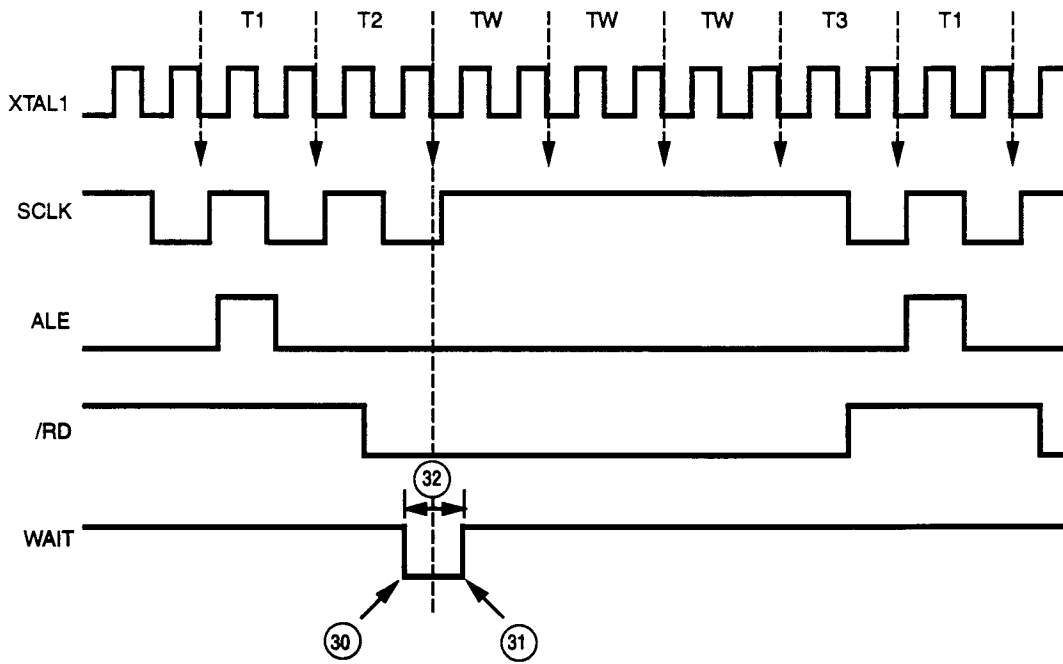
| No | Sym | Parameter | Max | Max | Units |
|----|-------------|--|-----|-----|-------|
| 1 | TdA(ALE) | Address Valid To ALE Fall Delay | 8 | | ns |
| 2 | ThALE(A) | ALE Fall To Address Hold Time | 15 | | ns |
| 3 | TdALE(DI) | ALE Fall To Data In Req'd Valid Delay | | 75 | ns |
| 4 | TwALE | ALE HIGH Width | 10 | | ns |
| 5 | TdAZ(RD) | Address Float To /RD Fall | 0 | | ns |
| 6 | TwRD | /RD Low Width | 60 | | ns |
| 7 | TwWR | /WR Low Width | 35 | | ns |
| 8 | TdRD(DI) | /RD Fall To Data in Req'd Valid Delay | | 40 | ns |
| 9 | ThRD(DI) | /RD Rise to Data In Hold Time | 0 | | ns |
| 10 | TdRDWR(A) | /RD or /WR Rise To Address Active Delay | 20 | | ns |
| 11 | TdRDWR(ALE) | /RD or /WR Rise To ALE Delay | 16 | | ns |
| 14 | TdDO(WR) | Data Out To /WR Fall Delay | 12 | | ns |
| 15 | ThWR(DO) | /WR Rise To Data Out Hold Time | 12 | | ns |
| 16 | TdA(DI) | Address Valid To Data In Req'd Valid Delay | | 90 | ns |
| 17 | TdALE(RD) | ALE Fall To /RD Fall Delay | 20 | | ns |
| 19 | TdDM(ALE) | /DM Valid To ALE Fall Delay | 10 | | ns |
| 20 | TdRDWR(DM) | /RD or /WR Rise To /DM Valid Delay | 15 | | ns |
| 21 | ThRDWR(A) | /RD or /WR Rise To Adress Valid Hold Time | 15 | | ns |
| 22 | TdXT(SCR) | XTAL Falling To SCLK Rising | | 30 | ns |
| 23 | TdXT(SCF) | XTAL Falling To SCLK Falling | | 30 | ns |
| 24 | TdXT(RDF) | XTAL Falling To /RD Falling | | 40 | ns |
| 25 | TdXT(RDR) | XTAL Falling To /RD Rising | | 30 | ns |
| 26 | TdXT(WRF) | XTAL Falling To/WR Falling | | 40 | ns |
| 27 | TdXT(WRR) | XTAL Falling To/WR Rising | | 30 | ns |
| 28 | TsW(XT) | Wait Set Up Time | | | ns |
| 29 | ThW(XT) | Wait Hold Time | | | ns |
| 30 | TsW | Wait Width (One Wait Time) | | | ns |

Notes:

1. Values based on external clock drive with a clock frequency.
2. Values are preliminary and are to be characterized.
3. When using extended memory timing, add 2TpC.
4. Timing numbers are given for minimum TpC.

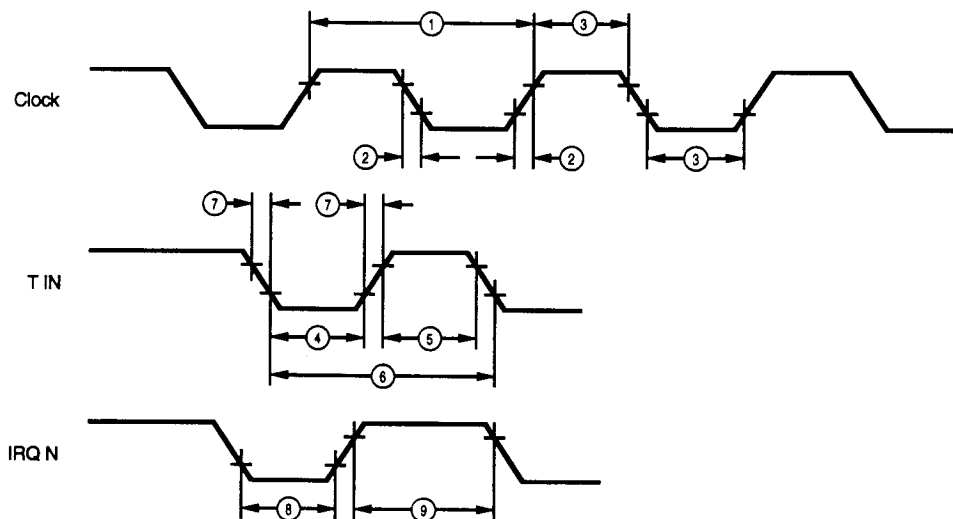


XTAL/SCLK To DSR and DSW Timing



XTAL/SCLK To WAIT Timing

AC CHARACTERISTICS
Additional Timing Diagram



Additional Timing

AC CHARACTERISTICS
Additional Timing Table

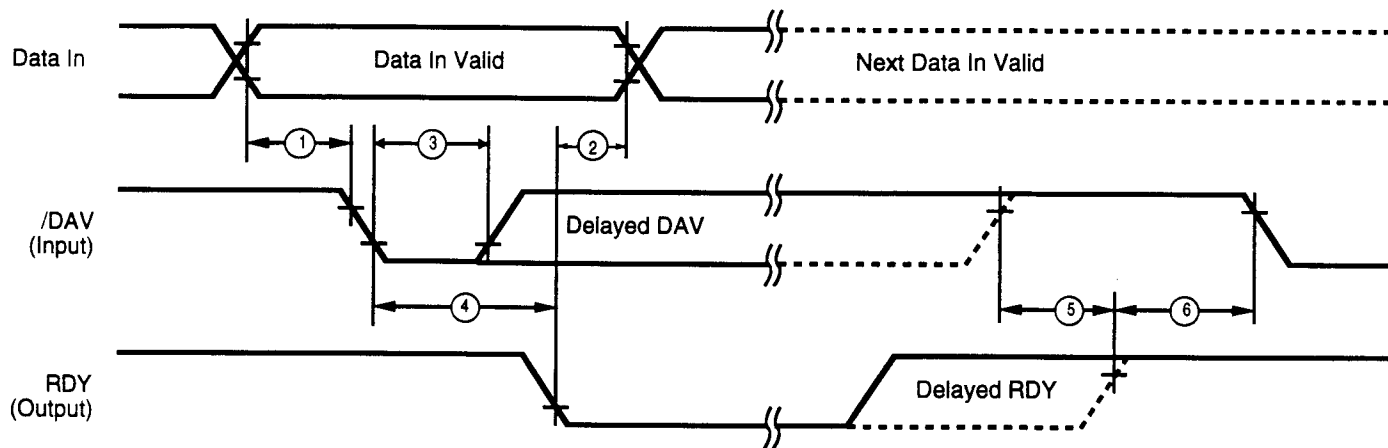
| No | Symbol | Parameter | $T_A = 0^\circ\text{C to } +70^\circ\text{C}$ 40 MHz | | Units | Notes |
|----|-------------|------------------------------------|---|------|-------|-------|
| | | | Min | Max | | |
| 1 | TpC | Input Clock Period | 25 | 1000 | ns | [1] |
| 2 | TrC,TfC | Clock Input Rise & Fall Times | | 4 | ns | [1] |
| 3 | TwC | Input Clock Width | 8 | | ns | [1] |
| 4 | TwTinL | Timer Input Low Width | 75 | | ns | [2] |
| 5 | TwTinH | Timer Input High Width | 3 TpC | | ns | [2] |
| 6 | TpTin | Timer Input Period | 8 TpC | | ns | [2] |
| 7 | TrTin,TfTin | Timer Input Rise & Fall Times | 100 | | ns | [2] |
| 8A | TwIL | Interrupt Request Input Low Times | 70 | | ns | [2,4] |
| 8B | TwIL | Interrupt Request Input Low Times | 5 TpC | | ns | [2,5] |
| 9 | TwIH | Interrupt Request Input High Times | 3 TpC | | ns | [2,3] |

Notes:

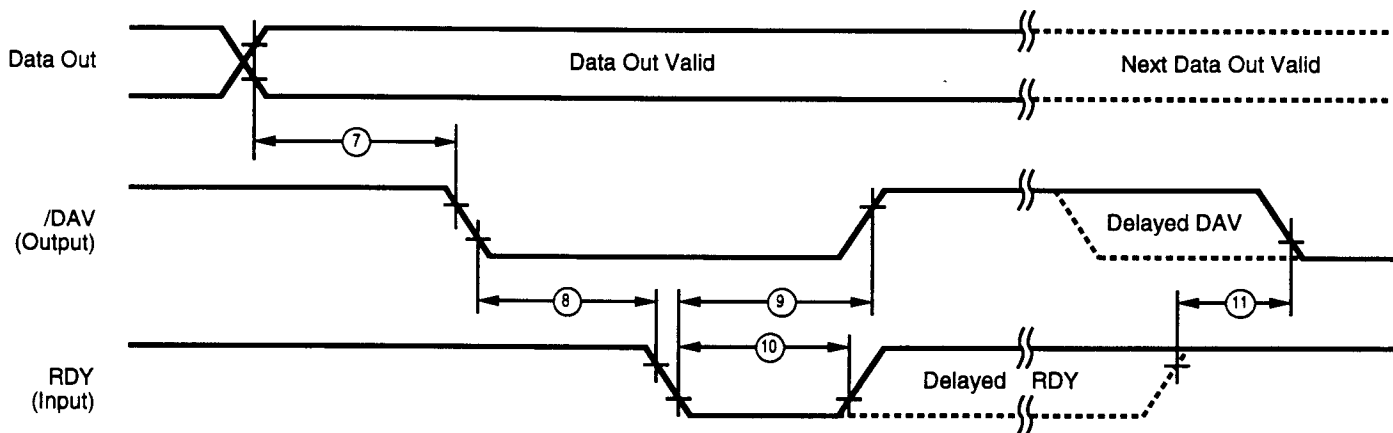
- [1] Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
- [2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
- [3] Interrupt references request through Port 3.
- [4] Interrupt request through Port 3 (P33-P31).
- [5] Interrupt request through Port 30.

AC CHARACTERISTICS

Handshake Timing Diagrams



Input Handshake Timing



Output Handshake Timing

AC CHARACTERISTICS
Handshake Timing Table

| Direction | No | Symbol | T Parameter | °C | | Max | Data Units |
|-----------|----|----------------|----------------------------|------------------|-----------|-----|---------------|
| | | | | $T_A = 0$ Min | +70 °C | | |
| | 1 | TsDI(DAV) | Data In Setup Time to /DAV | 0 | | ns | In |
| | 2 | ThDI(DAV) | RDY to Data In Hold Time | 0 | | ns | In |
| | 3 | TwDAV | /DAV Width | 80 | | ns | In |
| | 4 | TdDAVIf(RDYf) | /DAV to RDY Delay | | 120 | ns | In |
| | 5 | TdDAVr(RDYr) | DAV Rise to RDY Wait Time | | 40 | ns | In |
| | 6 | TdRDYOr(DAVIf) | RDY Rise to DAV Delay | 0 | | ns | In |
| | 7 | TdDO(DAV) | Data Out to DAV Delay | | TpC | ns | Out |
| | 8 | TdDAVOf(RDYIf) | /DAV to RDY Delay | 0 | | ns | Out |
| | 9 | TdRDYIf(DAVOr) | RDY to /DAV Rise Delay | | 120 | ns | Out |
| | 10 | TwRDY | RDY Width | 80 | | ns | Out |
| | 11 | TdRDYr(DAVOf) | RDY Rise to DAV Wait Time | | 40 | ns | Out |

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