DATASHEET

DJT090A0X43-SRPZ: Non-Isolated DC-DC

7.0 to 14.4V_{DC} input; 0.5 to 2V_{DC} output; 90A output current

RoHS Compliant

The DJT090A0X43-SRPZ Digital DLynxII™ power modules are non-isolated dc-dc converters that can deliver up to 90A of output current. These modules operate over a 7 to 14.4V_{DC} input range and provide a precisely regulated output voltage from 0.5 to 2V_{DC}. The output voltage is programmable via an external resistor and/or PMBus control. Features include a digital interface using the PMBus protocol, remote On/Off, adjustable output voltage, Power Good signal and overcurrent, overvoltage and overtemperature protection. The module also includes a real time compensation loop that allows optimizing the dynamic response of the converter to match the load with reduced amount of output capacitance leading to savings on cost and PWB area.

Application

- High current voltage rails for ASICs/High-Performance Processors
- High-Current FPGA Power (e.g. Xilinx, Intel)
- High-Performance ARM Processor Power
- Networking Processors (e.g. Broadcom, Marvell, NXP)
- Artificial intelligence (AI) processors and applications
- Distributed power architectures
- Intermediate bus voltage applications
- Telecommunications equipment
- Servers and storage applications
- Networking equipment
- Industrial equipment
- Test and Measurement equipment

Features

- Wide Input voltage range: 7.0 to 14.4V_{DC}
- Digital output voltage programming 0.5 to 2V_{DC}
- Delivers up to 90A output current
- Paralleling up to 8 units, 720A, interleaving and fault spreading
- A single cycle response (ASCR) charge mode controller provides fast transient response, reduced output capacitance and increased stability
- 328mm^2 (23.24x14.1mm), height 14.35mm MAX
- 0.508inch^2 (0.915x0.555inch), height 0.565inch MAX
- Output voltage setpoint accuracy +/-0.5% (0 to 85°C)
- Digital telemetry and control with PMBus 1.3
- Frequency synchronization
- Tracking / sequencing
- Protections: OVP, UVP, OCP, OTP
- Remote On/Off, positive logic
- Cycle by cycle output OCP/UCP
- Black Box - fault reporting with parametric capture
- Wide operating temperature range -40°C to 85°C
- UL* 62368-1, 2nd Ed. Recognized, and TUV (EN62368-1, 2nd Ed.) Licensed
- ISO** 9001 and ISO 14001 certified manufacturing facilities
- Compliant to RoHS II EU “Directive 2011/65/EU” and amended “Directive (EU) 2015/863”
- Compatible in a Pb-free or SnPb reflow environment
- Compliant to IPC-9592 (Sept. 2008), Category 2, Class I, Class II pending

Electrical Specifications

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only, functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect the device reliability. It is for example only.

Parameter	Device	Min	Max	Unit
Input Voltage (Continuous)	V_{in}	-0.3	15	V
CLK, DATA, SMBALERT, SYNC, ON/OFF, PG, DDC, V5P, SEQ, VS+, VS-		-0.3	6	V
VSET/SA, V1P5, ISHARE Operating Ambient Temperature (see Thermal Considerations section)	T_A	-40	85	°C
Storage Temperature	T_{stg}	-55	125	°C

CAUTION: This power module is not internally fused. An input line fuse must always be used.

This power module can be used in a wide variety of applications, ranging from simple standalone operation to an integrated part of sophisticated power architecture. To preserve maximum flexibility, internal fusing is not included, however, to achieve maximum safety and system protection, always use an input line fuse. The safety agencies require a fuse with a maximum rating of 35A (see Safety Considerations section). Based on the information provided in this Data Sheet on inrush energy and maximum dc input current, the same type of fuse with a lower rating can be used. Refer to the fuse manufacturer's Data Sheet for further information.

Recommended Operating Conditions

Parameter	Symbol	Min	Nominal	Max	Unit
Input Voltage (continuous)	V_{in} $V_{in,nom}$	7	12	14.4	V
Output voltage	V_o	0.5	1.2	2	V
Output current (continuous), $V_o = V_{o,min}$ to $V_{o,max}$	I_{out}	0		90	A
CLK, DATA, SMBALERT, SYNC, ON/OFF, PG, DDC, V5P, SEQ, VS+, VS-				5.0	V

Electrical Specifications

Unless otherwise indicated, specifications apply overall operating input voltage, resistive load, and temperature conditions.

Parameter	Condition	Symbol	Min	Typical	Max	Unit
Operating Input Voltage	All	V_{in}	7	12	14.4	Vdc
Maximum Input Current (V_{in}=7V to 14V, I_o=$I_{o,\,max}$)	All	$I_{in,\,max}$			32	Adc
Input No Load Current (V_{in} = 12V, I_o = 0, module enabled)	$V_{o,\,set}$ = 0.5 Vdc	$I_{in,\,no\,load}$		113		mA
Input No Load Current (V_{in} = 12V, I_o = 0, module enabled)	$V_{o,\,set}$ = 2.0 Vdc	$I_{in,\,no\,load}$		177		mA
Input Stand-by Current (V_{in} = 12V, module disabled)	All	$I_{in,\,stand\text{-}by}$		60		mA
Inrush Transient	All	I^2t			0.1	A^2s
Input Reflected Ripple Current, peak-to-peak (5Hz to 20MHz, 1µH source impedance; V_{in} =7V to 14.4V, I_o= $I_{o,max}$; C_{in} = 3 x 0.1uF || 4 x 10uF || 10 x 22uF || 4 x 470uF)	All			25	50	$mA_{pk\text{-}pk}$
Input Ripple Rejection (120Hz)	All			-43		dB
Output Voltage Set-point accuracy over entire output range	All	$V_{o,\,set}$	-0.5		+0.5	$\%V_{o,\,set}$
0 to 85°C, V_o = over entire range -40 to 85°C, V_o = over entire range	All	$V_{o,\,set}$	-0.7		+0.7	$\%V_{o,\,set}$
Voltage Regulation[1] Line Regulation (V_{in}=$V_{in,\,min}$ to $V_{in,\,max}$)	All			3		mV
Load Regulation (I_o = $I_{o,\,min}$ to $I_{o,\,max}$)	All			3		mV

[1]Worst case Line and load regulation data, all temperatures, from design verification testing as per IPC9592.

Electrical Specifications (continued)

Unless otherwise indicated, specifications apply overall operating input voltage, resistive load, and temperature conditions. See Feature Descriptions for additional information.

Parameter	Device	Symbol	Min	Typical	Max	Unit
Adjustment Range (selected by an external resistor)	All	V_o	0.6		1.8	Vdc
PMBus Adjustable Output Voltage	All	V_o	0.5		2.0	Vdc
PMBus Output Voltage Adjustment Step Size	All			±0.05		$\%V_{o, set}$
Remote Sense Range	All				0.1	Vdc
Output Ripple and Noise on nominal output (V_{in} = 12V, V_o = $V_{o, min}$ to $V_{o, max}$ and I_o=$I_{o, min}$ to $I_{o, max}$ C_o = 3 x 0.1uF || 4 x 22uF || 10 x 47uF || 3 x 680uF) Peak-to-Peak (5Hz to 20MHz bandwidth) RMS (5Hz to 20MHz bandwidth)	All			17 4.2		mV_{pk-pk} mV_{rms}
External Capacitance						
ESR ≥ 0.15 mΩ	All	C_o	2600		20000	µF
ESR ≥ 10 mΩ	All	C_o	2600		20000	µF
Output Current (in either sink or source mode)	All	$I_{o,max}$			90	A_{dc}
Output Current Limit Inception (Hiccup Mode), see current measurement accuracy I_{ACC}	All	$I_{o, lim}$		101		A
Efficiency (V_{in}= 12Vdc, T_A=25°C, I_o=$I_{o, max}$, V_o= $V_{o, set}$)	$V_{o, set}$ = 0.5Vdc	η		80.53		%
	$V_{o, set}$ = 0.8Vdc	η		85.64		%
	$V_{o, set}$ = 1.2Vdc	η		88.51		%
	$V_{o, set}$ = 2Vdc	η		91.15		%
Switching Frequency	All	f_{sw}		353		kHz
Frequency Synchronization						
Synchronization Frequency Range	All		-4		4	$\% f_{sw}$
High-Level Input Voltage	All	V_{IH}	2.0			V
Low-Level Input Voltage	All	V_{IL}			0.4	V
Minimum Pulse Width, SYNC	All	t_{SYNC}	200			ns
Maximum SYNC rise time	All	t_{SYNC_SH}			10	ns

General Specifications

Unless otherwise indicated, specifications apply overall operating input voltage, resistive load, and temperature conditions. See Feature Descriptions for additional information.

Parameter	Device	Symbol	Min	Typical	Max	Unit
On/Off Signal Interface						
Logic High (Module ON)						
Input High Current	All	I_{IH}			1	uA
Input High Voltage	All	V_{IH}	2.1		5	V
Logic Low (Module OFF)						
Input Low Current	All	I_{IL}			1	uA
Input Low Voltage	All	V_{IL}	0		0.8	V
Input Low Voltage Turn-On Delay and Rise Times (V_{in}=$V_{in,\ nom}$, I_o=$I_{o,\ max}$, V_o to within ±1% of steady state)	All	V_{IL}	0		0.5	V
Case I: On/OFF is enabled and then in put power is applied (delay from instant at which V_{in} = $V_{in,min}$ until Vo = 10% of $V_{o,set}$	All	T_{delay}		15		msec
Case II: Input power is applied for at least one second and then the On/Off input is enabled (delay from instant at which Von/Off is enabled until Vo = 10% of Vo, set)	All	T_{delay}		1.5		msec
Output voltage Rise time Time for Vo to rise from 10% of $V_{o,\ set}$ to 90% of $V_{o,\ set}$	All	Trise		10	125	msec
Output voltage Transient T_A = 25°C, V_{in}= $V_{in,\ min}$ to $V_{in,\ max}$, ASCR setting = Default I_o = 25% - 75% of $I_{o,\ max}$, slew rate = 10A/us With or without maximum external capacitance	All		-100		+100	mV
Over Temperature Protection (See Thermal Considerations section)	All	T_{OT}		110		°C
PMBus Over Temperature Warning Threshold Tracking Accuracy ($V_{in,\ min}$ to $V_{in,\ max}$; $I_{o,\ min}$ to $I_{o,\ max}$; 0V < V_{SEQ} < Vo)	All	T_{WARN}		100		°C
Power-Up: 2V/ms	All	V_{SEQ} –Vo			100	mV
Power-Down: 2V/ms	All	V_{SEQ} –Vo			200	mV
Input Undervoltage Lockout						
Turn-on Threshold	All			6.8		Vdc
Turn-off Threshold	All			5.8		Vdc
Hysteresis	All			1		Vdc
PMBus Adjustable Input Under Voltage Lockout Thresholds	All		5.8	6.8		Vdc
Input Overvoltage Lockout						
Turn-on Threshold	All			14.5		Vdc
Turn-off Threshold	All			16		Vdc
Hysteresis	All			1		Vdc
PMBus Adjustable Input Over Voltage Lockout Thresholds	All			14.5	16	Vdc
Resolution of Adjustable Input Under Voltage Threshold	All			8		mV
Overvoltage TH for PGOOD ON	All			90		%$V_{o,\ set}$
Overvoltage TH for PGOOD OFF	All			2.4		V
Undervoltage TH for PGOOD ON	All			90		%$V_{o,\ set}$
Undervoltage TH for PGOOD OFF	All			0.4		V
Pullup Resistance of PGOOD pin	All			10		kΩ
Sink current capability into PGOOD pin	All		-100		100	nA
Calculated MTBF (I_o=0.8$I_{o,max}$ T_A=40°C) Telcordia Issue 3 Method 1 Case 3	All			28,032,732		Hours
Weight	All			12.7(0.45)		g(oz.)

Feature Interface Specifications

Unless otherwise indicated, specifications apply overall operating input voltage, resistive load, and temperature conditions. See Feature Descriptions for additional information.

Parameter	Conditions	Symbol	Min	Typical	Max	Unit
PMBus Signal Interface Characteristics						
Input High Voltage (CLK, DATA)		V_{IH}	2.1			V
Input Low Voltage (CLK, DATA)		V_{IL}			0.8	V
Input high level current (CLK, DATA)		I_{IH}	-1		1	µA
Input low level current (CLK, DATA)		I_{IL}	-1		1	µA
Output Low Voltage (CLK, DATA, SMBALERT#)	I_{OUT}=2mA	V_{OL}			0.5	V
Output high level open drain leakage current (DATA, SMBALERT#)	V_{OUT}=3.6V	I_{OH}	-0.1		0.1	µA
PMBus Operating frequency range	Slave Mode	F_{PMB}	10		1000	kHz
Data hold time	Receive Mode Transmit Mode	$t_{HD:DAT}$	0 300			ns
Data setup time		$t_{SU:DAT}$	250			ns
Measurement System Characteristics						
Output current measurement range		I_{RNG}	-300		300	A
Output current measurement accuracy 25 to 85°C[1] V_{in}= $V_{in,\ min}$ to $V_{in,\ max}$, V_o = $V_{o,\ min}$ to $V_{o,\ max}$		I_{ACC}	-5		+10	% of FL
Output current measurement accuracy -40 to 85°C[1] V_{in}= $V_{in,\ min}$ to $V_{in,\ max}$, V_o = $V_{o,\ min}$ to $V_{o,\ max}$		I_{ACC}	-5		+20	% of FL
Temperature measurement accuracy @12Vin, 0°C to 85°C		T_{ACC}		±2		°C
V_{OUT} measurement range		$V_{OUT(rng)}$	0		2.5	V
V_{OUT} measurement accuracy		$V_{OUT,\ ACC}$	-2		1	%

[1] Output current measurement accuracy is valid for I_{out} >=15A

* *UL* is a registered trademark of Underwriters Laboratories, Inc.
† *CSA* is a registered trademark of Canadian Standards Association.
‡ *VDE* is a trademark of Verband Deutscher Elektrotechniker e.V.
** ISO is a registered trademark of the International Organization of Standards # The PMBus name and logo are registered trademarks of the System Management Interface Forum (SMIF)

Characteristics Curves

Characteristic Curves of 0.5V Output

The following figures provide typical characteristics for the 90A at 12Vin/0.5Vo 25°C.

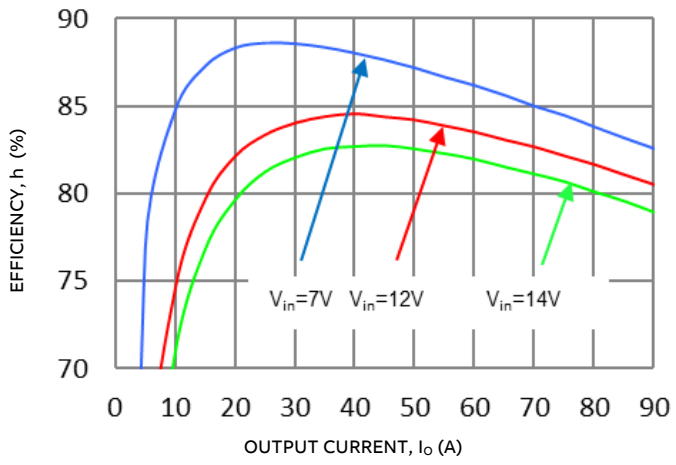


Figure 1. Converter Efficiency versus Output Current.

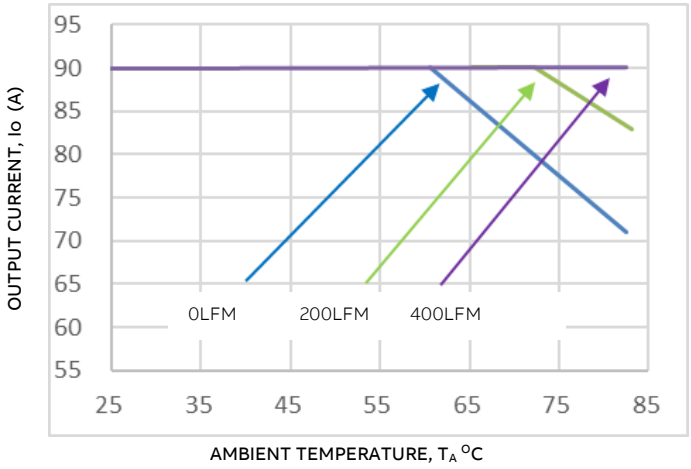


Figure 2. Derating Output Current versus Ambient Temperature and Airflow.

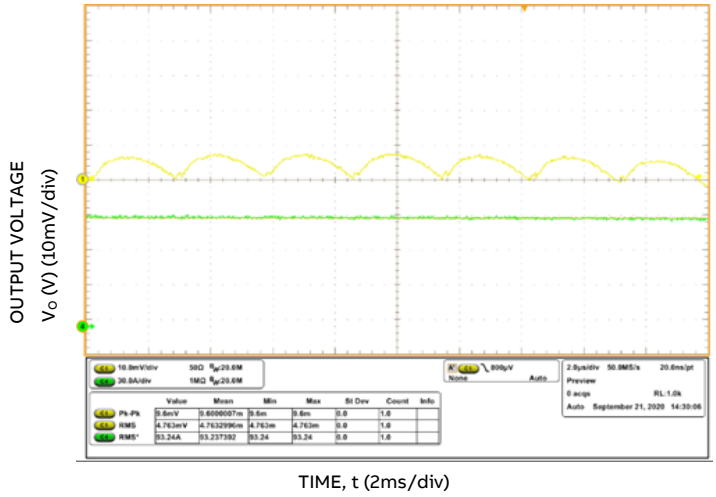


Figure 3. Typical output ripple and noise (C_o = 4 x 22uF + 12 x 47uF + 4 x 680uF, V_{in} = 12V, I_o = $I_{o,max,}$).

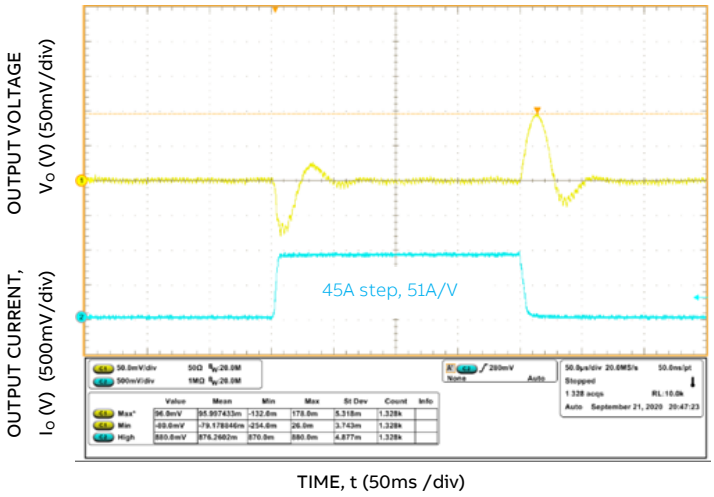


Figure 4. Transient Response to Dynamic Load Change from 0% to 50% at 12V_{in} 10A/us (C_o = 4 x 22uF + 12 x 47uF + 4 x 680uF, ASCR Gain = 270, ASCR

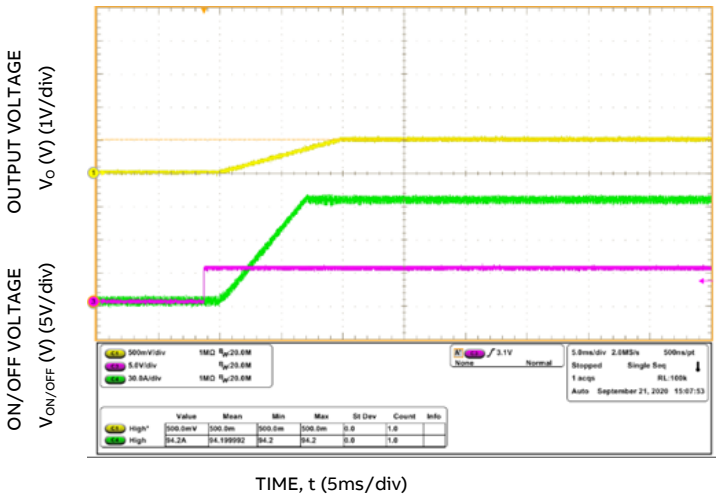


Figure 5. Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

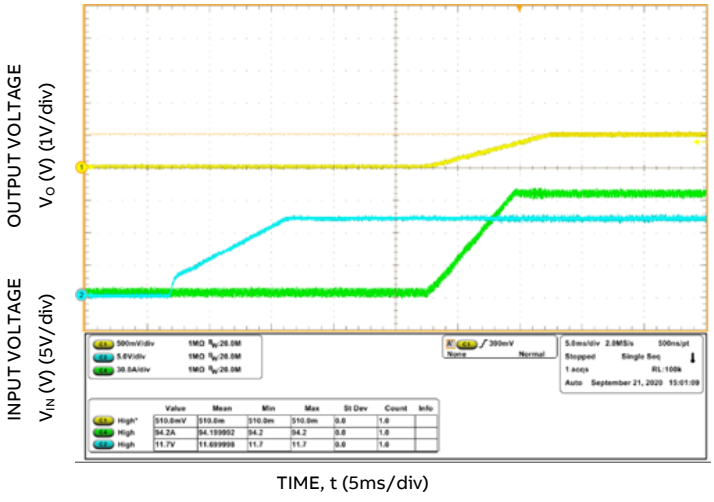


Figure 6. Typical Start-up Using Input Voltage (V_{in} = 12V, I_o = $I_{o,max}$).

Characteristics Curves

Characteristic Curves of 0.8V Output

The following figures provide typical characteristics for the 90A at 12Vin/0.8Vo 25°C.

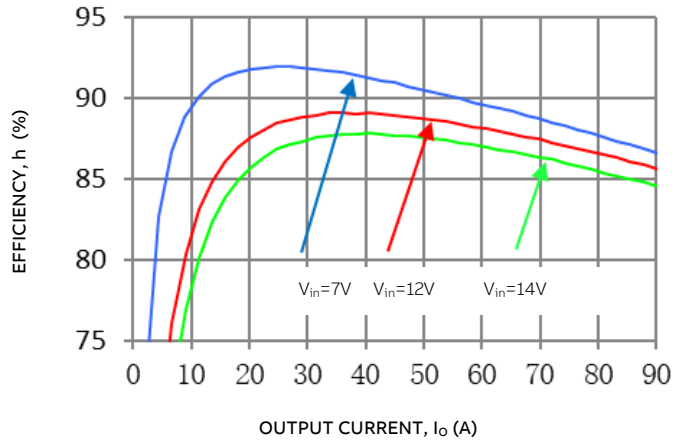


Figure 1. Converter Efficiency versus Output Current.

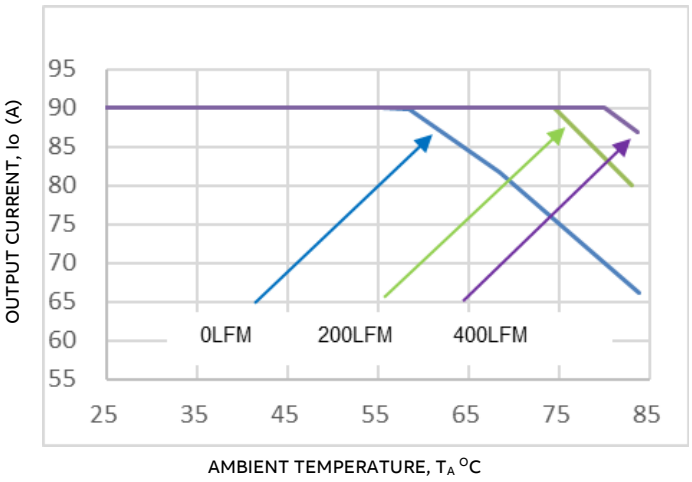


Figure 2. Derating Output Current versus Ambient Temperature and Airflow.

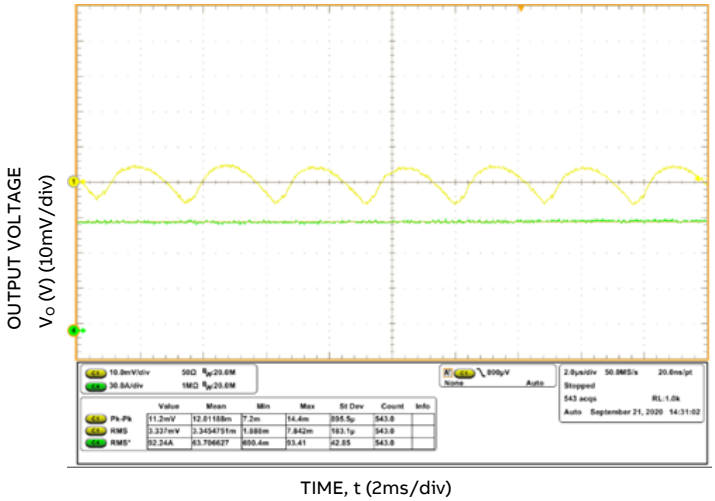


Figure 3. Typical output ripple and noise (C_o = 4 x 22uF + 12 x 47uF + 4 x 680uF, V_{in} = 12V, I_o = $I_{o,max,}$).

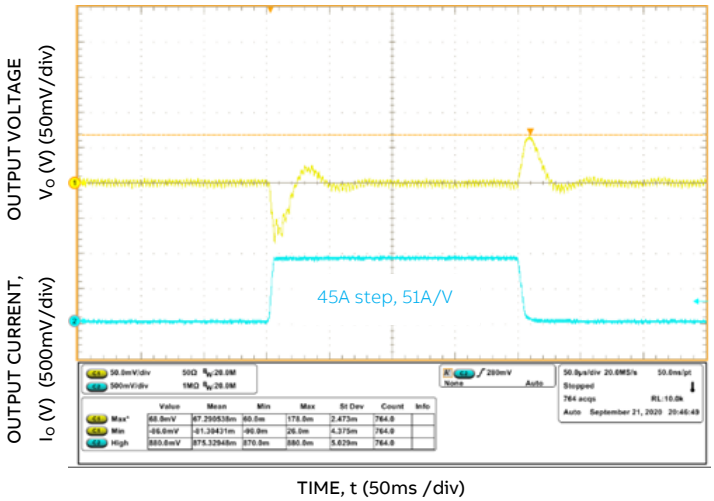


Figure 4. Transient Response to Dynamic Load Change from 0% to 50% at 12V_{in} 10A/us (C_o = 4 x 22uF + 12 x 47uF + 4 x 680uF, ASCR Gain = 270, ASCR

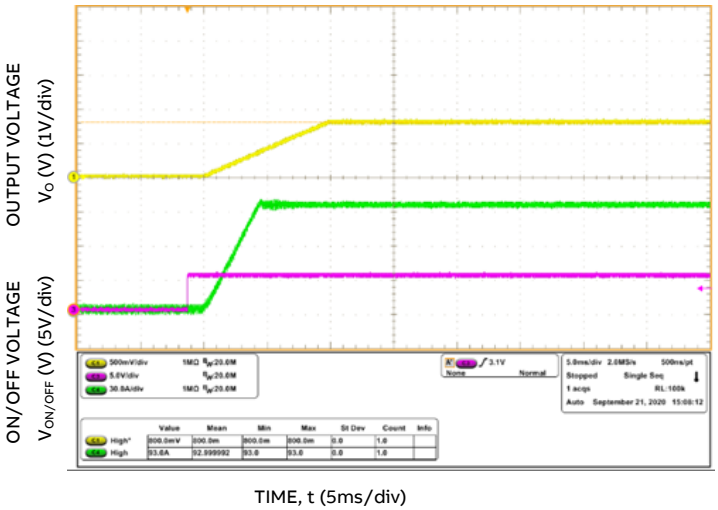


Figure 5. Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

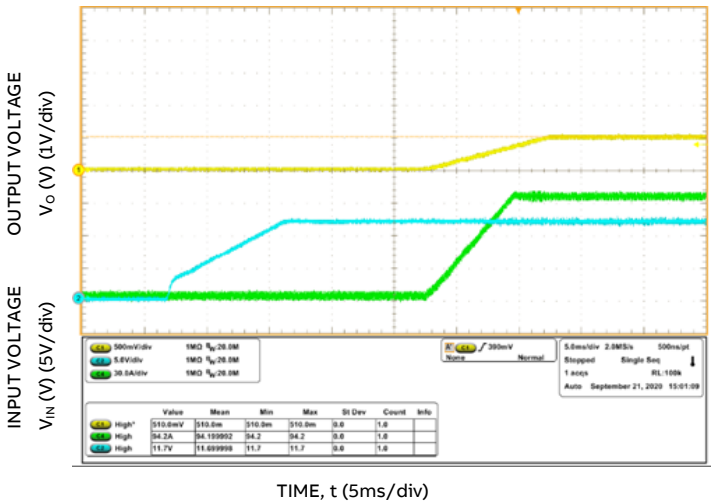


Figure 6. Typical Start-up Using Input Voltage (V_{in} = 12V, I_o = $I_{o,max}$).

Characteristics Curves

Characteristic Curves of 1.2V Output

The following figures provide typical characteristics for the 90A at 12Vin/1.2Vo 25°C.

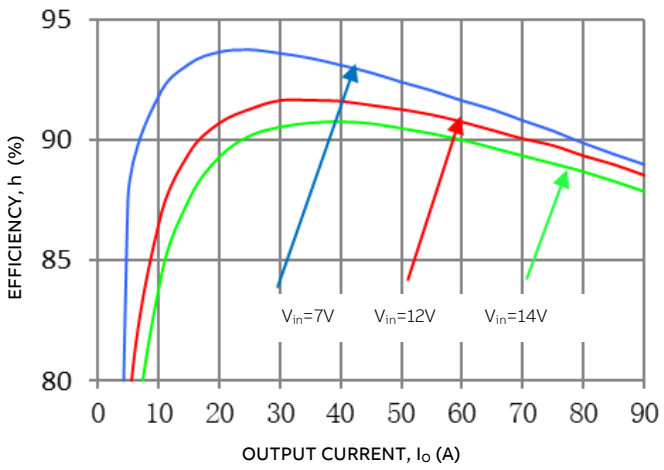


Figure 1. Converter Efficiency versus Output Current.

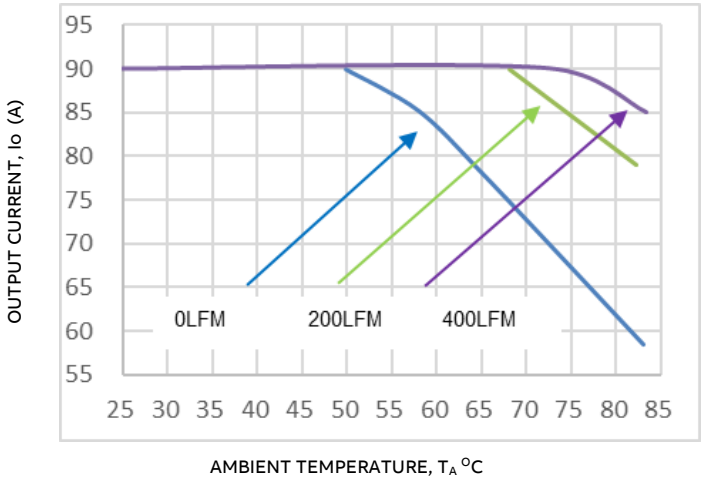


Figure 2. Derating Output Current versus Ambient Temperature and Airflow.

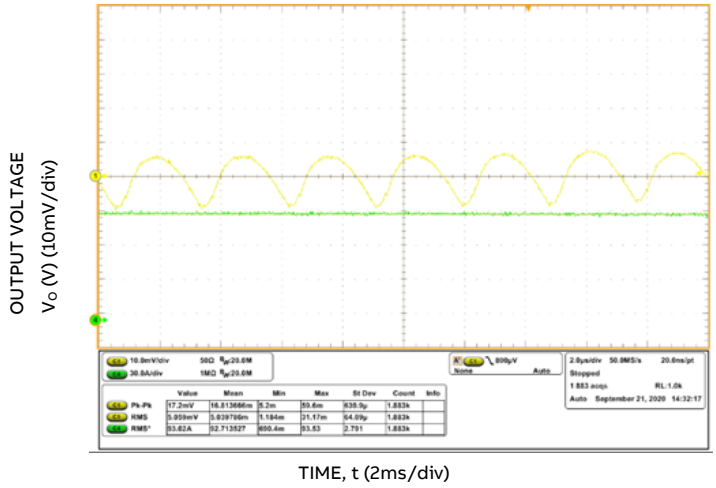


Figure 3. Typical output ripple and noise (C_o = 4 x 22uF + 12 x 47uF + 4 x 680uF, V_{in} = 12V, I_o = $I_{o,max,}$).

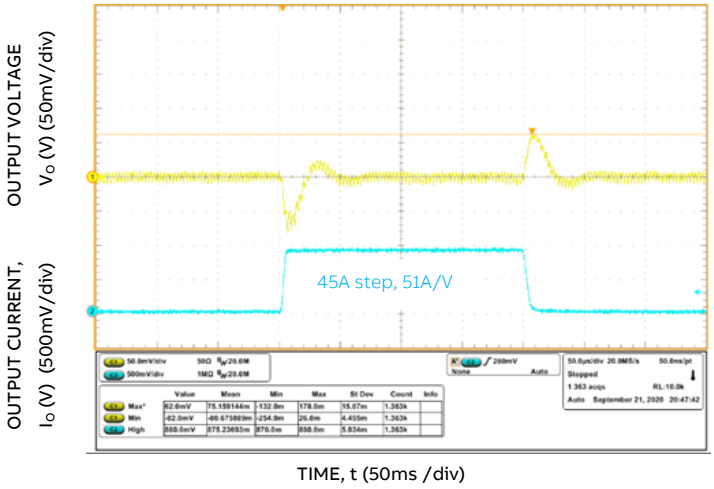


Figure 4. Transient Response to Dynamic Load Change from 0% to 50% at 12V_{in} 10A/us (C_o = 4 x 22uF + 12 x 47uF + 4 x 680uF, ASCR Gain = 270, ASCR

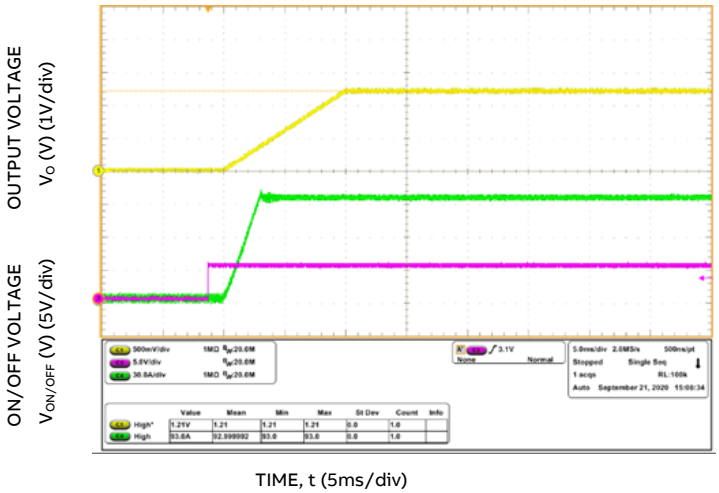


Figure 5. Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

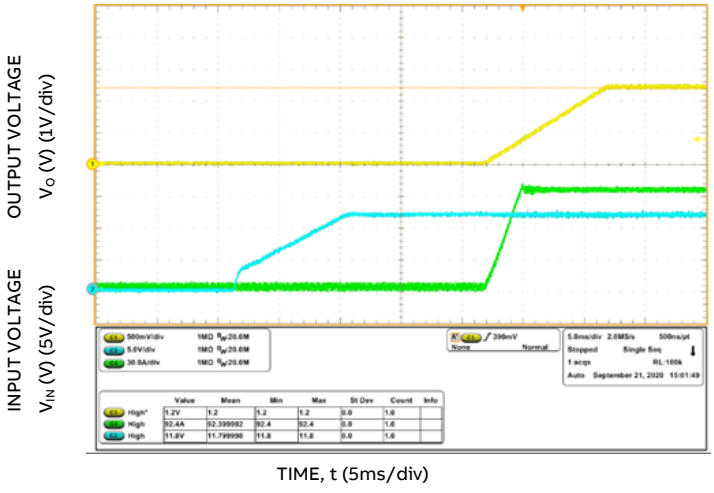


Figure 6. Typical Start-up Using Input Voltage (V_{in} = 12V, I_o = $I_{o,max}$).

Characteristics Curves

Characteristic Curves of 2.0V Output

The following figures provide typical characteristics for the 90A at 12Vin/2.0Vo 25°C.

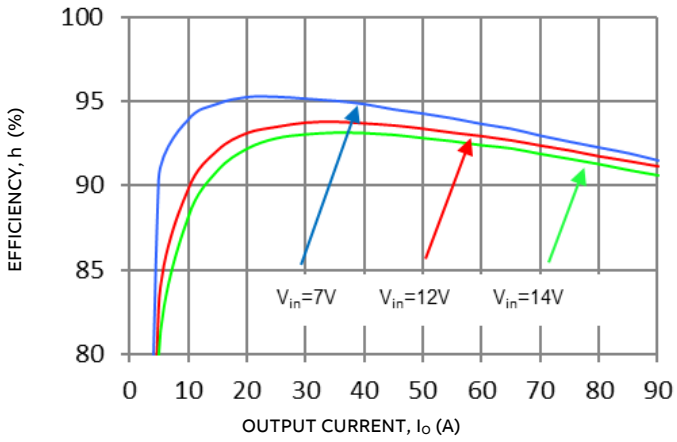


Figure 1. Converter Efficiency versus Output Current.

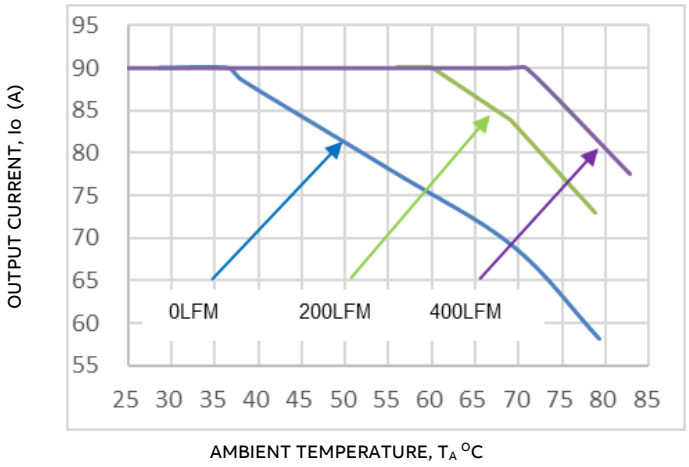


Figure 2. Derating Output Current versus Ambient Temperature and Airflow.

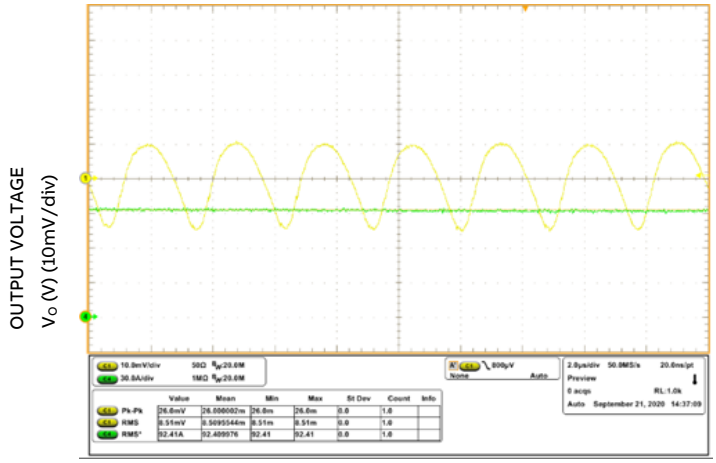


Figure 3. Typical output ripple and noise (C_o = 4 x 22uF + 12 x 47uF + 4 x 680uF, V_{in} = 12V, I_o = $I_{o,max}$,).

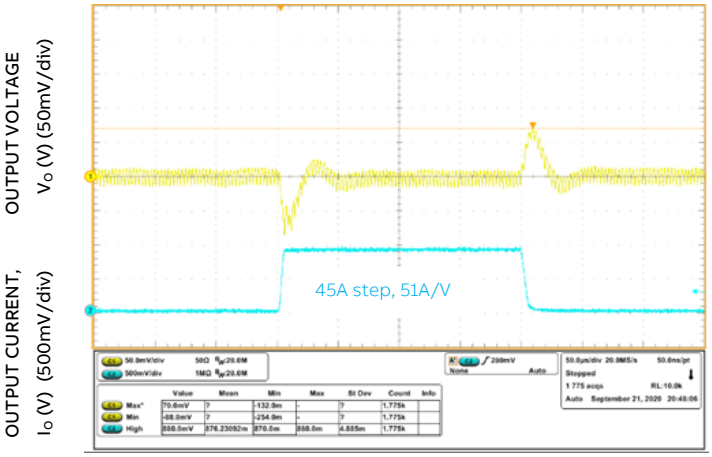


Figure 4. Transient Response to Dynamic Load Change from 0% to 50% at 12V_{in} 10A/us (C_o = 4 x 22uF + 12 x 47uF + 4 x 680uF, ASCR Gain = 270, ASCR

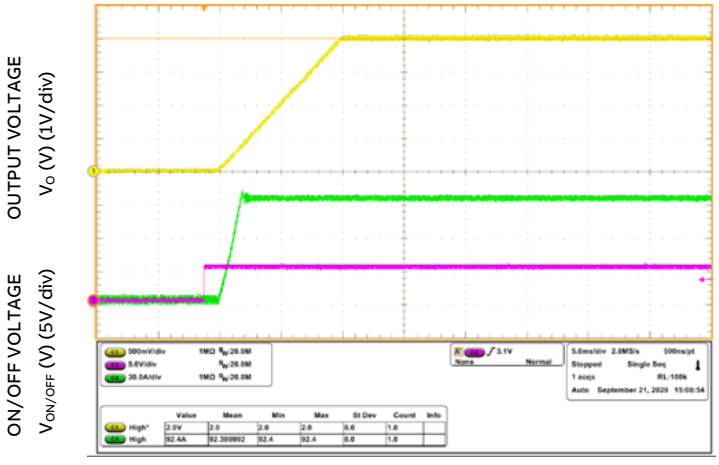


Figure 5. Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

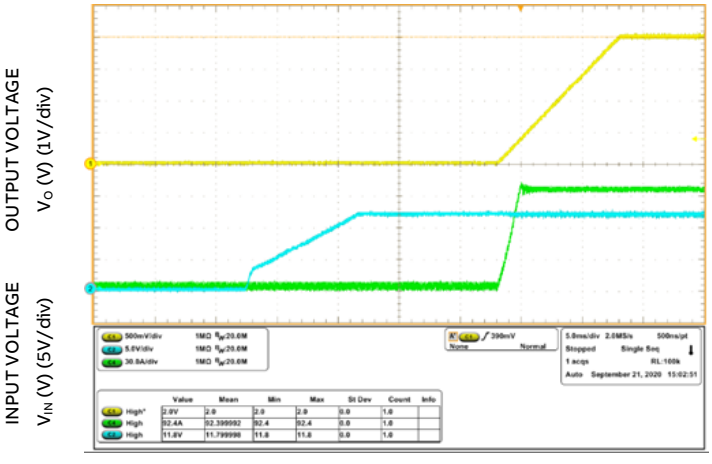


Figure 6. Typical Start-up Using Input Voltage (V_{in} = 12V, I_o = $I_{o,max}$).

Address and Output Voltage

Table I (0.6V-0.9V)

Vo		0.6V		0.7V		0.8V		0.9V	
ADDR	Hex Code	Ra (kΩ)	Rb (kΩ)	Ra (kΩ)	Rb (kΩ)	Ra (kΩ)	Rb (kΩ)	Ra (kΩ)	Rb (kΩ)
16	10	32.4	3.16	93.1	9.09	158	15.8	232	22.6
17	11	25.5	3.32	71.5	9.31	124	16.2	178	23.2
18	12	20.5	3.4	59	9.76	100	16.5	147	24.3
19	13	17.4	3.48	49.9	10	84.5	16.9	124	24.9
20	14	15	3.57	43.2	10.5	73.2	17.8	107	25.5
21	15	13.3	3.74	38.3	10.7	64.9	18.2	93.1	26.1
22	16	11.8	3.83	34	11	57.6	18.7	84.5	27.4
23	17	11	4.12	30.9	11.5	52.3	19.6	75	28
24	18	9.76	4.12	28	11.8	47.5	20	69.8	29.4
25	19	9.09	4.32	26.7	12.7	44.2	21	64.9	30.9
26	1A	8.25	4.42	23.7	12.7	41.2	22.1	59	31.6
27	1B	7.68	4.64	22.1	13.3	37.4	22.6	54.9	33.2
28	1C	7.32	4.87	21	14	34.8	23.2	52.3	34.8
30	1E	6.49	5.36	18.2	15	31.6	26.1	45.3	37.4
31	1F	6.04	5.62	17.4	16.2	30.1	28	42.2	39.2
32	20	5.76	5.9	16.5	16.9	28	28.7	41.2	42.2
33	21	5.49	6.19	15.4	17.4	27.4	30.9	38.3	43.2
34	22	5.11	6.49	14.7	18.7	25.5	32.4	36.5	46.4
35	23	4.99	6.98	14.3	20	24.3	34	35.7	49.9
36	24	4.87	7.68	13.7	21.5	23.2	36.5	33.2	52.3
37	25	4.52	7.87	13	22.6	22.6	39.2	32.4	56.2
38	26	4.42	8.66	12.4	24.3	21.5	42.2	30.9	60.4
39	27	4.22	9.31	12.1	26.7	20.5	45.3	30.1	66.5
47	2F	4.12	10.2	11.5	28.7	20	49.9	28.7	71.5
48	30	4.02	11.5	11	31.6	19.1	54.9	27.4	78.7
49	31	3.92	12.7	11	35.7	19.1	61.9	26.7	86.6
50	32	3.65	14	10.5	40.2	17.8	68.1	26.1	100
51	33	3.57	16.2	10	45.2	17.4	78.7	25.5	115
52	34	3.48	18.7	10	53.6	16.9	93.1	24.3	133
53	35	3.32	22.1	9.53	63.4	16.2	110	23.7	158
54	36	3.24	28	9.31	80.6	16.2	133	23.2	196

Address and Output Voltage

Table II (1.0V-1.8V)

Vo		1.0V		1.2V		1.5V		1.8V	
ADDR	Hex Code	Ra (kΩ)	Rb (kΩ)	Ra (kΩ)	Rb (kΩ)	Ra (kΩ)	Rb (kΩ)	Ra (kΩ)	Rb (kΩ)
16	10	309	30.1	392	38.3	475	47.5	576	57.6
17	11	237	30.9	301	39.2	374	48.7	453	59
18	12	196	32.4	249	41.2	301	49.9	365	60.4
19	13	165	33.2	210	42.2	261	52.3	309	61.9
20	14	143	34	182	44.2	221	53.6	267	64.9
21	15	127	35.7	158	44.2	196	54.9	237	66.5
22	16	113	36.5	143	46.4	178	57.6	215	69.8
23	17	102	38.3	130	48.7	158	59	191	71.5
24	18	93.1	39.2	118	49.9	143	60.4	174	73.2
25	19	86.6	41.2	107	51.1	133	63.4	165	78.7
26	1A	78.7	42.2	100	53.6	124	66.5	150	80.6
27	1B	73.2	44.2	93.1	56.2	113	68.1	140	84.5
28	1C	69.8	46.4	88.7	59	107	71.5	130	86.6
29	1D	64.9	48.7	82.5	61.9	100	75	121	90.9
30	1E	60.4	49.9	76.8	63.4	95.3	78.7	115	95.3
31	1F	57.6	53.6	73.2	68.1	90.9	84.5	110	102
32	20	54.9	56.2	69.8	71.5	84.5	86.6	100	102
33	21	52.3	59	66.5	75	82.5	93.1	100	113
34	22	49.9	63.4	63.4	80.6	76.8	97.6	93.1	118
35	23	47.5	66.5	60.4	84.5	75	105	88.7	124
36	24	45.3	71.5	57.6	90.9	69.8	110	84.5	133
37	25	43.2	75	54.9	95.3	69.8	121	84.5	147
38	26	42.2	82.5	53.6	105	64.9	127	78.7	154
39	27	40.2	88.7	51.1	113	63.4	140	75	165
47	2F	39.2	97.6	49.9	124	60.4	150	73.2	182
48	30	37.4	107	46.4	133	59	169	69.8	200
49	31	35.7	118	47.5	154	57.6	187	68.1	221
50	32	34.8	133	44.2	169	54.9	210	64.9	249
51	33	34	154	42.2	191	52.3	237	63.4	287
52	34	33.2	178	42.2	226	51.1	274	61.9	332
53	35	31.6	210	40.2	267	49.9	332	60.4	402
54	36	30.9	267	39.2	340	48.7	412	57.6	499

Design Consideration

Address and Output Voltage Selection

The address and output voltage are set by a 1% resistor divider from V1P5 pin to SIG_GND pin, the middle point of which is connected to the VSET pin. Varying combinations of resistor values will produce specific address and output voltage combinations. Refer to the Address and Output Voltage Table for possible combinations. Each DJT090A0X43-SRPZ module must have assigned a unique address. There are 32 available addresses and eight discrete output voltage settings from which to choose. The output voltage set point is not limited to the discrete values from the table and can be precisely adjusted by the VOUT_COMMAND 0x21. See parameter precedence below.

Please be advised that if the address resistors are omitted, resistor pair combination is wrong, or the connection to V1P5, VSET or SIG_GND pins is compromised, the controller will try to guess the intended address and output voltage settings, and therefor neither of them will be guaranteed. Compromised connections to module pins result in output voltage setting of 1.8V, unless VOUT_COMMAND value is stored into the non-volatile memory of the module!

Start-up Procedure

When the input voltage rises above the internal controller's Power-ON Reset (POR) level, approximately 4.5V, the module initialization begins. VSET and SYNC pins are read. These values along with the non-volatile FACTORY store are used to initialize the factory settings. Next, the contents of the DEFAULT store are read. Finally, the contents of the USER store are read. Upon completion of initialization routine, the PMBus communication is allowed and the controller begins to monitor the state of ON/OFF pin. Module initialization lasts approximately 15ms. The actual time depends on number of parameters stored into the non-volatile memory stores.

If a parameter is set by more than one mean, the value of the method with highest precedence wins. Assignment method precedence, from lowest to highest, is: pin-strap read, FACTORY store read, DEFAULT store read, USER store read and PMBus command write into volatile memory. The order of precedence could be changed by write protecting a parameter in the lower precedence store and enabling the password protection. See non-volatile memory management for details.

ON/OFF

The DJT090A0X43-SRPZ is a positive ON/OFF logic power module. The module is ON when the ON/OFF pin is at "logic high" state, and OFF when it is at "logic ON_OFF_CONFIG low" state. See parameter procedure below.

The module could be turned ON and OFF from an external enable signal or by the OPERATION 0x01 command. Desired behavior is set by ON_OFF_CONFIG 0x02 command. Use of external enable signal guarantee precise turn-on timing when several modules operate in parallel. For repeatable turn on delay, the enable signal should be asserted high after the controller initialization has been completed and the input voltage is above its undervoltage warning limit. When enabling the device exclusively only via OPERATION command, it is recommended that the ON/OFF pin is tied to any SGND pin. See below Pin Assignment.
The ON/OFF pin is edge triggered to achieve fast turn-on and turn-off times. As a result, minimum enable high and enable low pulse widths must be observed to ensure correct operation. Enable low and enable high times shorter than minimums shown below may result in the module not responding to the trailing edge of the pulse. For example, applying enable high pulse shorter than the minimum pulse width, will turn the module ON, but may not turn the module OFF until a valid enable high pulse is applied to the ON/OFF pin.

TEN_LOW > TOFF_DELAY + TOFF_FALL + 10.5ms

TEN_HIGH > TON_DELAY + TON_RISE + TPOWER_GOOD_DELAY + 5.5ms

The delay between the transition edge of enable signal or the receipt of an OPERATION command and the beginning of the change of the output voltage may be adjusted using TON_DELAY 0x60 and TOFF_DELAY 0x64 commands. When the Ton-delay time is set to 0ms, the device begins its ramp after the internal circuitry has initialized which takes approximately 100µs to complete.
The desired rising and falling slopes of the output voltage can be set by TON_RISE 0x61 and TOFF_FALL 0x65 commands. The Ton-rise time can be set to values less than 125ms; however, the Ton-rise time should be set to a value greater than 500µs to pre-

vent inadvertent fault conditions due to excessive inrush current. A lower Ton-rise time limit can be estimated using the formula:

TON_RISE (MIN) = COUT EXT x VOUT / (N x ILIMIT)

where COUT EXT is the total output capacitance, VOUT is the output voltage, N is the number of phases in parallel, and ILIMIT is the current limit setting for the module(s).

For negative logic control, user is recommended to setup external circuitry to control. See below example.

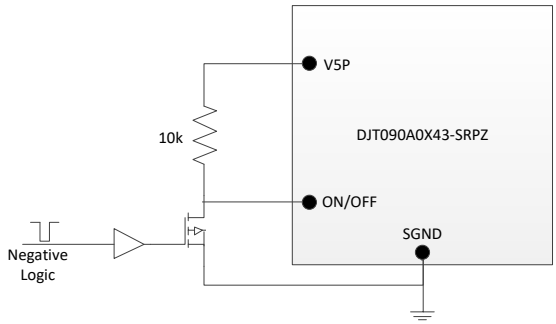


Figure 25. Negative Logic Setup

Power Good

The DJT090A0X43-SRPZ provides a power good signal, PG, that indicates the output voltage is within a specified tolerance of its target level and there are no fault conditions within the module. By default, the PG pin asserts if the output is within 10% of the target voltage. These limits and the configuration of the pin can be changed using POWER_GOOD_ON 0x5E and USER_CONFIG 0xD1 commands.

A PG delay period is defined as the time from when all the conditions within the module for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. The PG delay can be set using POWER_GOOD_DELAY 0xD4 command.

Pre-bias Startup

The DJT090A0X43-SRPZ supports pre-biased start-up operation in single mode and multi-phase operation mode. An output pre-bias condition exists when an externally applied voltage is present on a power supply's output before the power supply's is enabled. Certain applications require that the POL converter does not sink current during start up, if a pre-bias condition exists at the output. The module's control IC provides pre-bias protection by sampling the output voltage before initiating an output ramp. If a pre-bias voltage lower than the desired output voltage is present after the TON_DELAY 0x60 time the module starts switching with a duty cycle that matches the pre-bias voltage. This ensures that the ramp-up from the pre-bias voltage is monotonic. The output voltage is then ramped to the desired output voltage at the ramp rate set by the TON_RISE 0x61 command. The actual output voltage ramp duration vary with the pre-bias voltage level, however the output is always in regulation after a time interval equal to the sum of TON_DELAY 0x60 and TON_RISE 0x61.

If a pre-bias voltage higher than the target voltage exists after the preconfigured TON_DELAY 0x60 and TON_RISE 0x61 time have completed, the DJT090A0X43-SRPZ starts switching with a duty cycle that matches the pre-bias voltage, and then ramped down to the desired output voltage. This ensures that the ramp-down from the pre-bias voltage is monotonic. If a pre-bias voltage higher than the VOUT_OV_WARN_LIMIT 0x57 limit exists, the device does not initiate a turn-on sequence and stays off.

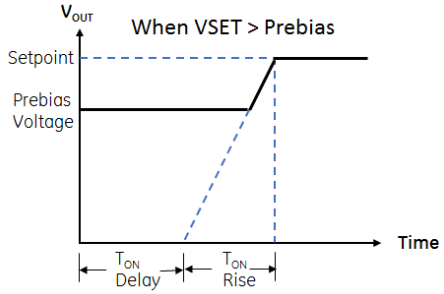


Figure 26a. Pre-bias Turn on

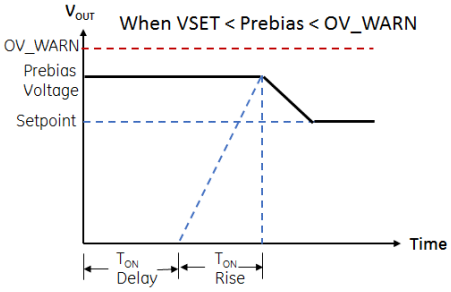


Figure 26b. Pre-bias Turn on

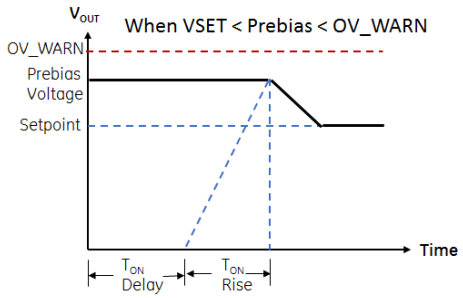


Figure 26c. Pre-bias Turn on

Voltage Tracking

The DJT090A0X43-SRPZ integrates a tracking scheme that allows its output to track a voltage that is applied to the SEQ pin with no external components required. The SEQ pin is an analog input that, when tracking mode is enabled, configures the voltage applied to the SEQ pin to act as a reference for the module's output voltage regulation. The tracking functionality could be configured by TRACK_CONFIG 0xE1 command.

There are two tracking modes – coincident and ratiometric. In coincident mode the tracking is configured to ramp module's output voltage at the same rate as the voltage applied to the SEQ pin until it reaches module's programmed output voltage. Usually the programmed output voltage of a module that is tracking another output voltage is lower than final level of the tracking signal. In ratiometric mode the module's output voltage is 50% of the signal applied to the SEQ pin. Different ratios may be implemented using external resistor divider.

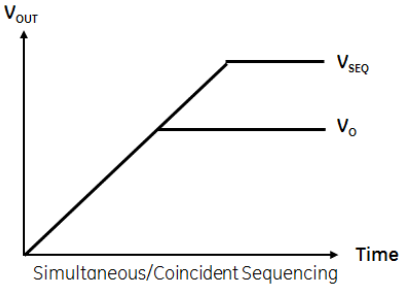


Figure 27a. Tracking

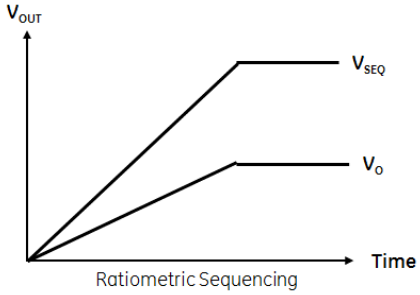


Figure 27b. Tracking

When tracking mode is enabled the output takes the characteristics of the tracked voltage. Sequencing events like enabling and disabling of the module as well as the soft-start settings TON_DELAY 0x60 and TON_RISE 0x61 are ignored. If the module's tracking target limit is chosen, the changes to VOUT_COMMAND 0x21 and output voltage margins are also ignored. POWER_GOOD_DELAY 0xD4 still applies.

The maximum tracking signal slew rate is 1V/ms. The device must be enabled at least 100µs before the tracking signal ramps up. If the voltage at the SEQ pin is greater than 0V prior to the module being enabled, the tracking voltage rises at the rate set by VOUT_TRANSITION_RATE 0x27 until it reaches the correct ratio of the tracked voltage. Until the output voltage is completed the initial ramp, the input tracking signal should not ramp up. To properly track during the turn-off ramp down, the TOFF_DELAY 0x64 must be set be long enough to ensure that the module is turned off after the tracking input signal ramps down to the final value.

Output Sequencing

A group of DJT090A0X43-SRPZ modules can be configured to power up and down in predetermined sequences. This feature is especially useful when powering advanced processors, FPGAs, and ASICs. Each module, or group of modules operating in parallel, in the sequencing chain is informed for the module or the rail that need to power up before and the one that need to power up after. The ON/OFF pins of all modules in the sequencing group are tied together. When sequencing on, the first device to ramp up, called the "prequel", sends a message through the DDC bus to the next device, called the "sequel" when the prequel's PG signal is driven high. When sequenc-

ing off, the sequel sends a message to the prequel to begin the prequel's ramp down after the sequel has completed its own ramp down. To achieve sequenced turn-off all the modules in the sequencing group should be configured for soft turn-off using the ON_OFF_CONFIG 0x02 command. Sequencing can be configured by the SEQUENCE 0xE0 command.

Input Overvoltage and Undervoltage Protections

The input overvoltage and undervoltage protections prevent the DJT090A0X43-SRPZ from operating when the input is above or falls below preset thresholds. The customers are strongly advised not to increase the preset input overvoltage limit or decrease input undervoltage limit as it may result in compromising product safety, violation of the module's absolute maximum and minimum ratings which will void the product warranty.

The input overvoltage and undervoltage protections could be adjusted by the following commands:
VIN_OV_FAULT_RESPONSE 0x56,
VIN_UV_FAULT_RESPONSE 0x5A,
VIN_OV_FAULT_LIMIT 0x55,
VIN_OV_WARN_LIMIT 0x57,
VIN_UV_WARN_LIMIT 0x58,
VIN_UV_FAULT_LIMIT 0x59.

See PMBus Commands for more details.

Output Overvoltage and Undervoltage Protections

The DJT090A0X43-SRPZ offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. The output voltage sensed through the VS+ and VS- pins is digitized and then compared to various programmable thresholds. The output undervoltage fault is masked during the module's soft-start output voltage ramp up, before the power good signal is asserted.

The DJT090A0X43-SRPZ overvoltage and undervoltage behavior ca be configured through the following commands: VOUT_OV_FAULT_RESPONSE 0x41,
VOUT_UV_FAULT_RESPON SE 0x45,
VOUT_OV_FAULT_LIMIT 0x40,
VOUT_OV_WARN_LIMIT 0x42,
VOUT_UV_WARN_LIMIT 0x43,
VOUT_UV_FAULT_LIMIT 0x44.

See PMBus Commands for more details.

Output Overcurrent and Undercurrent Protections

The output overcurrent and undercurrent protections prevent excessive forward current through the module and the load during abnormal operation and excessive reverse current through the module when, for example, the output is shorted to higher voltage rail. Overcurrent and undercurrent protections are cycle-by-cycle in nature. The cycle average current IOUT_AVG_OC_FAULT_LIMIT 0xE7 is set to 101A. If the output cycle average current exceeds this value more than 15 cycle, the OCP will be triggered. The actual cycle by cycle is set to much greater than 101A in order to prevent short time transient current false trigger. If the reverse cycle average current, IOUT_AVG_OC_FAULT_LIMIT 0xE8 exceeds -99A, UCP will be triggered.

The customers are strongly advised not to operate over these limit as it may result in compromising product safety, violation of the module's absolute maximum and minimum ratings which will void the product warranty.

The output overcurrent and undercurrent warning limits and fault response could be adjusted by the following commands:
IOUT_OC_WARN_LIMIT 0x4A,
IOUT_UC_WARN_LIMIT 0x4B,
MFR_IOUT_OC_FAULT_RESPONSE 0xE5,
MFR_IOUT_UC_FAULT_RESPONSE 0xE6.

See PMBus Commands for more details.

Overtemperature and Under-temperature Protections

The DJT090A0X43-SRPZ overtemperature protection ensures the temperature inside the module is below component's temperature maximum limit. The customers are strongly advised not to increase the preset overtemperature limit as it may result in compromising product safety, violation of the module's absolute maximum ratings which will void the product warranty. In addition to overtemperature protection,

there is also under-temperature protection which although not essential for the product safety may be useful in some applications.

The overtemperature and under-temperature protections could be adjusted by the following commands:
OT_FAULT_RESPONSE 0x50,
UT_FAULT_RESPONSE 0x54,
OT_FAULT_LIMIT 0x4F,
OT_WARN_LIMIT 0x51,
UT_WARN_LIMIT 0x52,
UT_FAULT_LIMIT 0x53.

See PMBus Commands for more details.

Monitoring through SMBus

The DJT090A0X43-SRPZ controller can monitor a wide variety of system parameters through the SMBus interface. The module can be monitor for fault conditions by monitoring the SMBALERT pin, which is asserted when any number of preconfigured fault conditions occur. The module can also be monitored continuously for any number of power conversion parameters. Some of most useful monitoring commands are:
STATUS_BYTE 0x78,
STATUS_WORD 0x79,
STATUS_VOUT 0x7A,
STATUS_IOUT 0x7B,
STATUS_INPUT 0x7C,
STATUS_TEMPERATURE 0x7D,
READ_VIN 0x88,
READ_VOUT 0x8B,
READ_IOUT 0x8C,
READ_TEMPERATURE_1 0x8D.

See PMBus Commands for more details.

Input and Output Filtering

Because of its small size and compact design only a fraction of required input and output capacitance are placed inside the module. The additional external input capacitors must be placed adjacent to the input pins of the module. Combination of low ESR electrolytic and high-quality ceramic capacitors is recommended. To minimize the input-voltage ripple the ceramic capacitors must be placed closest to the input pins of the module. In a typical single-phase application, one should consider using at least two 470µF/16V electrolytic capacitors, ten 22µF X7R ceramic capacitors and two 0.1 µF X7R high frequency capacitors.

The amount of external output capacitance depends on the output transient and output ripple requirements. Part of the additional external output capacitors must be placed adjacent to the output pins of the module and the other part to the load. Combination of low ESR polymer and high-quality ceramic capacitors is recommended. To minimize the output -voltage ripple part of the ceramic capacitors must be placed closer to the output of the module. To improve the load transient performance the other part of the ceramic capacitors must be placed closer to the load. In a typical single-phase application, see example application circuit. Some demanding applications may require more output capacitance.

For high di/dt application, capacitor equivalent series inductance (ESL) becomes one of dominating factors of transient performance. ABB recommends user to use low ESR tantalum polymer as output bulk capacitor. ABB suggests user to use online Power Module Wizard or simulation tool to estimate the amount of capacitance required for the application, then choose right amount/size/type accordingly.

Control Loop Tuning

The heart of DJT090A0X43-SRPZ is a fully digital controller IC with innovative Charge Mode Control modulation scheme. By default, this control loop is stable for a wide range of output capacitance and loads, however, it may be further tuned to achieve higher performance under more specific application requirements. Since the control scheme is digital from end to end there is no dependence upon external compensation networks. This simplifies the design process by removing such considerations as temperature and process variation of passive components. Control parameters are set by ASCR_CONFIG 0xDF and ASCR_ADVANCED 0xD5 commands.

The ASCR gain parameter ASCR_CONFIG[15:0] represents the scaling of the error voltage as applied to setting the PWM pulse width. Increasing this parameter decreases the time the controller takes to respond to a transient event at the expense of incorporating more high frequency noise into the loop.

Design Consideration (continued)

This value is the dominant parameter in transient response. We recommend increasing this parameter until the loop response time is sufficient for the application, but no more. Setting the ASCR gain parameter too high can lead to excessive output voltage ripple due to increased PWM jitter.

Integral gain ASCR_CONFIG[31:24] controls DC accuracy and the time taken to return to the output voltage set point following a transient event. Once ASCR gain is set appropriately, decrease integral gain while output voltage deviation is still acceptable.

Residual gain ASCR_CONFIG[23:16] is analogous to damping. The residual gain has the effect of removing or adding some fractional portion against the deviation of the PWM pulse width from steady state duty cycle in the next switch cycle created by the gain parameter. Increasing this parameter decreases output overshoot at the expense of prolonging the recovery to the output set point following a load transient. Its effect is delayed by one cycle relative to the gain effect and as such, it does not affect the peak voltage deviation during the transient, only the return to steady state.

In addition to the basic loop parameters, the controller incorporates a digital steady state gain reduction circuit to provide low jitter steady state operation while maintaining fast transient response. This circuit compares the error signal to the threshold set with ASCR_ADVANCED[11:0] over a period of time. If the error remains low, the controller begins dividing down the gain parameter according to the setting of ASCR_ADVANCED[13:12] to decrease the effect of high frequency noise on PWM pulse width. If the error exceeds the threshold in any cycle, the controller immediately reverts to the full gain setting to handle the transient. Once ASCR_CONFIG settings are chosen and output voltage ripple is acceptable in the application steady state conditions, increase the ASCR threshold setting until the gain reduction activates.

In general, ASCR gain should be tuned based on amount of output capacitors used. The default ASCR gain is set to 270 which would accommodate any capacitance above minimum capacitance requirement. In this case, the ASCR gain is already optimized and should not be increased too much. If much greater output capacitance is presented, then ASCR gain can potentially be tuned up proportional to the output capacitance used. This can achieve much better transient responses. See following simulation examples. Simulation parameters: Vin = 12V, Vout = 1.2V, ASCR Integral = 80(default), ASCR Residual = 80(default). Istep = 45A, slew rate = 10A/us. Combination Cout for Case I is 3000uF, see figure 28a. Combination Cout for Case II is 6000uF, see figure 28b. As shown in the simulation, a larger ASCR gain can achieve better under/overshoot, however it may introduce unwanted oscillation during transient. For common practice, the ASCR gain should be optimized when transient is about to reach marginal stable. Larger output capacitance would allow ASCR gain to be set higher. Note that PCB parasitic is not considered in the simulation. In reality, as the output capacitance increases, equivalent PCB parasitic impedance would increase. Eventually, the effectiveness of the output capacitance would diminish as the equivalent PCB parasitic impedance become significant. Thus choose right amount of capacitors to use.

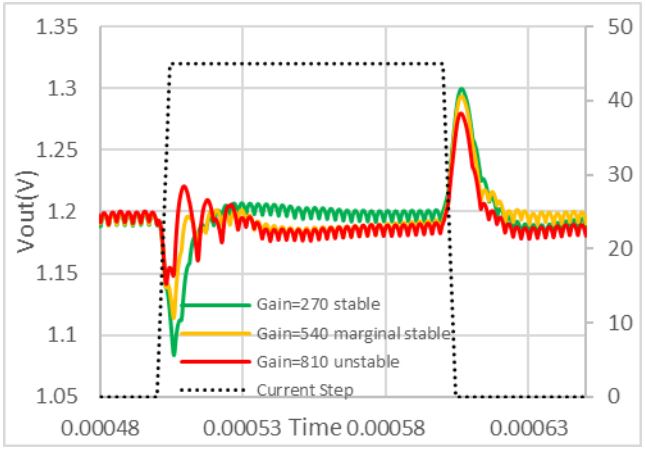


Figure 28a. Case I: Cout = 3000uF

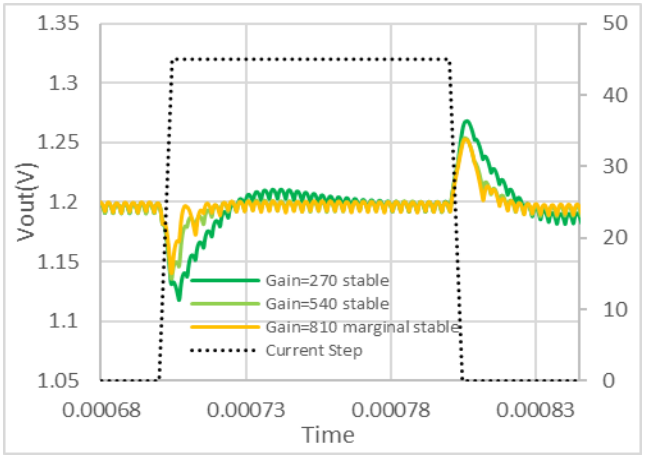


Figure 28b. Case II: Cout = 6000uF

DDC Bus

The Digital-DC Communications (DDC) bus provides communication channel between modules for features such as sequencing, fault spreading and current sharing. The DDC pin must be pulled-up to V5P before ON/OFF pin is set high, or to an external 3.3V or 5.0V supply which must be present before power-up. The DDC pull-up resistor must provide transition times shorter than, or equal to, 1µs. Generally, each module connected to the DDC bus presents approximately 12pF of capacitive loading. The ideal design uses a central pull-up resistor that is well-matched to the total load capacitance. The minimum pull-up resistance should be limited to a value that enables any device to assert the bus to a voltage that ensures a Logic Low, typically 0.8V. A 10kΩ resistor provides good performance on a DDC bus with fewer than 10 devices.

The DJT090A0X43-SRPZ modules can be configured to broadcast a fault event over the DDC bus to the other devices in the group. For details on DDC group ID assignment, addressing and configuration see DDC_CONFIG 0xD3 and DDC_GROUP 0xE2 commands.

Synchronization

The DJT090A0X43-SRPZ's controller incorporates a precise 30MHz clock and Phase-Locked Loop (PLL) to clock the internal circuit. The switching frequency of the module is generated by dividing the internal clock by the closest integer number of times the value of switching frequency setting. The module is optimized to operate at 353kHz**.** When using the internal oscillator, the SYNC pin of one module can be configured as a clock source for other modules to accomplish phase spreading or phase interleaving.

The internal PLL circuit can also be synchronized to an external clock source connected to the SYNC pin. When the SYNC pin is configured as an input pin, the incoming clock signal must be in the range of ±4% of nominal switching frequency, must be present and stable within 50ms after POR and when the enable pin is asserted. The operation frequencies are not limited to discrete values as when using the internal clock. The module supports wider synchronization frequency range, contact local ABB FAE for details.

In the event of a loss of the external clock signal, the PLL sets the External Switching Period Fault bit in the STATUS_MFR_SPECIFIC 0x80 and shut down the module. The module then changes the PLL input to its internal oscillator and commence switching at its programmed frequency upon re-enabling. To resume frequency synchronization, cycle POR with a valid clock signal applied at the SYNC pin or resend the USER_CONFIG 0xD1 command to "select external clock".

Phase Spreading

When multiple point-of-load converters share a common DC input supply, setting each converter to start its switching cycle at a different point in time can dramatically reduce the total peak and RMS input current and therefore improve system efficiency and reduce the input capacitance requirements. To enable phase spreading, all converters must be synchronized to the same switching clock. The phase offset can be configured using the INTERLEAVE 0x37 command.

Non-volatile Memory (NVM) Management

The DJT090A0X43-SRPZ has internal non-volatile memory where module's configurations are stored. There are three internal memory storage units: the USER store, the DEFAULT store and the FACTORY store. The USER store provides the end-user with ability to modify certain module settings while still protecting him, or her, from mistakes that may lead to a system level fault. The DEFAULT store provides a means to protect DJT090A0X43-SRPZ from damage by preventing the user from modifying certain values that are related to its physical construction, or safety and specification limits.

During the initialization process, the DJT090A0X43-SRPZ checks for stored values contained in its internal non-volatile memory. The parameters in USER store take priority over those in the DEFAULT store. If there are no values set in the USER, DEFAULT or FACTORY stores, the device uses the pin-strap setting value. Integrated security measures ensure that the user can only restore the module's configuration to a level that has been made available to them. For details regarding protection of the USER and DEFAULT stores, see the SECURITY_CONTROL 0xFA, PASSWORD 0xFB, WRITE_PROTECT 0xFD com-

mands.

The ON/OFF pin must be driven low whenever a PMBus command that could potentially damage the application circuit is sent to the module. It is always a good practice to turn the module OFF when saving configuration changes into the non-volatile memory.

Parallel Operation and Active Current Sharing

Up to 8 DJT090A0X43-SRPZ modules can be paralleled together to form a high current rail. The modules will share the current equally within a few percent, assuming output current sensing calibration is adequate. For most applications, factory performed calibration will be sufficient. In some application where the interconnecting impedances between modules are extremely low, in-system calibration may be necessary.

The DJT090A0X43-SRPZ employs “Master – Slave” active current sharing. The master in the current sharing rail continuously transmits its most recent output current reading through the SHARE bus, which the slave modules use as a reference for the purpose of the current balancing.

Only one master is allowed per current sharing rail. A simplified parallel operation schematic is shown blow figure. For several modules to form a current sharing group, the ON/OFF, SHARE, DDC and SYNC pins of one module must be connected to the same pin of all other modules. In addition, the output voltage sensing pins, VS+ and VS-, of each module in the group must be connected to the same output voltage regulation point. Often the ON/OFF bus would be configured for fault-spreading to ensure fast, 20µs typical delay time, fault response. In that scenario the ON/OFF bus would need a single 10kΩ pull-up resistor to V5P. When a module detects a fault condition, it will pull down the ON/OFF bus to disable the other modules in the current sharing group.

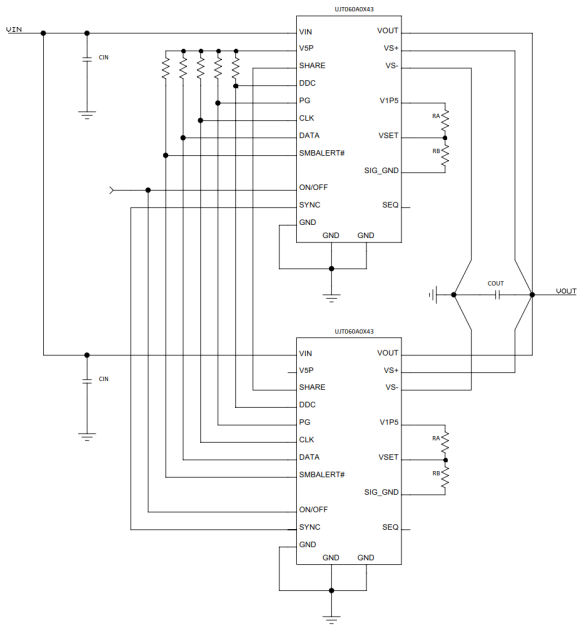


Figure 29. Example connection for two devices

A current sharing rail may be configured using the following commands: USER_CONFIG, DDC_CONFIG, DDC_GROUP and INTERLEAVE. The first step is to select a Rail ID number for the current sharing rail, establish the number of modules (phases) in the rail, and assign Phase IDs to each of the module. The Phase ID “0” identifies the master; all Phase ID settings in a rail must be sequential. All that could be configured by DDC_CONFIG 0xD3 command. Users must pay attention that every module in a multi-phase rail share the same BROADCAST_VOUT COMMAND and BROACAST_OPERATION DDC Group ID settings, which are distinct from DDC Rail IDs. DDC Group ID settings are configured with the DDC_GROUP 0xE2 command. By default, the phase interleaving of the modules in the current sharing rail is accomplished automatically. The controller of each module will choose its phase offset by the last four bits of its PMBus address. Therefore, it is a good practice, the addresses selected for the modules in a current sharing group to be sequential and to begin with the master of the group. The phase offset of the modules in the current sharing group could be altered by INTERLEAVE 0x37 command. For phase interleaving to work, all modules must be synchronized to an external clock, or to the clock of the master in the group. SYNC pin configuration could be set by USER_CONFIG 0xD1. The same command is used to configure the use of ON/OFF pin for fast fault-spreading.

Design Consideration (continued)

Layout Considerations

DJT090A0X43-SRPZ uses PCB to conduct both current and heat because PCB is a better thermal heatsink material than any top side cooling materials. Thus, proper PCB layout is required to successfully deliver full power while reduce switching noise mitigation, improve thermal performance and maximize the efficiency. ABB supplies two reference design along with PCB files for optimized layout. Refer to following application note:

- DJT090_DLynxII_Series_Single_Unit_Evaluation_Board_Application_Note
- DJT090_DLynxII_Series_Paralleling_Evaluation_Board_Application_Note

Common recommendations:

- Place multiple ceramic capacitors directly below the DJT090A0X43-SRPZ especially in between VIN and VIN_GND. This is the most critical decoupling capacitor which will improve efficiency and reduce noise, see Figure 30b, 31d.
- Use large on-pad filled-via array to distribute current into different layer. Evenly distribute current into different layer, see Figure 30a
- Identify input power flow path and output power flow path. Provide strong connection between input ground and output ground right below the DJT090A0X43-SRPZ
- Separate control signal ground with power grounds to avoid potential noise. Control signal ground is internally connected to the power grounds
- Orientation of the DJT090A0X43 may affect component population density. Match the best orientation for the application.
- Do not place any via under the EPAD48, 50, 52 or route any sensitive signal under it

For single DJT090A0X43-SRPZ unit layout, 6 power-plane with minimum 3-oz is recommended for deliver full power up to 90A.

- Use differential pair to route VS+ and VS-, connect them to the decoupling capacitor, which is closest to the load, see Figure 30b.

For parallel DJT090A0X43-SRPZ unit layout, 8 power-plane with minimum 2-oz is recommended for deliver full power up to 720A.

- Match the output impedance of each channel
- Use differential pair to route VS+ and VS-, connect to a single decoupling capacitor which is closest to the load see Figure 32.
- SGND 20-27 can be used along with GND to conduct current and thermal stress, see Figure 31a.

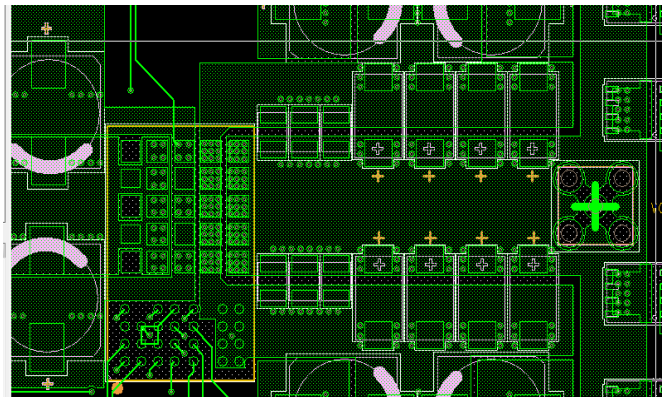


Figure 30a. Top layer (single)

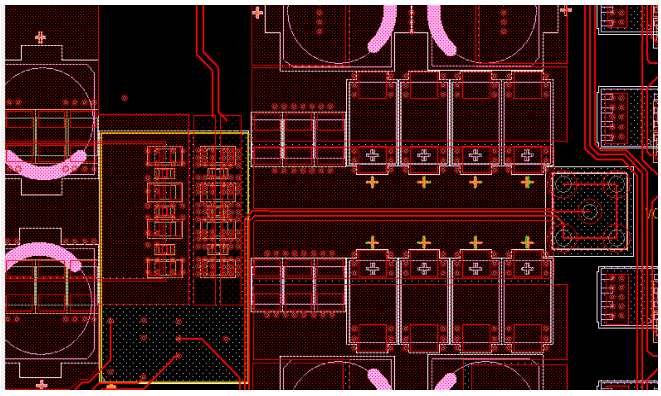


Figure 30b. Bottom layer (single)

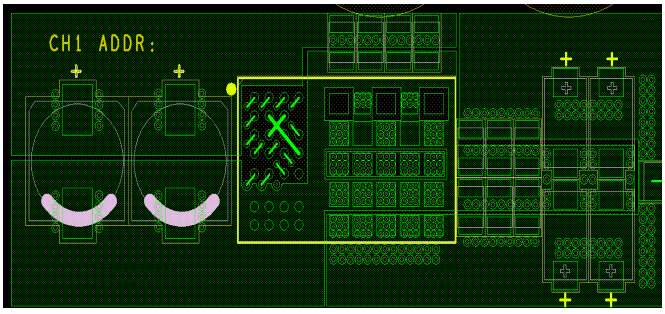


Figure 31a. Top layer (parallel)

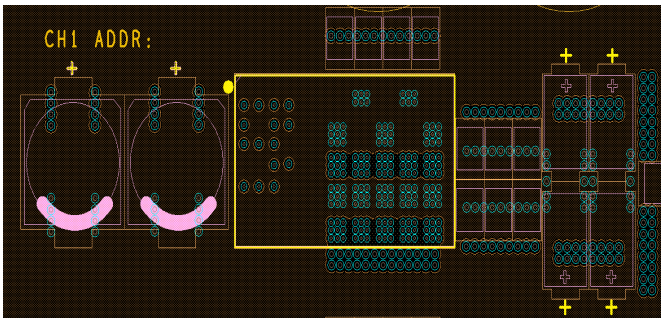


Figure 31b. Top layer (parallel)

Design Consideration (continued)

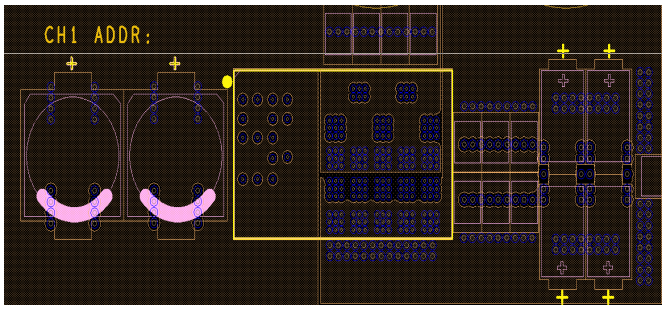


Figure 31c. Mid-Layer (parallel)

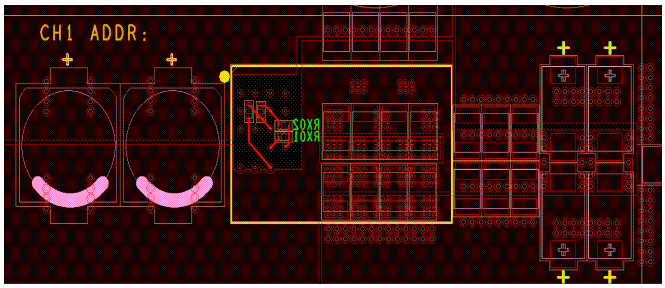


Figure 31d. Bottom layer (parallel)

Stencil Considerations

Solder volume is critical to the production process. Below table show the suggested stencil size for each pad based on 5mil stencil thickness of customer board.

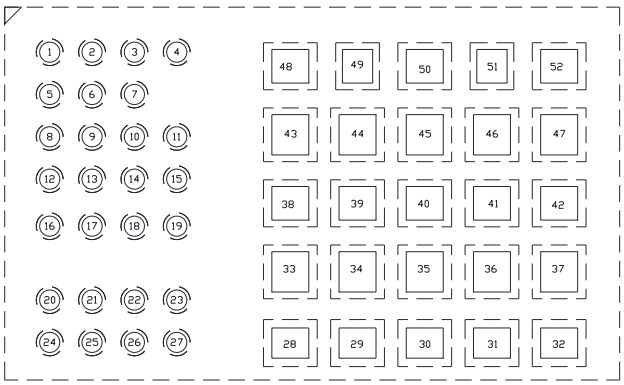


Figure 34. Stencil example

PAD NO.	PAD SIZE(MIL)	STENCIL SIZE(MIL)
1-27	40 DIA	30 DIA
28-32	80x70(X,Y)	55x45(X,Y)
38-42, 48,50,52	80x70(X,Y)	55x50(X,Y)
33-37,43-47	80x80(X,Y)	55x60(X,Y)
49,51	65x70(X,Y)	45x50(X,Y)

Safety Considerations

For safety agency approval the power module must be installed in compliance with the spacing and separation requirements of the end-use safety agency standards, i.e. UL* 62368-1, 2nd Ed. Recognized, and TUV (EN62368-1, 2nd Ed.) Licensed. For the converter output to be considered meeting the requirements of safety extra-low voltage (SELV), the input must meet SELV requirements. The power module has extra-low voltage (ELV) outputs when all inputs are ELV. The input to these units is to be provided with a slow-blow fuse.

Power Module Wizard

ABB offers a free web based easy to use tool that helps users simulate the Tunable Loop performance of the DJT090A0X43-SRPZ. Go to http://abb.transim.com and sign up for a free account and use the module selector tool. The tool also offers downloadable Simplis/Simetrix, models that can be used to assess transient performance, module stability, etc. PLECS model is also available, consult local ABB FAE for details.

Black-box Faults Logging

Black-box Faults logging features up to 8 fault condition recordings during any fault. User has the flexibility to choose which registers to arm. Use SNAPSHOT_FAULT_MASK (0xD7) to locate the registers that need to be armed and use SNAPSHOT_CONTROL (0xF3) to enable the feature. A 32-byte long memory is used to store detailed fault information. This can be found in SNAPSHOT(0xEA). Detailed info can be found in PMBus Command.

SMBus Interface and PMBus User Guidelines

The DJT090A0X43-SRPZ has a SMBus digital interface and can be used with any standard 2-wire SMBus host device. The module is compatible with SMBus version 2.0 and includes a SALERT line to help mitigate bandwidth limitations related to continuous fault monitoring. Pull-up resistors are required on the SMBus. The pull-up resistor can be tied to V5 or to an external 3.3V or 5V supply as long as this voltage is present before or during device power-up. The ideal design uses a central pull-up resistor that is well-matched to the total load capacitance. The minimum pull-up resistance should be limited to a value that enables any device to assert the bus to a voltage that ensures a Logic Low (typically 0.8V at the device monitoring point). Given the pull-up voltage of 5V and the pull-down current capability of the module (nominally 4mA), a 10kΩ resistor on each line provides good performance on an SMBus with fewer than 10 modules.

DJT090A0X43-SRPZ allows the user to adjust many parameters in order to optimize system performance. When configuring the module in a circuit, it should be disabled whenever most settings are changed with PMBus commands. Some exceptions to this recommendation are OPERATION 0x01, ON_OFF_CONFIG 0x02, CLEAR_FAULTS 0x03, VOUT_COMMAND 0x21, VOUT_MARGIN_HIGH 0x25, and VOUT_MARGIN_LOW 0x26. While the module is enabled any command can be read. Many commands do not take effect until after the device has been re-enabled, hence the recommendation that commands that change device settings are written while the device is disabled.

When sending the STORE_DEFAULT_ALL 0x11, STORE_USER_ALL 0x15, RESTORE_DEFAULT_ALL 0x12, and RESTORE_USER_ALL 0x16 commands, it is recommended that no other commands are sent to the device for 100ms after sending STORE or RESTORE commands. In addition, there should be a 2ms delay between repeated READ commands sent to the same device. When sending any other command, a 5ms delay is recommended between repeated commands sent to the same device.

The PMBus Host should respond to SALERT as follows: (1) Module pulls SALERT low. (2) PMBus host detects that SALERT is now low and performs transmission with Alert Response Address to find which module is pulling the SALERT low. (3) PMBus host talks to the module that has pulled SALERT low. The actions that the host performs are up to the system designer. If multiple modules are faulting and SALERT is low after performing the above steps, it requires transmission with the Alert Response Address repeatedly until all faults are cleared.

See ABB DPI-CLI Guide for examples.

PMBus Data Format

Linear-11 (L11)
The L11 data format uses 5-bit two's complement exponent (N) and 11-bit two's complement mantissa (Y) to represent real world decimal value (X). The relation between real world decimal value (X), N, and Y is: $X = Y \cdot 2^{N}$.
Linear-16 Unsigned (L16u)
The L16u data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit unsigned integer mantissa (Y) to represent real world decimal value (X). The relation between real world decimal value (X), N, and Y is: $X = Y \cdot 2^{-13}$.
Linear-16 Signed (L16s)
The L16s data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit two's complement mantissa (Y) to represent real world decimal value (X). The relation between real world decimal value (X), N, and Y is: $X = Y \cdot 2^{-13}$.
Bit Field (BIT)
A description of the Bit Field format is provided in each command details.
Custom (CUS)
A description of the Custom data format is provided in each command details. A combination of Bit Field and integer are common type of Custom data format.
ASCII (ASC)
A variable length string of text characters in the ASCII data format.

PMBus Command Summary

This section provides a summary of the DJT090A0X43 commands followed by their detailed description. The commands are outlined in the order of increasing command codes.

PMBUS CMD	CMD CODE	DATA BYTES	DATA FORMAT	DATA UNITS	TRANS-FER TYPE	PROTECT ABLE	DEFAULT VAL-UE
OPERATION	0x01	1	bit field		R/W	No	0x00
ON_OFF_CONFIG	0x02	1	bit field		R/W	Yes	0x16
CLEAR_FAULTS	0x03	0			W	No	
STORE_DEFAULT_ALL	0x11	0			W	Yes	
RESTORE_DEFAULT_ALL	0x12	0			W	No	
STORE_USER_ALL	0x15	0			W	Yes	
RESTORE_USER_ALL	0x16	0			W	No	
CAPABILITY	0x19	1	bit field		R		0xD0
VOUT_MODE	0x20	1	mode + exp		R	Yes	0x13
VOUT_COMMAND	0x21	2	16-bit linear	V	R/W	Yes	VSET 1)
VOUT_TRIM	0x22	2	16-bit linear	V	R/W	Yes	0.000V
VOUT_CAL_OFFSET	0x23	2	16-bit linear	V	R/W	Yes	0.000V
VOUT_MAX	0x24	2	16-bit linear	V	R/W	Locked	2.008V
VOUT_MARGIN_HIGH	0x25	2	16-bit linear	V	R/W	Yes	1.05 x VSET
VOUT_MARGIN_LOW	0x26	2	16-bit linear	V	R/W	Yes	0.95 x VSET
VOUT_TRANSITION_RATE	0x27	2	11-bit linear	V/ms	R/W	Yes	1V/ms
MAX_DUTY	0x32	2	11-bit linear	%	R/W	Locked	50%
POWER_MODE	0x34	1	bit field		R/W	Yes	0x00
INTERLEAVE	0x37	2	bit field		R/W	Yes	0x0000
VOUT_OV_FAULT_LIMIT	0x40	2	16-bit linear	V	R/W	Yes	2.4V
VOUT_OV_FAULT_RESPONSE	0x41	1	bit field		R/W	Yes	0xB8
VOUT_OV_WARN_LIMIT	0x42	2	16-bit linear	V	R/W	Yes	1.1 x VSET
VOUT_UV_WARN_LIMIT	0x43	2	16-bit linear	V	R/W	Yes	0.9 x VSET
VOUT_UV_FAULT_LIMIT	0x44	2	16-bit linear	V	R/W	Yes	0.4V
VOUT_UV_FAULT_RESPONSE	0x45	1	bit field		R/W	Yes	0xB8
IOUT_OC_WARN_LIMIT	0x4A	2	11-bit linear	A	R/W	Yes	95A
IOUT_UC_FAULT_LIMIT	0x4B	2	11-bit linear	A	R/W	Locked	-95A
OT_FAULT_LIMIT	0x4F	2	11-bit linear	°C	R/W	Locked	110
OT_FAULT_RESPONSE	0x50	1	bit field		R/W	Yes	0xB8
OT_WARN_LIMIT	0x51	2	11-bit linear	°C	R/W	Yes	100°C
UT_WARN_LIMIT	0x52	2	11-bit linear	°C	R/W	Yes	-45°C
UT_FAULT_LIMIT	0x53	2	11-bit linear	°C	R/W	Yes	-50°C

PMBus Command Summary

This section provides a summary of the DJT090A0X43 commands followed by their detailed description. The commands are outlined in the order of increasing command codes.

PMBUS CMD	CMD CODE	DATA BYTES	DATA FORMAT	DATA UNITS	TRANSFER TYPE	PROTECTABLE	DEFAULT VALUE
UT_FAULT_RESPONSE	0x54	1	bit field		R/W	Yes	0xB8
VIN_OV_FAULT_LIMIT	0x55	2	11-bit linear	V	R/W	Locked	16.0V
VIN_OV_FAULT_RESPONSE	0x56	1	bit field		R/W	Yes	0x80
VIN_OV_WARN_LIMIT	0x57	2	11-bit linear	V	R/W	Yes	14.5
VIN_UV_WARN_LIMIT	0x58	2	11-bit linear	V	R/W	Yes	6.8V
VIN_UV_FAULT_LIMIT	0x59	2	11-bit linear	V	R/W	Yes	5.8V
VIN_UV_FAULT_RESPONSE	0x5A	1	bit field		R/W	Yes	0xB8
POWER_GOOD_ON	0x5E	2	11-bit linear	V	R/W	Yes	0.90 x VSET
TON_DELAY	0x60	2	11-bit linear	ms	R/W	Yes	0ms
TON_RISE	0x61	2	11-bit linear	ms	R/W	Yes	10ms
TOFF_DELAY	0x64	2	11-bit linear	ms	R/W	Yes	0ms
TOFF_FALL	0x65	2	11-bit linear	ms	R/W	Yes	10ms
STATUS_BYTE	0x78	1	bit field		R		
STATUS_WORD	0x79	2	bit field		R		
STATUS_VOUT	0x7A	1	bit field		R		
STATUS_IOUT	0x7B	1	bit field		R		
STATUS_INPUT	0x7C	1	bit field		R		
STATUS_TEMPERATURE	0x7D	1	bit field		R		
STATUS_CML	0x7E	1	bit field		R		
STATUS_MFR_SPECIFIC	0x80	1	bit field		R		
READ_VIN	0x88	2	11-bit linear	V	R		
READ_IIN	0x89	2	11-bit linear	A	R		
READ_VOUT	0x8B	2	11-bit linear	V	R		
READ_IOUT	0x8C	2	11-bit linear	A	R		
READ_TEMPERATURE_1	0x8D	2	11-bit linear	°C	R		
READ_DUTY_CYCLE	0x94	2	11-bit linear	%	R		
READ_FREQUENCY	0x95	2	11-bit linear	kHz	R		
READ_POUT	0x96	2	11-bit linear	W	R		
READ_PIN	0x97	2	11-bit linear	W	R		
PMBUS_REVISION	0x98	1	bit field		R		1.3
MFR_ID	0x99	32	bit field		R/W	Yes	
MFR_MODEL	0x9A	32	bit field		R	Locked	DJT090A0X43-SRPZ
MFR_REVISION	0x9B	32	bit field		R/W	Yes	
MFR_LOCATION	0x9C	32	bit field		R/W	Yes	

PMBus Command Summary

This section provides a summary of the DJT090A0X43 commands followed by their detailed description. The commands are outlined in the order of increasing command codes.

PMBUS CMD	CMD CODE	DATA BYTES	DATA FORMAT	DATA UNITS	TRANSFER TYPE	PROTECTABLE	DEFAULT VALUE
MFR_DATE	0x9D	32	bit field		R/W	Yes	
MFR_SERIAL	0x9E	32	bit field		R	Locked	YYxxMMxxxxxx
USER_DATA_00	0xB0	32	bit field		R/W	Yes	
USER_DATA_01	0xB1	32	bit field		R/W	Yes	
USER_DATA_02	0xB2	32	bit field		R/W	Yes	
USER_CONFIG	0xD1	2	bit field		R/W	Yes	0x0C04
DDC_CONFIG	0xD3	2	bit field		R/W	Yes	0xXX00
POWER_GOOD_DELAY	0xD4	2	bit field	ms	R/W	Yes	1ms
ASCR_ADVANCED	0xD5	2	bit field		R/W	Yes	0x10FA
SNAPSHOT_FAULT_MASK	0xD7	2	bit field		R/W	Yes	0x0000
OVUV_CONFIG	0xD8	1	bit field		R/W	Yes	0x02
MFR_SMBALERT_MASK	0xDB	7	bit field		R/W	Yes	0x00...00
ASCR_CONFIG	0xDF	4	bit field		R/W	Yes	0x5050010E
SEQUENCE	0xE0	2	bit field		R/W	Yes	0x0000
TRACK_CONFIG	0xE1	1	bit field		R/W	Yes	0x00
DDC_GROUP	0xE2	4	bit field		R/W	Yes	0x00000000
MFR_IOUT_OC_FAULT_RESPONSE	0xE5	1	bit field		R/W	Yes	0xB8
MFR_IOUT_UC_FAULT_RESPONSE	0xE6	1	bit field		R/W	Yes	0xBA
IOUT_AVG_OC_FAULT_LIMIT	0xE7	2	11-bit linear	A	R/W	Locked	101A
IOUT_AVG_UC_FAULT_LIMIT	0xE8	2	11-bit linear	A	R/W	Locked	-99A
SNAPSHOT	0xEA	32	bit field		R/W	Yes	
SNAPSHOT_CONTROL	0xF3	2	bit field		R/W	Yes	0x0800
PINSTRAP_READ_STATUS	0xF5	5	bit field		R	Yes	
SECURITY_CONTROL	0xFA	1	bit field		R/W	No	0x01
PASSWORD	0xFB	9	bit field		W	No	
WRITE_PROTECT	0xFD	32	bit field		R/W	Yes	

NOTES: 1) Output voltage setting according to VSET/SA pin-strap table.

Detailed Description of Supported PMBus Commands

Each command will have the following basic information.
Command Name (Code)
Definition
Data format
Factory default
Additional information may be provided if necessary.

OPERATION (0x01)

Definition: Sets Enable, Disable, and VOUT Margin settings. Writing Immediate off turns off the output and ignore TOFF_DELAY and TOFF_FALL settings. With Immediate off, both the GH and GL gate drive signals are set to 0 without delay (both FETs turned off). This command is not stored like other PMBus commands. When this command is written, the command takes effect, but if a STORE _USER_ALL written and the device is re-enabled, the OPERATION settings may not be the same settings that were written before the device was re-enabled. This command only reflects the last value written. If the state of the enable is desired, the STATUS_BYTE/WORD can be read.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	N/A							

Bits	Purpose	Bit Value	Meaning
7	Controls Device Output State	0	Off (see ON_OFF_CONFIG)
		1	On (see ON_OFF_CONFIG)
6	Turn Off Behavior. This Bit is Ignored if Bit 7 = 1	0	Device is immediately turned off. TOFF_DELAY and TOFF_FALL are ignored.
		1	Device is turned off observing TOFF_DELAY and TOFF_FALL
5:4	Output Voltage	00	VOUT is set by VOUT_COMMAND
		01	VOUT is set by VOUT_MARGIN_LOW
		10	VOUT is set by VOUT_MARGIN_HIGH
		11	Not used
3:2	Margin Fault Response	00	Not used
		01	Faults caused by VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW are ignored.
		10	Faults caused by VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW are acted on
		11	Not used
1:0	Not used	00	Not used

ON_OFF_CONFIG (0x02)

Definition: Configures the interpretation and coordination of the OPERATION command and the ENABLE pin (EN). When Bit 0 is set to 1 (turn off the output immediately), the TOFF_FALL setting is ignored. Note that with Bits 3 and 2 set to “1”, the device turns on only when the EN pin is high and the OPERATION command instructs the device to enable. With Bits 3 and 2 set to “1”, the device turns off when EN is set low or the OPERATION command instructs the device to disable.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	1	0	1	1	0

Bits	Purpose	Bit Value	Meaning
7:5	Not Used	000	Not Used
4	Sets the default for the on/off behavior of the device to be controlled by the EN pin and OPERATION command.	0	Device is always on
		1	Device does not power up until commanded by the EN pin and OPERATION command (as programmed in Bits [3:0]).
3	Controls how the device responds to commands received through the PMBus.	0	Device ignores the on/off portion of the OPERATION command
		1	To start, the device requires that the on/off portion of the OPERATION command is instructing the device to enable the output. Depending on Bit 2, the device may also require the EN pin to be asserted for the device to start and enable the output.
2	Controls how the device responds to the EN pin.	0	Device ignores the EN pin (on/off controlled only by the Operation command).
		1	Device requires the EN pin to be asserted to start the unit. Depending on Bit 3, the OPERATION command may also be required to instruct the device to start before the output is energized.
1	Polarity of ENABLE pin	0	Not Used
		1	Active high only
0	ENABLE pin action when commanding the unit to turn off	0	Use the configured ramp-down settings (“soft-off”)
		1	Turn off the output immediately

CLEAR_FAULTS (0x03)

Definition: Clears all fault bits in all registers and releases the SALRT pin (if asserted) simultaneously. If a fault condition still exists, the bit reasserts immediately. This command does not restart a device if it has shut down, it only clears the faults.

STORE_DEFAULT_ALL (0x11)

Definition: Stores all current PMBus values from the operating memory into the nonvolatile DEFAULT store memory. To clear the DEFAULT store, perform a RESTORE_FACTORY then STORE_DEFAULT_ALL. To add to the DEFAULT store, perform a RESTORE_DEFAULT_ALL, write commands to be added, then STORE_DEFAULT_ALL. This command should not be used during device operation, the device is unresponsive for 100ms while storing values.

RESTORE_DEFAULT_ALL (0x12)

Definition: Restores PMBus settings from the nonvolatile DEFAULT store memory into the operating memory. These settings are loaded during at power-up if not superseded by settings in USER store. Security level is changed to Level 1 following this command. This command should not be used during device operation, the device is unresponsive for 100ms while storing values.

STORE_USER_ALL (0x15)

Definition: Stores all PMBus settings from the operating memory to the nonvolatile USER store memory. To clear the USER store, perform a RESTORE_FACTORY then STORE_USER_ALL. To add to the USER store, perform a RESTORE_USER_ALL, write commands to be added, then STORE_USER_ALL. This command should not be used during device operation; the device is unresponsive for 100ms while storing values.

RESTORE_USER_ALL (0x16)

Definition: Restores all PMBus settings from the USER store memory to the operating memory. Command performed at power-up. Do not use this command during device operation; the device is unresponsive for 100ms while restoring values.

CAPABILITY (0x19)

Definition: Reports some of the device's communications capabilities and limits.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	1	0	1	0	0	0	0
Bits	Purpose			Bit Value	Meaning			
7	Packet Error Checking			0	Packet Error Checking not supported.			
				1	Packet Error Checking is supported.			
6:5	Maximum Bus Speed			10	Maximum supported bus speed is 1MHz			
4	SMBALERT#			0	The device does not have a SMBALERT# pin and does not support the SMBus Alert Response protocol.			
				1	The device has a SMBALERT# pin and supports the SMBus Alert Response protocol.			
3	Numeric Format			0	Numeric data is in LINEAR or DIRECT format.			
				1	Numeric data is in IEEE Half Precision Floating Point Format.			
2	AVSBus Support			0	AVSBus is not supported.			
				1	AVSBus is supported.			
1:0	Not Used			00	Not used			
Note: If Bit 7 is zero, then the rest of the bits are reported as "0".								

Detailed Description of Supported PMBus Commands

VOUT_MODE (0x20)

Definition: Reports the VOUT mode and provides the exponent used in calculating several VOUT settings.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	1	0	0	1	1
Mode	Bits 7:5	Bits 4:0 (Parameter)`						
Linear	000	5-bit two's complement exponent for the mantissa delivered as the data bytes for an output voltage related command.						

VOUT_COMMAND (0x21)

Definition: Sets or reports the target output voltage. The integer value is multiplied by 2 raised to the power of -13h. This command cannot be set higher than VOUT_MAX. If a value is written to this command below or above the range given below, the device sets the value to the lower or upper limit respectively, a warning is recorded in STATUS_VOUT.

Units: V

Equation: VOUT = VOUT_COMMAND × 2^{-13}

Range: 0.45V to VOUT_MAX

Example: VOUT_COMMAND = 699Ah = 27034 Target voltage equals 27034 × 2-13 = 3.3V

Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	VSET/SA Pin-strap Setting															

VOUT_TRIM (0x22)

Definition: Applies a fixed trim voltage to the output voltage command value. This command is typically used by the manufacturer of a power supply subassembly to calibrate a device in the subassembly circuit. The two bytes are formatted as a two's complement binary mantissa, used in conjunction with the exponent of -13h. Values outside of the range are not accepted.

Units: V

Equation: VOUT trim = VOUT_TRIM × 2^{-13}

Range: ±0.15V

Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VOUT_CAL_OFFSET (0x23)

Definition: Applies a fixed offset voltage to the output voltage command value. This command is typically used by the user to calibrate a device in the application circuit. The two bytes are formatted as a two's complement binary mantissa, used in conjunction with the exponent of -13h. Values outside of the range are not accepted.

Units: V

Equation: VOUT calibration offset = VOUT_CAL_OFFSET × 2^{-13}

Range: ±0.15V

Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VOUT_MAX (0x24)

Definition: Sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output overprotection. A VOUT_COMMAND greater than the existing VOUT_MAX is not set and VOUT_COMMAND remains the same. If a VOUT_MAX is sent less than the current VOUT_COMMAND, output voltage is limited to VOUT_MAX.

Units: V

Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	2.008V															

VOUT_MARGIN_HIGH (0x25)

Definition: Sets the value of the VOUT during a margin high. This VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to "Margin High". Values outside of the range are not accepted.

Units: V
Equation: VOUT margin high = VOUT_MARGIN_HIGH x 2^{-13}
Range: 0.1V to VOUT_MAX

Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1.05 x VSET/SA pin-strap setting															

VOUT_MARGIN_LOW (0x26)

Definition: Sets the value of the VOUT during a margin low. This VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin Low”. Values outside of the range are not accepted.

Units: V
Equation: VOUT margin low = VOUT_MARGIN_LOW
Range: 0.1V to VOUT_MAX

Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.95 x VSET/SA pin-strap setting															

VOUT_TRANSITION_RATE (0x27)

Definition: Sets the rate at which the output should change for any reason beside enable/disable such as a change to VOUT_COMMAND, or a margin change. The maximum possible positive value of the two data bytes indicates that the device should make the transition as quickly as possible. This commanded rate does not apply when the device is commanded to turn on or to turn off. Values outside of the range are not accepted.

Units: V/ms

Equation: VOUT_TRANSITION_RATE = $Y \times 2^N$

Range: 0.1 to 4V/ms

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0

MAX_DUTY (0x32)

Definition: Sets the maximum allowable duty cycle of the PWM output. NOTE: MAX_DUTY should not be used to set the output voltage of the device. VOUT_COMMAND is the proper method to set the output voltage. Values outside of the range are not accepted. It is locked to 50%.

Units: Percent (%)

Equation: MAX_DUTY = $Y \times 2^N$

Range: 0 to 100%

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	0	0	1	1	0	0	1	0	0	0	0	0

Detailed Description of Supported PMBus Commands

POWER_MODE (0x34)

Definition: Enables and disables Diode Emulation Mode (DEM).

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0
Bits	Purpose			Bit Value	Meaning			
7:1	Not Used			0	Packet Error Checking not supported.			
0	Maximum Efficiency			1	Packet Error Checking is supported.			
				0	Maximum supported bus speed is 1MHz			

INTERLEAVE (0x37)

Definition: Configures the phase offset of a device that is sharing a common SYNC clock with other devices. A desired phase position is specified. Interleave is used for setting the phase offset between individual devices, current sharing groups, and/or combinations of devices and current sharing groups. For devices within single current sharing group, the phase offset is set automatically by default.

Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	Last 4 bits of PMBus Address			

Bits	Purpose	Value	Description
15:8	Not Used	0	Not used
7:4	Not Used	0	Not used
3:0	Position in Group (Interleave Order)	0 to 15d	Sets position of the device's rail within the group. A value of 0 is interpreted as 16. Position 1 has a 22.5 degree offset.

VOUT_OV_FAULT_LIMIT (0x40)

Definition: Sets the V_{out} overvoltage fault threshold. VOUT_OV_WARN_LIMIT must be set below the VOUT_OV_FAULT_LIMIT in order for fault responses with restart attempts to function properly. When the VOUT_OV_FAULT_RESPONSE is set to retry, a retry is not attempted until the output voltage has fallen below the VOUT_OV_WARN_LIMIT. In response to the VOUT_OV_FAULT_LIMIT being exceeded, the device: Sets the VOUT bit in STATUS_WORD, Sets the VOUT_OV_FAULT bit in STATUS_VOUT, and notifies the host. Values outside of the range are not accepted.

Units: V

Equation: VOUT OV fault limit = VOUT_OV_FAULT_LIMIT $\times 2^{-13}$

Range: 0V to 6.0V

Format	**Linear-16 Unsigned**															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	2.4V															

VOUT_OV_FAULT_RESPONSE (0x41)

Definition: Configures the VOUT overvoltage fault response between latch off or retry infinitely. The delay time is the time between fault detected to restart attempts.

Format	**Bit Field**							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	1	1	1	0	0	0

Bits	Purpose	Bit Value	Description
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the	00-01,11	Not used
5:3	Retry Setting	00-01,11	Not used
		001-111	Attempts to restart continuously, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the output voltage falls below the VOUT_OV_WARN_LIMIT. The time between the start of each attempt to restart is set by the value in Bits [2:0] multiplied by 35ms.
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

VOUT_OV_WARN_LIMIT (0x42)

Definition: Sets the VOUT overvoltage warning threshold. VOUT_OV_WARN_LIMIT must be set below the VOUT_OV_FAULT_LIMIT in order for fault responses with restart attempts to function properly. When the VOUT_OV_FAULT_RESPONSE is set to retry, a retry is not attempted until the output voltage has fallen below the VOUT_OV_WARN_LIMIT. In response to the VOUT_OV_WARN_LIMIT being exceeded, the device: Sets the VOUT bit in STATUS_WORD, sets the VOUT_OV_WARNING bit in STATUS_VOUT and notifies the host. Values outside of the range are not accepted. In the case of a fast VOUT overvoltage transition, a VOUT_OV_WARN_LIMIT fault may not be recorded.

Units: V

Equation: VOUT UV fault limit = VOUT_UV_FAULT_LIMIT × 2^{-13}

Range: 0V to 5.5V

Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1.08 x VSET/SA pin-strap setting															

VOUT_UV_WARN_LIMIT (0x43)

Definition: Sets the VOUT undervoltage fault threshold. This fault is masked during ramp, before power-good is asserted or when the device is disabled. VOUT_UV_FAULT_LIMIT must be set to a value below VOUT_UV_WARN_LIMIT and POWER_GOOD_ON. In response to the VOUT_UV_FAULT_LIMIT being exceeded, the device: Sets the VOUT bit in STATUS_WORD, sets the VOUT_UV_FAULT bit in STATUS_VOUT and notifies the host. Values outside of the range are not accepted.

Units: V

Equation: VOUT UV fault limit = VOUT_UV_FAULT_LIMIT × 2^{-13}

Range: 0V to 5.5V

Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.88 x VSET/SA pin-strap setting															

VOUT_UV_FAULT_LIMIT (0x44)

Definition: Sets the VOUT undervoltage fault threshold. This fault is masked during ramp, before power-good is asserted or when the device is disabled. VOUT_UV_FAULT_LIMIT must be set to a value below VOUT_UV_WARN_LIMIT and POWER_GOOD_ON. In response to the VOUT_UV_FAULT_LIMIT being exceeded, the device: Sets the VOUT bit in STATUS_WORD, sets the VOUT_UV_FAULT bit in STATUS_VOUT and notifies the host. Values outside of the range are not accepted.

Units: V

Equation: VOUT UV fault limit = VOUT_UV_FAULT_LIMIT × 2^{-13}

Range: 0V to 5.5V

Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.4V															

VOUT_UV_FAULT_RESPONSE (0x45)

Definition: Configures the VOUT undervoltage fault response. Note that VOUT UV faults can only occur after Power-good (PG) has been asserted. Under some circumstances this causes the output to stay fixed below the power-good threshold indefinitely. If this behavior is undesired, use setting 80h. The delay time is the time between fault detected to restart attempts. TON_DELAY is still observed during a retry attempt after the retry delay has expired.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	1	1	1	0	0	0

Bits	Purpose	Bit Value	Meaning
7:6	Response Behavior: the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01,11	Not used
		10	Disable and Retry according to the setting in Bits [5:3].
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-111	Attempts to restart continuously, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. The time between the start of each attempt to restart is set by the value in Bits [2:0] multiplied by 35ms.
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

IOUT_OC_WARN_LIMIT (0x4A)

Definition: Sets the IOUT peak overcurrent warn threshold. When a warn occurs the corresponding bit is set in STATUS_IOUT. Values outside of the range are not accepted. This limit must be set below IOUT_OC_FAULT_LIMIT in order for fault responses with restart attempts to function properly.

Units: Amps

Equation: IOUT_OC_WARN_LIMIT = $Y \times 2^N$

Range: 0A to 100A

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	95A															

IOUT_UC_FAULT_LIMIT (0x4B)

Definition: Sets the IOUT valley undercurrent fault threshold. This feature shares the UC fault bit operation (in STATUS_IOUT) and IOUT_UC_FAULT_RESPONSE with IOUT_AVG_UC_FAULT_LIMIT. Values outside of the range are not accepted.

Units: Amps

Equation: IOUT_OC_FAULT_LIMIT = $Y \times 2^N$

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	-99A															

OT_FAULT_LIMIT (0x4F)

Definition: Sets the temperature at which the device should indicate an over-temperature fault. OT_WARN_LIMIT must be set below the OT_FAULT_LIMIT in order for fault responses with restart attempts to function properly. When the OT_FAULT_RESPONSE is set to retry, a retry is not attempted until the temperature has fallen below the OT_WARN_LIMIT. In response to the OT_FAULT_LIMIT being exceeded, the device: Sets the TEMPERATURE bit in STATUS_WORD, sets the OT_FAULT bit in STATUS_TEMPERATURE and notifies the host. This fault is recorded in Bit 1 of STATUS_MFR_SPECIFIC. Values outside of the range are not accepted.

Units: Degrees Celsius (°C)

Equation: OT_FAULT_LIMIT = $Y \times 2^N$

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	110°C															

OT_FAULT_RESPONSE (0x50)

Definition: Instructs the device on what action to take in response to an over-temperature fault. The delay time is the time between fault detected and restart attempts.
Units: Retry time unit = 35ms

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	1	1	1	0	0	0
Bits	Purpose			Bit Value	Meaning			
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.			00-01,11	Not used			
				10	Disable and Retry according to the setting in Bits [5:3].			
5:3	Retry Setting			00-01,11	Not used			
				001-111	Attempts to restart continuously, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the temperature falls below the OT_WARN_LIMIT. The time between the start of each attempt to restart is set by the value in Bits [2:0].			
2:0	Retry Delay			000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.			

OT_WARN_LIMIT (0x51)

Definition: Sets the temperature at which the device should indicate an over-temperature warning alarm. OT_WARN_LIMIT must be set below the OT_FAULT_LIMIT in order for fault responses with restart attempts to function properly. When the OT_FAULT_RESPONSE is set to retry, a retry is not attempted until the temperature has fallen below the OT_WARN_LIMIT. In response to the OT_WARN_LIMIT being exceeded, the device: Sets the TEMPERATURE bit in STATUS_WORD, sets the OT_WARNING bit in STATUS_TEMPERATURE and notifies the host. Values outside of the range are not accepted.

Units: Degrees Celsius (°C)

Equation: $OT\_WARN\_LIMIT = Y \times 2^{N}$

Range: 0°C to +175°C

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	100°C															

UT_WARN_LIMIT (0x52)

Definition: Sets the temperature at which the device should indicate an under-temperature warning alarm. UT_WARN_LIMIT must be set above the UT_FAULT_LIMIT in order for fault responses with restart attempts to function properly. When the UT_FAULT_RESPONSE is set to retry, a retry is not attempted until the temperature has risen above the UT_WARN_LIMIT. In response to the UT_WARN_LIMIT being exceeded, the device: Sets the TEMPERATURE bit in STATUS_WORD, sets the UT_WARNING bit in STATUS_TEMPERATURE and notifies the host. Values outside of the range are not accepted.

Units: Degrees Celsius (°C)

Equation: UT_WARN_LIMIT = $Y \times 2^N$

Range: -55°C to +25°C

Format	**Linear-11**															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	-45°C															

UT_FAULT_LIMIT (0x53)

Definition: Sets the temperature, in degrees Celsius, at which the device should indicate an under-temperature fault. UT_WARN_LIMIT must be set above the UT_FAULT_LIMIT in order for fault responses with restart attempts to function properly. When the UT_FAULT_RESPONSE is set to retry, a retry is not attempted until the temperature has risen above the UT_WARN_LIMIT. Values outside of the range are not accepted.

Units: Degrees Celsius (°C)

Equation: UT_FAULT_LIMIT = $Y \times 2^N$

Range: -55°C to + 25°C

Format	**Linear-11**															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	-50°C															

UT_FAULT_RESPONSE (0x54)

Definition: Configures the under-temperature fault response as defined by the table below. The delay time is the time between fault detected and restart attempts.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	1	1	1	0	0	0

Bits	Purpose	Bit Value	Meaning
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01,11	Not used
		10	Disable and Retry according to the setting in Bits [5:3].
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-111	Attempts to restart continuously, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the temperature rises above UT_WARN_LIMIT. The time between the start of each attempt to restart is set by the value in Bits [2:0].
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

VIN_OV_FAULT_LIMIT (0x55)

Definition: Sets the VIN overvoltage fault threshold. VIN_OV_WARN_LIMIT must be set below the VIN_OV_FAULT_LIMIT in order for fault responses with restart attempts to function properly. When the VIN_OV_FAULT_RESPONSE is set to retry, a retry is not attempted until the input voltage has fallen below the VIN_OV_WARN_LIMIT. Values outside of the range are not accepted.

Units: Volts

Equation: $VIN\_OV\_FAULT\_LIMIT = Y \times 2^{N}$

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	16V															

VIN_OV_FAULT_RESPONSE (0x56)

Definition: Configures the VIN overvoltage fault response as defined by the table below.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	1	1	1	0	0	0

Bits	Purpose	Bit Value	Description
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01,11	Not used
		10	Disable and Retry according to the setting in Bits [5:3].
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-111	Attempts to restart continuously, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the temperature rises above VIN_OV_WARN_LIMIT. The time between the start of each attempt to restart is set by the value in Bits [2:0].
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

VIN_OV_WARN_LIMIT (0x57)

Definition: Sets the VIN overvoltage warning threshold as defined by the table below. VIN_OV_WARN_LIMIT must be set below the VIN_OV_FAULT_LIMIT in order for fault responses with restart attempts to function properly. When the VIN_OV_FAULT_RESPONSE is set to retry, a retry is not attempted until the input voltage has fallen below the VIN_OV_WARN_LIMIT. In response to the OV_WARN_LIMIT being exceeded, the device: Sets the NONE OF THE ABOVE and INPUT bits in STATUS_WORD, sets the VIN_OV_WARNING bit in STATUS_INPUT and notifies the host. Values outside of the range are not accepted.

Units: Volts

Equation: VIN_OV_FAULT_LIMIT = $Y \times 2^{N}$

Range: 0V to 18V

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	14.5V															

VIN_UV_WARN_LIMIT (0x58)

Definition: Sets the VIN undervoltage warning threshold. VIN_UV_WARN_LIMIT must be set above the VIN_UV_FAULT_LIMIT for fault responses with restart attempts to function properly. When the VIN_UV_FAULT_RESPONSE is set to retry, a retry is not attempted until the input voltage has risen above the VIN_UV_WARN_LIMIT. In response to the VIN_UV_WARN_LIMIT being exceeded, the device sets the NONE OF THE ABOVE and INPUT bits in STATUS_WORD, sets the VIN_UV_WARNING bit in STATUS_INPUT, and notifies the host. Values outside of the range are not accepted.

Units: V

Equation: VIN_UV_WARN_LIMIT = $Y \times 2^N$

Range: 0V to 16V

Format	**Linear-11**															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	6.8V															

VIN_UV_FAULT_LIMIT (0x59)

Definition: Sets the VIN undervoltage fault threshold. VIN_UV_WARN_LIMIT must be set above the VIN_UV_FAULT_LIMIT in order for fault responses with restart attempts to function properly. When the VIN_UV_FAULT_RESPONSE is set to retry, a retry is not attempted until the input voltage has risen above the VIN_UV_WARN_LIMIT. In response to the VIN_UV_FAULT_LIMIT being exceeded, the device: sets the NONE OF THE ABOVE and INPUT bits in STATUS_WORD, sets the VIN_UV_FAULT bit in STATUS_INPUT, and notifies the host. Values outside of the range are not accepted.

Units: V

Equation: VIN_UV_FAULT_LIMIT = $Y \times 2^N$

Range: 0V to 16V

Format	**Linear-11**															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	5.8V															

VIN_UV_FAULT_RESPONSE (0x5A)

Definition: Configures the VIN undervoltage fault response as defined by the table below. The delay time is the time between fault detected and restart attempts.

Bits	Purpose	Bit Value	Description
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01,11	Not used
		10	Disable and Retry according to the setting in Bits [5:3].
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-111	Attempts to restart continuously, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the temperature rises above VIN_UV_WARN_LIMIT. The time between the start of each attempt to restart is set by the value in Bits [2:0].
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

POWER_GOOD_ON (0x5E)

Definition: Sets the voltage threshold for power-good indication. Power-Good asserts when the output voltage exceeds POWER_GOOD_ON and de-asserts when the output voltage is less than VOUT_UV_FAULT_LIMIT. POWER_GOOD_ON should be set to a value above VOUT_UV_FAULT_LIMIT, and VOUT_UV_WARN_LIMIT. Values outside of the range are not accepted. Power-Good may not assert if the device is enabled for less than 2ms.

Units: Volts

Range: 0V to 5.5V

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.9 x VSET/SA pin-strap setting															

TON_DELAY (0x60)

Definition: Sets the delay time from when the device is enabled to the start of VOUT rise. Values outside of the range are not accepted.

Units: milliseconds (ms)

Equation: TON_DELAY = $Y \times 2^N$

Range: 0ms to 125ms

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	0ms															

TON_RISE (0x61)

Definition: Sets the rise time of VOUT after the TON_DELAY time has elapsed. Values outside of the range are not accepted.

Units: milliseconds (ms)

Equation: TON_RISE = $Y \times 2^N$

Range: 0ms to 125ms. Although values can be set below 0.50ms, rise time accuracy cannot be guaranteed. In addition, short rise times may cause excessive input and output currents to flow, thus triggering overcurrent faults at start-up.

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	10ms															

TOFF_DELAY (0x64)

Definition: Sets the delay time from DISABLE to start of VOUT_FALL. Values outside of the range are not accepted.

Units: milliseconds (ms)

Equation: TON_DELAY = $Y \times 2^N$

Range: 0ms to 125ms

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	0ms															

TOFF_FALL (0x65)

Definition: Sets the fall time for VOUT after the TOFF_DELAY has expired. Setting the TOFF_FALL to values less than 0.5ms causes the device to turn-off both the high and low-side FETs immediately after the expiration of the TOFF_DELAY time. Values outside of the range are not accepted.

Units: milliseconds (ms)

Equation: TOFF_FALL = $Y \times 2^N$

Range: 0ms to 125ms. Values less than 0.5ms causes the device to turn-off both the high and low-side FETs immediately after the expiration of the TOFF_DELAY time.

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	10ms															

STATUS_BYTE (0x78)

Definition: Returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE (78h) command.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

Bit Number	Status Bit Name	Description
7	Not Used	Not used
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory or logic fault has occurred.
0	Not used	Not used

STATUS_WORD (0x79)

Definition: Returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE command.

Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Status Bit Name	Description
15	VOUT	An output voltage fault or warning has occurred.
14	IOUT	An output current fault has occurred.
13	INPUT	An input voltage fault or warning has occurred.
12	MFR_SPECIFIC	A manufacturer specific fault or warning has occurred.
11	POWER_GOOD #	The POWER_GOOD signal, if present, is negated*
10	NOT USED	Not used
9	OTHER	A bit in STATUS_VOUT, STATUS_IOUT, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_CML, or STATUS_MFR_SPECIFIC is set.
8	Not Used	Not used
7	Not Used	Not used
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory, or logic fault has occurred.
0	Not Used	Not used

* If the POWER_GOOD# bit is set, this indicates that the POWER_GOOD signal, if present, is signaling that the output power is not good. POWER_GOOD may not assert if the device is enabled for less than 2ms.

STATUS_VOUT (0x7A)

Definition: Returns one data byte with the status of the output voltage. Note that warning bits may not be set when the corresponding fault bits are set. This can occur with rapidly changing fault waveforms.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0
Bit Number	Status Bit Name			Description				
7	VOUT_OV_FAULT			Indicates an output overvoltage fault.				
6	VOUT_OV_WARNING			Indicates an output overvoltage warning. May not be set when an overvoltage fault occurs.				
5	VOUT_UV_WARNING			Indicates an output undervoltage warning. May not be set when an undervoltage fault occurs.				
4	VOUT_UV_FAULT			Indicates an output undervoltage fault.				
3	VOUT_MAX_WARNING			Attempted to set VOUT_COMMAND greater than VOUT_MAX or below 0.1V.				
2:0	Not used			Not used				

STATUS_IOUT (0x7B)

Definition: Returns one data byte with the status of the output current. Note that warning bits may not be set when the corresponding fault bits are set. This can occur with rapidly changing fault waveforms.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0
Bit Number	Status Bit Name			Description				
7	IOUT_OC_FAULT			An output overcurrent fault has occurred.				
6	Not Used			Not used				
5	IOUT_OC_WARNING			An output overcurrent warning has occurred. May not be set when an output overcurrent fault occurs.				
4	IOUT_UC_FAULT			An output undercurrent fault has occurred.				
3:0	Not Used			Not used				

STATUS_INPUT (0x7C)

Definition: Returns one byte of information with a summary of input voltage related faults or warnings. Note that warning bits may not be set when the corresponding fault bits are set. This can occur with rapidly changing fault waveforms.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0
Bit Number	Status Bit Name			Description				
7	VIN_OV_FAULT			An input overvoltage fault has occurred.				
6	VIN_OV_WARNING			An input overvoltage warning has occurred. May not be set when an over-voltage fault occurs.				
5	VIN_UV_WARNING			An input undervoltage warning has occurred. May not be set when an un-dervoltage fault occurs.				
4	VIN_UV_FAULT			An input undervoltage fault has occurred.				
3:0	Not Used			Not used				

STATUS_TEMPERATURE (0x7D)

Definition: Returns one byte of information with a summary of any temperature related faults or warnings. Note that warning bits may not be set when the corresponding fault bits are set. This can occur with rapidly changing fault waveforms.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0
Bit Number	Status Bit Name			Description				
7	OT_FAULT			An over-temperature fault has occurred.				
6	OT_WARNING			An over-temperature warning has occurred. May not be set when an over-temperature fault occurs.				
5	UT_WARNING			An under-temperature warning has occurred. May not be set when an under-temperature fault occurs.				
4	UT_FAULT			An under-temperature fault has occurred.				
3:0	Not Used			Not used				

STATUS_CML (0x7E)

Definition: Returns one byte of information with a summary of any communications, logic, and/or memory errors. Status bits can only be cleared with the CLEAR_FAULTS command or by disabling, then re-enabling the device.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0
Bit Number	Description							
7	Invalid or unsupported PMBus command was received.							
6	The PMBus command was sent with invalid or unsupported data.							
5	A Packet Error Check (PEC) failed on a PMBus command.							
4:2	Not used							
1	A PMBus command tried to write to a read only or protected command, or too few or too many bytes were received for a given command.							
0	Not used							

STATUS_MFR_SPECIFIC (0x80)

Definition: Returns one byte of information providing the status of the device's voltage monitoring and clock synchronization faults.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0
Bit Number	Status Bit Name			Description				
7	Not Used			Not used				
6	Phase Fault			A phase in the current sharing group has failed, when configured as part of a current sharing rail.				
5	Not Used			Not used				
4	DDC fault			An error was detected on the DDC bus.				
3	External Switching Period Fault			Loss of external clock synchronization has occurred.				
2	Fault Group			A fault was spread using DDC fault group				
1	Not Used			Not used				
0	Fault Bus			Device was shutdown by the enable pin when using the enable pin as a fault bus				

READ_VIN (0x88)

Definition: Returns the input voltage reading.

Units: V

Equation: READ_VIN = Y × 2^N

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A															

READ_IIN (0x89)

Definition: Returns the input current reading. This is a calculated value based on the output current, duty cycle, and IIN_CAL_OFFSET. It is not accurate when the device is in Diode Emulation Mode (DEM).

Units: A

Equation: READ_IIN = Y × 2^N

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A															

READ_VOUT (0x8B)

Definition: Returns the output voltage reading.

Units: V

Equation: READ_VOUT = READ_VOUT × 2^{-13}

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default Value	N/A															

READ_IOUT (0x8C)

Definition: Returns the output current reading. No reading is returned if the PWM output is not active, that is, the output is not being regulated. It is not accurate when the device is in Diode Emulation Mode (DEM).

Units: A

Equation: READ_IOUT = Y × 2^N

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A															

READ_TEMPERATURE_1 (0x8D)

Definition: Returns the temperature reading internal to the device.

Units: °C

Equation: READ_TEMPERATURE_1 = Y × 2^N

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A															

READ_DUTY_CYCLE (0x94)

Definition: Reports the actual duty cycle of the converter while the device is enabled.

Units: %

Equation: READ_DUTY_CYCLE = Y × 2^N

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A															

READ_FREQUENCY (0x95)

Definition: Reports the actual configured switching frequency of the device.

Units: kHz

Equation: READ_FREQUENCY = Y × 2^N

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A															

READ_POUT (0x96)

Definition: Returns the calculated output power in Watts.

Units: W

Equation: READ_POUT = Y × 2^N

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A															

READ_PIN (0x97)

Definition: Returns the calculated input power in Watts.

Units: W

Equation: READ_PIN = Y × 2^N

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A															

PMBUS_REVISION (0x98)

Definition: Returns the revision of the PMBus Specification to which the device is compliant.

Default Value: 33h (Part 1 Revision 1.3, Part 2 Revision 1.3)

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	1	1	0	0	1	1
Bits 7:4	Part 1 Revision			Bits 3:0		Part 2 Revision		
0011	1.3			0011		1.3		

MFR_ID (0x99)

Definition: Sets a user defined identification string not to exceed 32bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.
Data Format: ASCII, ISO/IEC 8859-1

MFR_MODEL (0x9A)

Definition: Sets a user defined model string not to exceed 32bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.
Data Format: ASCII, ISO/IEC 8859-1

MFR_REVISION (0x9B)

Definition: Sets a user defined revision string not to exceed 32bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.
Data Format: ASCII. ISO/IEC 8859-1

MFR_LOCATION (0x9C)

Definition: Sets a user defined location identifier string not to exceed 32bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.
Data Format: ASCII. ISO/IEC 8859-1

MFR_DATE (0x9D)

Definition: Sets a user defined date string not to exceed 32bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.
Data Format: ASCII. ISO/IEC 8859-1

MFR_SERIAL (0x9E)

Definition: Sets a user defined serialized identifier string not to exceed 32bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.
Data Format: ASCII. ISO/IEC 8859-1

USER_DATA_00 (0xB0)

Definition: Sets a user defined data string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128bytes This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.
Data Format: ASCII. ISO/IEC 8859-1

USER_DATA_01 (0xB1)

Definition: Sets a user defined data string not to exceed 32bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128bytes This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.
Data Format: ASCII. ISO/IEC 8859-1

USER_DATA_02 (0xB2)

Definition: Sets a user defined data string not to exceed 32bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128bytes This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Data Format: ASCII. ISO/IEC 8859-1

USER_CONFIG (0xD1)

Definition: Configures several user-level features. This command should be saved immediately after being written to the desired user or default store. This is recommended when written as an individual command or as part of a series of commands in a configuration file or script.

Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0	0

Bits	Field Name	Value	Setting	Description
15:11	Minimum Duty Cycle	00000	0-31d	Set the Minimum Duty Cycle in percent (%). The percentage value is defined by the following expression: Minimum Duty Cycle = 2 X (Setting+1) / 512. This feature must be enabled by setting Bit 10 to 1 (enabled).
10	Minimum Duty Cycle Enable	0	Disable	Minimum duty cycle disabled
		1	Enable	Minimum duty cycle enabled
9	DEM Boot Cap Refresh	0	Disable	Low-side gate minimum pulse width disabled
		1	Enable	Low-side gate minimum pulse width enabled during diode emulation mode. This ensures that the top FET bootstrap capacitor is recharged every switch cycle.
8	Not Used	0	Not Used	Not used
7	Enable Fault Bus	0	Disable	Disable Fault Bus
		1	Enable	Enable Fault Bus
6	Not Used	0	Not Used	Not used
5	Power-Good Pin Configuration	0	Open Drain	0 = PG is open-drain output
		1	Push-Pull	1 = PG is push-pull output
4:3	Temp Fault Select	00	Internal temperature sensor selected	Select internal temperature sensor to determine temperature faults.
		01-11	Not Used	Not used
2	Not Used	0	Not Used	Not used
1:0	Sync Pin Configuration	00	Internal Clock	Use internal clock (frequency initially set with pin-strap)
		01	Use and Output Internal Clock	Use internal clock and output internal clock (not for use with pin-strap)
		10	External Clock	Use external clock
		11	Not Used	Not used

DDC_CONFIG (0xD3)

Definition: Configures DDC addressing and current sharing for up to eight phases. To operate as a 2-phase controller, set both phases (devices) to the same rail ID, set phases in rail to 2, then set each phase ID sequentially as 0 and 1. The devices automatically equally offset the phases in the rail. For example, in a 2-phase rail the phases are offset by 180 degrees. When a device is configured to be part of a current sharing rail, DDC_GROUP must be configured such that all phases in the current sharing rail have the same DDC_GROUP ID and are set to respond to DDC_GROUP OPERATION and VOUT COMMAND messages. See the DDC_GROUP command for more details.

Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	Lower 5 bits of device address					0	0	0	0	0	0	0	0

Bits	Field Name	Value	Setting	Description
15:13	Phase ID	0 to 7	0	Sets the output's phase position within the rail
12:8	Rail ID	0 to 31d	0	Identifies the device as part of a current sharing rail (Shared output)
7:3	Not Used	00	00	Not used
2:0	Phases In Rail	0 to 7	0	Identifies the number of phases on the same rail (+1)

POWER_GOOD_DELAY (0xD4)

Definition: Sets the delay applied between the output exceeding the PG threshold (POWER_GOOD_ON) and asserting the PG pin. The delay time can range from 0ms up to 125ms. Values outside of the range are not accepted.

Units: milliseconds (ms)

Equation: POWER_GOOD_DELAY = $Y \times 2^N$

Range: 0ms to 125ms

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0

ASCR_ADVANCED (0xD5)

Detailed Description of Supported PMBus Commands

Definition: Allows user configuration of advanced ASCR settings which have an impact on PWM jitter. ASCR Threshold sets the level that determines when the output voltage is considered to be at a steady state level. ASCR Threshold gain sets the ASCR gain reduction amount when the output voltage is considered to be in the steady state condition.

Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Not Used		ASCR TH Gain Setting				ASCR Threshold Setting									
Default Value	0	0	0	1	0	0	0	0	1	1	1	1	1	0	1	0

Bits	Purpose	Value	Description
15:14	Not used	00	Not used
13:12	ASCR Threshold Gain Select Setting	00	Divide by 1
		01	Divide by 2
		10	Divide by 4
		11	Divide by 8
11:0	ASCR Threshold Setting	0-FFFh	ASCR Threshold

SNAPSHOT_FAULT_MASK (0xD7)

Definition: Prevents faults from causing a SNAPSHOT event (and store) from occurring.

Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Status Bit Name	Description
15	Fault Phase	Ignore phase faults in a current sharing rail
14	Fault Group	Ignore rail faults in a fault spreading group
13	Fault CPU	Ignore CPU faults
12	Fault UT	Ignore under-temperature faults
11	Fault OT	Ignore over-temperature faults
10	Fault peak OC	Ignore peak output overcurrent faults
9	Fault peak UC	Ignore peak output undercurrent faults
8	Fault EN pin as fault bus	Ignore Enable pin faults when the Enable pin is used as a fault bus
7	Fault VIN_OV	Ignore input overvoltage faults
6	Fault VOUT_OV	Ignore output overvoltage faults
5	Fault VOUT_UV	Ignore output undervoltage faults
4	Not Used	Not Used
3	Fault Sync	Ignore loss of synchronization faults
2	Fault VIN_UV	Ignore Input undervoltage faults
1	Fault IOUT_OC	Ignore output average overcurrent faults
0	Fault IOUT_UC	Ignore output average undercurrent faults

OVUV_CONFIG (0xD8)

Definition: Configures the output voltage OV and UV fault detection parameters.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	1	0

Bits	Purpose	Bit Value	Description
7:4	Not Used	0	Not used
3:0	Defines the number of consecutive limit violations required to declare an OV or UV fault	N	N+1 consecutive OV or UV violations initiate a fault response

MFR_SMBALERT_MASK (0xDB)

Definition: Used to prevent faults from activating the SALRT pin. The bits in each byte correspond to a specific fault type as defined in the STATUS command.

Format	Bit Field							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Bit Position	55	54	53	52	51	50	49	48
Default Value Byte 6	0	0	0	0	0	0	0	0
Bit Position	47	46	45	44	43	42	41	40
Default Value Byte 5	0	0	0	0	0	0	0	0
Bit Position	39	38	37	36	35	34	33	32
Default Value Byte 4	0	0	0	0	0	0	0	0
Bit Position	31	30	29	28	27	26	25	24
Default Value Byte 3	0	0	0	0	0	0	0	0
Default Value Byte 3	0	0	0	0	0	0	0	0
Bit Position	23	22	21	20	19	18	17	16
Default Value Byte 2	0	0	0	0	0	0	0	0
Bit Position	15	14	13	12	11	10	9	8
Default Value Byte 1	0	0	0	0	0	0	0	0
Bit Position	7	6	5	4	3	2	1	0
Default Value Byte 0	0	0	0	0	0	0	0	0

Byte	Status Byte Name	Description
6	STATUS_MFR_SPECIFIC	Mask manufacturer specific faults as identified in the STATUS_MFR_SPECIFIC byte.
5	STATUS_OTHER	Not used
4	STATUS_CML	Mask communications, memory or logic specific faults as identified in the STATUS_CML byte.
3	STATUS_TEMPERATURE	Mask temperature specific faults as identified in the STATUS_TEMPERATURE byte
2	STATUS_INPUT	Mask input specific faults as identified in the STATUS_INPUT byte
1	STATUS_IOUT	Mask output current specific faults as identified in the STATUS_IOUT byte
0	STATUS_VOUT	Mask output voltage specific faults as identified in the STATUS_VOUT byte

ASCR_CONFIG (0xDF)

Definition: Allows user configuration of ASCR settings. ASCR gain and residual value are automatically set by the DJT090A0X43-SRPZ based on input voltage and output voltage. ASCR Gain is analogous to bandwidth, ASCR Residual is analogous to damping. To improve load transient response performance, increase ASCR Gain. To lower transient response overshoot, increase ASCR Residual. Increasing ASCR gain can result in increased PWM jitter and should be evaluated in the application circuit. Excessive ASCR gain can lead to excessive output voltage ripple. Increasing ASCR Residual to improve transient response damping can result in slower recovery times, but does not affect the peak output voltage deviation. Typical ASCR Gain settings range from 100 to 1000, and typical ASCR Residual settings range from 10 to 90.

Format	Bit Field															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Integral Gain								ASCR Residual							
Default Value	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	ASCR Gain															
Default Value	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0

Bits	Purpose	Value	Description
31:24	Integral Gain	0-7Fh	Error signal gain
23:16	ASCR residual	0-7Fh	ASCR residual
15:0	ASCR gain	0-FFFFh	ASCR gain

SEQUENCE (0xE0)

Definition: Identifies the Rail DDC ID of the prequel and sequel rails when performing multi-rail sequencing. The device enables its output when its EN or OPERATION enable state, as defined by ON_OFF_CONFIG, is set and the prequel device has issued a power-good event on the DDC bus as a result of the prequel's Power-Good (PG) signal going high. The device disables its output (using the programmed delay values) when the sequel device has issued a power-down event on the DDC bus at the completion of its ramp-down (its output voltage is 0V).

The data field is a two-byte value. The most significant byte contains the 5-bit Rail DDC ID of the prequel device. The least significant byte contains the 5-bit Rail DDC ID of the sequel device. The most significant bit of each byte contains the enable of the prequel or sequel mode.

Fault spreading is not automatic in devices that have a prequel or sequel. When a device shuts down due to a fault, it does not disable its output and does not send a message to its sequel or prequel to disable. If fault spreading behavior is desired, the DDC_GROUP commands should be used. Automatic fault retry is not supported for fault spreading or sequencing groups.

A device that is tracking another device (tracking the signal on its VTRK pin), cannot be a sequel or prequel in a sequencing group.

Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Value	Setting	Description
15	Prequel Enable	0	Disable	Disable, no prequel preceding this rail
		1	Enable	Enable, prequel to this rail is defined by Bits 12:8
14:13	Not Used	0	Not Used	Not used
12:8	Prequel Rail DDC ID	0-31d	DDC ID	Set to the DDC ID of the prequel rail
7	Sequel Enable	0	Disable	Disable, no sequel following this rail
		1	Enable	Enable, sequel to this rail is defined by Bits 4:0
6:5	Not Used	0	Not Used	Not used
4:0	Sequel Rail DDC ID	0-31d	DDC ID	Set to the DDC ID of the sequel rail

TRACK_CONFIG (0xE1)

Definition: Configures the voltage tracking modes of the device. When tracking, the TOFF_DELAY in the tracking device must be greater than TOFF_DELAY + TOFF_FALL in the device being tracked. When configured to track, VOUT_COMMAND must be set to the desired steady state output voltage. Devices that are providing the VTRK signal and the tracking device must have their EN pins tied together. If PMBus enabling is used using the OPERATION command, the DDC_GROUP must be configured on both devices with the same BROADCAST_OPERATION group ID (Bits 12:8) and have BROADCAST_OPERATION response enabled (Bit 13 set to 1).

Pre-biasedtracking: The device tracking the voltage applied to the VTRK pin (called the “tracker”) slews to whatever voltage is present at the VTRK pin when the tracker is enabled. Depending on how much pre-bias voltage is present on the VTRK pin, the output voltage may overshoot, or an overcurrent fault may occur as the device attempts to rapidly track to this voltage. For this reason, it is recommended that prebias voltage on the VTRK pin be no more than 20% of the tracker’s desired steady state output voltage.

Sequencing: A tracking device cannot be part of a sequencing group; it cannot be a prequel or sequel.

Margining: VOUT_MARGIN_HIGH and VOUT_MARGIN_LOW do not apply to devices that are tracking.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0
Bits	Field Name		Value	Setting	Description			
7	Voltage Tracking Control		0	Disable	Tracking is disabled.			
			1	Enable	Tracking is enabled.			
6:3	Not Used		000	Not Used	Not used			
2	Tracking Ratio Control		0	100%	Output tracks at 100% ratio of VTRK input.			
			1	50%	Output tracks at 50% ratio of VTRK input.			
1	Target Limit		0	Target Voltage	Output voltage is limited by target voltage.			
			1	VTRK Voltage	Output voltage is limited by VTRK voltage.			
0	Not Used		0	Not Used	Not used			

DDC_GROUP (0xE2)

Definition: Rails (output voltages) are assigned Group numbers to share specified behaviors. The DDC_GROUP command configures fault spreading group ID and enable, broadcast OPERATION group ID and enable, and broadcast VOUT_COMMAND group ID and enable. Note that DDC Groups are separate and unique from DDC Rail IDs .Current sharing rails must be in the same DDC Group to respond to broadcast VOUT_COMMAND and OPERATION commands.

Devices in a current sharing rail are not required to have the same POWER_FAIL group ID. Faults are automatically spread when a device is configured to be part of a current sharing rail. If you want a current sharing rail to spread faults with another rail, all the devices in that current sharing rail should have the same POWER_FAIL group ID as the rail it is expected to share POWER_FAIL faults with. Automatic fault retry behavior is not supported for fault spreading or sequencing groups.

When a device is set to ignore DDC GROUP messages, the device still transmits DDC messages with its own DDC ID. Note that the default DDC_GROUP ID is set to 0d, which is a valid DDC_GROUP number, so even a device with the default setting (ignore all DDC groups, all DDC group IDs set to 0d) still transmits DDC GROUP messages, despite ignoring DDC_GROUP messages from other devices on the DDC bus.

Format	Bit Field															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Not Used										EN	VOUT_COMMAND Group ID				
Default Value	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Not Used		EN	OPERATION Group ID					Not Used		EN	Power Fail Group ID				
Default Value	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1

Bits	Purpose	Value	Description
31:22	Not Used	00	Not used
21	BROADCAST_VOUT_COMMAND response	1	Responds to broadcast VOUT_COMMAND with same Group ID
		0	Ignores broadcast VOUT_COMMAND
20:16	BROADCAST_VOUT_COMMAND group ID	0-31d	Group ID sent as data for broadcast VOUT_COMMAND events
15:14	Not Used	00	Not used
13	BROADCAST_OPERATION response	1	Responds to broadcast OPERATION with same Group ID
		0	Ignores broadcast OPERATION
12:8	BROADCAST_OPERATION group ID	0-31d	Group ID sent as data for broadcast OPERATION events
7:6	Not Used	00	Not used
2	POWER_FAIL response	1	Responds to POWER_FAIL events with same Group ID
		0	Ignores POWER_FAIL events with same Group ID
4:0	POWER_FAIL group ID	0-31d	Group ID sent as data for broadcast POWER_FAIL events

MFR_IOUT_OC_FAULT_RESPONSE (0xE5)

Definition: Configures the IOUT overcurrent fault response as defined by the table below. The command format is the same as the PMBus standard fault responses except that it sets the overcurrent status bit in STATUS_IOUT. The retry time is the time between restart attempts.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	1	1	1	0	0	0

Bits	Purpose	Bit Value	Description
7:6	Response behavior, for all modes, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Not used
		01	Not used
		10	Disable without delay and retry according to the setting in Bits 5:3.
		11	Not used.
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. The time between the start of each attempt to restart is set by the value in Bits [2:0] multiplied by 35ms.
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

MFR_IOUT_UC_FAULT_RESPONSE (0xE6)

Definition: Configures the IOUT undercurrent fault response as defined by the table below. The command format is the same as the PMBus standard fault responses except that it sets the undercurrent status bit in STATUS_IOUT. The retry time is the time between restart attempts.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	1	1	1	0	0	0

Bits	Purpose	Bit Value	Description
7:6	Response behavior, for all modes, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Not used
		01	Not used
		10	Disable without delay and retry according to the setting in Bits 5:3.
		11	Not used.
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. The time between the start of each attempt to restart is set by the value in Bits [2:0].
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

IOUT_AVG_OC_FAULT_LIMIT (0xE7)

Definition: Sets the IOUT average overcurrent fault threshold. This feature shares the OC fault bit operation (in STATUS_IOUT) and OC fault response with IOUT_ OC_FAULT_LIMIT. Values outside of the range are not accepted.

Units: A

Equation: IOUT_AVG_OC_FAULT_LIMIT $= Y \times 2^{N}$

Range: 0A to 100A

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	101A															

IOUT_AVG_UC_FAULT_LIMIT (0xE8)

Definition: Sets the IOUT average undercurrent fault threshold. This feature shares the UC fault bit operation (in STATUS_IOUT) and UC fault response with IOUT_ UC_FAULT_LIMIT. Values outside of the range are not accepted.

Units: A

Equation: IOUT_AVG_UC_FAULT_LIMIT = $Y \times 2^N$

Range: -100A to 0 A

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	-99A															

SNAPSHOT (0xEA)

Definition: A 32-byte read-back of parametric and status values. It allows monitoring and status data to be stored to flash either during a fault condition or through a system-defined time using the SNAPSHOT_CONTROL command. Snapshot is continuously updated in RAM and can be read using the SNAPSHOT command. When a fault occurs, the latest snapshot in RAM is stored to flash. Snapshot data can read back by writing a 01h to the SNAPSHOT_CONTROL command, then reading SNAPSHOT.

Byte	Value	PMBus Command	Format
31:30	Duty Cycle	READ_DUTY_CYCLE (94h)	2 Byte Linear-11
29:28	Switching Frequency	READ_FREQUENCY (95h)	2 Byte Linear-11
27:26	External Temperature 2 (TMON)	READ_TEMPERATURE_3 (8Fh)	2 Byte Linear-11
25:24	External Temperature 1	READ_TEMPERATURE_2 (8Eh)	2 Byte Linear-11
23:22	Internal Temperature	READ_TEMPERATURE_1 (8Dh)	2 Byte Linear-11
21	Manufacturer Specific Status Byte	STATUS_MFR_SPECIFIC (80h)	1 Byte Bit Field
20	CML Status Byte	STATUS_CML (7Eh)	1 Byte Bit Field
19	Temperature Status Byte	STATUS_TEMPERATURE (7Dh)	1 Byte Bit Field
18	Input Status Byte	STATUS_INPUT (7Ch)	1 Byte Bit Field
17	IOUT Status Byte	STATUS_IOUT (7Bh)	1 Byte Bit Field
16	VOUT Status Byte	STATUS_VOUT (7Ah)	1 Byte Bit Field
15:14	Highest Measured Output Current	N/A (Peak measured output current)	2 Byte Linear-11
13:12	Output Current	READ_IOUT (8Ch)	2 Byte Linear-11
11:10	Output Voltage	READ_VOUT (8Bh)	2 Byte Linear-16 Unsigned
9:8	Input Voltage	READ_VIN (88h)	2 Byte Linear-11
7:6	All Faults	N/A	2 Byte Bit Field
5	First Fault	N/A	1 Byte Bit Field
4:1	Uptime	N/A	4 Byte Integer
0	Flash Memory Status Byte	N/A	1 Byte Bit Field

First Fault		
Bit Number	Status Bit Name	Description
7:4	Not Used	Not Used
3	IOUT_PEAK_OC	Peak output overcurrent was the first fault
2	IOUT_AVG_OC	Average output overcurrent was the first fault
1	VOUT_OV	Output overvoltage was the first fault
0	VIN_UV	Input undervoltage was the first fault
All Faults		
Bit Number	Status Bit Name	Description
15	Fault Phase	A DDC rail fault occurred
14	Fault Group	A DDC group fault occurred
13	Fault CPU	A CPU fault occurred
12	Fault UT	An under-temperature fault occurred
11	Fault OT	An over-temperature fault occurred
10	Fault peak OC	A peak output overcurrent fault occurred
9	Fault peak UC	A peak output undercurrent fault occurred
8	Fault EN pin as fault bus	The EN pin was pulled low in response to a fault
7	Fault VIN_OV	An input overvoltage fault occurred
6	Fault VOUT_OV	An output overvoltage fault occurred
5	Fault VOUT_UV	An output undervoltage fault occurred
4	Not Used	Not Used
3	Fault Sync	A loss of clock synchronization fault occurred
2	Fault VIN_UV	An input undervoltage fault occurred
1	Fault IOUT_OC	An average output overcurrent fault occurred
0	Fault IOUT_UC	An average output undercurrent fault occurred

SNAPSHOT_CONTROL (0xF3)

Definition: Controls, configures, and erases SNAPSHOT data. As shown in the following table, this command is used to arm and disarm SNAPSHOT, report back the number of SNAPSHOT data record locations that are available for new data, select the data record to read back, specify whether a single or multiple SNAPSHOT should be taken after a device as been disabled, if a SNAPSHOT can only be taken when the device is enabled, enabling and disabling SNAPSHOT_CONTROL, and erasing all SNAPSHOT data.

The Erase All bit must be sent as a separate command. All other bits are ignored when the Erase All bit is sent. For example, 0000 0000 0000 0010b and 1111 1111 1111 1111b both (only) erase all SNAPSHOT data. The hose must wait at least 20ms before issuing any other PMBus commands after writing the Erase All bit.

Format	**Bit/Field**															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Value	Setting	Description
15	Snapshot Armed	0	Disabled	Not Armed
		1	Enabled	Armed. Snapshot happens on next fault (provided it is not masked)
14:12	Not Used	000	Not Used	Not used
11:8	Available Snapshots	0000-1000	N/A	Number of 8 byte SNAPSHOT records available
7	One Time	0	Disabled	Snapshot is taken whenever a fault occurs
		1	Enabled	One Snapshot is taken when a fault occurs. Another Snapshot is not taken until the device has been disabled.
6	After Enable	0	Disabled	Snapshot may be taken at any time.
		1	Enabled	Snapshot is only taken when the device is enabled (“turned on”)
5	Not used	0	Not used	Not used
4:2	Read Location	000-111	NA/	Specifies which SNAPSHOT data record to return when the SNAPSHOT command is read.
1	Erase All	1	(Write Only)	Erases all SNAPSHOT data. This causes Available Snapshots Remaining to become 8 (1000d) THIS BIT MUST BE SENT AS A SEPARATE COMMAND; such as, not combined with other bit settings.
0	Enable	0	Disabled	Disables SNAPSHOT_CONTROL
		1	Enabled	Enables SNAPSHOT_CONTROL

PINSTRAP_READ_STATUS (0xF5)

Definition: A 5-byte read-back of an index from 0 to 31 that corresponds to the resistor value for the designated pin-strap position.

Byte	Value	Format
Byte 4	Reserved	8-Bit Integer
Byte 3	Reserved	8-Bit Integer
Byte 2	SYNC resistor index	8-Bit Integer
Byte 1	Factory Mode	8-Bit Integer
Byte 0 Bits 7:3	VSET/SA VSET resistor index	5-Bit Integer
Byte 0 Bits 2:0	VSET/SA Address resistor index	3-Bit Integer

SECURITY_CONTROL (0xFA)

Definition: Reads back the security status of the USER and DEFAULT stores, clears protection status of non-password protected commands, and enables the automatic command protection mode (Auto Protect Mode). SECURITY_CONTROL is used along with the PASSWORD and WRITE_PROTECT commands to allow the user to disallow changes to selected commands.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

Bits	Field Name	Bit Value	Description
7:6	Not used	00	Not used
5	DEFAULT store protected	0	1 indicates that the DEFAULT store is protected.
4	USER store protected	0	1 indicates that the USER store is protected.
3:2	Not used	00	Not used.
1	Clear protected	0	Writing a “1” clears all protected commands except the commands that are password protected.
0	Auto protect	0	Writing a “1” enables auto protection mode.

PASSWORD (0xFB)

Definition: Sets the password string for the USER and DEFAULT stores. The USER and DEFAULT stores can have unique passwords. The initial (default) password for both stores is null (9 bytes of zeroes in hexidecimal format - not 9 ASCII “0” characters). The DEFAULT store password has priority over the USER store password. That is, when the DEFAULT store password is written, protected commands in both the DEFAULT and USER stores can be written to. Data Format: ASCII. ISO/IEC 8859-1

WRITE_PROTECT (0xFD)

Definition: Sets a 256-bit (32-byte) parameter that identifies which commands are to be protected against write-access. Each bit in this parameter corresponds to a command according to the command's code. The command with a code of 00h (PAGE - not used in this device) is protected by the least-significant bit of the least-significant byte, followed by the command with a code of 01h and so forth. Note that all possible commands have a corresponding bit regardless of whether they are can be protected or are supported by the device. Setting a command's WRITE_PROTECT bit to "1" indicates that write-access to that command is only allowed if the appropriate password has been written to the device. Note that the USER and DEFAULT stores have unique passwords, and that writing the DEFAULT store password allows changes to both the USER and DEFAULT stores.

Digital Power Insight (DPI)

ABB offers a software tool that helps users evaluate and simulate the PMBus performance of the DJT090 modules without the need to write software. The software can be downloaded for free at http://powertalk.campaigns.abb.com/DigitalPowerInsight.html An ABB's USB to I2C adapter and associated cable set are required for proper functioning of the software suite. For first time users, we recommend using the ABB's DPI Evaluation Kit, which can be purchase from any of the leading distributors. Please ensure the ABB USB to I2C adapter being used/purchased is Version 2.2 or higher.

Thermal Considerations

Power modules operate in a variety of thermal environments; however, sufficient cooling should always be provided to help ensure reliable operation. Considerations include ambient temperature, airflow, module power dissipation, and the need for increased reliability. A reduction in the operating temperature of the module will result in an increase in reliability. The thermal data presented here is based on physical measurements taken in a wind tunnel. The test set-up is shown in Figure 35a. The thermal reference points, Tref used in the specifications are also shown in Figure 35b. For reliable operation the temperatures at U3 should not exceed 122°C for open-frame applications. The output power of the module should not exceed the rated power of the module (Vo_set x Io,max). Please refer to the Application Note “Thermal Characterization Process for Open-Frame Board-Mounted Power Modules” for a detailed discussion of thermal aspects including maximum device temperatures. Increased airflow over the module enhances the heat transfer via convection. The thermal derating of figures 2, 8, 14, 20 show the maximum output current that can be delivered by each module in the indicated orientation without exceeding the maximum Tref temperature versus local ambient temperature (T_A) for several air flow conditions.

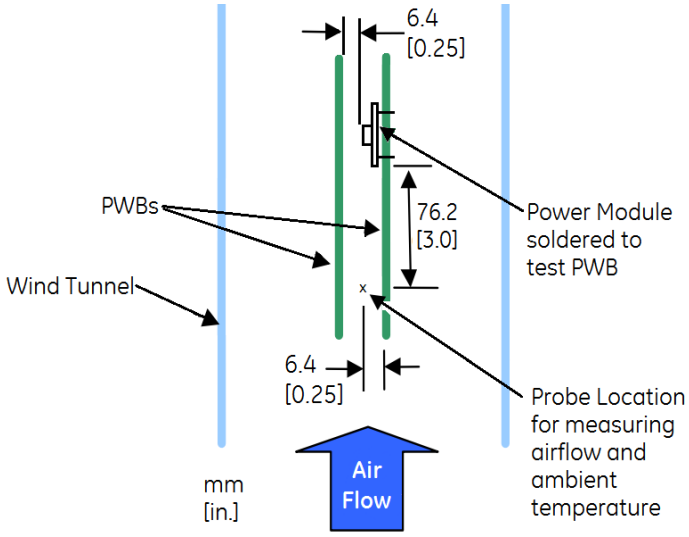


Figure 35a. Thermal testing setup

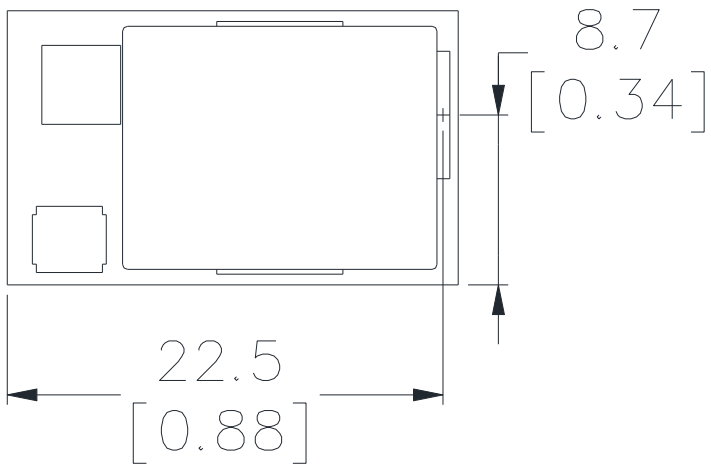


Figure 35b. Location of the thermal reference temperature

Example Application Circuit

Requirements:

Vin: 12V

Vout: 1.2V

Iout: 90A max.

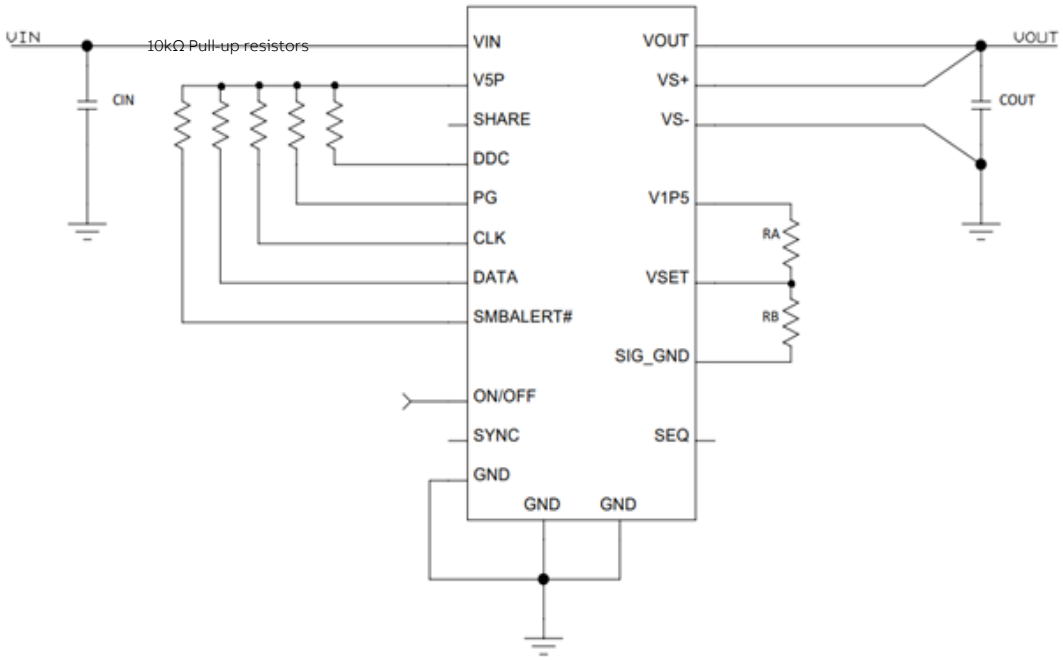


Figure 36. Example Application Circuit

Cin	3 x 0.1uF(ceramic) || 4 x 10uF (ceramic) || 10 x 22uF (ceramic) || 2 x 470uF (Aluminum Polymer)
Cout	4 x 22uF (ceramic) || 12 x 47uF (ceramic) || 4 x 680uF (Tantalum Polymer)
RA	392kΩ
RB	38.3kΩ

ASCR Controller Settings:

ASCR Gain = 270

ASCR Integral = 80

ASCR Residual = 80

Steady State Gain Reduction = 2

Threshold = 250

Mechanical Outline

Dimensions are in millimeters and (inches).

Tolerances: x.x mm ± 0.5 mm (x.xx in. ± 0.02 in.) [unless otherwise indicated]

x.xx mm ± 0.25 mm (x.xxx in ± 0.010 in.)

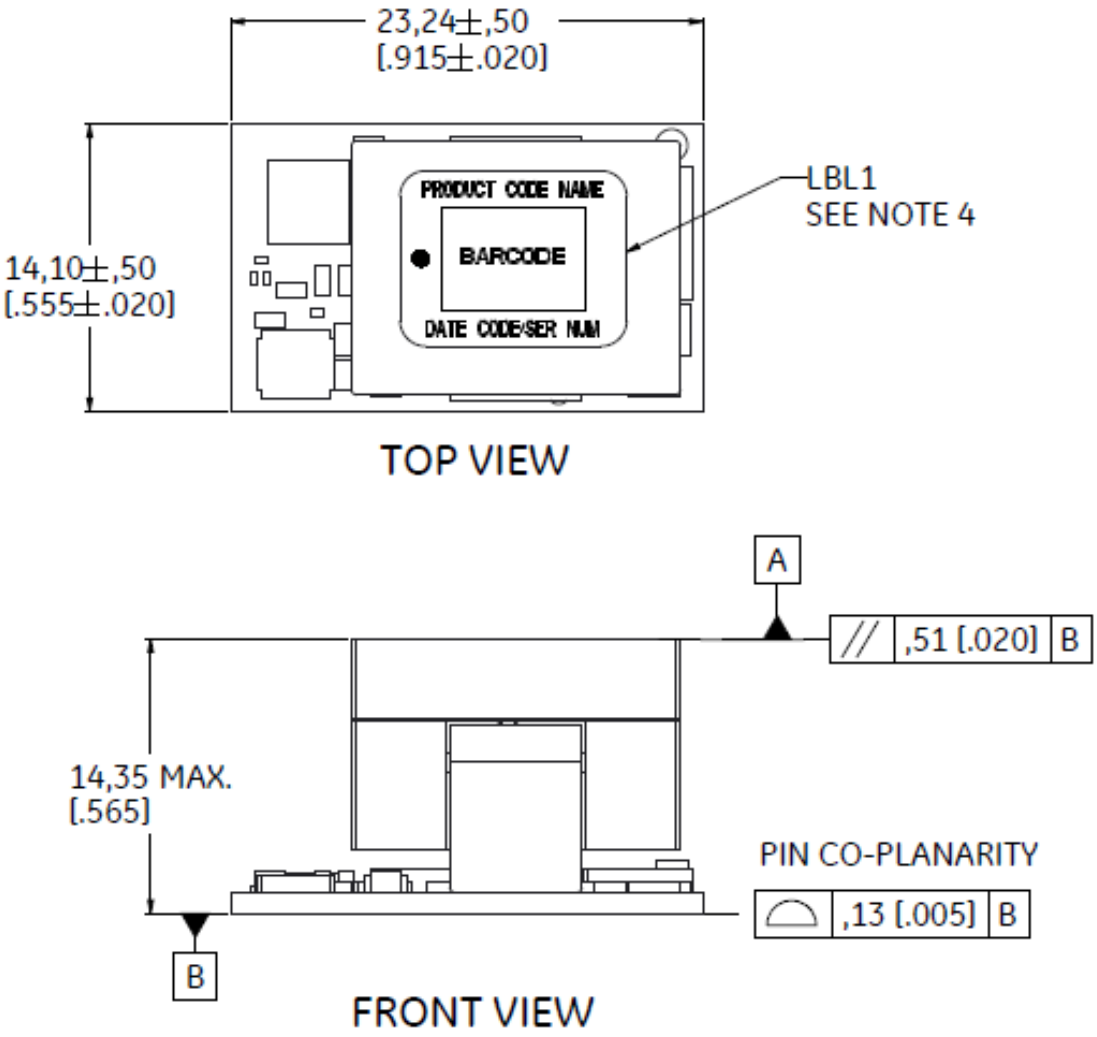


Figure 37. Physical dimensions

Recommended Pad Layout

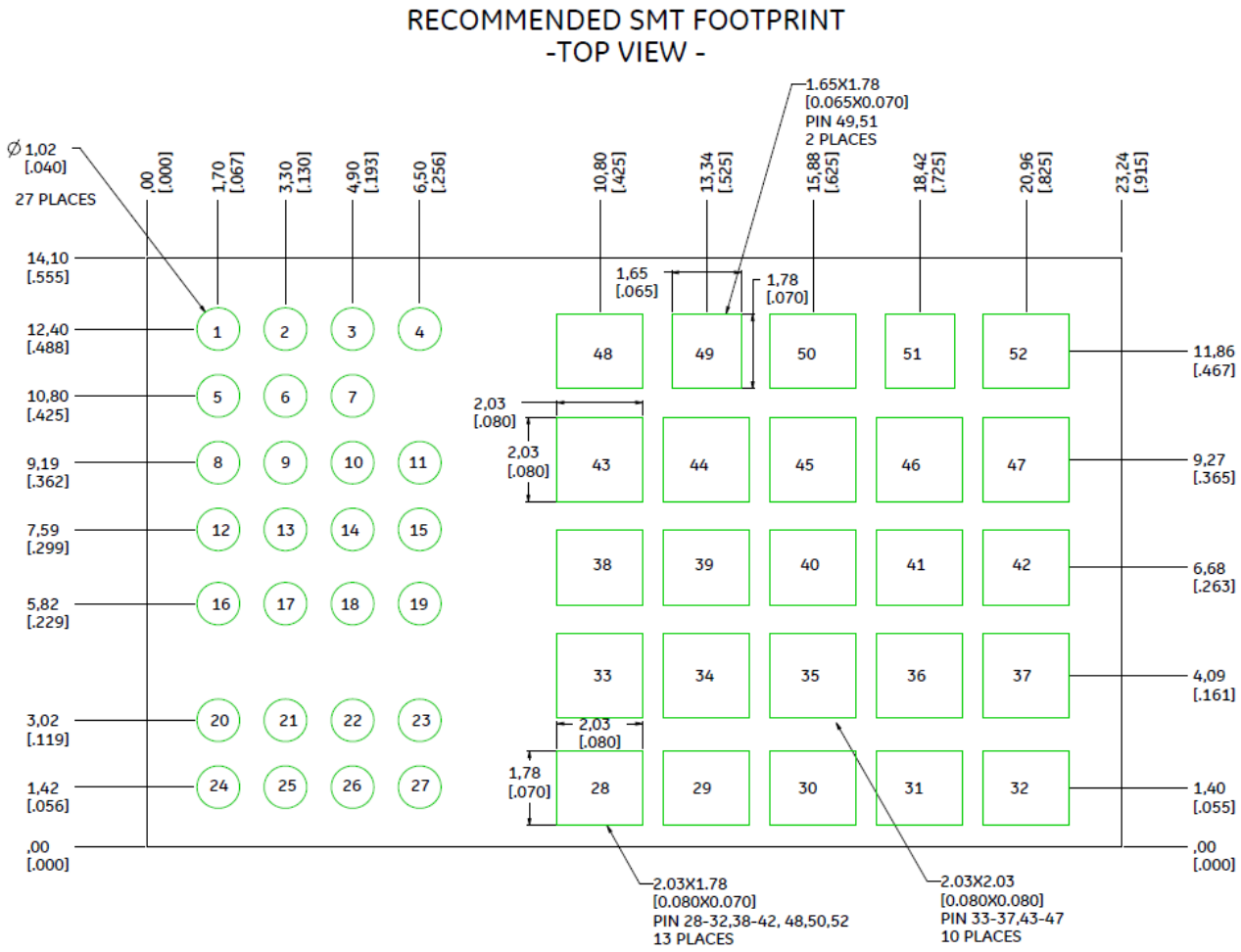


Figure 38. Dimension of footprint

Pin Assignment Table

Pin	Label	Type	Description
1	CLK	I/O	Serial clock. Connect to external host and/or to other modules. Requires a pull-up resistor to a 3.3V or 5.5V source. V5 source recommended.
2	SMBALERT#	O	Serial alert. Connect to external host if desired. Requires a pull-up resistor to a 3.3V or 5.5V source. V5 source recommended. If not used, this pin should be left floating.
3	SHARE	I/O	Current sharing communication bus. Connect to other current share enabled modules to achieve droop-less current sharing. If not used, this pin should be left floating.
4	ON/OFF	I	Enable input. Active signal enables device. Recommended to be tied low during device configuration. The ON/OFF signal must be glitch free to achieved specified delay timing. Positive or negative pulse widths shorter than 10µs are ignored.
5	DATA	I/O	Serial data. Connect to external host and/or to other devices. Requires a pull-up resistor to a 3.3V or 5.5V source. V5 source recommended.
8	SYNC	I/O	Clock synchronization input. Used to sync to an external clock or to output the internal clock. When used as part of a SYNC bus in order to achieve phase spreading or as part of a current sharing rail, one of the devices must have this pin configured as an output, with no pull-up or pull-down resistors on the bus.
11	DDC	I/O	Single-wire current sharing and inter-device communication bus. Requires a pull-up resistor to a 3.3V or 5.5V source. V5 source recommended. Pull-up voltage must be present when the device is powered.
12	PG	O	Power-good output. Configured as open-drain by default. Require 10k pull-up to V5P. Could be re-configured as push-pull via PMBus.
13	SEQ	I	Output tracking voltage input. Reference the tracking source to pin 10. If not used, connect to SIG_GND.
14	VSET	Multi	Used to set the POL address and the output voltage. See address table for details. Connect to the middle point of the resistor divider between V1P5 and SIG_GND.
16	VS-	I	Differential remote sense input. Connect to negative output regulation point.
17	VS+	I	Differential remote sense input. Connect to positive output regulation point.
18	V1P5	O	Auxiliary 1.5V low power bus. Do not connect any external load except VSET resistor divider. Does not require external filtering. See layout recommendations.
19	V5P	O	Auxiliary 5V low power (5mA max) bus. Does not need external filter capacitors.
6-7, 9-10, 15, 20-27	SIG_GND	SGND	Analog signal ground return. Internal connected to GND. 20-27 can be tied to GND to improve conductivity. See layout recommendation section for details
28-32	VOUT	PWR	Output voltage rail. Connect the output filter capacitors between rail 28-32 and rail 33-37. See layout recommendation section for details. Minimum recommended capacitance 3 x 680µF (tantalum polymer) || 10 x 47 µF || 2 x 0.1µF.
33-37	GND	PWR	Output rail return.
38-42	VIN	PWR	Input voltage rail. Connect the input filter capacitors between rail 38-42 and rail 43-47. See layout recommendation section for details. Minimum recommended capacitance 2 x 470µF (electrolytic) || 10 x 22 µF || 2 x 0.1µF.
43-47,49,51	GND	PWR	Input rail return.
48, 50, 52	EPAD	Thermal	Leave floating, do not place any via or sensitive signal below EPAD

Packaging Details

The DJT090 Open Frame modules are supplied in tape & reel as standard. Modules are shipped in quantities of 110 modules per reel. All Dimensions are in millimeters and (in inches).

Pick and Place Location

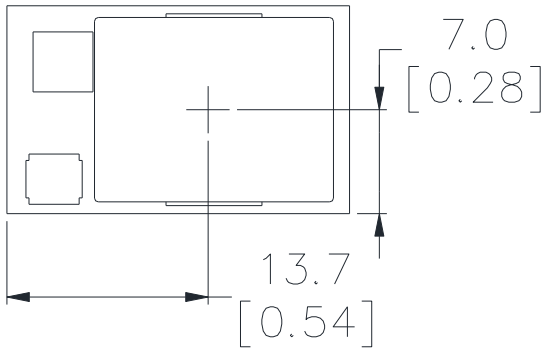
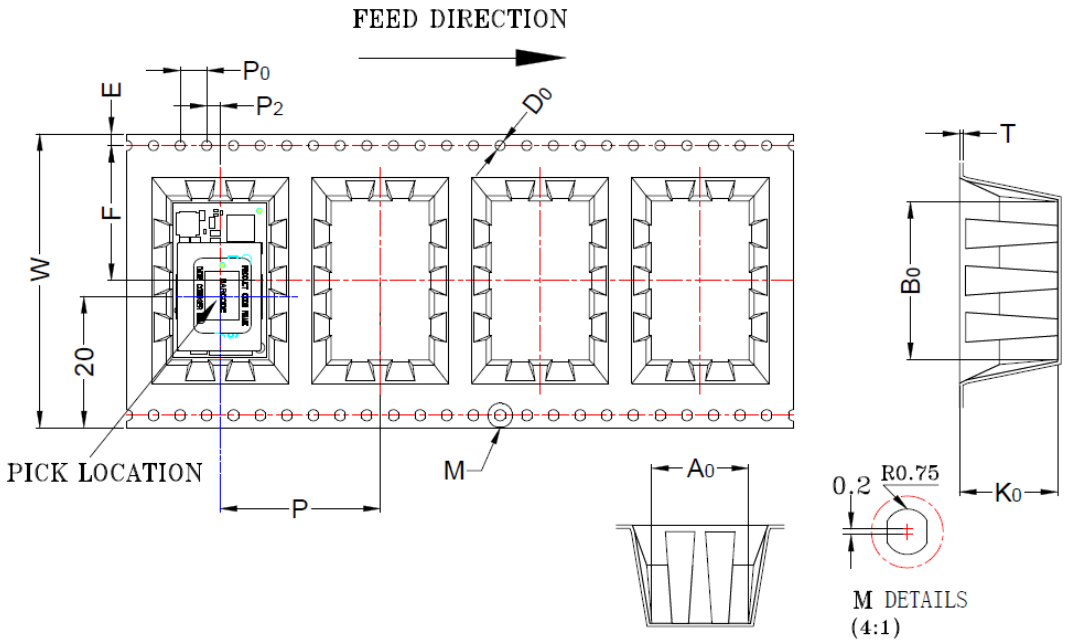


Figure 39. Pick and place location

Reel Dimensions:

Outside Dimensions: 330.2 mm (13.00”)
Inside Dimensions: 177.8 mm (7.00”)
Tape Width: 44.00 mm (1.732”)



ITEM	W	A_0	B_0	K_0	P	F	E	D_0	P_0	P_2	T
SIZE (MM)	44.0	14.70	23.84	14.80	24.0	20.2	1.75	1.50	4.00	2.00	0.5

DEFAULT TOLERANCE ± 0.2MM

Figure 40. Reel Dimensions

Packaging Details

Surface Mount Information

Pick and Place

The DJT090 Open Frame modules use an open frame construction and are designed for a fully automated assembly process. The modules are fitted with a label designed to provide a large surface area for pick and place operations. The label meets all the requirements for surface mount processing, as well as safety standards, and is able to withstand reflow temperatures of up to 300 ℃. The label also carries product information such as product code, serial number and the location of manufacture.

Nozzle Recommendations

Stencil thickness of 6 mils minimum must be used for this product. The module weight has been kept to a minimum by using open frame construction. Variables such as nozzle size, tip style, vacuum pressure and placement speed should be considered to optimize this process. The minimum recommended inside nozzle diameter for reliable operation is 3mm. The maximum nozzle outer diameter, which will safely fit within the allowable component spacing, is 7 mm.

Bottom Side / First Side Assembly

This module is not recommended for assembly on the bottom side of a customer board. If such an assembly is attempted, components may fall off the module during the second reflow process.

Lead Free Soldering

The modules are lead-free (Pb-free) and RoHS compliant and fully compatible in a Pb-free soldering process. Failure to observe the instructions below may result in the failure of or cause damage to the modules and can adversely affect long-term reliability.

Pb-free Reflow Profile

Power Systems will comply with J-STD-020 Rev. D (Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices) for both Pb-free solder profiles and MSL classification procedures. This standard provides a recommended forced-air-convection reflow profile based on the volume and thickness of the package (table 4-2). The suggested Pb-free solder paste is Sn/Ag/Cu (SAC). The recommended linear reflow profile using Sn/Ag/Cu solder is shown in Fig. 33. Soldering outside of the recommended profile requires testing to verify results and performance.

Packaging Details

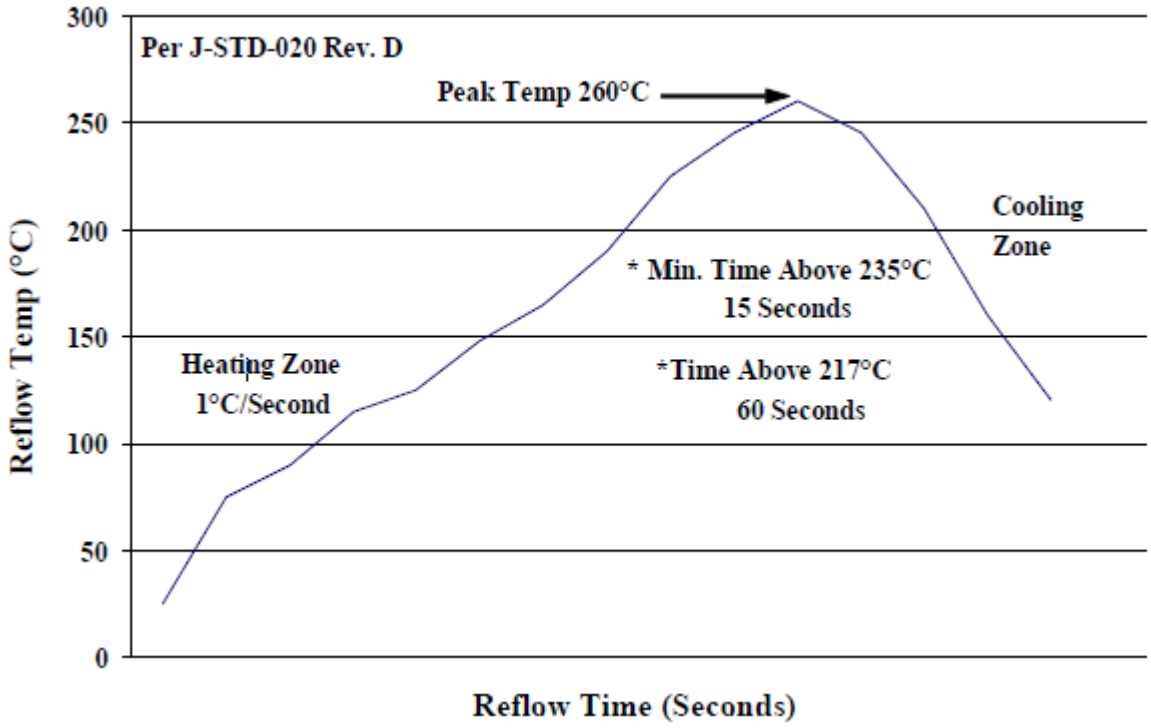


Figure 41. Recommended linear reflow profile using Sn/Ag/Cu solder

MSL Rating

The DJT090 Open Frame modules have a MSL rating of 2a.

Storage and Handling

The recommended storage environment and handling procedures for moisture-sensitive surface mount packages is detailed in J-STD-033 Rev. A (Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices). Moisture barrier bags (MBB) with desiccant are required for MSL ratings of 2 or greater. These sealed packages should not be broken until time of use. Once the original package is broken, the floor life of the product at conditions of 30°C and 60% relative humidity varies according to the MSL rating (see J-STD-033A). The shelf life for dry packed SMT packages will be a minimum of 12 months from the bag seal date, when stored at the following conditions: < 40° C, < 90% relative humidity.

Post Solder Cleaning and Drying Considerations

Post solder cleaning is usually the final circuit-board assembly process prior to electrical board testing. The result of inadequate cleaning and drying can affect both the reliability of a power module and the testability of the finished circuit-board assembly. For guidance on appropriate soldering, cleaning and drying procedures, refer to *Board Mounted Power Modules: Soldering and Cleaning* Application Note (AN04-001).

Change History (excludes grammar & clarifications)

Version	Date	Description of the change
1.0	03/17/2020	Initial Release
1.1	04/24/2020	Major Revision
1.2	06/16/2020	Major Revision
1.3	07/01/2020	Major Revision
2.0	09/21/2020	Major Revision
2.1	10/05/2020	Minor Revision
2.2	10/23/2020	Major Revision
2.3	10/28/2020	Minor Revision
2.5	11/10/2020	Minor Revision
2.6	04/08/2021	Minor revision
2.7	05/19/2021	Revision to startup delay
2.8	07/12/2021	References to Switching frequency adj removed

Ordering Information

Please contact your ABB Sales Representative for pricing, availability and optional features.

Device Codes

Product Codes	Input Voltage	Output Voltage	Output Current	MSL Rating	Comcode
DJT090A0X43-SRPZ	7-14.4Vdc	0.5-2Vdc	90A	2a	1600276298A

Coding Scheme

Package Identifier	Family	Sequencing Option	Output current	Output voltage	On/Off logic	Remote Sense	Options		ROHS Compli-ance
D	J	T	90A0	X	4	3	-SR	-P	Z
P=Pico U=Micro D=Deca M=Mega G=Giga T=Tera	J = DLynx II Digital	T=with EZ Sequence X=without sequencing	90A	X = pro-gramm able output	4 = positive No entry = negative	3 = Remote Sense	S = Surface Mount R = Tape & Reel No entry = Through hole	Paralleling Pins	Z = ROHS6

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