S-19611A

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AUTOMOTIVE, 105°C OPERATION, LOW INPUT OFFSET VOLTAGE CMOS OPERATIONAL AMPLIFIER

Rev.1.2_00

This IC incorporates a general purpose analog circuit in a small package. This is a zero-drift operational amplifier with Rail-to-Rail input and output, which uses auto-zeroing techniques to provide low input offset voltage.
This IC is suitable for applications requiring less offset voltage.
The S-19611AB is a dual operational amplifier (2 circuits).

Caution This product can be used in vehicle equipment and in-vehicle equipment. Before using the product for these purposes, it is imperative to contact our sales representatives.

■ Features

- Low input offset voltage: V_{IO} = +17 μV max. (Ta = +25°C)
  V_{IO} = +100 μV max. (Ta = −40°C to +105°C)
- Operation power supply voltage range: V_{DD} = 2.65 V to 5.50 V
- Low current consumption (Per circuit): I_{DD} = 200 μA typ.
- Internal phase compensation: No external parts required
- Rail-to-Rail input and output
- Operation temperature range: Ta = −40°C to +105°C
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 qualified[*1]

***1.** Contact our sales representatives for details.

■ Applications

- High-accuracy current detection
- Various sensor interfaces
- Strain gauge amplifier

■ Package

- TMSOP-8

■ Block Diagram

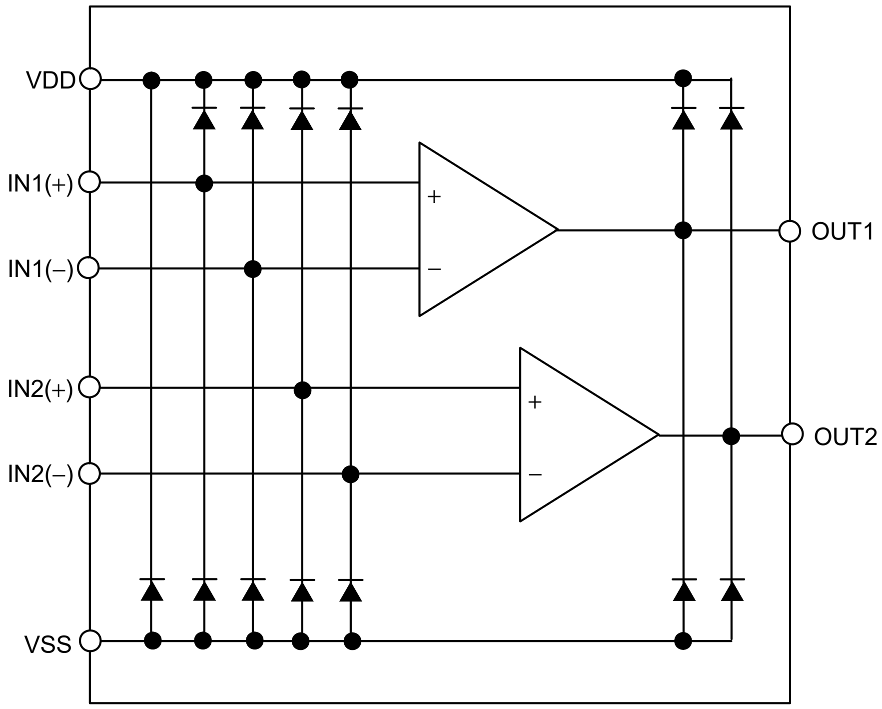


Figure 1

■ AEC-Q100 Qualified

This IC supports AEC-Q100 for the operation temperature grade 2.
Contact our sales representatives for details of AEC-Q100 reliability specification.

■ Product Name Structure

Refer to "**1. Product name**" regarding the contents of product name, "**2. Package**" regarding the package drawings and "**3. Product name list**" regarding the product type.

1. Product name

S-19611A B 0 H - K8T2 U

- **U** — Environmental code
  U: Lead-free (Sn 100%), halogen-free
- **K8T2** — Package abbreviation and IC packing specifications*1
  K8T2: TMSOP-8, Tape
- **H** — Operation temperature
  H: Ta = −40°C to +105°C
- **B** — Number of circuits
  B: 2

***1.** Refer to the tape drawing.

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD

3. Product name list

Table 2

Product Name	Package
S-19611AB0H-K8T2U	TMSOP-8

■ Pin Configuration

1. TMSOP-8

Top view

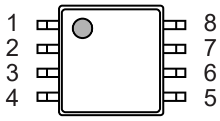


Figure 2

Table 3

Pin No.	Symbol	Description
1	OUT1	Output pin 1
2	IN1(−)	Inverted input pin 1
3	IN1(+)	Non-inverted input pin 1
4	VSS	GND pin
5	IN2(+)	Non-inverted input pin 2
6	IN2(−)	Inverted input pin 2
7	OUT2	Output pin 2
8	VDD	Positive power supply pin

■ Absolute Maximum Ratings

Table 4

(Ta = −40°C to +105°C unless otherwise specified)

Item	Symbol	Absolute Maximum Rating	Unit
Power supply voltage	V_{DD}	V_{SS} − 0.3 to V_{SS} + 6.0	V
Input voltage	$V_{IN(+)}$, $V_{IN(-)}$	V_{SS} − 0.3 to V_{DD} + 0.3	V
Output voltage	V_{OUT}	V_{SS} − 0.3 to V_{DD} + 0.3	V
Differential input voltage	V_{IND}	±5.5	V
Output pin current	I_{SOURCE}	10.0	mA
	I_{SINK}	10.0	mA
Operation ambient temperature	T_{opr}	−40 to +105	°C
Storage temperature	T_{stg}	−55 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 5

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	TMSOP-8	Board A	–	160	–	°C/W
			Board B	–	133	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

1. Recommended operation condition

Table 6

(Ta = –40°C to +105°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation power supply voltage range	V_{DD}	–	2.65	5.00	5.50	V	–

2. V_{DD} = 5.0 V

Table 7

DC Electrical Characteristics (Ta = –40°C to +105°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Current consumption (2 circuits)	I_{DD}	$V_{CMR} = V_{OUT} = \frac{V_{DD}}{2}$	–	400	600	μA	5
Input offset voltage	V_{IO}	$V_{CMR} = \frac{V_{DD}}{2}$, Ta = +25°C	–17	±1	+17	μV	1
		$V_{CMR} = \frac{V_{DD}}{2}$	–100	±1	+100	μV	1
Input offset voltage drift	$\frac{\Delta V_{IO}}{\Delta Ta}$	$V_{CMR} = \frac{V_{DD}}{2}$	–	±0.1	–	μV/°C	1
Input bias current	I_{BIAS}	Ta = +25°C	–	±70	–	pA	–
		–	–	±3000	–	pA	–
Input offset current	I_{IO}	Ta = +25°C	–	±140	–	pA	–
		–	–	±300	–	pA	–
Common-mode input voltage range	V_{CMR}	–	V_{SS} – 0.1	–	V_{DD} + 0.1	V	2
Voltage gain (open loop)	A_{VOL}	$V_{SS} + 0.1\ V \le V_{OUT} \le V_{DD} - 0.1\ V$, $V_{CMR} = \frac{V_{DD}}{2}$, R_L = 10 kΩ	106	130	–	dB	8
Maximum output swing voltage	V_{OH}	R_L = 10 kΩ	4.9	–	–	V	3
	V_{OL}	R_L = 10 kΩ	–	–	0.1	V	4
Common-mode input signal rejection ratio	CMRR	$V_{SS} - 0.1\ V \le V_{CMR} \le V_{DD} + 0.1\ V$	100	130	–	dB	2
Power supply voltage rejection ratio	PSRR	$2.65\ V \le V_{DD} \le 5.50\ V$	95	120	–	dB	1
Source current	I_{SOURCE}	$V_{OUT} = V_{DD} - 0.1\ V$	0.8	2.5	–	mA	6
Sink current	I_{SINK}	V_{OUT} = 0.1 V	1.0	2.9	–	mA	7

Table 8

AC Electrical Characteristics (Ta = –40°C to +105°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Slew rate	SR	R_L = 1.0 MΩ, C_L = 15 pF (Refer to **Figure 11**)	–	0.22	–	V/μs
Gain-bandwidth product	GBP	C_L = 0 pF	–	320	–	kHz

■ Test Circuits (Per circuit)

1. Power supply voltage rejection ratio, input offset voltage

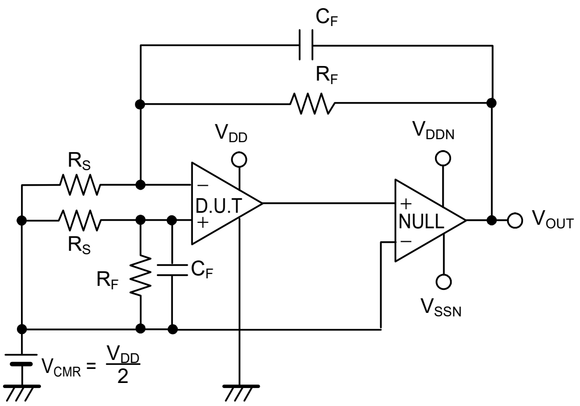


Figure 3 Test Circuit 1

• **Power supply voltage rejection ratio (PSRR)**

The power supply voltage rejection ratio (PSRR) can be calculated by the following expression, with V_{OUT} measured at each V_{DD}.

Test conditions:
V_{DD} = 2.65 V: $V_{DD} = V_{DD1}$, $V_{OUT} = V_{OUT1}$
V_{DD} = 5.50 V: $V_{DD} = V_{DD2}$, $V_{OUT} = V_{OUT2}$

$$\text{PSRR} = 20 \log \left(\left| \frac{V_{DD1} - V_{DD2}}{\left(V_{OUT1} - \frac{V_{DD1}}{2}\right) - \left(V_{OUT2} - \frac{V_{DD2}}{2}\right)} \right| \times \frac{R_F + R_S}{R_S} \right)$$

• **Input offset voltage (V_{IO})**

$$V_{IO} = \left(V_{OUT} - \frac{V_{DD}}{2}\right) \times \frac{R_S}{R_F + R_S}$$

2. Common-mode input signal rejection ratio, common-mode input voltage range

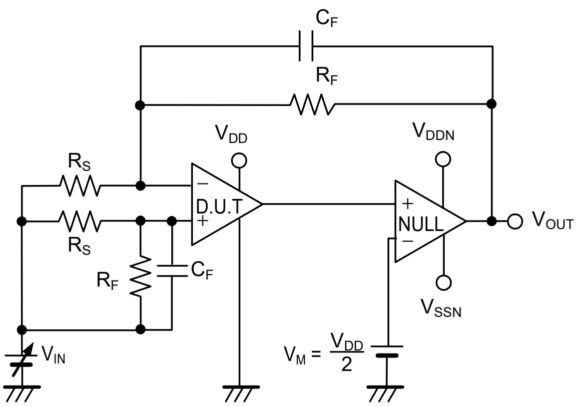


Figure 4 Test Circuit 2

• **Common-mode input signal rejection ratio (CMRR)**

The common-mode input signal rejection ratio (CMRR) can be calculated by the following expression, with V_{OUT} measured at each V_{IN}.

Test conditions:
$V_{IN} = V_{CMR\ Max.}$: $V_{IN} = V_{IN1}$, $V_{OUT} = V_{OUT1}$
$V_{IN} = V_{CMR\ Min.}$: $V_{IN} = V_{IN2}$, $V_{OUT} = V_{OUT2}$

$$\text{CMRR} = 20 \log \left(\left| \frac{V_{IN1} - V_{IN2}}{(V_{OUT1} - V_{IN1}) - (V_{OUT2} - V_{IN2})} \right| \times \frac{R_F + R_S}{R_S} \right)$$

• **Common-mode input voltage range (V_{CMR})**

The common-mode input voltage range is the range of V_{IN} in which V_{OUT} satisfies the common-mode input signal rejection ratio specifications when V_{IN} is changed.

3. Maximum output swing voltage

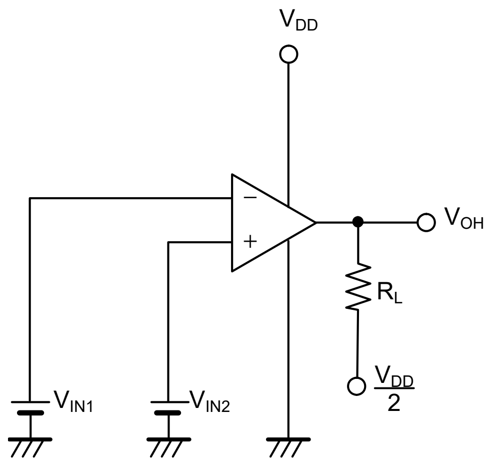


Figure 5 Test Circuit 3

- **Maximum output swing voltage (V_{OH})**

Test conditions:

$V_{IN1} = \frac{V_{DD}}{2} - 0.1\ V$

$V_{IN2} = \frac{V_{DD}}{2} + 0.1\ V$

$R_L = 10\ k\Omega$

4. Maximum output swing voltage

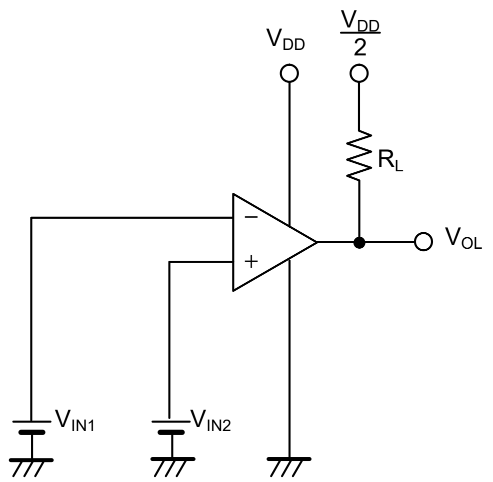


Figure 6 Test Circuit 4

- **Maximum output swing voltage (V_{OL})**

Test conditions:

$V_{IN1} = \frac{V_{DD}}{2} + 0.1\ V$

$V_{IN2} = \frac{V_{DD}}{2} - 0.1\ V$

$R_L = 10\ k\Omega$

5. Current consumption

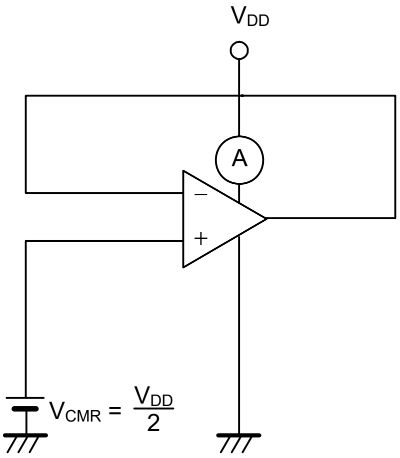


Figure 7 Test Circuit 5

• **Current consumption (I_{DD})**

6. Source current

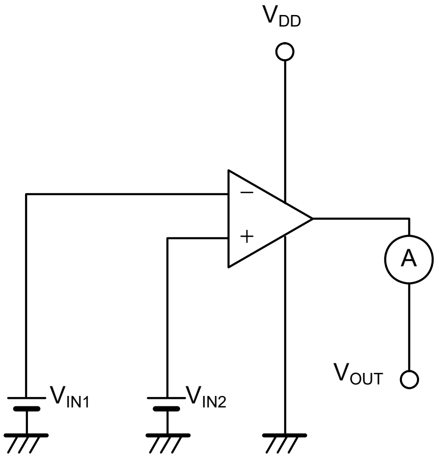


Figure 8 Test Circuit 6

• **Source current (I_{SOURCE})**

Test conditions:

$V_{OUT} = V_{DD} - 0.1\ V$

$V_{IN1} = \frac{V_{DD}}{2} - 0.1\ V$

$V_{IN2} = \frac{V_{DD}}{2} + 0.1\ V$

7. Sink current

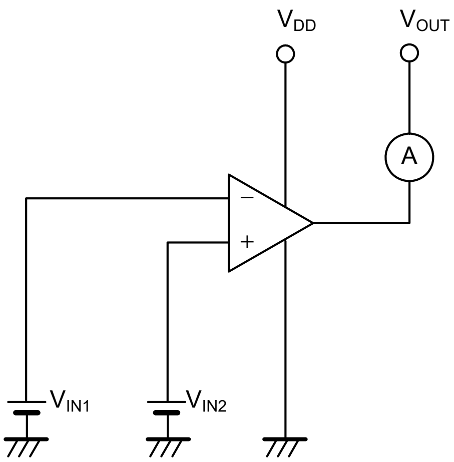


Figure 9 Test Circuit 7

• **Sink current (I_{SINK})**

Test conditions:

$V_{OUT} = 0.1\ V$

$V_{IN1} = \frac{V_{DD}}{2} + 0.1\ V$

$V_{IN2} = \frac{V_{DD}}{2} - 0.1\ V$

8. Voltage gain

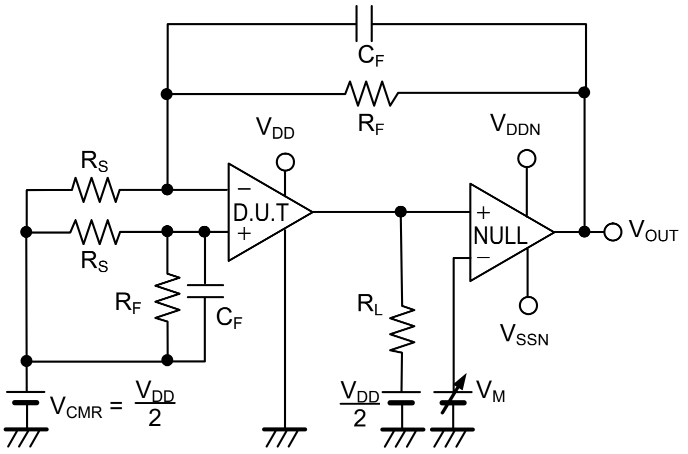


Figure 10 Test Circuit 8

• **Voltage gain (open loop) (A_{VOL})**

The voltage gain (A_{VOL}) can be calculated by the following expression, with V_{OUT} measured at each V_M.

Test conditions:
$V_M = V_{DD} - 0.1$ V: $V_M = V_{M1}$, $V_{OUT} = V_{OUT1}$
$V_M = 0.1$ V: $V_M = V_{M2}$, $V_{OUT} = V_{OUT2}$

$$A_{VOL} = 20 \log \left(\left| \frac{V_{M1} - V_{M2}}{V_{OUT1} - V_{OUT2}} \right| \times \frac{R_F + R_S}{R_S} \right)$$

$R_L = 10$ kΩ

9. Slew rate

Measured by the voltage follower circuit.

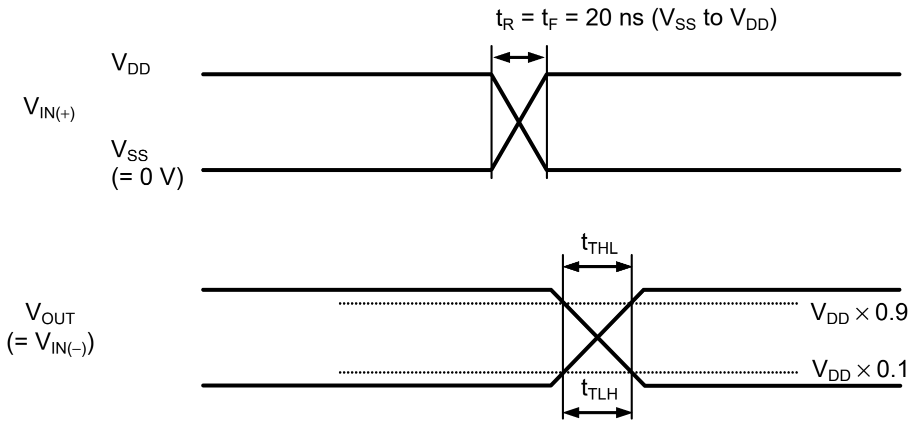


Figure 11

• **Slew rate (SR)**

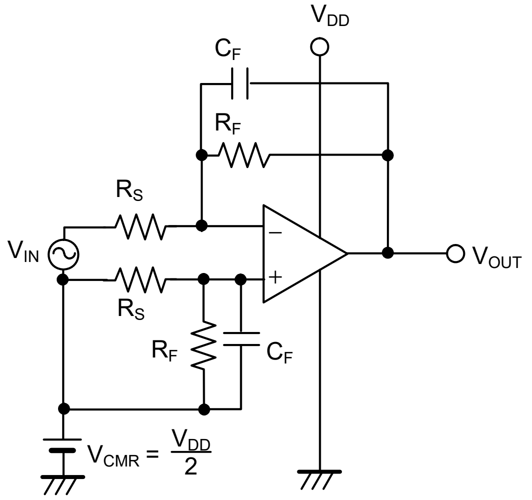
When falling

$$SR = \frac{V_{DD} \times 0.8}{t_{THL}}$$

When rising

$$SR = \frac{V_{DD} \times 0.8}{t_{TLH}}$$

■ Usage Examples



[Example of Gain = 1000 times]
R_S = 1 kΩ
R_F = 1 MΩ
C_F = 1000 pF

[Example of Gain = 100 times]
R_S = 1 kΩ
R_F = 100 kΩ
C_F = 1000 pF

Figure 12 Differential Amplifier Circuit

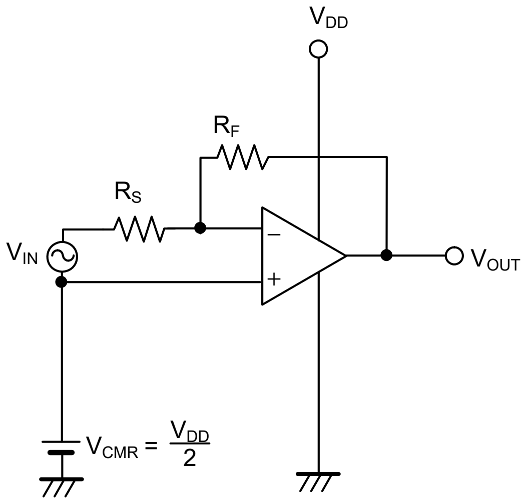


Figure 13 Inverting Amplifier Circuit

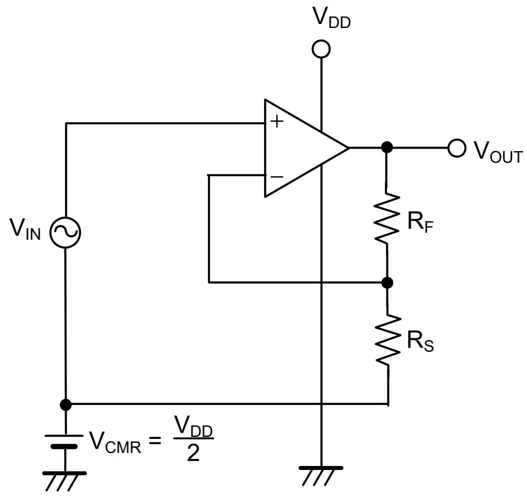


Figure 14 Non-inverting Amplifier Circuit

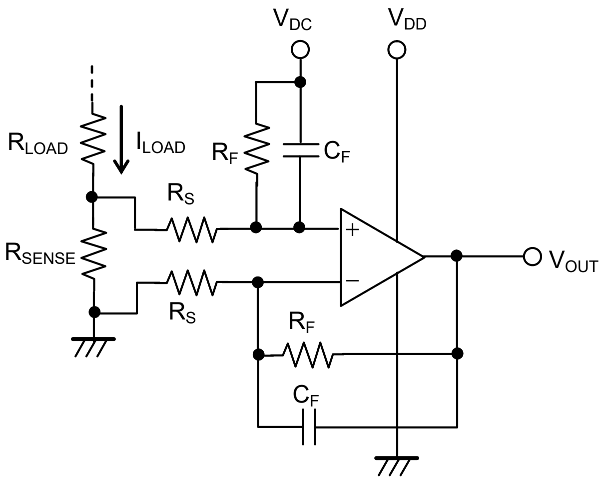


Figure 15 Low-side Current Detection Circuit

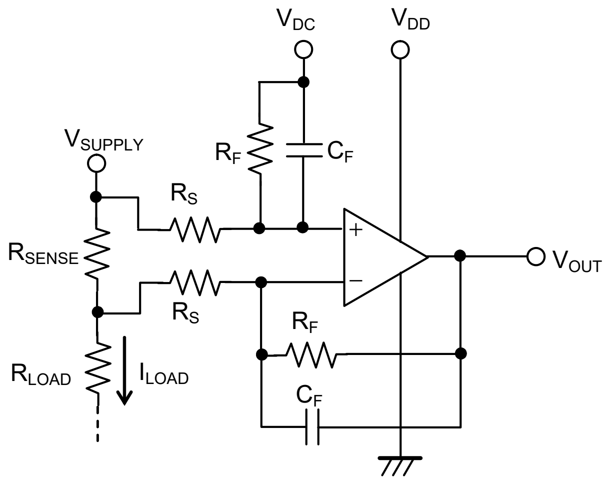


Figure 16 High-side Current Detection Circuit

Caution The above connection diagrams and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

■ Precautions

- During the operation of an operational amplifier circuit, when $V_{OUT} \leq V_{SS} + 100$ mV or $V_{OUT} \geq V_{DD} - 100$ mV, the signal becomes difficult to be output, and the output voltage (V_{OUT}) may become V_{SS} or V_{DD}. If this happens, supply an appropriate input signal to the operational amplifier so that V_{OUT} is within the range of V_{SS} + 100 mV to V_{DD} − 100 mV. Contact our sales representatives if you have any questions for use in the above operation conditions.

- Generally an operational amplifier may cause oscillation depending on the selection of external parts. Perform thorough evaluation using the actual application to set the constant.

- Do not apply an electrostatic discharge to this IC that exceeds performance ratings of the built-in electrostatic protection circuit.

- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

- Use this IC with the output current of 10 mA or less.

- When using the voltage follower circuit (Gain = 1 time), connect a resistor of 470 Ω or more for the stable operation as shown in **Figure 17**. The operation may become unstable depending on the value of the load capacitance connected to the output pin, even when the voltage follower circuit is not used. Use the product under thorough evaluation.

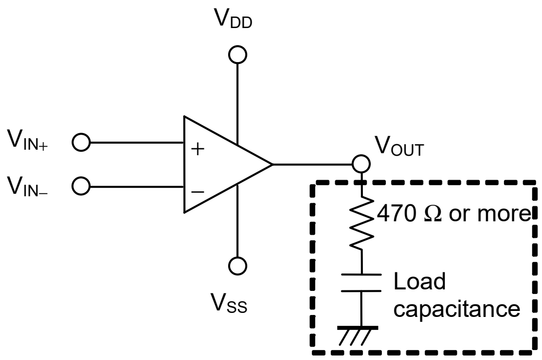
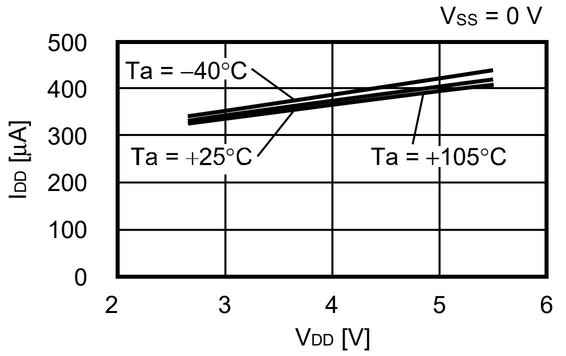


Figure 17

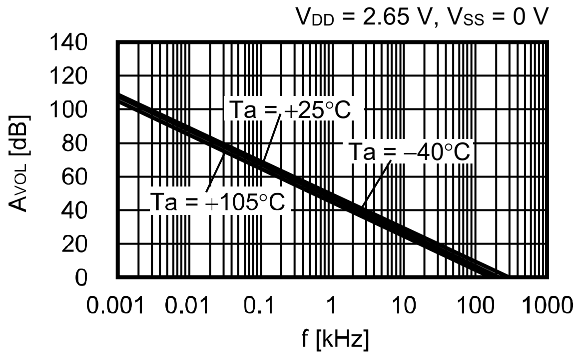
**Caution The above connection diagram and constant will not guarantee successful operation.
Perform thorough evaluation using the actual application to set the constant.**

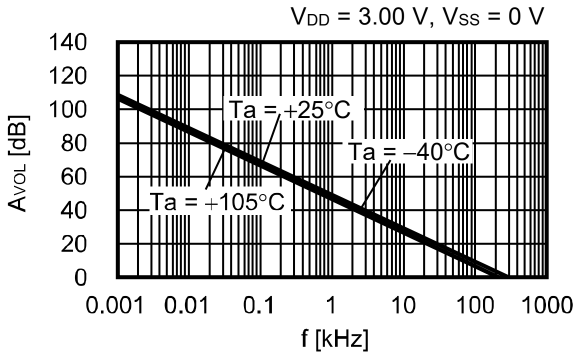
■ Characteristics (Typical Data)

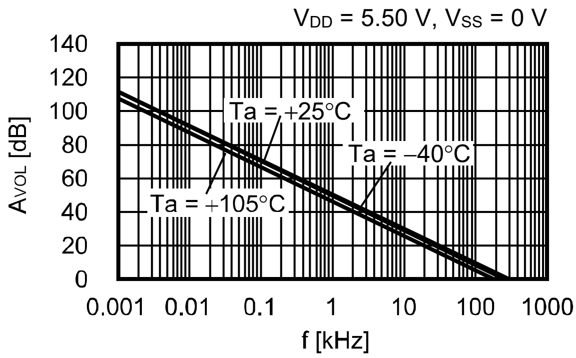
1. Current consumption (I_{DD}) (2 circuits) vs. Power supply voltage (V_{DD})



2. Voltage gain (A_{VOL}) vs. Frequency (f)

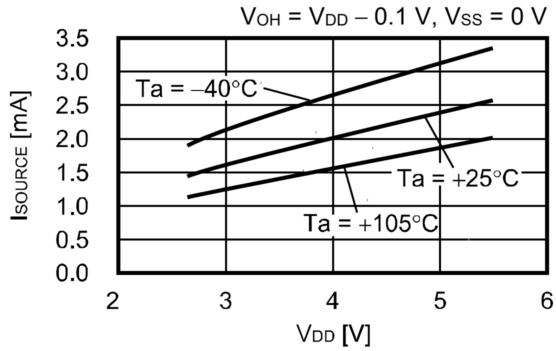




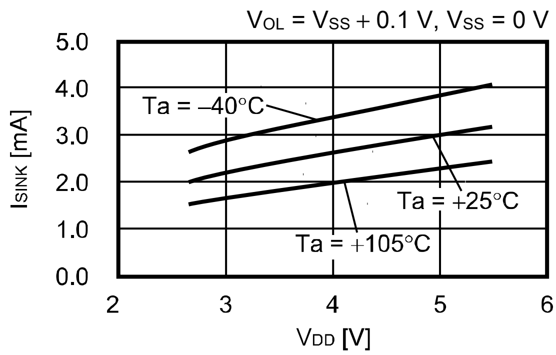


3. Output current

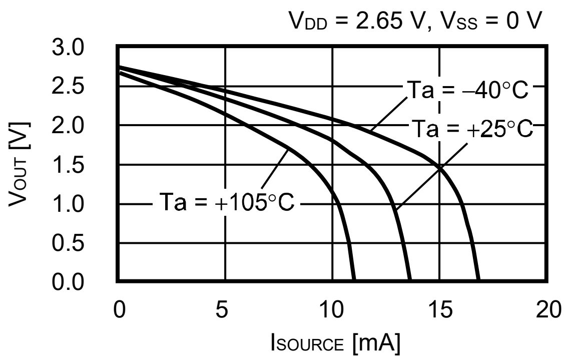
3. 1 Source current (I_{SOURCE}) vs. Power supply voltage (V_{DD})

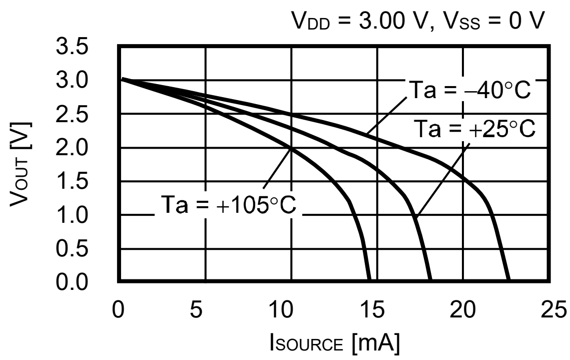


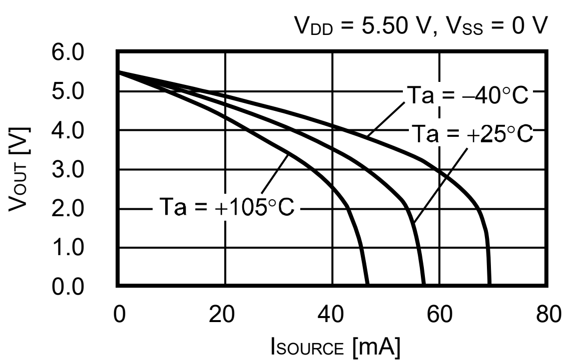
3. 2 Sink current (I_{SINK}) vs. Power supply voltage (V_{DD})



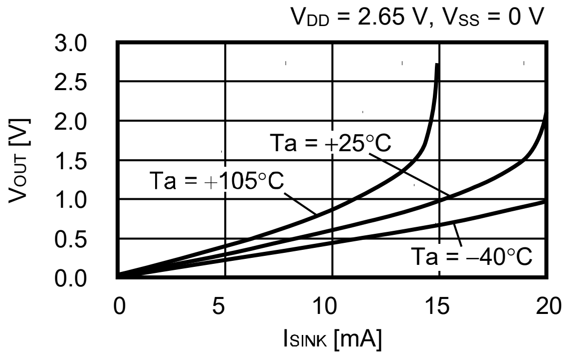
3. 3 Output voltage (V_{OUT}) vs. Source current (I_{SOURCE})

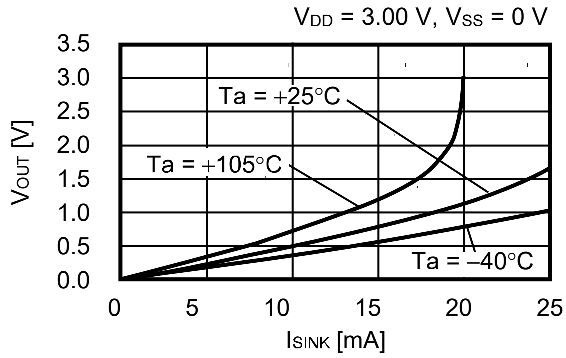


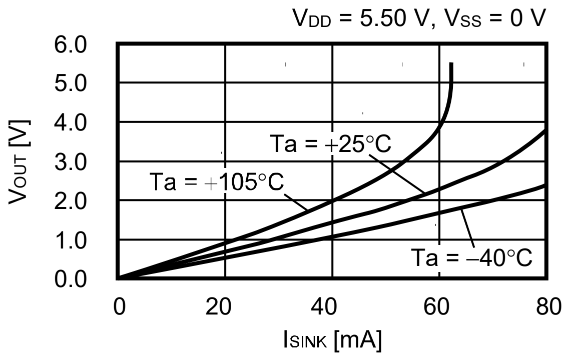




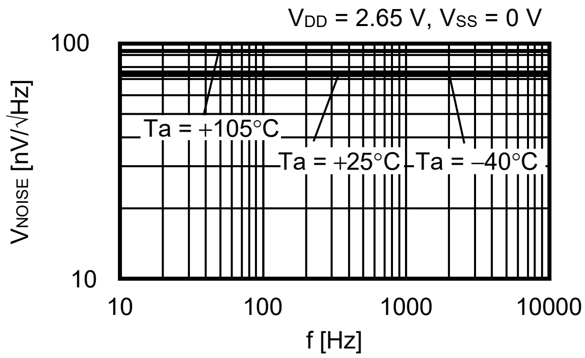
3. 4 Output voltage (V_{OUT}) vs. Sink current (I_{SINK})

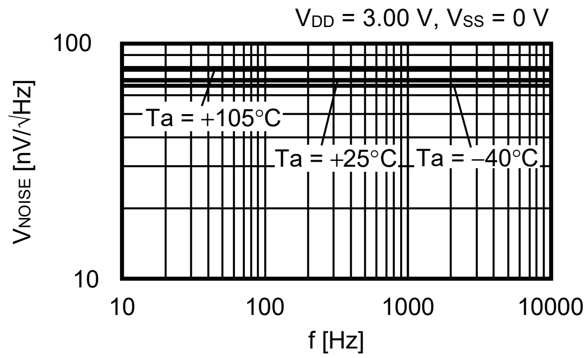


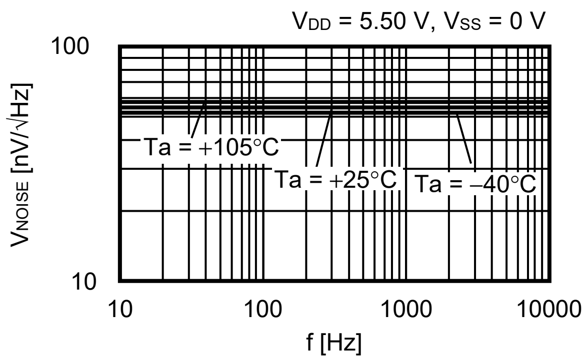




4. Input noise voltage density (V_{NOISE}) vs. Frequency (f)

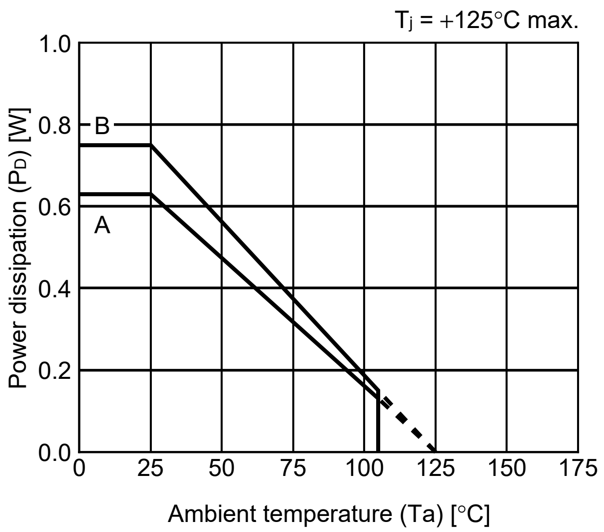






■ Power Dissipation

TMSOP-8

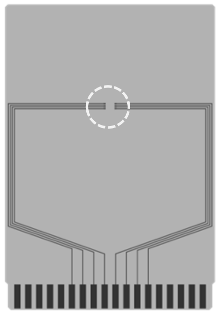


Board	Power Dissipation (P_D)
A	0.63 W
B	0.75 W
C	–
D	–
E	–

TMSOP-8 Test Board

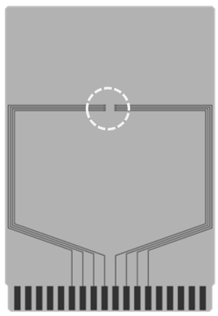
IC Mount Area

(1) Board A



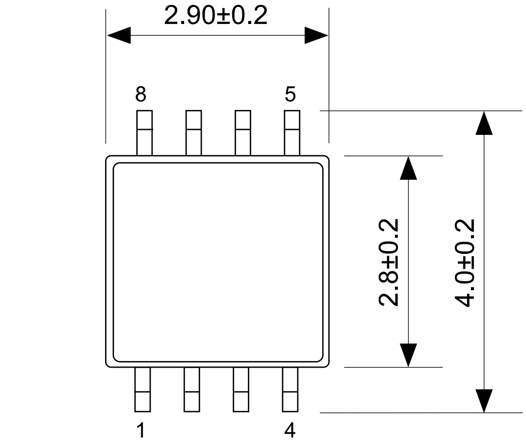
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

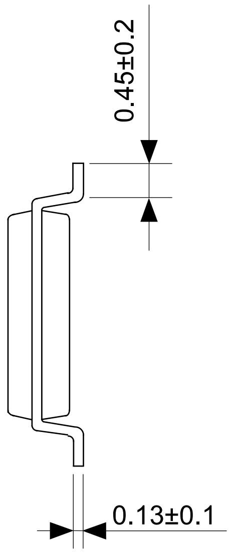
(2) Board B

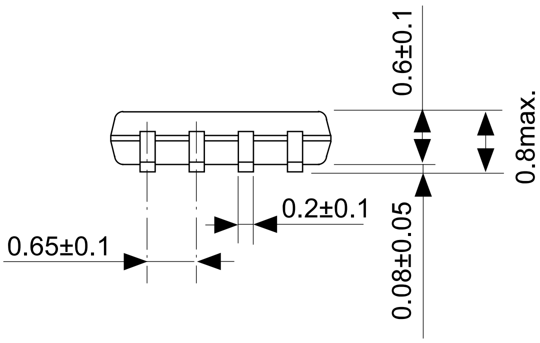


Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. TMSOP8-A-Board-SD-1.0



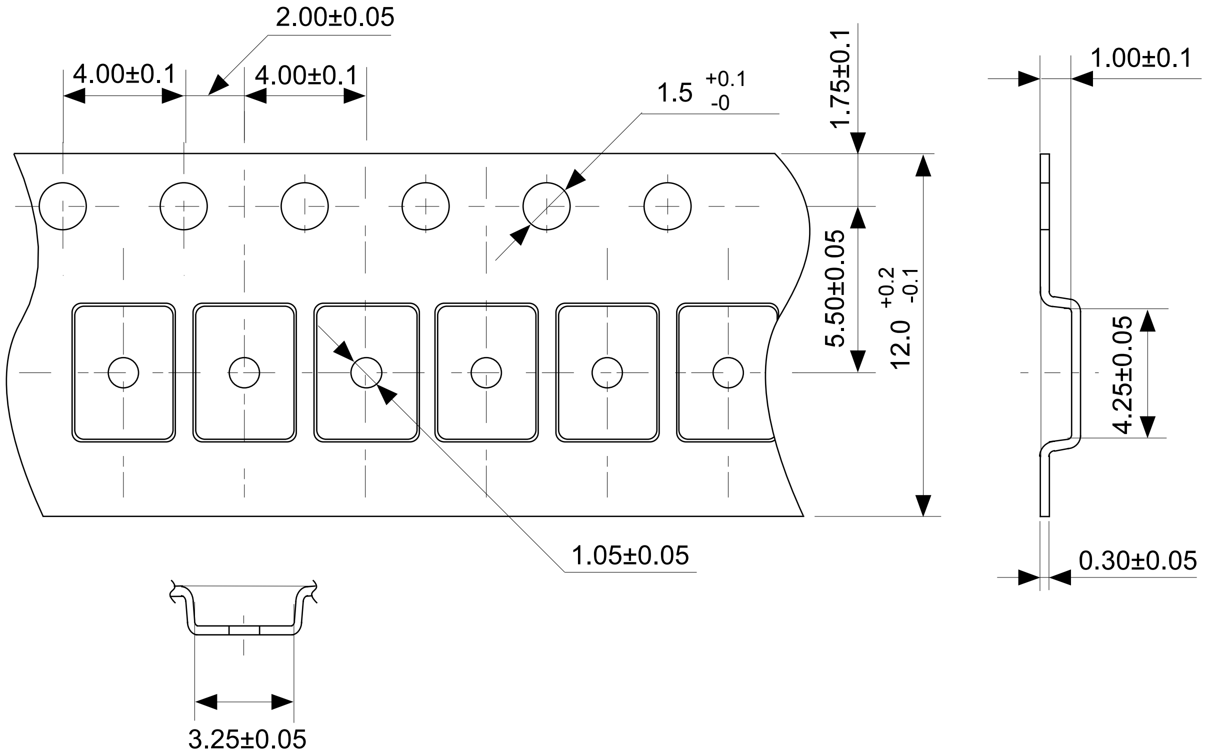


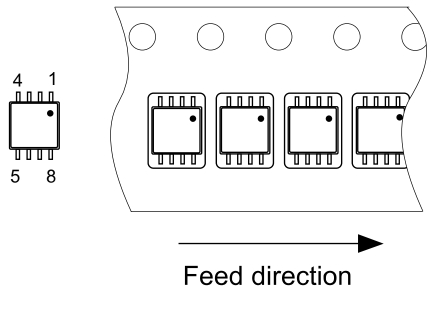


No. FM008-A-P-SD-1.2

TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	
UNIT	mm

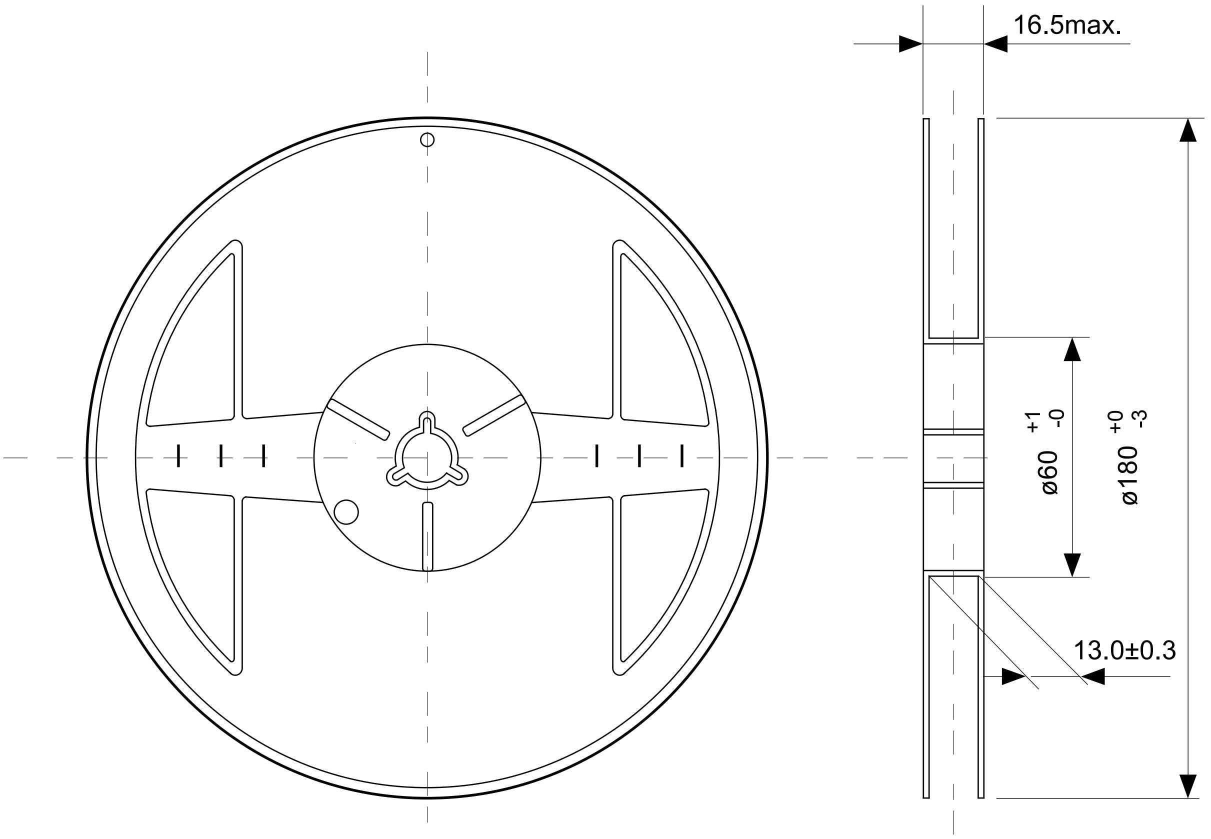
ABLIC Inc.



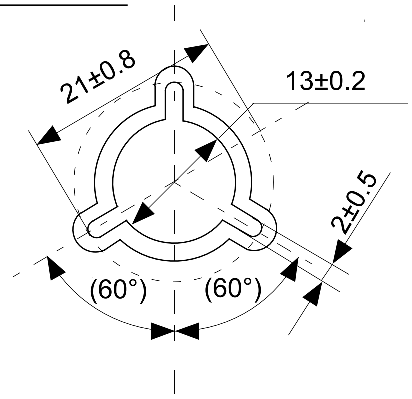


No. FM008-A-C-SD-2.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part



No. FM008-A-R-SD-1.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

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2.4-2019.07