S-5718 Series

LOW VOLTAGE OPERATION OMNIPOLAR / UNIPOLAR DETECTION TYPE HALL EFFECT SWITCH IC WITH SWITCHABLE DETECTION POLE FUNCTION

This IC, developed by CMOS technology, is a high-accuracy Hall effect switch IC with switchable detection pole function that operates at a low voltage and low current consumption.
The output voltage changes when this IC detects the intensity level of magnetic flux density of the polarity according to the input pin status. The inclusion of a switchable detection pole function makes it possible to reduce the number of parts and realize a variety of different systems by using this IC with a magnet. High-density mounting is possible by using the super small SNT-4A package.
Due to its low voltage operation and low current consumption, this IC is suitable for battery-operated portable devices. Its high-accuracy magnetic characteristics also allow this IC to reduce operation dispersion in magnet combination systems.

ABLIC Inc. offers a "magnetic simulation service" that provides the ideal combination of magnets and our Hall effect ICs for customer systems. Our magnetic simulation service will reduce prototype production, development period and development costs. In addition, it will contribute to optimization of parts to realize high cost performance.
For more information regarding our magnetic simulation service, contact our sales office.

■ Features

- Switchable detection pole function: Omnipolar detection, S pole detection, N pole detection
- Output logic[*1]: Active "L"
  Active "H"
- Output form: CMOS output
- Magnetic sensitivity (hysteresis width)[*1]: B_{OP} = 1.8 mT typ. (B_{HYS} = 0.7 mT typ.)
  B_{OP} = 3.0 mT typ. (B_{HYS} = 0.8 mT typ.)
  B_{OP} = 3.0 mT typ. (B_{HYS} = 1.3 mT typ.)
  B_{OP} = 4.5 mT typ. (B_{HYS} = 1.0 mT typ.)
  B_{OP} = 4.5 mT typ. (B_{HYS} = 2.5 mT typ.)
- Operating cycle (current consumption)[*1]: t_{CYCLE} = 102.1 ms typ. (I_{DD} = 1.4 μA typ.)
  t_{CYCLE} = 50.5 ms typ. (I_{DD} = 2.0 μA typ.)
  t_{CYCLE} = 5.7 ms typ. (I_{DD} = 12.0 μA typ.)
- Power supply voltage range[*2]: V_{DD} = 1.45 V to 3.6 V
- Operation temperature range: Ta = −40°C to +85°C
- Lead-free (Sn 100%), halogen-free

***1.** The option can be selected.
***2.** Power supply voltage range is different by optional combination.

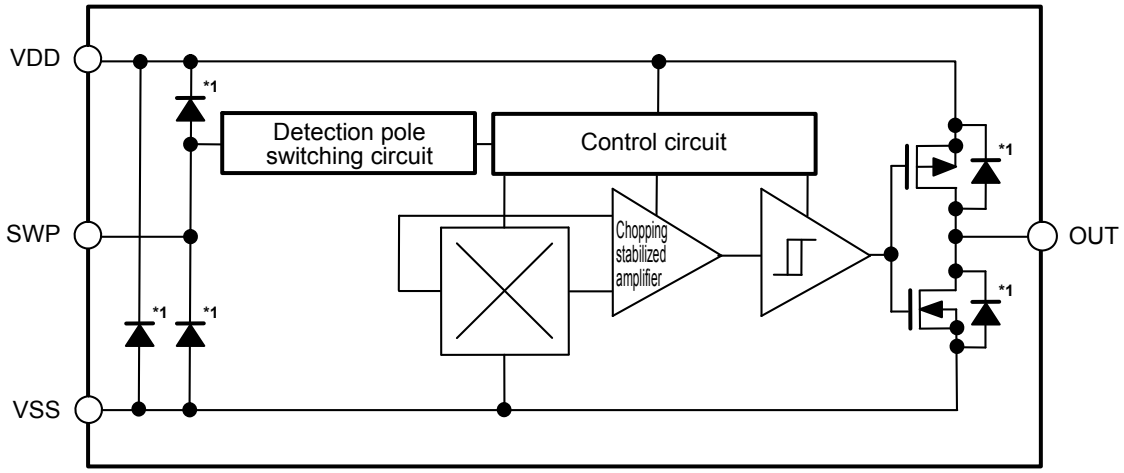
■ Applications

- Mobile phone, smart phone
- Notebook PC, tablet PC
- Wearable device
- Plaything, portable game
- Home appliance

■ Package

- SNT-4A

■ Block Diagram



***1.** Parasitic diode

Figure 1

■ Product Name Structure

1. Product name

S-5718 x C x x x - I4T1 U

- Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- Package abbreviation and packing specifications*1
  - I4T1: SNT-4A, Tape
- Magnetic sensitivity*2
  - 0: B_{OP} = 1.8 mT typ.
  - 1: B_{OP} = 3.0 mT typ.
  - 2: B_{OP} = 4.5 mT typ.
- Output logic
  - L: Active "L"
  - H: Active "H"
- Hysteresis width*2
  - S: Standard
  - W: Wide
- Output form
  - C: CMOS output
- Operating cycle
  - A: t_{CYCLE} = 102.1 ms typ.
  - B: t_{CYCLE} = 50.5 ms typ.
  - C: t_{CYCLE} = 5.7 ms typ.

***1.** Refer to the tape drawing.
***2.** Magnetic sensitivity and hysteresis width combinations are as follows.

Magnetic Sensitivity	Hysteresis Width	
	S (Standard)	W (Wide)
0 (B_{OP} = 1.8 mT typ.)	B_{HYS} = 0.7 mT typ.	–
1 (B_{OP} = 3.0 mT typ.)	B_{HYS} = 0.8 mT typ.	B_{HYS} = 1.3 mT typ.
2 (B_{OP} = 4.5 mT typ.)	B_{HYS} = 1.0 mT typ.	B_{HYS} = 2.5 mT typ.

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SNT-4A	PF004-A-P-SD	PF004-A-C-SD	PF004-A-R-SD	PF004-A-L-SD

3. Product name list

Table 2

Product Name	Operating Cycle (t_{CYCLE})	Output Form	Hysteresis Width (B_{HYS})	Output Logic	Magnetic Sensitivity (B_{OP})
S-5718CCWL1-I4T1U	5.7 ms typ.	CMOS output	Wide (1.3 mT typ.)	Active "L"	3.0 mT typ.
S-5718CCSH0-I4T1U*1	5.7 ms typ.	CMOS output	Standard (0.7 mT typ.)	Active "H"	1.8 mT typ.
S-5718CCSL0-I4T1U*1	5.7 ms typ.	CMOS output	Standard (0.7 mT typ.)	Active "L"	1.8 mT typ.

***1.** V_{DD} = 1.6 V to 3.6 V

Remark Please contact our sales office for products other than the above.

■ Pin Configuration

1. SNT-4A

Top view

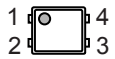


Figure 2

Table 3

Pin No.	Symbol	Pin Description
1	VDD	Power supply pin
2	VSS	GND pin
3	SWP	Detection pole switching pin*1
4	OUT	Output pin

***1.** For details, refer to "**3. Basic operation**" in "**■ Operation**".

■ Absolute Maximum Ratings

Table 4

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applicable Pin	Absolute Maximum Rating	Unit
Power supply voltage	V_{DD}	–	V_{SS} – 0.3 to V_{SS} + 7.0	V
Input voltage	V_{IN}	SWP	V_{SS} – 0.3 to V_{DD} + 0.3	V
Output current	I_{OUT}	OUT	±1.0	mA
Output voltage	V_{OUT}	OUT	V_{SS} – 0.3 to V_{DD} + 0.3	V
Operation ambient temperature	T_{opr}	–	–40 to +85	°C
Storage temperature	T_{stg}	–	–40 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 5

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	SNT-4A	Board A	–	300	–	°C/W
			Board B	–	242	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W

***1.** Test environment: Compliant with JEDEC STANDARD JESD51-2A

Remark Refer to "**■ Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

1. S-5718Axxxx

Table 6

(Ta = +25°C, V_{DD} = 1.8 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–	1.45	1.8	3.6	V	–
Current consumption	I_{DD}	Average value	–	1.4	3.0	μA	1
High level input voltage	V_{IH}	–	$V_{DD} \times 0.85$	–	V_{DD}	V	2
Medium level input voltage	V_{IM}	–	$V_{DD} \times 0.45$	–	$V_{DD} \times 0.55$	V	2
Low level input voltage	V_{IL}	–	V_{SS}	–	$V_{DD} \times 0.15$	V	2
High level output voltage	V_{OH}	I_{OUT} = –0.5 mA	V_{DD} – 0.4	–	–	V	3
Low level output voltage	V_{OL}	I_{OUT} = 0.5 mA	–	–	0.4	V	4
High level input current	I_{IH}	Peak value	9	18	36	μA	5
Low level input current	I_{IL}	Peak value	–36	–18	–9	μA	6
Awake mode time	t_{AW}	–	–	0.1	–	ms	–
Sleep mode time	t_{SL}	–	–	102.0	–	ms	–
Operating cycle	t_{CYCLE}	$t_{AW} + t_{SL}$	–	102.1	200.0	ms	–
Detection pole switching time	t_{SWP}	–	–	102.1	400.0	ms	–

2. S-5718Bxxxx

Table 7

(Ta = +25°C, V_{DD} = 1.8 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–	1.45	1.8	3.6	V	–
Current consumption	I_{DD}	Average value	–	2.0	4.0	μA	1
High level input voltage	V_{IH}	–	$V_{DD} \times 0.85$	–	V_{DD}	V	2
Medium level input voltage	V_{IM}	–	$V_{DD} \times 0.45$	–	$V_{DD} \times 0.55$	V	2
Low level input voltage	V_{IL}	–	V_{SS}	–	$V_{DD} \times 0.15$	V	2
High level output voltage	V_{OH}	I_{OUT} = –0.5 mA	V_{DD} – 0.4	–	–	V	3
Low level output voltage	V_{OL}	I_{OUT} = 0.5 mA	–	–	0.4	V	4
High level input current	I_{IH}	Peak value	9	18	36	μA	5
Low level input current	I_{IL}	Peak value	–36	–18	–9	μA	6
Awake mode time	t_{AW}	–	–	0.1	–	ms	–
Sleep mode time	t_{SL}	–	–	50.4	–	ms	–
Operating cycle	t_{CYCLE}	$t_{AW} + t_{SL}$	–	50.5	100.0	ms	–
Detection pole switching time	t_{SWP}	–	–	50.5	200.0	ms	–

3. S-5718Cxxxx

Table 8

(Ta = +25°C, V_{DD} = 1.8 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–	1.45	1.8	3.6	V	–
		S-5718CCSx0	1.6	1.8	3.6	V	–
Current consumption	I_{DD}	Average value	–	12.0	22.0	μA	1
High level input voltage	V_{IH}	–	$V_{DD} \times 0.85$	–	V_{DD}	V	2
Medium level input voltage	V_{IM}	–	$V_{DD} \times 0.45$	–	$V_{DD} \times 0.55$	V	2
Low level input voltage	V_{IL}	–	V_{SS}	–	$V_{DD} \times 0.15$	V	2
High level output voltage	V_{OH}	I_{OUT} = –0.5 mA	V_{DD} – 0.4	–	–	V	3
Low level output voltage	V_{OL}	I_{OUT} = 0.5 mA	–	–	0.4	V	4
High level input current	I_{IH}	Peak value	9	18	36	μA	5
Low level input current	I_{IL}	Peak value	–36	–18	–9	μA	6
Awake mode time	t_{AW}	–	–	0.1	–	ms	–
Sleep mode time	t_{SL}	–	–	5.6	–	ms	–
Operating cycle	t_{CYCLE}	$t_{AW} + t_{SL}$	–	5.7	12.0	ms	–
Detection pole switching time	t_{SWP}	–	–	5.7	24.0	ms	–

■ Magnetic Characteristics

1. Product with B_{OP} = 1.8 mT typ. (B_{HYS} = 0.7 mT typ.)

Table 9

(Ta = +25°C, V_{DD} = 1.8 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	SWP pin = V_{IM} or V_{IL}	0.6	1.8	3.0	mT	7
	N pole	B_{OPN}	SWP pin = V_{IM} or V_{IH}	−3.0	−1.8	−0.6	mT	7
Release point*2	S pole	B_{RPS}	SWP pin = V_{IM} or V_{IL}	0.1	1.1	2.4	mT	7
	N pole	B_{RPN}	SWP pin = V_{IM} or V_{IH}	−2.4	−1.1	−0.1	mT	7
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	−	0.7	−	mT	7
	N pole	B_{HYSN}	$B_{HYSN} = \|B_{OPN} - B_{RPN}\|$	−	0.7	−	mT	7

2. Product with B_{OP} = 3.0 mT typ. (B_{HYS} = 0.8 mT typ.)

Table 10

(Ta = +25°C, V_{DD} = 1.8 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	SWP pin = V_{IM} or V_{IL}	1.6	3.0	4.0	mT	7
	N pole	B_{OPN}	SWP pin = V_{IM} or V_{IH}	−4.0	−3.0	−1.6	mT	7
Release point*2	S pole	B_{RPS}	SWP pin = V_{IM} or V_{IL}	1.1	2.2	3.7	mT	7
	N pole	B_{RPN}	SWP pin = V_{IM} or V_{IH}	−3.7	−2.2	−1.1	mT	7
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	−	0.8	−	mT	7
	N pole	B_{HYSN}	$B_{HYSN} = \|B_{OPN} - B_{RPN}\|$	−	0.8	−	mT	7

3. Product with B_{OP} = 3.0 mT typ. (B_{HYS} = 1.3 mT typ.)

Table 11

(Ta = +25°C, V_{DD} = 1.8 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	SWP pin = V_{IM} or V_{IL}	1.6	3.0	4.0	mT	7
	N pole	B_{OPN}	SWP pin = V_{IM} or V_{IH}	−4.0	−3.0	−1.6	mT	7
Release point*2	S pole	B_{RPS}	SWP pin = V_{IM} or V_{IL}	0.5	1.7	2.8	mT	7
	N pole	B_{RPN}	SWP pin = V_{IM} or V_{IH}	−2.8	−1.7	−0.5	mT	7
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	−	1.3	−	mT	7
	N pole	B_{HYSN}	$B_{HYSN} = \|B_{OPN} - B_{RPN}\|$	−	1.3	−	mT	7

4. Product with B_{OP} = 4.5 mT typ. (B_{HYS} = 1.0 mT typ.)

Table 12

(Ta = +25°C, V_{DD} = 1.8 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	SWP pin = V_{IM} or V_{IL}	2.5	4.5	6.0	mT	7
	N pole	B_{OPN}	SWP pin = V_{IM} or V_{IH}	−6.0	−4.5	−2.5	mT	7
Release point*2	S pole	B_{RPS}	SWP pin = V_{IM} or V_{IL}	2.0	3.5	5.5	mT	7
	N pole	B_{RPN}	SWP pin = V_{IM} or V_{IH}	−5.5	−3.5	−2.0	mT	7
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	−	1.0	−	mT	7
	N pole	B_{HYSN}	$B_{HYSN} = \|B_{OPN} - B_{RPN}\|$	−	1.0	−	mT	7

5. Product with B_{OP} = 4.5 mT typ. (B_{HYS} = 2.5 mT typ.)

Table 13

(Ta = +25°C, V_{DD} = 1.8 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	SWP pin = V_{IM} or V_{IL}	2.5	4.5	6.0	mT	7
	N pole	B_{OPN}	SWP pin = V_{IM} or V_{IH}	−6.0	−4.5	−2.5	mT	7
Release point*2	S pole	B_{RPS}	SWP pin = V_{IM} or V_{IL}	0.8	2.0	3.5	mT	7
	N pole	B_{RPN}	SWP pin = V_{IM} or V_{IH}	−3.5	−2.0	−0.8	mT	7
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	−	2.5	−	mT	7
	N pole	B_{HYSN}	$B_{HYSN} = \lvert B_{OPN} - B_{RPN} \rvert$	−	2.5	−	mT	7

***1.** B_{OPN}, B_{OPS}: Operation points
B_{OPN} and B_{OPS} are the values of magnetic flux density when the output voltage (V_{OUT}) changes after the magnetic flux density applied to this IC by the magnet (N pole or S pole) is increased (by moving the magnet closer).
Even when the magnetic flux density exceeds B_{OPN} or B_{OPS}, V_{OUT} retains the status.

***2.** B_{RPN}, B_{RPS}: Release points
B_{RPN} and B_{RPS} are the values of magnetic flux density when the output voltage (V_{OUT}) changes after the magnetic flux density applied to this IC by the magnet (N pole or S pole) is decreased (the magnet is moved further away).
Even when the magnetic flux density falls below B_{RPN} or B_{RPS}, V_{OUT} retains the status.

***3.** B_{HYSN}, B_{HYSS}: Hysteresis widths
B_{HYSN} and B_{HYSS} are the difference of magnetic flux density between B_{OPN} and B_{RPN}, and B_{OPS} and B_{RPS}, respectively.

Remark The unit of magnetic flux density mT can be converted by using the formula 1 mT = 10 Gauss.

■ Test Circuits

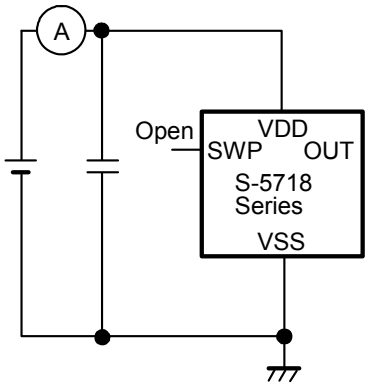


Figure 3 Test Circuit 1

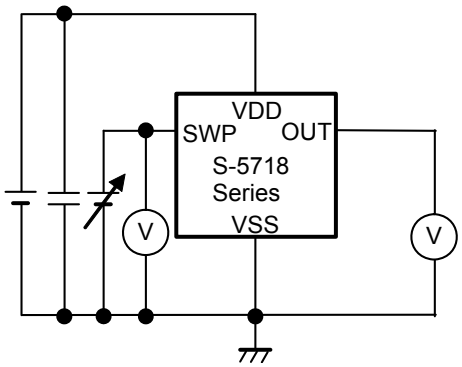


Figure 4 Test Circuit 2

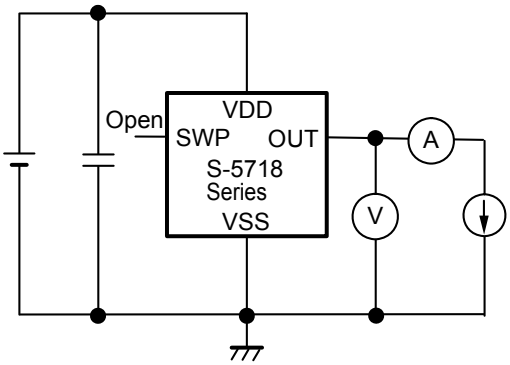


Figure 5 Test Circuit 3

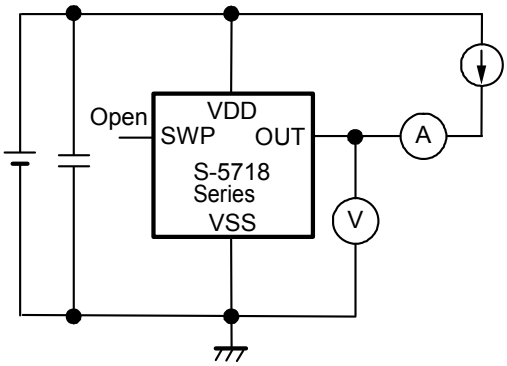


Figure 6 Test Circuit 4

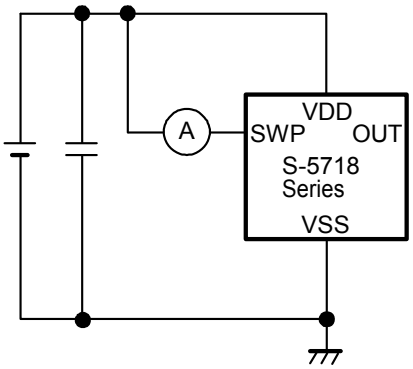


Figure 7 Test Circuit 5

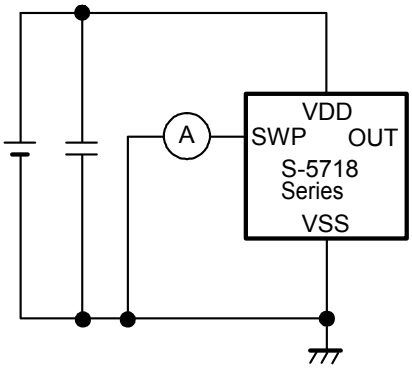


Figure 8 Test Circuit 6

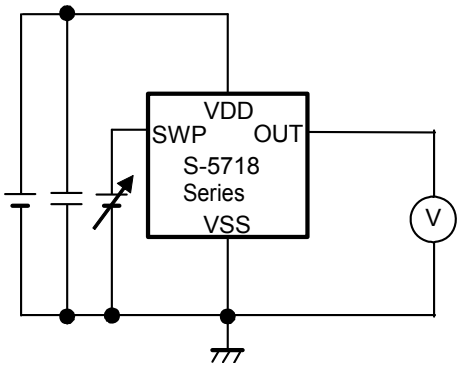


Figure 9 Test Circuit 7

■ Standard Circuits

1. **Omnipolar detection operation (SWP pin = Open)**

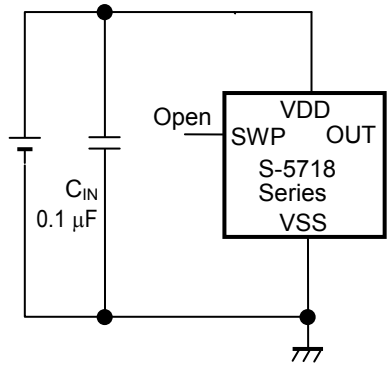


Figure 10

2. **S pole detection operation (SWP pin = V_{SS})**

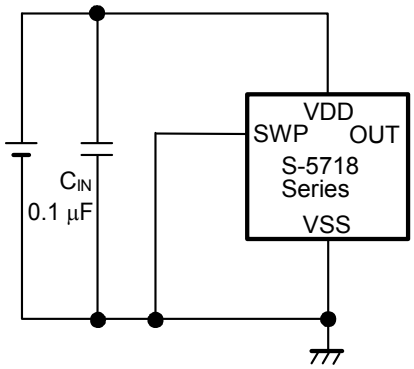


Figure 11

3. **N pole detection operation (SWP pin = V_{DD})**

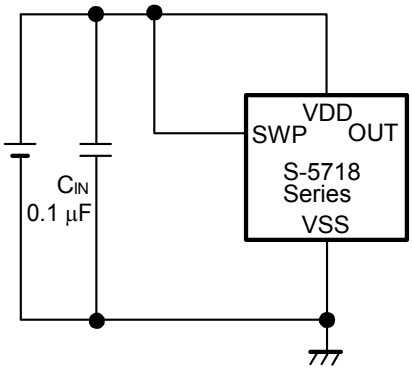


Figure 12

4. **Detection pole switching operation (SWP pin = Open / V_{SS} / V_{DD})**

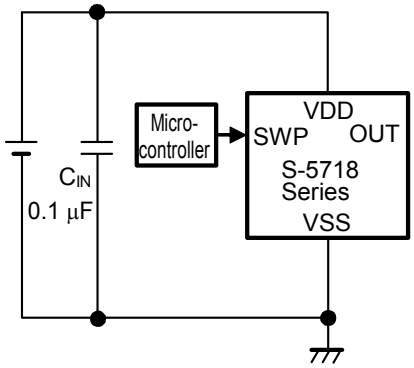


Figure 13

Caution The above connection diagrams and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

■ Operation

1. Direction of applied magnetic flux

This IC detects the magnetic flux density which is vertical to the marking surface.
Figure 14 shows the direction in which magnetic flux is being applied.

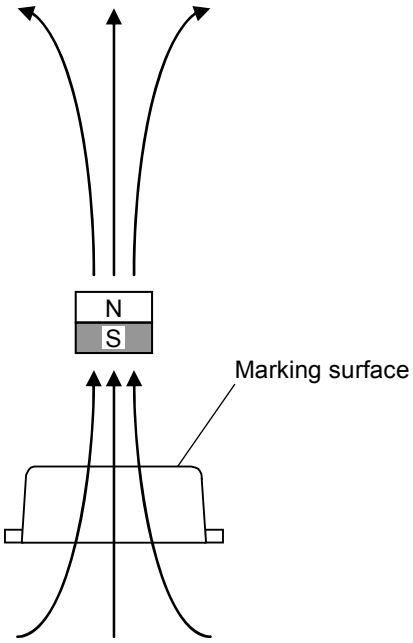


Figure 14

2. Position of Hall sensor

Figure 15 shows the position of Hall sensor.
The center of this Hall sensor is located in the area indicated by a circle, which is in the center of a package as described below.
The following also shows the distance (typ. value) between the marking surface and the chip surface of a package.

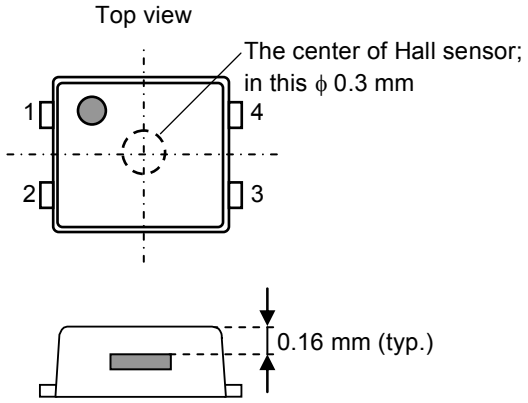


Figure 15

3. Basic operation

This IC changes the output voltage (V_{OUT}) according to the level of the magnetic flux density (N pole or S pole) applied by a magnet.
This IC can also switch the detection pole according to the SWP pin input voltage (V_{IN}) status.
The following explains the operation for active "L" products.

3. 1 When V_{IN} is medium level input voltage (V_{IM})

This IC performs omnipolar detection operation. Set the SWP pin to an open status or input V_{IM} to the SWP pin.
If a capacitor with large capacitance is connected to the SWP pin when using the pin in the open status, steep changes in power supply voltage at power-on and during power supply fluctuations may cause erroneous N pole or S pole detection operation. For this reason, it is recommended that the SWP pin capacity be set to 100 pF or lower including parasitic capacitance.

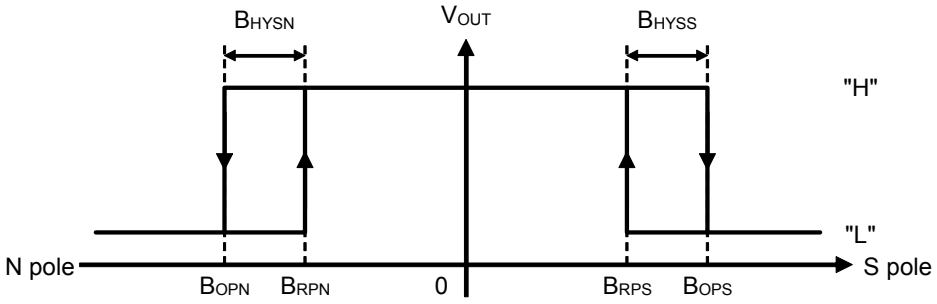


Figure 16

3. 2 When V_{IN} is low level input voltage (V_{IL})

This IC performs S pole detection operation. Connect the SWP pin to VSS pin with a resistor having 10 kΩ or lower, or input V_{IL} to the SWP pin.

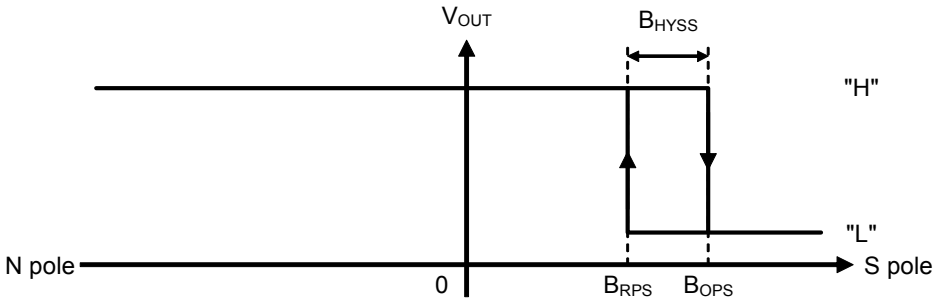


Figure 17

3. 3 When V_{IN} is high level input voltage (V_{IH})

This IC performs N pole detection operation. Connect the SWP pin to VDD pin with a resistor having 10 kΩ or lower, or input V_{IH} to the SWP pin.

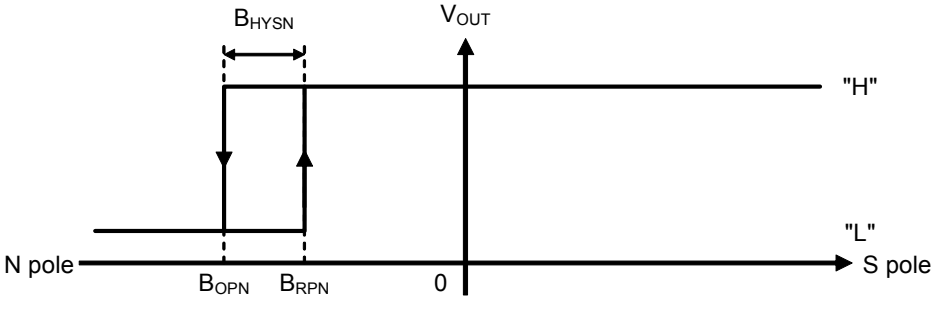


Figure 18

4. Time dependency in the current consumption

This IC performs the intermittent operation, and operates at a low current consumption by repeating sleep mode and awake mode.

Figure 19 shows the time dependency in the current consumption.

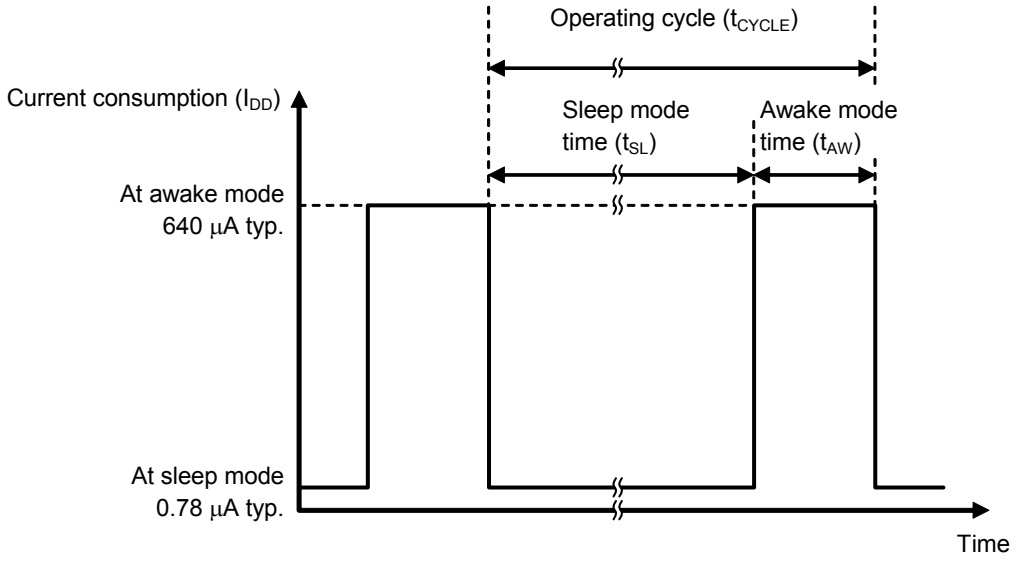


Figure 19

5. Timing chart for magnetic flux density response

Figure 20 shows the operation timing chart for active "L" products.

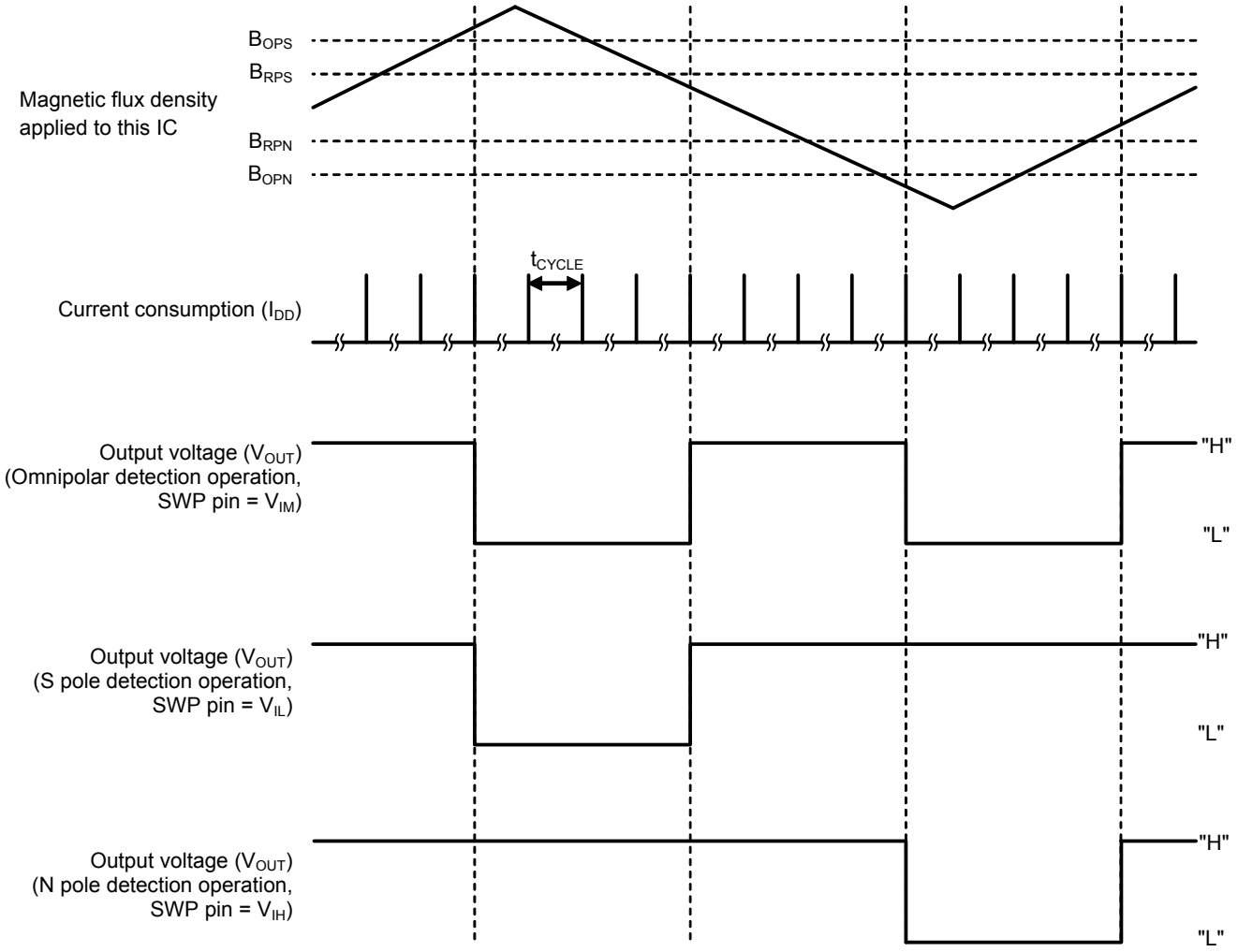


Figure 20

6. Timing chart for detection pole switching

During awake mode time (t_{AW}), this IC detects the SWP pin input voltage (V_{IN}), and the detection pole switches when t_{AW} ends. **Figure 21** and **Figure 22** show the timing chart for switching from N pole detection to S pole detection when magnetic flux density (B) > B_{OPS} in active "L" products.

When V_{IN} changes during sleep mode time (t_{SL}) between t_{AW}<1> and t_{AW}<2> and does not change during t_{AW}<2>, this IC outputs the output voltage (V_{OUT}) according to the detection pole when t_{AW}<2> ends.

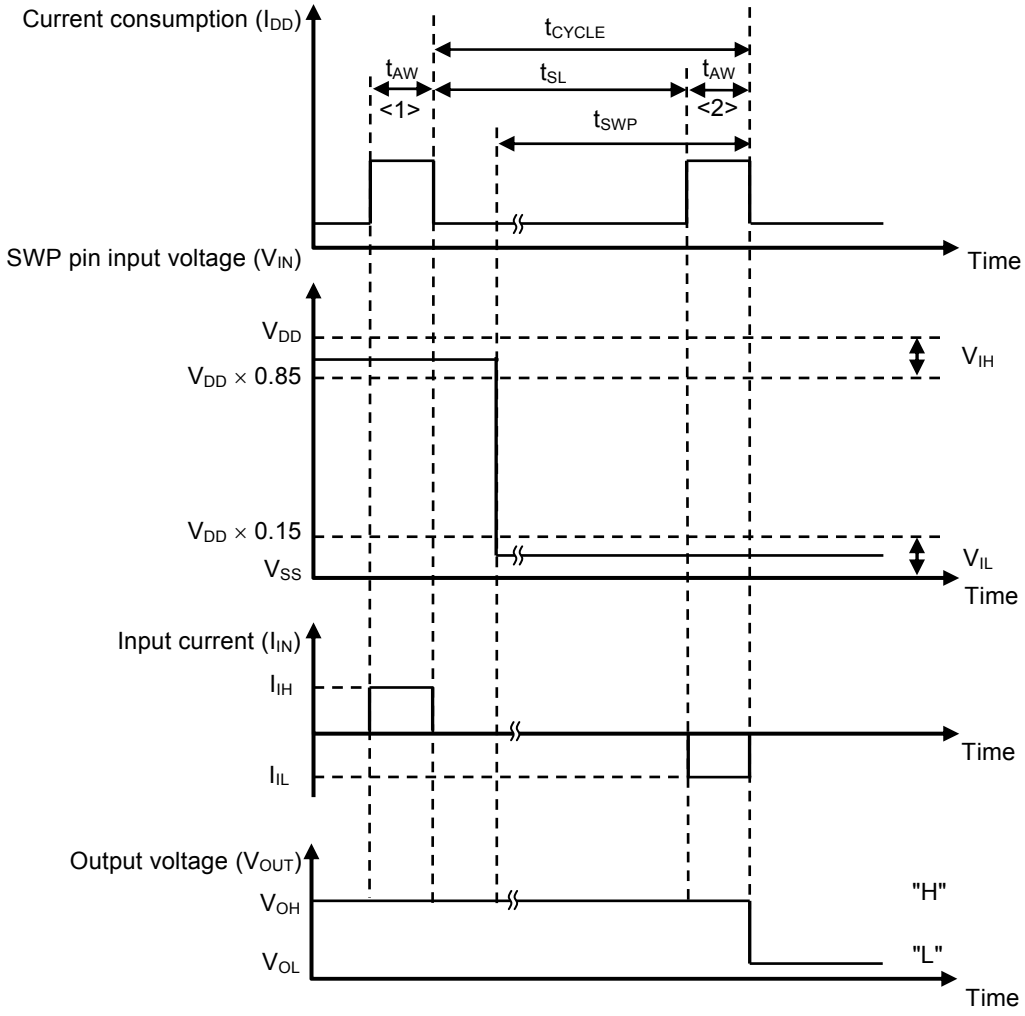


Figure 21 When V_{IN} does not Change during t_{AW}<2>

When V_{IN} changes during t_{AW}<2>, this IC may output V_{OUT} according to the detection pole when t_{AW}<1> ends. Refer to **Figure 21** for the operation of t_{AW}<3>.

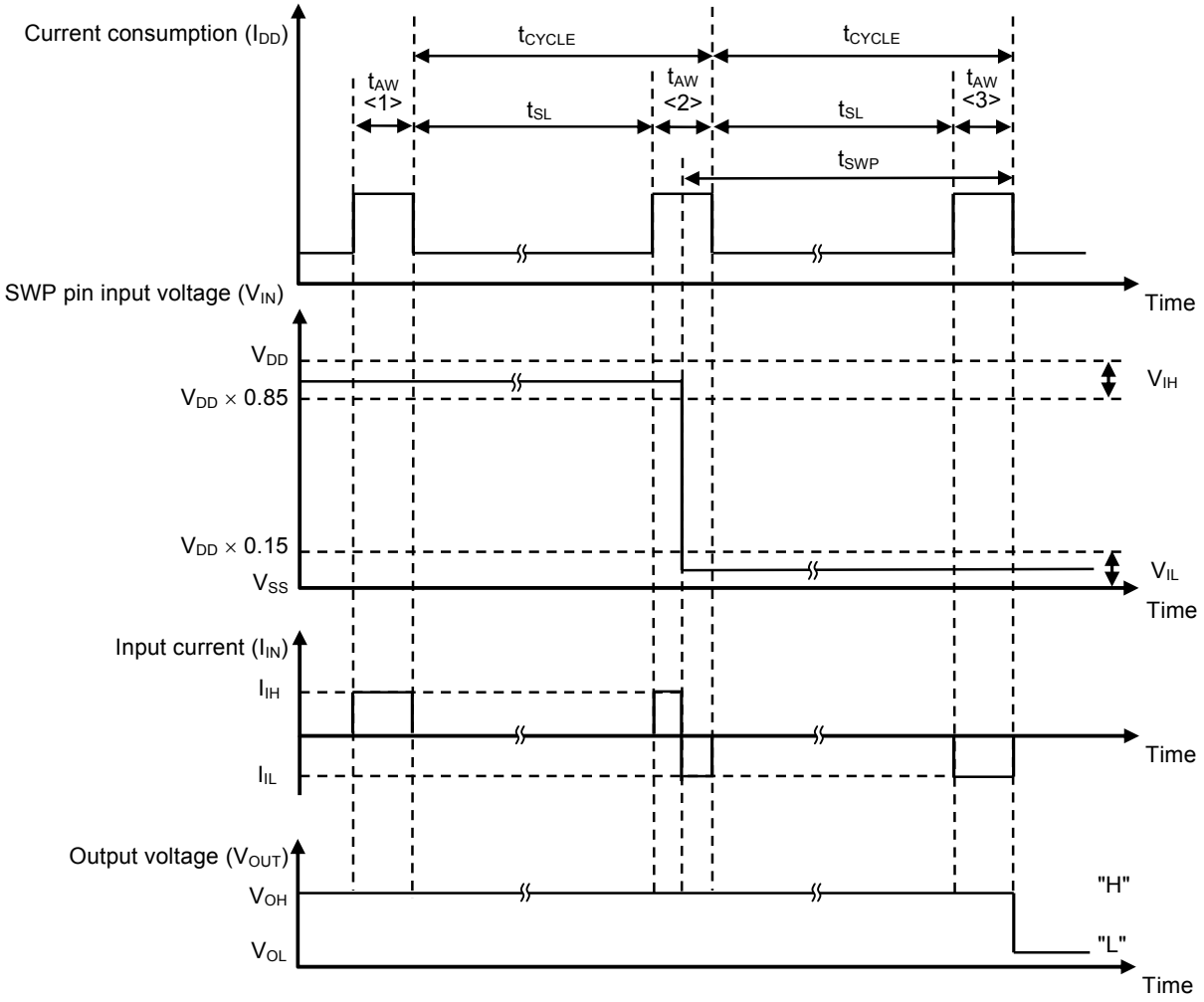


Figure 22 When V_{IN} Changes during t_{AW}<2>

■ Precautions

- If the impedance of the power supply is high, the IC may malfunction due to a supply voltage drop caused by feed-through current. Take care with the pattern wiring to ensure that the impedance of the power supply is low.

- Note that the IC may malfunction if the power supply voltage rapidly changes. When the IC is used under the environment where the power supply voltage rapidly changes, it is recommended to judge the output voltage of the IC by reading it multiple times.

- Note that the IC may malfunction in the following situations.
  When the OUT pin is shorted to VSS pin or VDD pin.
  When the OUT pin is affected by noise.
  When the intermediate potential is applied to the OUT pin.

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- Large stress on this IC may affect the magnetic characteristics. Avoid large stress which is caused by the handling during or after mounting the IC on a board.

- Note that the output voltage may change if the intermediate value of magnetic flux density between the operation point and release point is applied to this IC over a long time.

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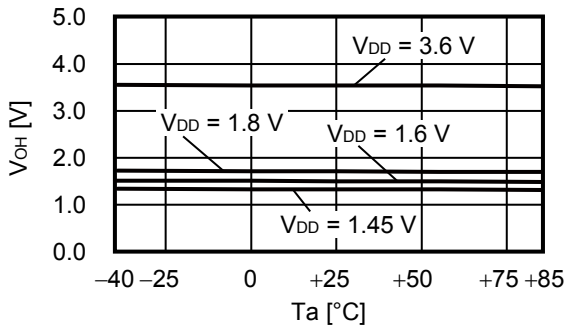
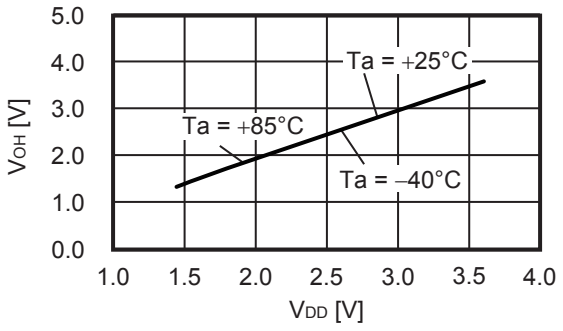
■ Characteristics (Typical Data)

1. Output voltage

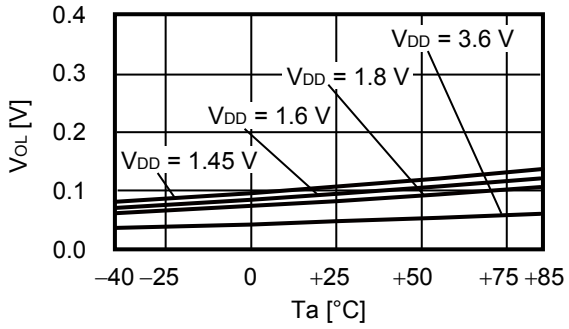
1. 1 High level output voltage (V_{OH}) vs. Temperature (Ta)



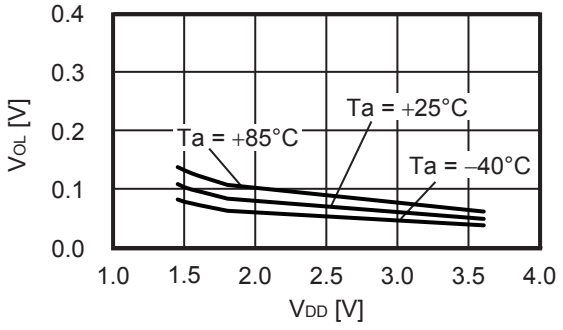
1. 2 High level output voltage (V_{OH}) vs. Power supply voltage (V_{DD})



1. 3 Low level output voltage (V_{OL}) vs. Temperature (Ta)



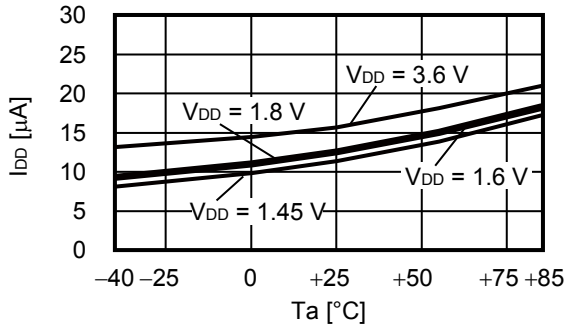
1. 4 Low level output voltage (V_{OL}) vs. Power supply voltage (V_{DD})



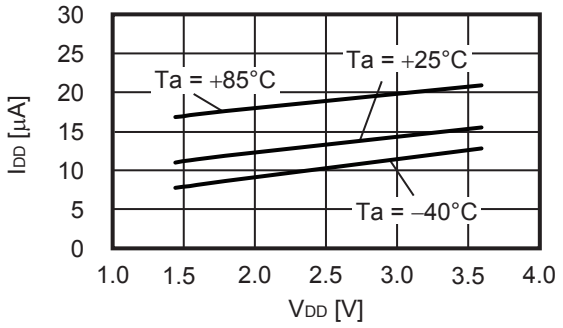
2. Current consumption, operating cycle

2. 1 S-5718Cxxxx

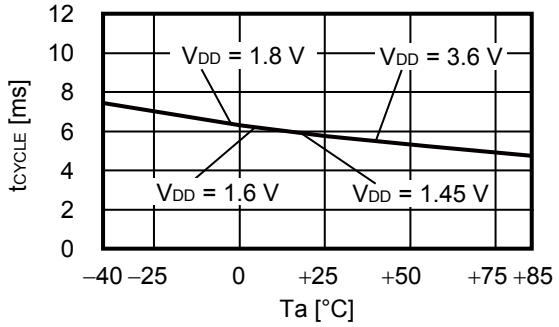
2. 1. 1 Current consumption (I_{DD}) vs. Temperature (Ta)



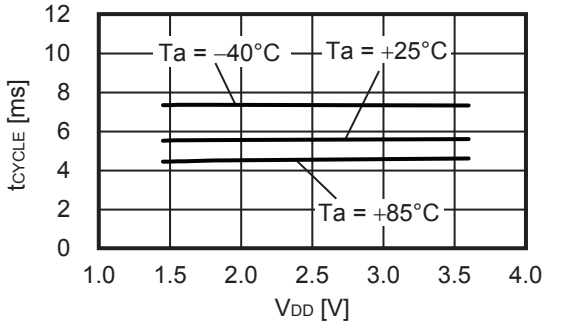
2. 1. 2 Current consumption (I_{DD}) vs. Power supply voltage (V_{DD})



2. 1. 3 Operating cycle (t_{CYCLE}) vs. Temperature (Ta)



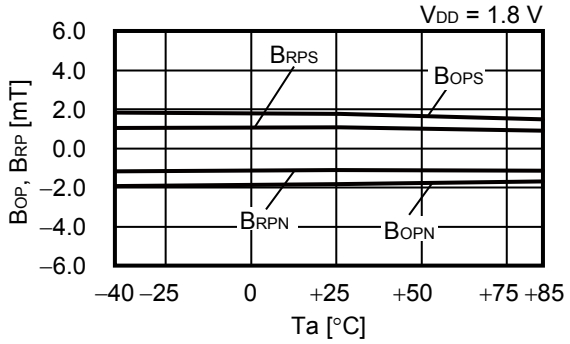
2. 1. 4 Operating cycle (t_{CYCLE}) vs. Power supply voltage (V_{DD})



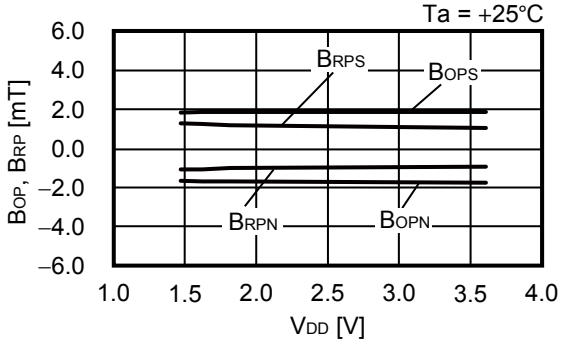
3. Magnetic sensitivity

3. 1 S-5718xxSx0

3. 1. 1 Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)

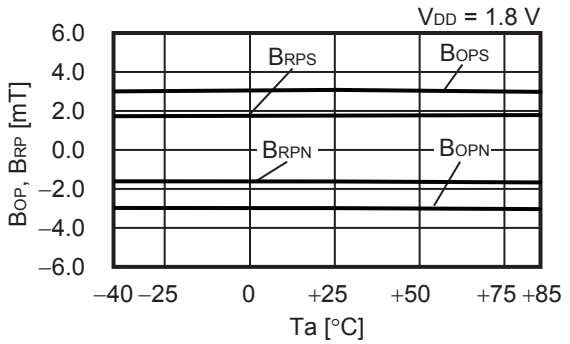


3. 1. 2 Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})

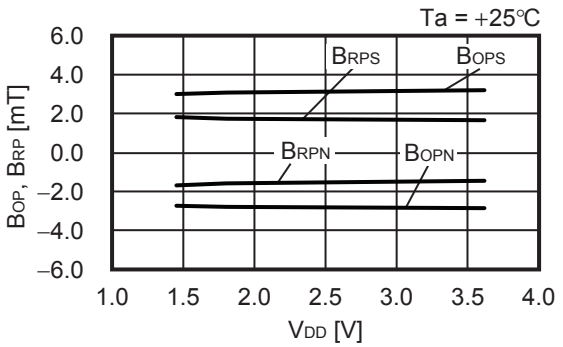


3. 2 S-5718xxWx1

3. 2. 1 Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)

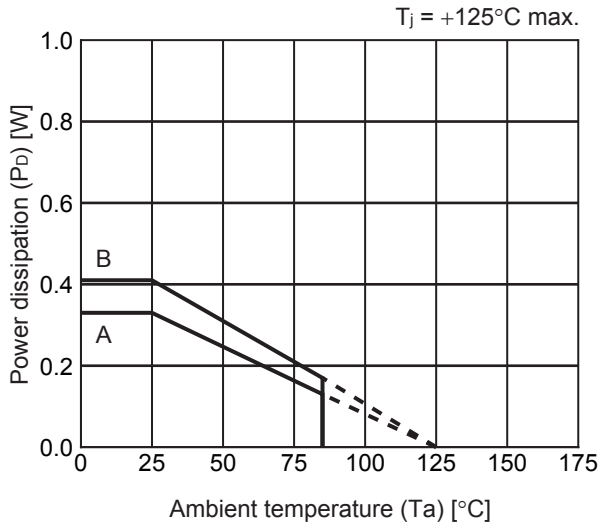


3. 2. 2 Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})



■ Power Dissipation

SNT-4A

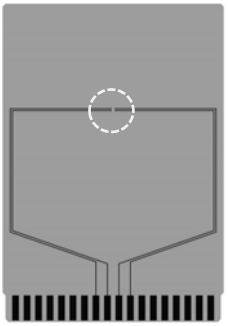


Board	Power Dissipation (P_D)
A	0.33 W
B	0.41 W
C	–
D	–
E	–

SNT-4A Test Board

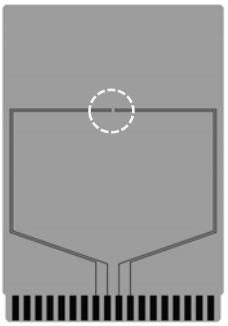
IC Mount Area

(1) Board A



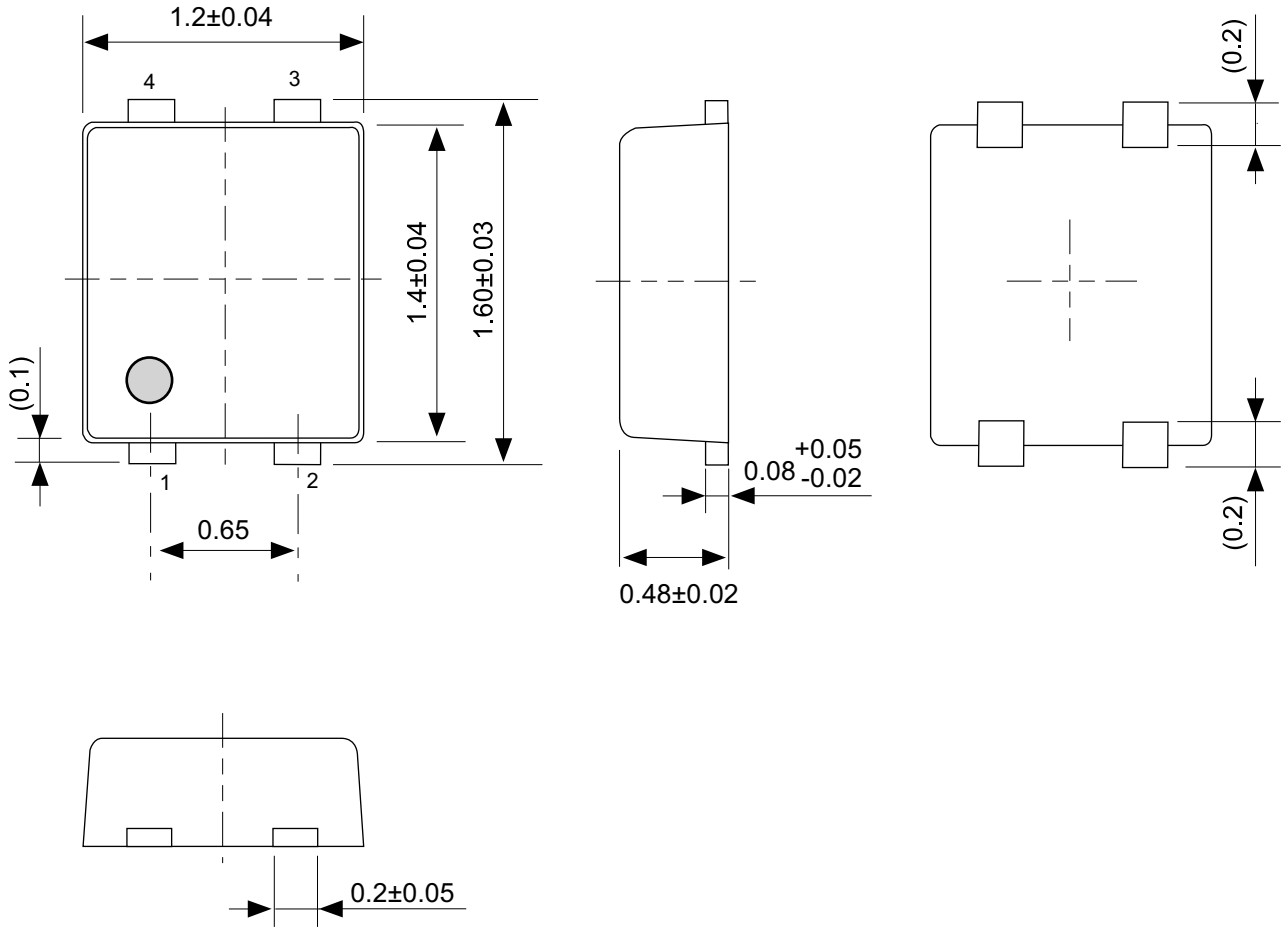
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



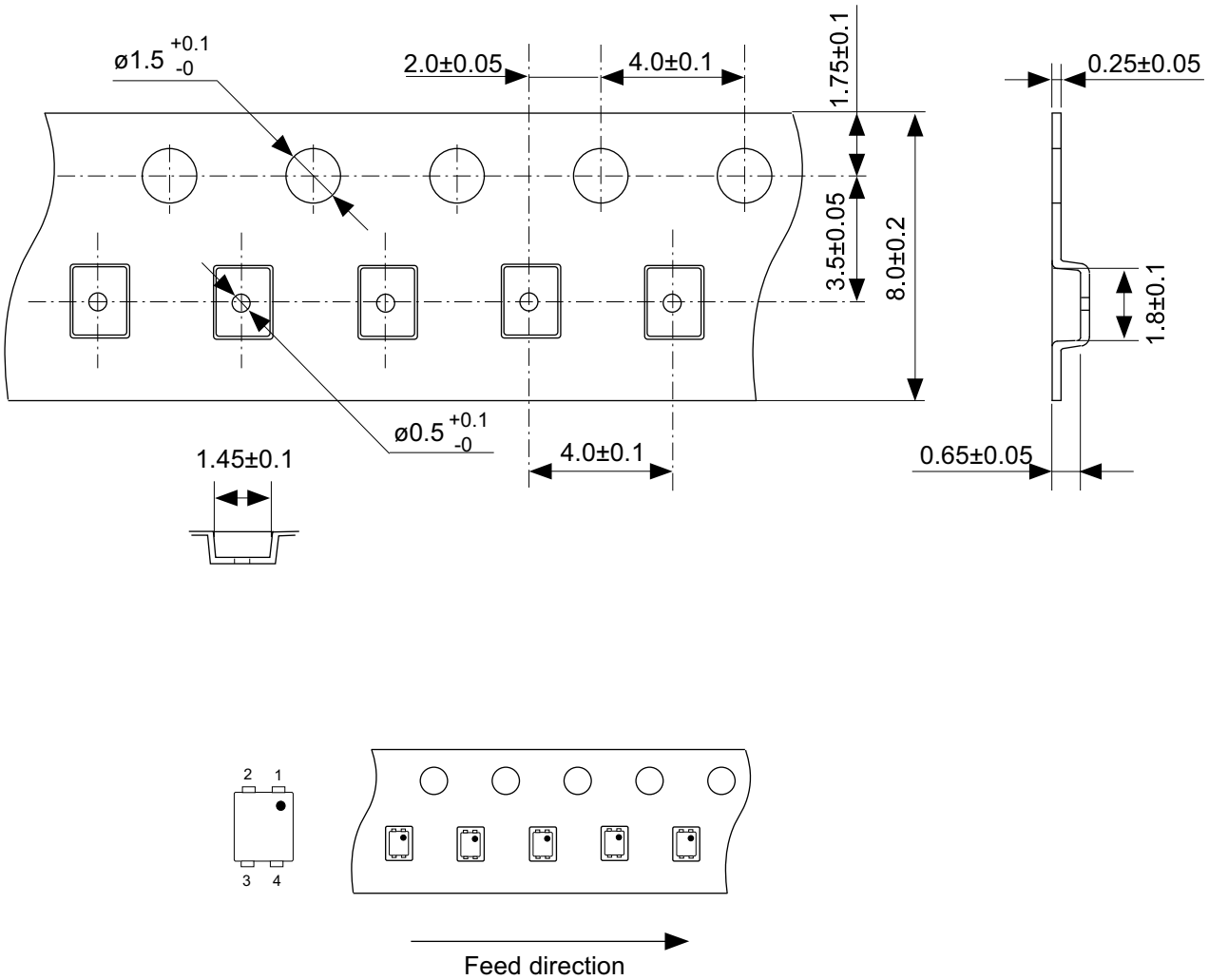
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. SNT4A-A-Board-SD-1.0



No. PF004-A-P-SD-6.0

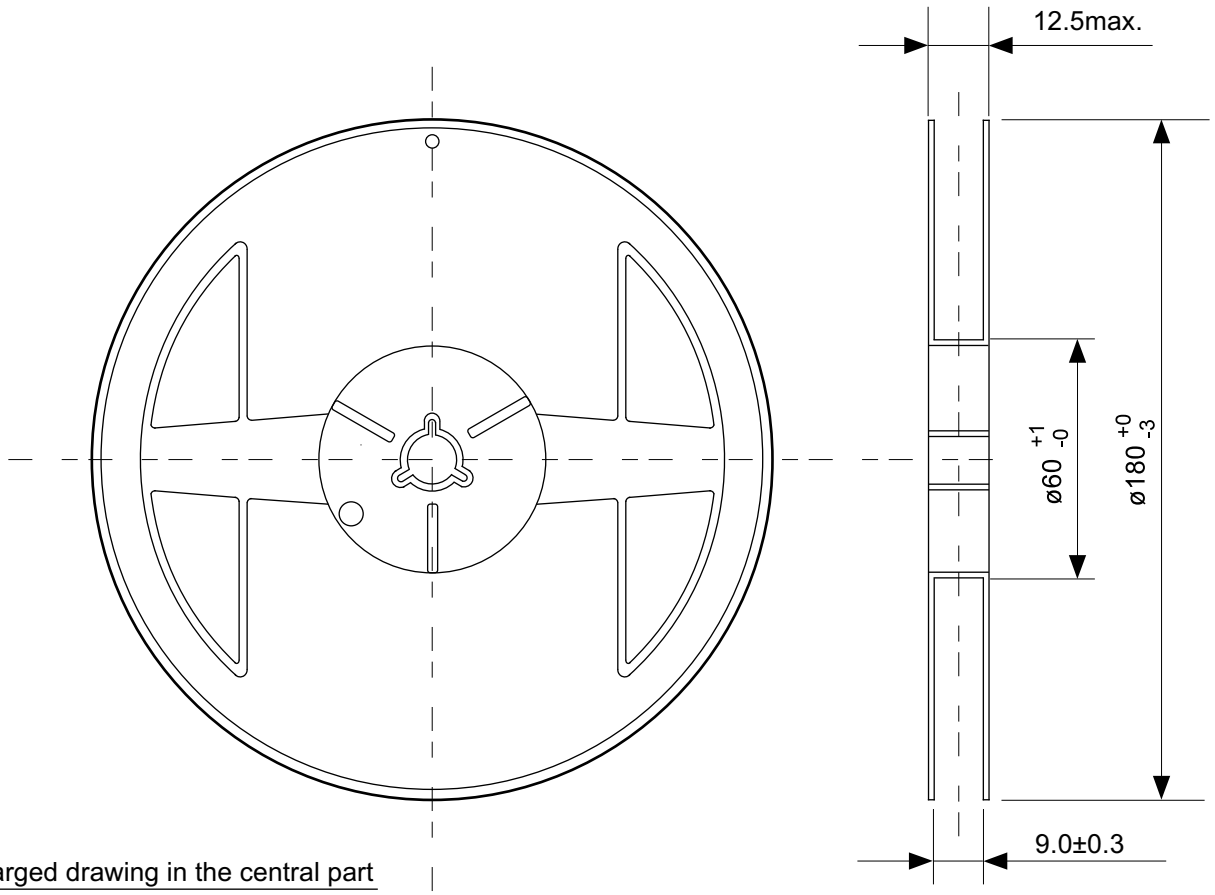
TITLE	SNT-4A-A-PKG Dimensions
No.	PF004-A-P-SD-6.0
ANGLE	
UNIT	mm
ABLIC Inc.	



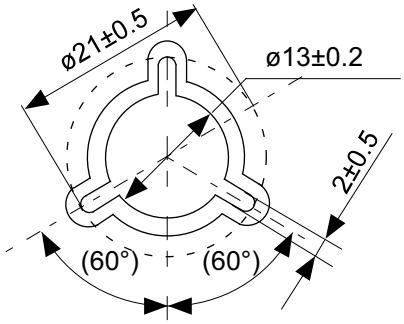
No. PF004-A-C-SD-2.0

TITLE	SNT-4A-A-Carrier Tape
No.	PF004-A-C-SD-2.0
ANGLE	
UNIT	mm

ABLIC Inc.



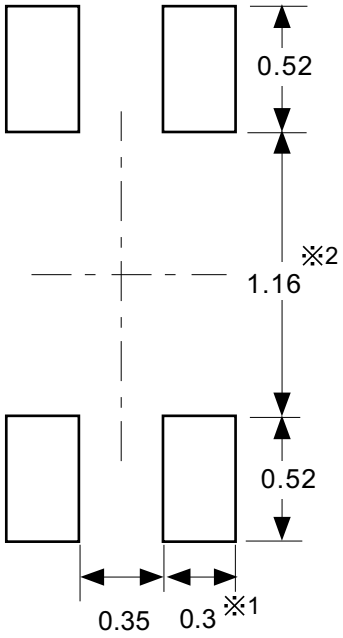
Enlarged drawing in the central part



No. PF004-A-R-SD-1.0

TITLE	SNT-4A-A-Reel		
No.	PF004-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		

ABLIC Inc.



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.10 mm ~ 1.20 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から**0.03 mm** 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は ″SNTパッケージ活用の手引き″ を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.10 mm to 1.20 mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.10 mm ~ 1.20 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PF004-A-L-SD-4.1

TITLE	SNT-4A-A -Land Recommendation
No.	PF004-A-L-SD-4.1
ANGLE	
UNIT	mm

ABLIC Inc.

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2.4-2019.07

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