

S-75V00ANC

MINI LOGIC SERIES 2 INPUT NAND GATE

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Rev.4.0_01

The S-75V00ANC is a single 2-Input NAND Gate fabricated by utilizing advanced silicon-gate CMOS technology which provides the inherent benefit of CMOS low power consumption to achieve ultra high speed operation correspond to LSTTL IC's.

All gates of the internal circuitry have buffered outputs to ensure high noise immunity and output stability,

1.0 μA max. (at 5.5 V, 25°C)

 t_{PD} = 3.7 ns (at 5 V) V_{NIH} = V_{NIL} = 28% V_{CC} min.

2 V to 5.5 V

All pins

Input voltage is allowed to be applied even if power voltage is not supplied because no diode is inserted between an input pin and V_{CC} .

This allows for interfaces between power supplies of different voltage, output level conversion from 5 V to 3 V and battery backup applications.

Features

- Wide power supply range:
- Low current consumption:
- Typical propagation delay:
- High noise immunity:
- Power down protection:
- Lead-free

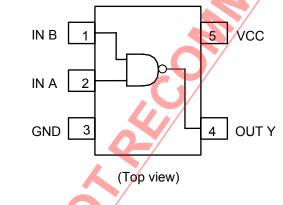
Applications

- Personal computers, peripherals
- Cellular phones
- Cameras
- Games

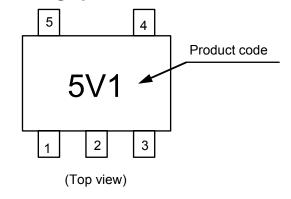
Package

• SC-88A

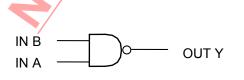
Pin Configuration



Marking Specification

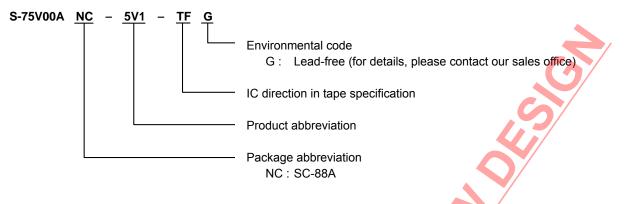


Logic Diagram



Thue values									
А	В	Y							
L	L	Н							
L	Н	Н							
Н	L	Н							
Н	Н	L							

True volues



Absolute Maximum Ratings

		(Ta = 25°C unless other	wise specified
Item	Symbol	Absolute Maximum Ratings	Unit
Power supply voltage	V _{CC}	-0,5 to +7.0	V
Input voltage	V _{IN}	-0.5 to +7.0	V
Output voltage	V _{OUT}	-0.5 to V _{CC} + 0.5	V
Input parasitic diode current	I _{IK}	-20	mA
Output parasitic diode current	Ι _{οκ}	±20	mA
Output current	I _{OUT}	±25	mA
V _{CC} /GND current	I _{CC}	±50	mA
Dewer dissinction		200 (When not mounted on board)	mW
Power dissipation	PD	350 ^{*1}	mW
Operating ambient temperature	T _{opr}	_40 to +85	°C
Storage temperature	T _{stg}	-65 to +150	°C
Lead temperature (10 s)	TL	260	°C

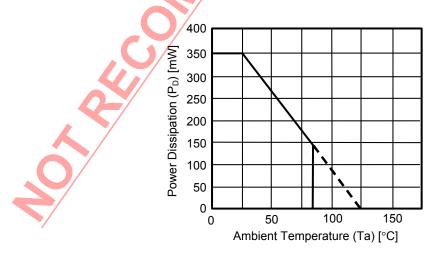
*1. When mounted on board

[Mounted board]

(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm

(2) Board name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.



Power Dissipation of Package (When Mounted on Board)

Recommended Operating Conditions

Item	Symbol	Standard	Unit
Power voltage	V _{CC}	2 to 5.5	V
Input voltage	V _{IN}	0 to 5.5	V
Output voltage	V _{OUT}	0 to V _{CC}	V
langest size of fall times		0 to 100 (V _{CC} = 3.3±0.3 V)	ns
Input rise / fall time	t _R , t _F	0 to 20 (V _{CC} = 5±0.5 V)	ns

■ DC Electrical Characteristics

				Canditiana			Ta - 2500		To - 40	te 0500	
Iter	n	Symbol		Conditions	14		Ta = 25°Q		Ta = -40		Unit
	1				V_{CC}	Min.	Тур.	Max.	Min.	Max.	
	"H" level	VIH			2.0	1.5		<i>—</i>	1.5		V
Input	II level	VIH			3 to 5.5	$V_{CC} \times 0.7$	H.	/_	$V_{CC} \times 0.7$		V
voltage	"!" lovel	V			2.0	_		0.5		0.5	V
	"L" level	V _{IL}		_	3 to 5.5			$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	V
					2.0	1.9	2.0	_	1.9		V
			., .,	I _{OH} = –50 μA	3.0	2.9	3.0	_	2.9	_	V
	"H" level	V _{OH}	$V_{IN} = V_{IL}$		4.5	4.4	4.5	_	4.4	_	V
			or V _{IH}	I _{он} = –4 mA	3.0	2.58	_	_	2.48	_	V
Output				I _{он} = –8 mA	4.5	3.94	_	_	3.80	_	V
voltage					2.0		0	0.1		0.1	V
				I _{OL} = 50 μA	3.0	/ _	0	0.1	_	0.1	V
	"L" level	V _{OL}	$V_{IN} = V_{IH}$		4.5	_	0	0.1	_	0.1	V
				I _{OL} = 4 mA	3.0			0.36		0.44	V
				I _{OL} = 8 mA	4.5			0.36	_	0.44	V
Input curren	t	I _{IN}	V _{IN} = 5.5 V	V _{IN} = 5.5 V or GND				±0.1		±1.0	μA
Current con	sumption	Icc	$V_{IN} = V_{CC} o$	r GND	5.5			1.0		10.0	μA

<u>5.5 V</u> <u>J = V_{CC} or </u>

MINI LOGIC SERIES 2 INPUT NAND GATE S-75V00ANC

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■ AC Electrical Characteristics

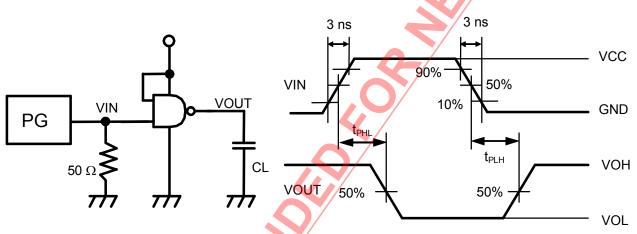
					(1	input t _r = 1	i _F = 3 ns u	niess othe	rwise spe	cified)			
lto an	Currah al	Measur	rement Co	onditions		Ta = 25°C		Ta = -40	to 85°C	Linit			
Item	Symbol		V _{CC} (V)	C _L (pF)	Min.	Тур.	Max.	Min.	Max.	Unit			
				15	_	5.5	7.9	1.0	9.5	ns			
Dranagation dology time	t _{PLH} ,	_	_			3.3±0.3	50		10.0	14.0	1.0	15.0	ns
Propagation delay time	t _{PHL}			EQUOE	15		3.7	5.5	1.0	6.5	ns		
			5.0±0.5	50		6.1	8.5	1.0	9.0	ns			
Input capacitance	C _{IN}	_			4	10	7	10	pF				
Equivalent internal capacitance	C _{PD} ^{*1}		_			14		_		pF			

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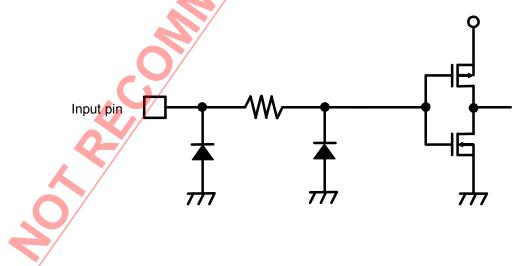
*1. C_{PD} is the no-load equivalent capacitance inside the circuitry. Refer to the measurement circuit shown below. Current consumption is averaged by the following equation.

 $I_{CC(opr)} = C_{PD} \times V_{CC} \times fin + I_{CC}$

Measurement Circuit



Remark No-load output during measurement of current consumption.





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S-75V02ANC

MINI LOGIC SERIES 2 INPUT NOR GATE

Rev.4.0_01

The S-75V02ANC is a single 2-input NOR gate fabricated by utilizing advanced silicon-gate CMOS technology which provides the inherent benefit of CMOS low power consumption to achieve ultra high speed operation correspond to LSTTL IC's.

All gates of the internal circuitry have buffered outputs to ensure high noise immunity and output stability,

Input voltage is allowed to be applied even if power voltage is not supplied because no diode is inserted between an input pin and V_{CC} .

This allows for interfaces between power supplies of different voltage, output level conversion from 5 V to 3 V and battery backup applications.

Features

- Wide power supply range:
- Low current consumption:
- Typical propagation delay:
- High noise immunity:
- Power down protection:
- Lead-free

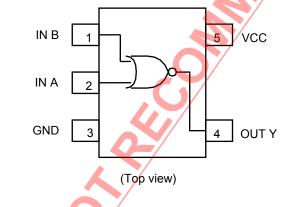
Applications

- Personal computers, peripherals
- Cellular phones
- Cameras
- Games

Package

• SC-88A

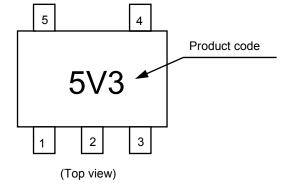
Pin Configuration



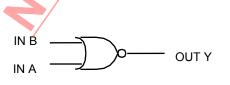
2 V to 5.5 V

- 1.0 μA max. (at 5.5 V, 25°C)
- t_{PD} = 3.6 ns (at 5 V)
- $V_{NIH} = V_{NIL} = 28\% V_{CC} min.$ All pins

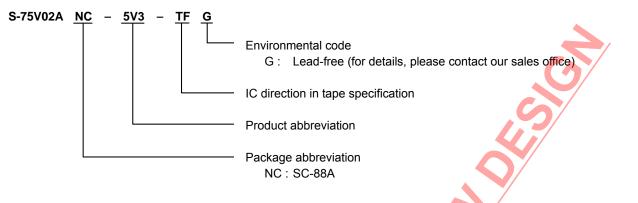
Marking Specification



Logic Diagram



True values		
A	В	Y
L	L	Н
L	Н	L
Н	L	L
Н	Н	L



Absolute Maximum Ratings

		(Ta ≠ 25°C unless other	wise specified
ltem	Symbol	Absolute Maximum Ratings	Unit
Power supply voltage	V _{CC}	0,5 to +7.0	V
Input voltage	V _{IN}	-0.5 to +7.0	V
Output voltage	V _{OUT}	0.5 to V _{CC} + 0.5	V
Input parasitic diode current	I _{IK}	-20	mA
Output parasitic diode current	Ι _{οκ}	±20	mA
Output current	I _{OUT}	±25	mA
V _{CC} /GND current	I _{CC}	±50	mA
Dever dissignation		200 (When not mounted on board)	mW
Power dissipation	PD	350 ^{*1}	mW
Operating ambient temperature	T _{opr}	-40 to +85	°C
Storage temperature	T _{stq}	-65 to +150	°C
Lead temperature (10 s)	TL	260	°C
Lead temperature (10 s)		260	°C

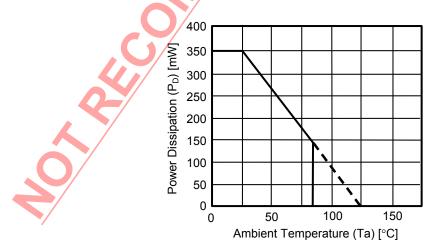
*1. When mounted on board

[Mounted board]

(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm

(2) Board name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.



Power Dissipation of Package (When Mounted on Board)

Recommended Operating Conditions

Item	Symbol	Standard	Unit
Power voltage	V _{cc}	2 to 5.5	V
Input voltage	V _{IN}	0 to 5.5	V
Output voltage	V _{OUT}	0 to V _{CC}	V
Innut rice / fell time		0 to 100 (V _{CC} = 3.3±0.3 V)	ns
Input rise / fall time	t _R , t _F	0 to 20 (V _{CC} = 5±0.5 V)	ns

DC Electrical Characteristics

14	_	O wash al		Conditions			Ta = 25°C		Ta = -40) to 85°C	1.1 14		
lter	T1	Symbol			V_{CC}	Min.	Тур.	Max.	Min.	Max.	Unit		
	"II" Javal	V			2.0	1.5			1.5		V		
Input	"H" level	V _{IH}		_	3 to 5.5	V _{CC} ×0.7			$V_{CC} \times 0.7$		V		
voltage	"L" level	V			2.0	_		0.5	_	0.5	V		
	Lievei	V _{IL}			3 to 5.5			$V_{CC} \times 0.3$	_	$V_{CC} \times 0.3$	V		
					2.0	1.9	2.0		1.9		V		
				I _{OH} = –50 μA	3.0	2.9	3.0	_	2.9	_	V		
	"H" level	V _{OH}	$V_{IN} = V_{IL}$	$V_{IN} = V_{IL}$	$V_{IN} = V_{IL}$		4.5	4.4	4.5	_	4.4	_	V
				I _{OH} = -4 mA	3.0	2.58	_	_	2.48	_	V		
Output				I _{OH} = –8 mA	4.5	3.94	_	_	3.80	_	V		
voltage					2.0		0	0.1	_	0.1	V		
			V - V	I _{OL} = 50 μA	3.0	/	0	0.1	_	0.1	V		
	"L" level	V _{OL}	$V_{IN} = V_{IH}$		4.5		0	0.1	_	0.1	V		
			or V _{IL}	I _{OL} = 4 mA	3.0	_	_	0.36		0.44	V		
				I _{OL} = 8 mA	4.5			0.36		0.44	V		
Input curren	t	I _{IN}	V _{IN} = 5.5 V	V _{IN} = 5.5 V or GND				±0.1		±1.0	μA		
Current con	sumption	I _{CC}	$V_{IN} = V_{CC} o$	r GND	5.5			1.0		10.0	μA		

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■ AC Electrical Characteristics

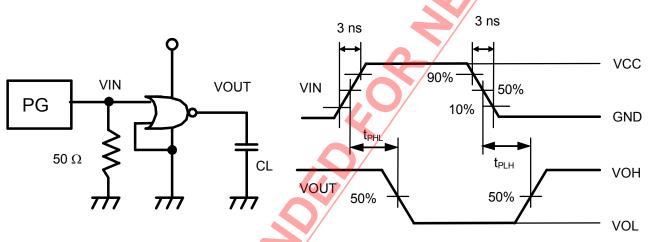
(Input $t_R = t_F = 3$ ns unless otherwise specified								cified)					
Itom	Symbol	Measur	ement Co	onditions		Ta = 25°C		Ta = -40	to 85°C	Linit			
Item	Symbol		V _{CC} (V)	C _L (pF)	Min.	Тур.	Max.	Min.	Max.	Unit			
		_		15	_	5.6	7.9	1.0	9.5	ns			
Dranagation dology time	t _{PLH} ,		_			3.3±0.3	50		10.0	14.0	1.0	15.0	ns
Propagation delay time	t _{PHL}			5.0±0.5	15		3.6	5.5	1.0	6.5	ns		
			5.0±0.5	50		5.7	8.0	1.0	9.0	ns			
Input capacitance	CIN		_			4	10		10	pF			
Equivalent internal capacitance	C _{PD} ^{*1}		—			15		_		pF			

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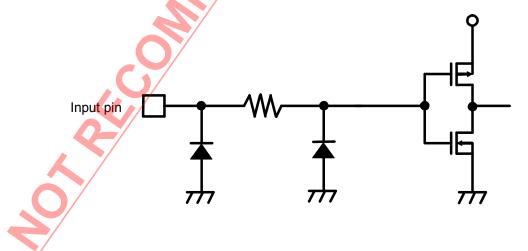
*1. C_{PD} is the no-load equivalent capacitance inside the circuitry. Refer to the measurement circuit shown below. Current consumption is averaged by the following equation.

 $I_{\text{CC(opr)}} = C_{\text{PD}} \times V_{\text{CC}} \times fin + I_{\text{CC}}$

Measurement Circuit



Remark No-load output during measurement of current consumption.





S-75V04ANC

MINI LOGIC SERIES

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Rev.4.0_01

The S-75V04ANC is a INVERTER fabricated by utilizing advanced silicon-gate CMOS technology which provides the inherent benefit of CMOS low power consumption to achieve ultra high speed operation correspond to LSTTL IC's. The special purpose unbuffered circuit design is suitable for a wide variety of linear circuits.

Input voltage is allowed to be applied even if power voltage is not supplied because no diode is inserted between an input pin and V_{CC} .

This allows for interfaces between power supplies of different voltage, output level conversion from 5 V to 3 V and battery backup applications.

2 V to 5.5 V

All pins

1.0 μA max. (at 5.5 V, 25°C)

 $t_{\rm PD}$ = 3.8 ns (at 5 V) V_{NIH} = V_{NIL} = 28% V_{CC} min.

Features

- Wide power supply range:
- Low current consumption:
- Typical propagation delay:
- High noise immunity:
- Power down protection:
- Lead-free

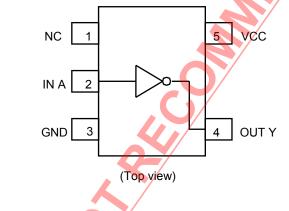
Applications

- Personal computers, peripherals
- Cellular phones
- Cameras
- Games

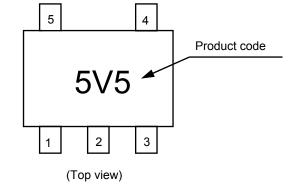
Package

• SC-88A





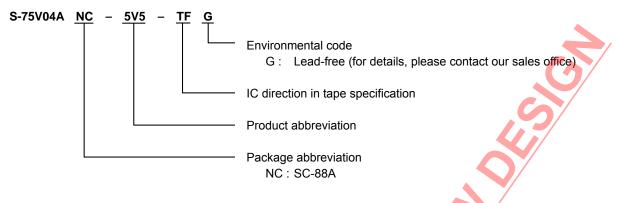
Marking Specification



Logic Diagram

\mathbf{A}		
IN A —	$\sqrt{2}$	OUT Y

True values					
А	Y				
L	Н				
Н	L				



Absolute Maximum Ratings

		(Ta = 25°C unless other	wise specified
Item	Symbol	Absolute Maximum Ratings	Unit
Power supply voltage	V _{CC}	-0,5 to +7.0	V
Input voltage	V _{IN}	-0.5 to +7.0	V
Output voltage	V _{OUT}	-0.5 to V _{CC} + 0.5	V
Input parasitic diode current	I _{IK}	-20	mA
Output parasitic diode current	Ι _{ΟΚ}	±20	mA
Output current	I _{OUT}	±25	mA
V _{CC} /GND current	I _{cc}	±50	mA
Dewer disaination		200 (When not mounted on board)	mW
Power dissipation	P _D	350 ^{*1}	mW
Operating ambient temperature	T _{opr}	-40 to +85	°C
Storage temperature	Tstg	-65 to +150	°C
Lead temperature (10 s)	TL	260	°C

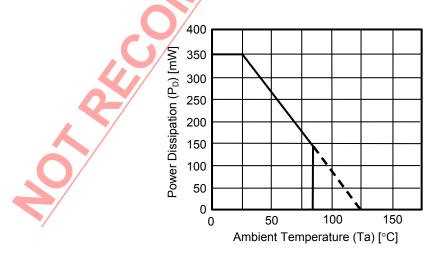
*1. When mounted on board

[Mounted board]

(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm

(2) Board name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.



Power Dissipation of Package (When Mounted on Board)

Recommended Operating Conditions

Item	Symbol	Standard	Unit
Power voltage	V _{cc}	2 to 5.5	V
Input voltage	V _{IN}	0 to 5.5	V
Output voltage	V _{OUT}	0 to V _{CC}	V
length rises / fell times		0 to 100 (V _{CC} = 3.3±0.3 V)	ns
Input rise / fall time	t _R , t _F	0 to 20 (V _{CC} = 5±0.5 V)	ns

DC Electrical Characteristics

	Conditions						Ta = 25°C			a = -40 to 85°C		
Iter	n	Symbol				Min.	Тур. 💧	Max.	Min.	Max.	Unit	
	"I I" Joy of	V			2.0	1.5	_		1.5		V	
Input	"H" level	VIH			3 to 5.5	V _{CC} ×0.7			V _{CC} ×0.7		V	
voltage	"L" level	V			2.0			0.5		0.5	V	
	L level	V _{IL}			3 to 5.5			V _{CC} ×0.3		$V_{CC} \times 0.3$	V	
			$V_{IN} = V_{IL}$		2.0	1.9 ┥	2.0		1.9		V	
				I _{OH} = -50 μA	3.0	2.9	3.0		2.9		V	
	"H" level	V _{OH}			4.5	4.4	4.5		4.4		V	
						I _{OH} = –4 mA	3.0	2.58			2.48	
Output				I _{OH} = -8 mA	4.5	3.94			3.80		V	
voltage					2.0		0	0.1		0.1	V	
				I _{OL} = 50 μA	3.0		0	0.1		0.1	V	
	"L" level	V _{OL}	$V_{IN} = V_{IH}$		4.5	—	0	0.1		0.1	V	
				I _{OL} = 4 mA	3.0	_		0.36		0.44	V	
				I _{OL} = 8 mA	4.5			0.36		0.44	V	
Input curren	nt	I _{IN}	V _{IN} = 5.5 V	$V_{IN} = 5.5 V \text{ or GND}$				±0.1		±1.0	μA	
Current con	sumption	I _{CC}	$V_{IN} = V_{CC} o$	r GND	5.5			1.0		10.0	μA	

 $\frac{|\mathbf{u}_{i}|^{2}}{|\mathbf{u}_{i}|^{2} \otimes \mathbf{mA}} (\mathbf{u}_{i}) = \frac{1}{|\mathbf{u}_{i}|^{2} \otimes \mathbf{mA}} (\mathbf{u}_{i}) = \frac{1}{|\mathbf{u}_{i}|$

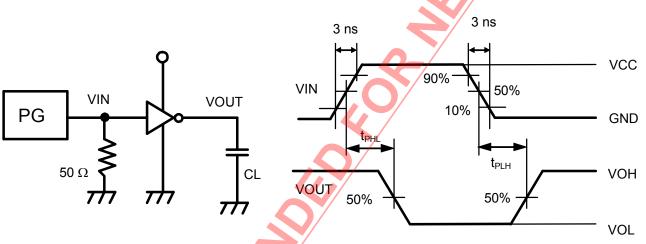
AC Electrical Characteristics

(Input $t_R = t_F = 3$ ns unless otherwise specified)										
lt a va	Symbol	Measu	rement Co	onditions		Ta = 25°C		Ta = -40	to 85°C	Linit
Item	Symbol		V _{CC} (V)	C _L (pF)	Min.	Тур.	Max.	Min.	Max.	Unit
	t _{PLH} , t _{PHL}		3.3±0.3	15		5.0	7.1	1.0	8.5	ns
			5.5±0.5	50		9.6	13.5	1.0	14.5	ns
Propagation delay time			5.0±0.5	15	_	3.8	5.5	1.0	6.5	ns
			5.0±0.5	50		5.7	8.0	1.0	9.0	ns
Input capacitance	CIN					4	10		10	pF
Equivalent internal capacitance	C _{PD} ^{*1}					13		_		pF

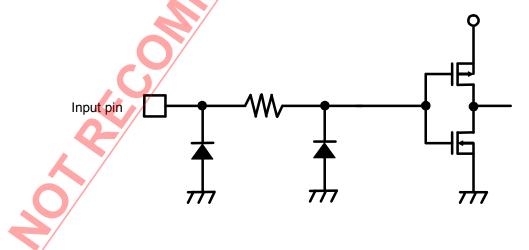
*1. C_{PD} is the no-load equivalent capacitance inside the circuitry. Refer to the measurement circuit shown below. Current consumption is averaged by the following equation.

 $I_{\text{CC(opr)}} = C_{\text{PD}} \times V_{\text{CC}} \times \text{fin} + I_{\text{CC}}$

Measurement Circuit



Remark No-load output during measurement of current consumption.





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S-75VU04ANC

MINI LOGIC SERIES INVERTER (unbuffer)

Rev.4.0_01

The S-75VU04ANC is a inverter fabricated by utilizing advanced silicon-gate CMOS technology which provides the inherent benefit of CMOS low power consumption to achieve ultra high speed operation correspond to LSTTLIC's. The special purpose unbuffered circuit design is suitable for a wide variety of linear circuits.

Input voltage is allowed to be applied even if power voltage is not supplied because no diode is inserted between an input pin and V_{CC} .

This allows for interfaces between power supplies of different voltage, output level conversion from 5 V to 3 V and battery backup applications.

2 V to 5.5 V

All pins

1.0 μA max. (at 5.5 V, 25°C)

 $\label{eq:tpd} \begin{array}{l} t_{\text{PD}} = 3.5 \text{ ns (at 5 V)} \\ V_{\text{NIH}} = V_{\text{NIL}} = 10\% \ V_{\text{CC}} \text{ min.} \end{array}$

Features

- Wide power supply range:
- Low current consumption:
- Typical propagation delay:
- High noise immunity:
- Power down protection:
- Fower down protect
- Lead-free

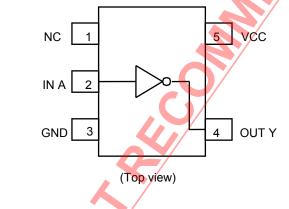
Applications

- Personal computers, peripherals
- Cellular phones
- Cameras
- Games

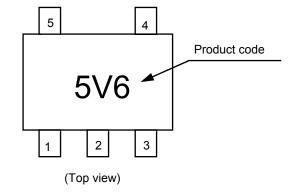
Package

• SC-88A





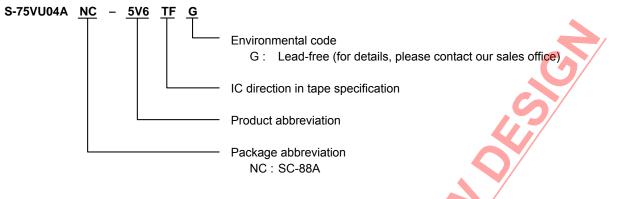
Marking Specification



Logic Diagram

\rightarrow —	OUT Y

True values						
Y						
Н						
L						



Absolute Maximum Ratings

		(Ta = 25°C unless other	wise specified
Item	Symbol	Absolute Maximum Ratings	Unit
Power supply voltage	V _{CC}	-0,5 to +7.0	V
Input voltage	V _{IN}	-0.5 to +7.0	V
Output voltage	V _{OUT}	-0.5 to V _{CC} + 0.5	V
Input parasitic diode current	I _{IK}	-20	mA
Output parasitic diode current	Ι _{οκ}	±20	mA
Output current	I _{OUT}	±25	mA
V _{CC} /GND current	I _{CC}	±50	mA
Dewer dissinction		200 (When not mounted on board)	mW
Power dissipation	PD	350 ^{*1}	mW
Operating ambient temperature	T _{opr}	_40 to +85	°C
Storage temperature	T _{stg}	-65 to +150	°C
Lead temperature (10 s)	TL	260	°C

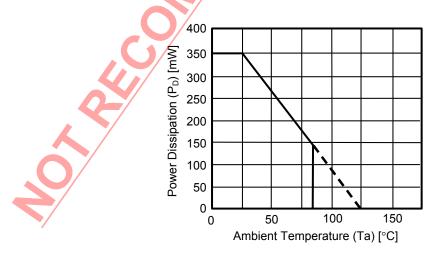
*1. When mounted on board

[Mounted board]

(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm

(2) Board name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.



Power Dissipation of Package (When Mounted on Board)

Rev.4.0_01

Recommended Operating Conditions

Item	Symbol	Standard	Unit
Power voltage	V _{CC}	2 to 5.5	V
Input voltage	V _{IN}	0 to 5.5	V
Output voltage	V _{OUT}	0 to V_{CC}	V

DC Electrical Characteristics

		r	1								
Iter	~	Symbol		Conditions		Conditions Ta = 25°C			Ta = -40) to 85°C	Unit
iter	Π	Symbol				Min.	Тур.	Max.	Min.	Max.	Unit
	"I I" Iovial	V	V _V		2.0	1.7	_		1.7		V
Input	"H" level	VIH	$V_{OUT} = V_{OL}$		3 to 5.5	$V_{CC} \times 0.8$		—	V _{CC} ×0.8		V
voltage	"I" lovel	V	V _V		2.0		4	0.3		0.3	V
	"L" level	V _{IL}	$V_{OUT} = V_{OH}$		3 to 5.5			V _{CC} ×0.2		$V_{CC} \times 0.2$	V
					2.0	1.8	2.0	_	1.8		V
			н	I _{OH} = –50 μA	3.0	2.7 👅	3.0		2.7		V
	"H" level	V _{OH}			4.5	4.0	4.5		4.0		V
				I _{OH} = –4 mA	3.0	2.58			2.48		V
Output			V _{IN} = GND	I _{OH} = –8 mA	4.5	3.94	_		3.80		V
voltage					2.0		0	0.2		0.2	V
			$V_{IN} = V_{IH}$	I _{OL} = 50 μA	3.0		0	0.3		0.3	V
	"L" level	V _{OL}			4.5		0	0.5		0.5	V
			V - V	I _{OL} = 4 mA	3.0	/_		0.36		0.44	V
			$V_{IN} = V_{CC}$	I _{OL} = 8 mA	4.5			0.36		0.44	V
Input curren	nt	I _{IN}	V _{IN} = 5.5 V	V _{IN} = 5.5 V or GND				±0.1		±1.0	μA
Current con	sumption	I _{CC}	$V_{IN} = V_{CC} o$	r GND	5.5			1.0		10.0	μA

 $\frac{10L}{|l_{0L}|^{2} 8 mA}}{\frac{1}{|l_{0L}|^{2} 8 mA}}$

MINI LOGIC SERIES INVERTER (unbuffer) S-75VU04ANC

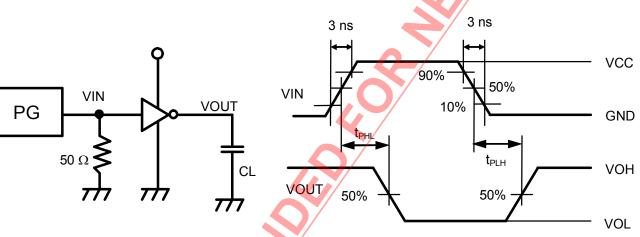
■ AC Electrical Characteristics

(Input $t_R = t_F = 3$ ns unless otherwise specified)										
Item	Symbol	Measur	ement Co	onditions		Ta = 25°C		Ta = -40	to 85°C	Linit
	Symbol		V _{CC} (V)	C _L (pF)	Min.	Тур.	Max.	Min.	Max.	Unit
			3.3±0.3	15		5.0	8.9	1.0	10.5	ns
Dranagation dology time	t _{PLH} , t _{PHL}	_	5.5±0.5	50		8.9	12.5	1.0	13.5	ns
Propagation delay time			5.0±0.5	15		3.5	5.5	1.0	6.5	ns
			5.0±0.5	50		5.4	7.5	1.0	8.0	ns
Input capacitance	CIN					5	10		10	pF
Equivalent internal capacitance	C _{PD} ^{*1}					6				pF

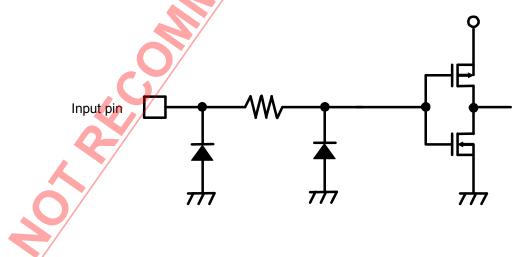
*1. C_{PD} is the no-load equivalent capacitance inside the circuitry. Refer to the measurement circuit shown below. Current consumption is averaged by the following equation.

 $I_{CC(opr)} = C_{PD} \times V_{CC} \times fin + I_{CC}$

Measurement Circuit



Remark No-load output during measurement of current consumption.





S-75V08ANC

MINI LOGIC SERIES 2 INPUT AND GATE

Rev.4.0_01

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The S-75V08ANC is a Single 2-Input AND Gate fabricated by utilizing advanced silicon-gate CMOS technology which provides the inherent benefit of CMOS low power consumption to achieve ultra high speed operation correspond to LSTTL IC's.

All gates of the internal circuitry have buffered outputs to ensure high noise immunity and output stability,

1.0 μA max. (at 5.5 V, 25°C)

 t_{PD} = 4.3 ns (at 5 V) V_{NIH} = V_{NIL} = 28% V_{CC} min.

2 V to 5.5 V

All pins

Input voltage is allowed to be applied even if power voltage is not supplied because no diode is inserted between an input pin and V_{CC} .

This allows for interfaces between power supplies of different voltage, output level conversion from 5 V to 3 V and battery backup applications.

Features

- Wide power supply range:
- Low current consumption:
- Typical propagation delay:
- High noise immunity:
- Power down protection:
- Lead-free

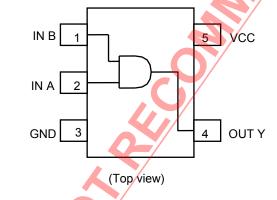
Applications

- Personal computers, peripherals
- Cellular phones
- Cameras
- Games

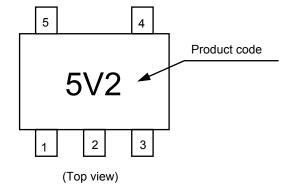
Package

• SC-88A

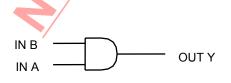
Pin Configuration



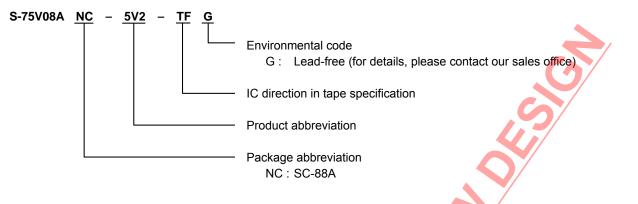
Marking Specification



Logic Diagram



True values		
А	В	Y
L	L	L
L	Н	L
Н	L	L
Н	Н	Н



Absolute Maximum Ratings

		(Ta = 25°C unless other	wise specified
Item	Symbol	Absolute Maximum Ratings	Unit
Power supply voltage	V _{CC}	-0,5 to +7.0	V
Input voltage	V _{IN}	-0.5 to +7.0	V
Output voltage	V _{OUT}	-0.5 to V _{CC} + 0.5	V
Input parasitic diode current	I _{IK}	-20	mA
Output parasitic diode current	Ι _{ΟΚ}	±20	mA
Output current	I _{OUT}	±25	mA
V _{CC} /GND current	I _{CC}	±50	mA
Deuver disaination		200 (When not mounted on board)	mW
Power dissipation	PD	350 ^{*1}	mW
Operating ambient temperature	T _{opr}	-40 to +85	°C
Storage temperature	T _{stq}	–65 to +150	°C
Lead temperature (10 s)	TL	260	°C

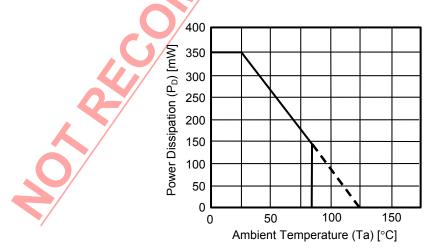
*1. When mounted on board

[Mounted board]

(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm

(2) Board name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.



Power Dissipation of Package (When Mounted on Board)

Recommended Operating Conditions

Item	Symbol	Standard	Unit
Power voltage	V _{CC}	2 to 5.5	V
Input voltage	V _{IN}	0 to 5.5	V
Output voltage	V _{OUT}	0 to V _{CC}	V
Innut view / fell times		0 to 100 (V _{CC} = 3.3±0.3 V)	ns
Input rise / fall time	t _R , t _F	0 to 20 (V _{CC} = 5±0.5 V)	ns

DC Electrical Characteristics

				Conditions			Ta = 25°C		Ta = –40 to 85°C		
Iter	n	Symbol			V _{CC}	Min.	Тур. 🎸	Max.	Min.	Max.	Unit
	"H" level	V				1.5	_		1.5		V
Input	п ievei	VIH				$V_{CC} \times 0.7$			V _{CC} ×0.7		V
voltage	"L" level	V			2.0			0.5		0.5	V
	L level	V _{IL}			3 to 5.5			V _{CC} ×0.3		$V_{CC} \times 0.3$	V
					2.0	1.9 ┥	2.0		1.9		V
"H" level			I_{OH} = $-50 \ \mu A$	3.0	2.9	3.0		2.9		V	
	"H" level	V _{OH}	V _{IN} = V _{IH}		4.5	4.4	4.5		4.4		V
				I _{OH} = -4 mA	3.0	2.58	_		2.48		V
Output				I _{OH} = –8 mA	4.5	3.94	_		3.80		V
voltage				I _{OL} = 50 μA	2.0		0	0.1		0.1	V
			V -V		3.0		0	0.1		0.1	V
	"L" level	V _{OL}	$V_{IN} = V_{IH}$		4.5	/ _	0	0.1		0.1	V
			or V _{IL}	I _{OL} = 4 mA	3.0	_	_	0.36		0.44	V
				I _{OL} = 8 mA	4.5			0.36		0.44	V
Input curren	it	I _{IN}	V _{IN} = 5.5 V	$V_{IN} = 5.5 V \text{ or GND}$		—		±0.1	—	±1.0	μA
Current con	sumption	I _{CC}	$V_{IN} = V_{CC} o$	r GND	5.5			1.0		10.0	μA

 $\frac{|\mathbf{u}_{i}|^{2}}{|\mathbf{u}_{i}|^{2}} = 8 \text{ mA}}{|\mathbf{u}_{i}|^{2}} = 8 \text{ mA}}$

unless otherwise energified)

■ AC Electrical Characteristics

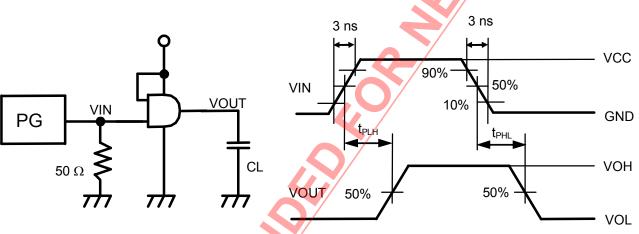
	(Input $t_R = t_F = 3$ ns unless otherwise specified)											
Item	Symbol	Measurement Conditio		onditions		Ta = 25°C		Ta = -40	Linit			
nem	Symbol		V _{CC} (V)	C _L (pF)	Min.	Тур.	Max.	Min.	Max.	Unit		
Deservation dalar time	t _{PLH} , t _{PHL}		3.3±0.3	15		6.2	8.8	1.0	10.5	ns		
		_	3.3±0.3	50		9.6	13.5	1.0	14.5	ns		
Propagation delay time			5.0±0.5	15		4.3	5.9	1.0	7.0	ns		
				50		5.7	7.9	1.0	9.0	ns		
Input capacitance	CIN				4	10		10	pF			
Equivalent internal capacitance	C _{PD} ^{*1}					14		_		pF		

.....

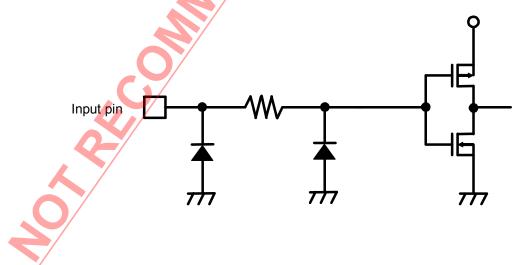
*1. C_{PD} is the no-load equivalent capacitance inside the circuitry. Refer to the measurement circuit shown below. Current consumption is averaged by the following equation.

 $I_{CC(opr)} = C_{PD} \times V_{CC} \times fin + I_{CC}$

Measurement Circuit



Remark No-load output during measurement of current consumption.





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S-75V14ANC

MINI LOGIC SERIES SCHMITT INVERTER

Rev.4.0_01

The S-75V14ANC is a SCHMITT INVERTER fabricated by utilizing advanced silicon-gate CMOS technology which provides the inherent benefit of CMOS low power consumption to achieve ultra high speed operation correspond to LSTTL IC's. All gates of the internal circuitry have buffered outputs to ensure high noise immunity and output stability. Input voltage is allowed to be applied even if power voltage is not supplied because no diode is inserted between an input pin and V_{CC} .

This allows for interfaces between power supplies of different voltage, output level conversion from 5 V to 3 V and battery backup applications.

2 V to 5.5 V

All pins

1.0 μA max. (at 5.5 V, 25°C)

 $t_{\rm PD}$ = 5.5 ns (at 5 V) V_{NIH} = V_{NIL} = 28% V_{CC} min.

Features

- Wide power supply range:
- Low current consumption:
- Typical propagation delay:
- High noise immunity:
- Power down protection:
- Lead-free

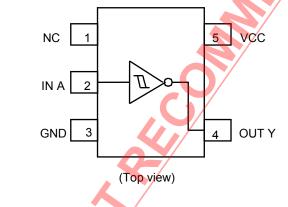
Applications

- Personal computers, peripherals
- Cellular phones
- Cameras
- Games

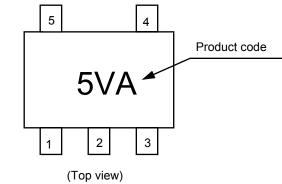
Package

• SC-88A

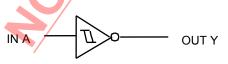
Pin Configuration

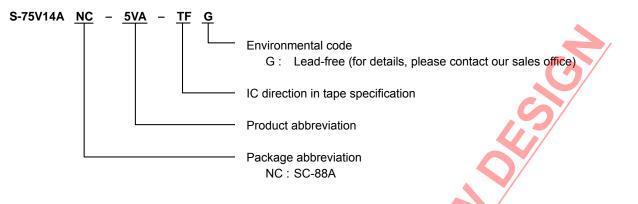


Marking Specification



Logic Diagram





Absolute Maximum Ratings

		(Ta ≠ 25°C unless otherwise specified				
Item	Symbol	Absolute Maximum Ratings	Unit			
Power supply voltage	V _{CC}	-0.5 to +7.0	V			
Input voltage	V _{IN}	-0.5 to +7.0	V			
Output voltage	V _{OUT}	-0.5 to V _{CC} + 0.5	V			
Input parasitic diode current	I _{IK}	-20	mA			
Output parasitic diode current	Ι _{ΟΚ}	±20	mA			
Output current	I _{OUT}	±25	mA			
V _{CC} /GND current	I _{CC}	±50	mA			
Device discipation		200 (When not mounted on board)	mW			
Power dissipation	PD	350*1	mW			
Operating ambient temperature	T _{opr}	-40 to +85	°C			
Storage temperature	T _{stg}	-65 to +150	°C			
Lead temperature (10 s)	T	260	°C			

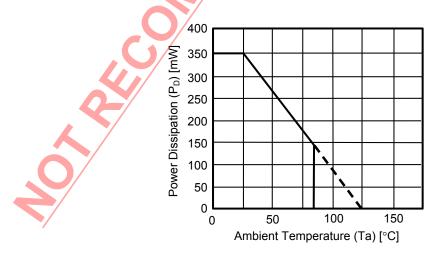
*1. When mounted on board

[Mounted board]

(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm

(2) Board name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.



Power Dissipation of Package (When Mounted on Board)

Rev.4.0_01

Recommended Operating Conditions

Item	Symbol	Standard	Unit
Power voltage	V _{CC}	2 to 5.5	V
Input voltage	V _{IN}	0 to 5.5	V
Output voltage	V _{OUT}	0 to V_{CC}	V

DC Electrical Characteristics

											1
Iter	n	Symbol		Conditions			Ta = 25°C		Ta ≠ -40) to 85°C	Unit
iter	11	Symbol			V _{CC}	Min.	Тур.	Max.	Min.	Max.	Unit
					3.0	_		2.20		2.20	V
	"H" level	VP			4.5	_	—	3.15		3.15	V
Threshold					5.5		_	3.85		3.85	V
voltage					3.0	0.90			0.90	—	V
	"L" level	V _N			4.5	1.35	H	/	1.35		V
				5.5	1.65			1.65		V	
				3.0	0.30		1.20	0.30	1.20	V	
Hysteresis v	/oltage	V _H			4.5	0.40		1.40	0.40	1.40	V
					5.5	0.5	/_	1.60	0.5	1.60	V
				I _{OH} = –50 μA	2.0	1.9	2.0		1.9	—	V
					3.0	2.9	3.0		2.9	—	V
	"H" level	V _{OH}	$V_{IN} = V_{IL}$		4.5	4,4	4.5	_	4.4	—	V
				I _{OH} = -4 mA	3.0	2.58	—	_	2.48	—	V
Output				I _{OH} = -8 mA	4.5	3.94	—	_	3.80	—	V
voltage					2.0		0	0.1	—	0.1	V
				I _{OL} = 50 μA	3.0	_	0	0.1	—	0.1	V
	"L" level	V _{OL}	$V_{IN} = V_{IH}$		4.5	_	0	0.1	—	0.1	V
				I _{OL} = 4 mA	3.0	_	—	0.36	—	0.44	V
			I _{OL} = 8 mA	4.5	_	—	0.36	—	0.44	V	
Input currer	nt	I _{IN}	V _{IN} = 5.5 V	or GND	0 to 5.5	—	—	±0.1	—	±1.0	μA
Current con	sumption	I _{cc}	$V_{IN} = V_{CC} o$	r GND	5.5			1.0		10.0	μA

 V_{lh}

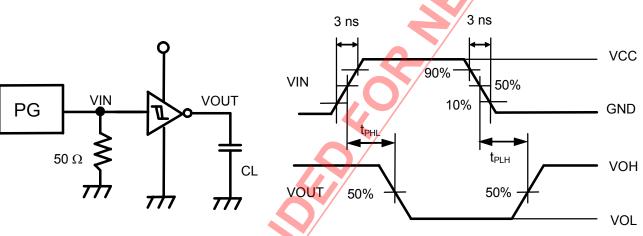
■ AC Electrical Characteristics

	(Input $t_R = t_F = 3$ ns unless otherwise specified)											
Itom	Symbol	Measur	Measurement Conditions		Ta = 25°C			Ta = -40	Linit			
Item			V _{CC} (V)	C _L (pF)	Min.	Тур.	Max.	Min.	Max.	Unit		
Dranasation dalay time	t _{PLH} , t _{PHL}		3.3±0.3	15		8.3	12.8	1.0	15.0	ns		
		—	3.3±0.3	50		10.8	16.3	1.0	18.5	ns		
Propagation delay time			5.0±0.5	15		5.5	8.6	1.0	10.0	ns		
				50		7.0	10.6	1.0	12.0	ns		
Input capacitance	C _{IN}	_				4	10	7	10	pF		
Equivalent internal capacitance	C _{PD} ^{*1}				_	14		_		pF		

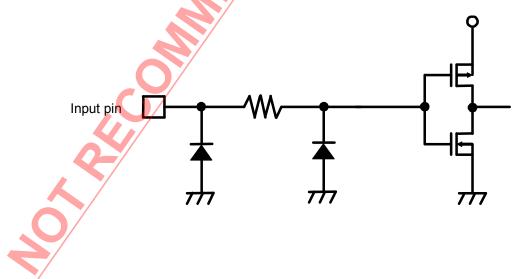
*1. C_{PD} is the no-load equivalent capacitance inside the circuitry. Refer to the measurement circuit shown below. Current consumption is averaged by the following equation.

 $I_{CC(opr)} = C_{PD} \times V_{CC} \times fin + I_{CC}$

Measurement Circuit



Remark No-load output during measurement of current consumption.





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S-75V32ANC

MINI LOGIC SERIES 2 INPUT OR GATE

Rev.4.0_01

The S-75V32ANC is a single 2-input OR gate fabricated by utilizing advanced silicon-gate CMOS technology which provides the inherent benefit of CMOS low power consumption to achieve ultra high speed operation correspond to LSTTL IC's. All gates of the internal circuitry have buffered outputs to ensure high noise immunity and output stability. Input voltage is allowed to be applied even if power voltage is not supplied because no diode is inserted between an input pin and V_{CC} .

This allows for interfaces between power supplies of different voltage, output level conversion from 5 V to 3 V and battery backup applications.

2 V to 5.5 V

All pins

1.0 µA max. (at 5.5 V, 25°C)

 $t_{\rm PD}$ = 3.8 ns (at 5 V) V_{NIH} = V_{NIL} = 28% V_{CC} min.

Features

- Wide power supply range:
- Low current consumption:
- Typical propagation delay:
- High noise immunity:
- Power down protection:
- Lead-free

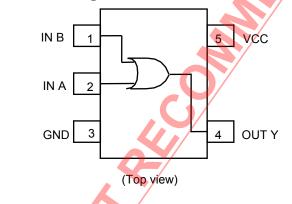
Applications

- Personal computers, peripherals
- Cellular phones
- Cameras
- Games

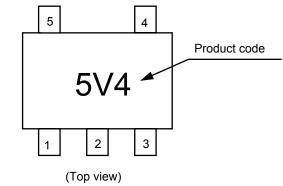
Package

• SC-88A

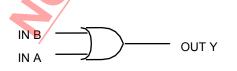
Pin Configuration



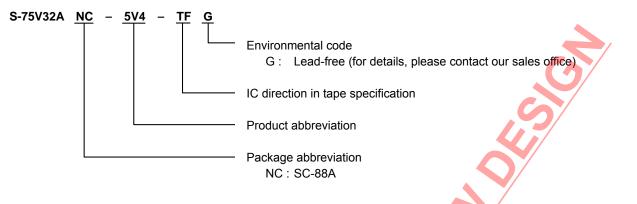
Marking Specification



Logic Diagram



I rue values		
А	В	Y
L	L	L
L	Н	Н
Н	L	Н
Н	Н	Н



Absolute Maximum Ratings

		(Ta ≠ 25°C unless otherwise specified				
Item	Symbol	Absolute Maximum Ratings	Unit			
Power supply voltage	V _{CC}	-0.5 to +7.0	V			
Input voltage	V _{IN}	-0.5 to +7.0	V			
Output voltage	V _{OUT}	0.5 to V _{CC} + 0.5	V			
Input parasitic diode current	I _{IK}	-20	mA			
Output parasitic diode current	Ι _{ΟΚ}	±20	mA			
Output current	I _{OUT}	±25	mA			
V _{CC} /GND current	I _{CC}	±50	mA			
Device discipation		200 (When not mounted on board)	mW			
Power dissipation	PD	$ \begin{array}{c} -0.5 \text{ to } +7.0 \\ -0.5 \text{ to } +7.0 \\ -0.5 \text{ to } V_{CC} + 0.5 \\ -20 \\ \pm 20 \\ \pm 25 \\ \pm 50 \\ \end{array} $	mW			
Operating ambient temperature	T _{opr}	-40 to +85	°C			
Storage temperature	T _{stg}	-65 to +150	°C			
Lead temperature (10 s)	TL	260	°C			

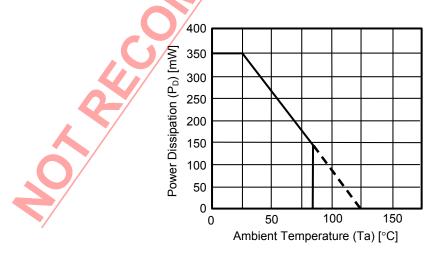
*1. When mounted on board

[Mounted board]

(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm

(2) Board name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.



Power Dissipation of Package (When Mounted on Board)

Recommended Operating Conditions

Item	Symbol	Standard	Unit
Power voltage	V _{CC}	2 to 5.5	V
Input voltage	V _{IN}	0 to 5.5	V
Output voltage	V _{OUT}	0 to V _{CC}	V
lanut rice / fell time		0 to 100 (V _{CC} = 3.3±0.3 V)	ns
Input rise / fall time	t _R , t _F	0 to 20 (V _{CC} = 5±0.5 V)	ns

DC Electrical Characteristics

				Conditions			Ta = 25°C		Ta = –40) to 85°C	
Iter	n	Symbol			V _{CC}	Min.	Тур.	Max.	Min.	Max.	Unit
	"H" level	V				1.5	_		1.5		V
Input	п ievei	VIH				$V_{CC} \times 0.7$			V _{CC} ×0.7		V
voltage	"L" level	V			2.0			0.5		0.5	V
	Lievei	V _{IL}			3 to 5.5			V _{CC} ×0.3		$V_{CC} \times 0.3$	V
"Н" level V _{он}			I _{OH} = -50 μA	2.0	1.9 ┥	2.0		1.9		V	
				3.0	2.9	3.0		2.9		V	
	"H" level	V _{OH}	OH V _{IN} = V _{IL} or V _{IH}		4.5	4.4	4.5		4.4		V
				I _{OH} = -4 mA	3.0	2.58	_		2.48		V
Output				I _{OH} = –8 mA	4.5	3.94	_		3.80		V
voltage					2.0		0	0.1		0.1	V
				I _{OL} = 50 μA	3.0		0	0.1		0.1	V
	"L" level	V _{OL}	$V_{IN} = V_{IL}$		4.5	/ _	0	0.1		0.1	V
				I _{OL} = 4 mA	3.0	_	_	0.36		0.44	V
				I _{OL} = 8 mA	4.5			0.36		0.44	V
Input curren	it	I _{IN}	V _{IN} = 5.5 V	V _{IN} = 5.5 V or GND				±0.1		±1.0	μA
Current con	sumption	I _{CC}	$V_{IN} = V_{CC} o$	r GND	5.5			1.0		10.0	μA

 $\frac{|\mathbf{u}_{i}|^{2} + \mathbf{u}_{i}|^{2}}{|\mathbf{u}_{i}|^{2} + \mathbf{u}_{i}|^{2}} + \frac{|\mathbf{u}_{i}|^{2} + \mathbf{u}_{i}|^{2}}{|\mathbf{u}_{i}|^{2} + |\mathbf{u}_{i}|^{2}} + \frac{|\mathbf{u}_{i}|^{2} + |\mathbf{u}_{i}|^{2}}{|\mathbf{u}_{i}|^{2} + |\mathbf{u}_{i}|^{2} + |\mathbf$

unless otherwise energified)

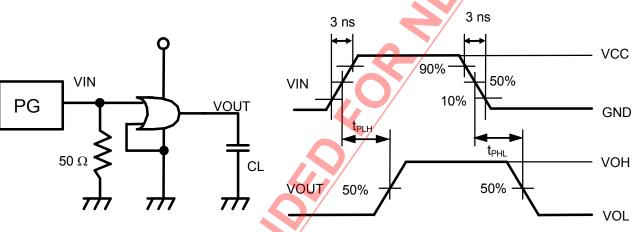
■ AC Electrical Characteristics

(input $t_R = t_F = 3$ ns unless otherwise specified										cifiea)
Item	Symbol	Measurement Conditions		Ta = 25°C			Ta = -40 to 85°C		L lunit	
			V _{CC} (V)	C _L (pF)	Min.	Тур.	Max.	Min.	Max.	Unit
Propagation delay time			3.3±0.3	15	_	5.5	7.9	1.0	9.5	ns
	t _{PLH} , t _{PHL}	_		50		10.0	14.0	1.0	15.0	ns
			5.0±0.5	15		3.8	5.5	1.0	6.5	ns
				50		6.1	8.5	1.0	9.0	ns
Input capacitance	CIN	_				4	10	7	10	pF
Equivalent internal capacitance	C _{PD} ^{*1}	—				15		_		pF

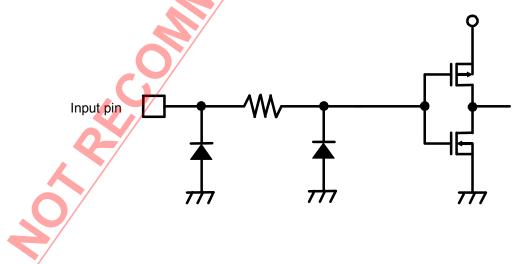
*1. C_{PD} is the no-load equivalent capacitance inside the circuitry. Refer to the measurement circuit shown below. Current consumption is averaged by the following equation.

 $I_{CC(opr)} = C_{PD} \times V_{CC} \times fin + I_{CC}$

Measurement Circuit



Remark No-load output during measurement of current consumption.





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The S-75V86ANC is a EXCLUSIVE OR GATE fabricated by utilizing advanced silicon-gate CMOS technology which provides the inherent benefit of CMOS low power consumption to achieve ultra high speed operation correspond to LSTTL IC's.

All gates of the internal circuitry have buffered outputs to ensure high noise immunity and output stability.

Input voltage is allowed to be applied even if power voltage is not supplied because no diode is inserted between an input pin and V_{CC} .

This allows for interfaces between power supplies of different voltage, output level conversion from 5 V to 3 V and battery backup applications.

Features

- Wide power supply range:
- Low current consumption:
- Typical propagation delay:
- High noise immunity:
- Power down protection:
- Lead-free

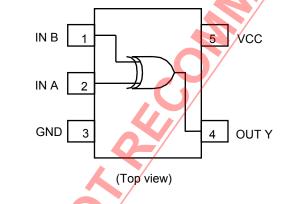
Applications

- Personal computers, peripherals
- Cellular phones
- Cameras
- Games

Package

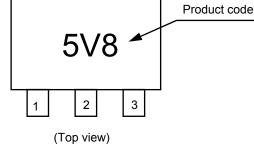
• SC-88A

Pin Configuration



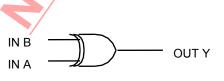
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Marking Specification



4

Logic Diagram



True values		
А	В	Y
L	L	L
L	Н	Н
Н	L	Н
Н	Н	L

2 V to 5.5 V

- 1.0 μA max. (at 5.5 V, 25°C)
- t_{PD} = 4.8 ns (at 5 V) V_{NIH} = V_{NIL} = 28% V_{CC} min.

All pins

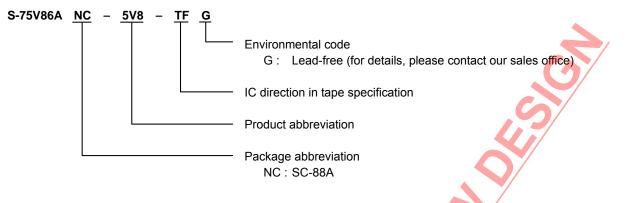
H

S-75V86ANC

MINI LOGIC SERIES EXCLUSIVE OR GATE

29

Rev.4.0_01



Absolute Maximum Ratings

		(Ta ≠ 25°C unless other	wise specified
Item	Symbol	Absolute Maximum Ratings	Unit
Power supply voltage	V _{CC}	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 to +7.0	V
Output voltage	V _{OUT}	0.5 to V _{CC} + 0.5	V
Input parasitic diode current	I _{IK}	-20	mA
Output parasitic diode current	Ι _{ΟΚ}	±20	mA
Output current	I _{OUT}	±25	mA
V _{CC} /GND current	I _{CC}	±50	mA
Deuron disaination		200 (When not mounted on board)	mW
Power dissipation	PD	350 ^{*1}	mW
Operating ambient temperature	T _{opr}	-40 to +85	°C
Storage temperature	T _{stg}	-65 to +150	°C
Lead temperature (10 s)	TL	260	°C

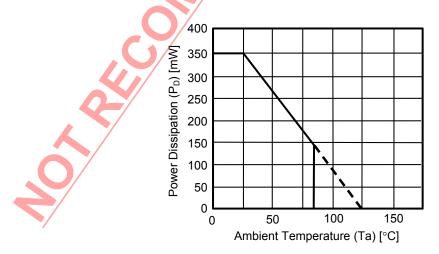
*1. When mounted on board

[Mounted board]

(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm

(2) Board name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.



Power Dissipation of Package (When Mounted on Board)

Recommended Operating Conditions

Item	Symbol	Standard	Unit
Power voltage	V _{CC}	2 to 5.5	V _
Input voltage	V _{IN}	0 to 5.5	V
Output voltage	V _{OUT}	0 to V _{CC}	V
length rises (fell times		0 to 100 (V _{CC} = 3.3±0.3 V)	ns
Input rise / fall time	t _R , t _F	0 to 20 (V _{CC} = 5±0.5 V)	ns

DC Electrical Characteristics

Item		Conditions			Ta = 25°C			Ta = -40 to 85°C			
		Symbol		V _{cc}			Тур.	Max.	Min.	Max.	Unit
	"H" loval	V				1.5	_		1.5		V
Input "H" level		VIH			3 to 5.5	$V_{CC} \times 0.7$			V _{CC} ×0.7		V
voltage	"I " lovol	V			2.0			0.5		0.5	V
"L" level	Lievei	V _{IL}			3 to 5.5			V _{CC} ×0.3		$V_{CC} \times 0.3$	V
"H" level			V _{IN} = V _{IL} or V _{IH}	I _{OH} = -50 μA I _{OH} = -4 mA	2.0	1.9 ┥	2.0		1.9		V
					3.0	2.9	3.0		2.9		V
	"H" level	V _{OH}			4.5	4.4	4.5		4.4		V
					3.0	2.58	_		2.48		V
				I _{OH} = –8 mA	4.5	3.94	_		3.80		V
voltage				I _{OL} = 50 μA	2.0		0	0.1		0.1	V
"L" leve					3.0		0	0.1		0.1	V
	"L" level	V _{OL}	$V_{IN} = V_{IL}$		4.5	/ _	0	0.1		0.1	V
			or V _{IH}	I _{OL} = 4 mA	3.0			0.36		0.44	V
				I _{OL} = 8 mA	4.5			0.36		0.44	V
Input curren	it	I _{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—		±0.1	—	±1.0	μA
Current con	sumption	I _{CC}	$V_{IN} = V_{CC} o$	r GND	5.5			1.0		10.0	μA

 $\frac{|O_{L}|^{2}}{|O_{L}|^{2}} \otimes \frac{|O_{L}|^{2}}{|O_{L}|^{2}} \otimes \frac{|O_{L}|^{2}} \otimes \frac{|O_{L}|^{2}}{|O_{L}|^{2}} \otimes \frac{|O_{L}|^{2}}{|O_{L}|^{2}} \otimes \frac{|O_{L}|^{2}} \otimes \frac{|O_{L}|^{2$

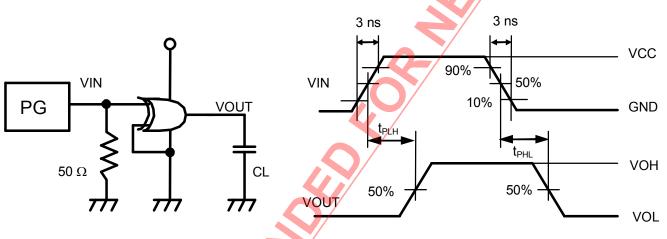
■ AC Electrical Characteristics

(Input t _R = t _F = 3 ns unless otherwise specified)										
Item	Symbol	Measurement Cond		onditions	nditions Ta = 25°C		Ta = -40		to 85°C	Linit
			V _{CC} (V)	C _L (pF)	Min.	Тур.	Max.	Min.	Max.	Unit
Propagation delay time	t _{PLH} , t _{PHL}	_	3.3±0.3	15	_	7.0	11.0	1.0	13.0	ns
				50		10.4	14.5	1.0	16.5	ns
			5.0±0.5	15		4.8	6.8	1.0	8.0	ns
				50		6.5	9.0	1.0	10.0	ns
Input capacitance	CIN	_				4	10		10	pF
Equivalent internal capacitance	C _{PD} ^{*1}	_				18		_		pF

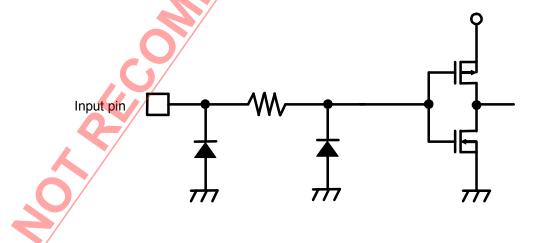
*1. C_{PD} is the no-load equivalent capacitance inside the circuitry. Refer to the measurement circuit shown below. Current consumption is averaged by the following equation.

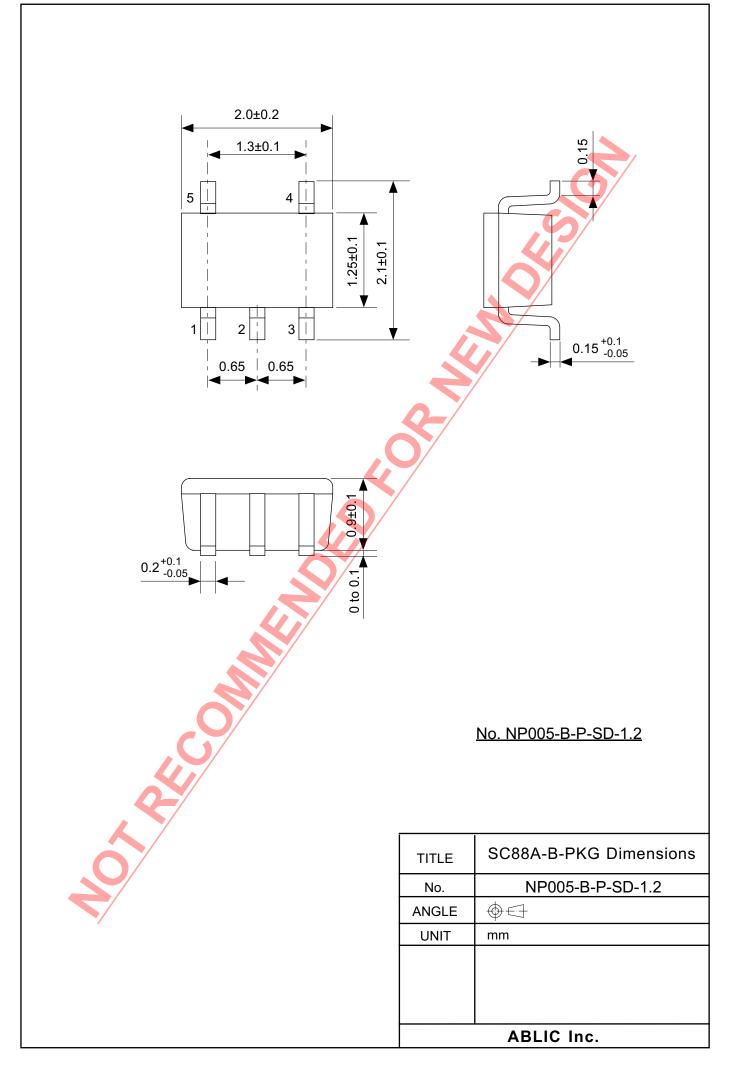
 $I_{\text{CC(opr)}} = C_{\text{PD}} \times V_{\text{CC}} \times fin + I_{\text{CC}}$

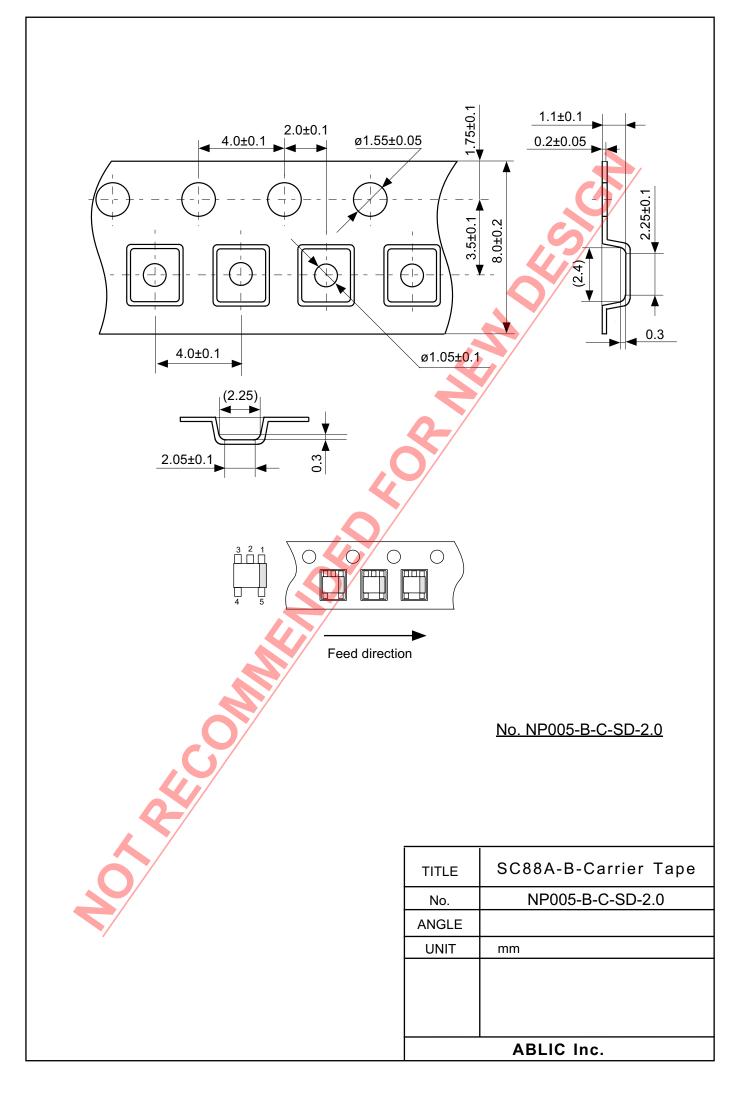
Measurement Circuit

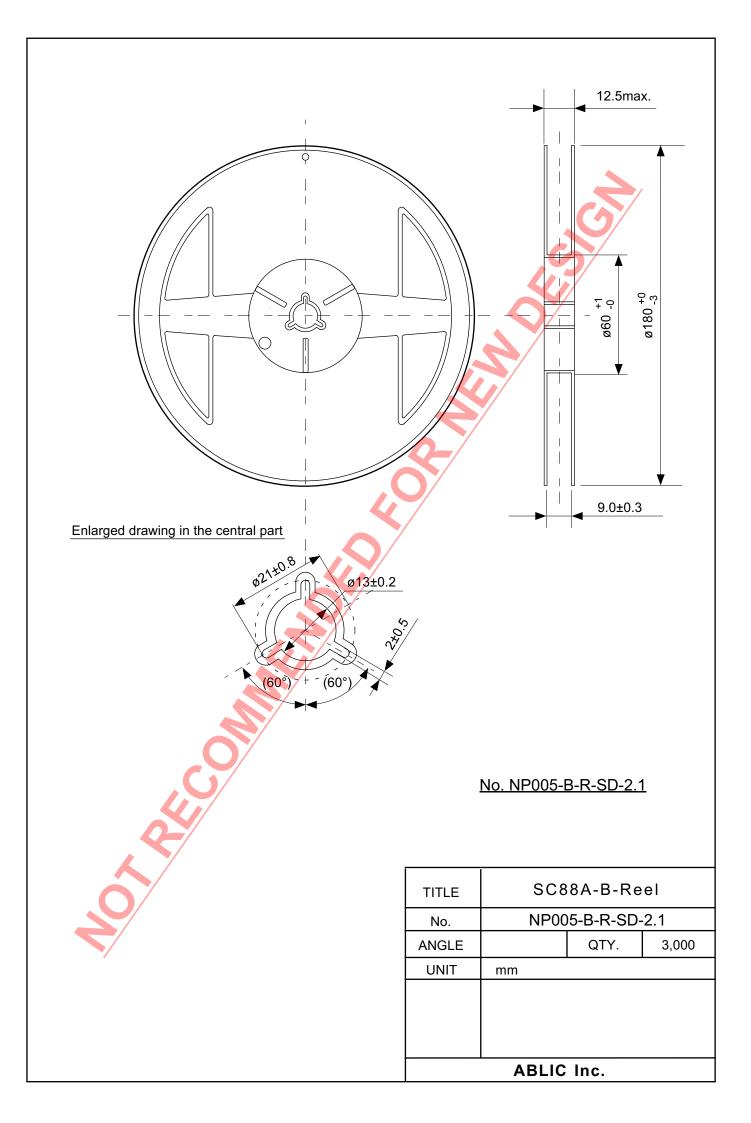


Remark No-load output during measurement of current consumption.









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