

Ultra-Low Jitter, Fixed-Frequency SMD Clock Oscillator

AK3B

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ESD Sensitive



3.2 x 2.5 x 1.0 mm

RoHS/RoHS II Compliant

MSL Level = N/A

Features

- Exceptionally Low RMS Jitter: 54fs Typ (LVDS @ 156.25MHz)
- Available in industry standard frequencies between 100MHz and 250MHz
- ± 25 ppm stability over industrial operating temperature (-40°C to +85°C)
- 1.8V, 2.5V, 3.3V, 2.375V to 3.63V Continuous supply voltage options
- LVPECL, LVDS, HCSL differential output logic
- Industry standard 3.2 x 2.5 x 1.0 mm footprint
- Based on 3rd overtone, quartz crystal technology
- Available in Abracon's global distribution network
- Output Enable (Pad 1 or Pad 2 Active High) options available

Applications

- Optical Transceivers and Modules
- Data Centers, Storage, and Servers
- Networking switches and gateways
- 100G/200G/400G/800G Ethernet
- Fibre Channel/SONET/SDH/PCIe
- Industrial and FPGA applications
- Test & measurement

Key Electrical Specifications

Parameters	Min.	Typ.	Max.	Unit	Notes
Frequency Range	100		250	MHz	Supply voltage and output logic dependent
Standard Available Frequencies	100.000, 122.880, 125.000, 148.500, 150.000, 155.520, 156.250, 200.000, 212.500, 250.000			MHz	Contact Abracon for availability of frequencies not listed
Supply Voltage (Vdd) [Note 1]	2.97	3.3	3.63	V	Option "A"
	2.375	2.5	2.625		Option "B"
	1.71	1.8	1.89		Option "C" (≤ 175 MHz only)
	2.375		3.63		Option "D"
Supply Current (Idd)	LVPECL	52	65	mA	@ 200MHz; @ Vdd=3.3V
	LVDS	25	35		@ 200MHz; @ Vdd=3.3V
	HCSL	32	40		@ 156.25MHz; @ Vdd=3.3V
Operating Temperature Range	-20		70	°C	Option "D"
	-40		85		Option "F" or "Q"
Storage Temperature	-55		150	°C	
Frequency Tolerance [Note 2]	-10	$< \pm 5$	10	ppm	
Frequency Stability over [Note 3,4] Operating Temperature Range	-15	$< \pm 10$	15	ppm	Option "D" (-20°C to +70°C)
	-20	$< \pm 15$	20		Option "Q" (-40°C to +85°C)
	-25	$< \pm 20$	25		Option "F" (-40°C to +85°C)
First Year Aging	-3		3	ppm	At 25°C
All-Inclusive Frequency Accuracy (Total Stability) [Notes 5]	-40		40	ppm	Option "D" (-20°C to +70°C)
	-45		45		Option "Q" (-40°C to +85°C)
	-50		50		Option "F" (-40°C to +85°C)
Rise (Tr) / Fall (Tf) Time [Notes 6]	LVPECL	0.15	0.4	ns	$R_L=50\Omega$ to Vdd-2.0V on outputs
	LVDS	0.15	0.3		$R_L=100\Omega$ between outputs
	HCSL	0.2	0.6		$R_L=50\Omega$ to ground on each output
Duty Cycle	45		55	%	Measured at 50% amplitude of single-ended signal
Start-up Time [Note 3]		< 2	5	ms	



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Parameters		Min.	Typ.	Max.	Unit	Notes	
Differential Output High Voltage (V _{OH}) Output Low Voltage (V _{OL})	LVPECL	V _{OH}	V _{dd} -1.085	V _{dd} -0.95	V _{dd} -0.86	V	R _L =50Ω to V _{dd} -2.0V on each output
		V _{OL}	V _{dd} -1.81	V _{dd} -1.7	V _{dd} -1.62		
	LVDS	V _{OH}		1.43	1.60		R _L =100Ω between outputs
		V _{OL}	0.90	1.10			
	HCSL	V _{OH}	0.55	0.74	1.00		R _L =50Ω to ground on each output
		V _{OL}	-0.15	0.00	0.15		
Output Voltage Swing (V _{opp})		0.400			V	LVPECL	
		0.494				LVDS	
		0.450				HCSL	
Output Enable & Disable Control		0.7*(V _{dd})			V	Output Enable or No Connect	
				0.3*(V _{dd})		Output Disable (High Impedance)	
Output Enable Time			< 1	5.0	ms		
Output Disable Time				200	ns		
Output Disable Current Consumption				30	μA	OE ≤ 0.3V	
RMS Phase Jitter (12kHz to 20MHz from Carrier)		See Table 1 below				V _{dd} , output logic type and carrier frequency dependent	

- Note 1: Supply voltage (V_{dd}) = 1.8V option not available with LVPECL output, LVDS option only available ≤ 175MHz
- Note 2: Frequency Accuracy (Initial Set-Tolerance), at time of shipment (pre-reflow), relative to carrier frequency, @ +25°C
- Note 3: Relative to initial measured frequency @ +25°C
- Note 4: Option Q only available in select frequencies. Please contact Abracon for availability
- Note 5: Includes post reflow frequency accuracy, temperature stability, load pulling, power supply variation, and 10-year aging
- Note 6: Measured over 20% to 80% of waveform

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Table 1
RMS Phase Jitter 12kHz – 20MHz BW, Vdd=1.8V, 2.5V, 3.3V [Note 7, 8]

Carrier Frequency	Output Logic	Supply Voltage (1.8V)		Supply Voltage (2.5V)		Supply Voltage (3.3V)	
		RMS Jitter		RMS Jitter		RMS Jitter	
		Typ. (fs)	Max (fs)	Typ. (fs)	Max (fs)	Typ. (fs)	Max (fs)
100	LVDS	110	120	93	120	93	120
	LVPECL	NA	NA	97	120	97	120
	HCSL	96	120	97	120	97	120
125	LVDS	78	120	63	120	63	120
	LVPECL	NA	NA	64	100	64	100
	HCSL	69	120	66	100	66	100
156.25	LVDS	68	80	54	75	54	75
	LVPECL	NA	NA	54	75	54	75
	HCSL	61	80	54	75	54	75
200	LVDS	NA	NA	40	60	40	60
	LVPECL	NA	NA	43	60	43	60
	HCSL	NA	NA	NA	NA	NA	NA
250	LVDS	NA	NA	37	50	37	50
	LVPECL	NA	NA	35	50	35	50
	HCSL	NA	NA	NA	NA	NA	NA

Note 7: Guaranteed by characterization; RMS Phase Jitter specifications are inclusive of any spurs

Note 8: Phase jitter measured with Keysight E5052B Signal Source Analyzer

Absolute Maximum Ratings [Note 9]

Parameters	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	-0.3		4.5	V	
Input Voltage	-0.3		V _{DD} +0.3	V	
Output Voltage	-0.3		V _{DD} +0.3	V	
Maximum Junction Operating Temperature			150	°C	
Ambient Operating Temperature Range	-40		85	°C	Industrial
Ambient Operating Temperature Range	-20		70	°C	Extended Commercial
Reflow Temperature			260	°C	See Reflow Profile
ESD Protection	4kV HBM, 300V MM, 2kV CDM				

Note 9: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability. The data sheet limits are not guaranteed if the device is operated beyond the recommended operating conditions.



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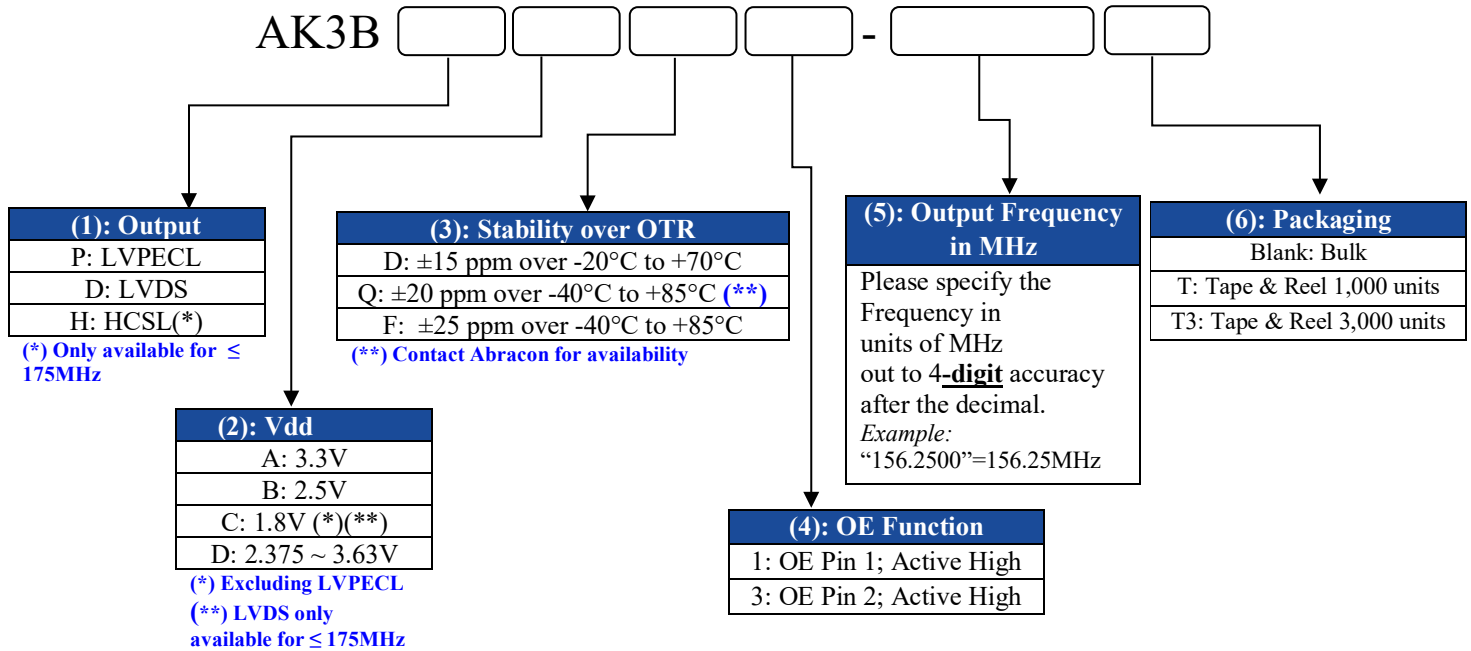


ESD Sensitive



3.2 x 2.5 x 1.0 mm
RoHS/RoHS II Compliant
 MSL Level = N/A

Options and Part Identification ^[Note 10]



Part Number Example:

AK3BDAF1-156.2500
 AK3BDAF1-156.2500T
 AK3BDAF1-156.2500T3

Note 10: Contact Abracon for non-standard part number configurations and/or requests with carrier frequency callouts up to 5 & 6 digit accuracy after the decimal.

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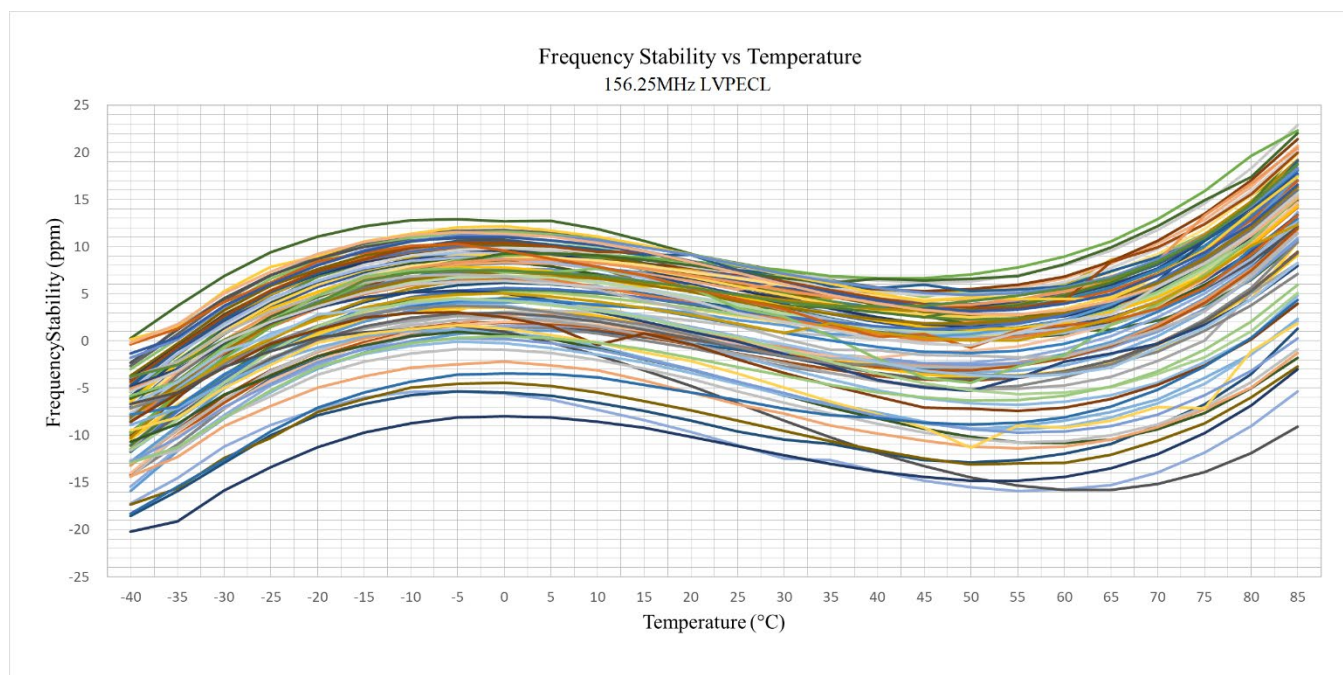
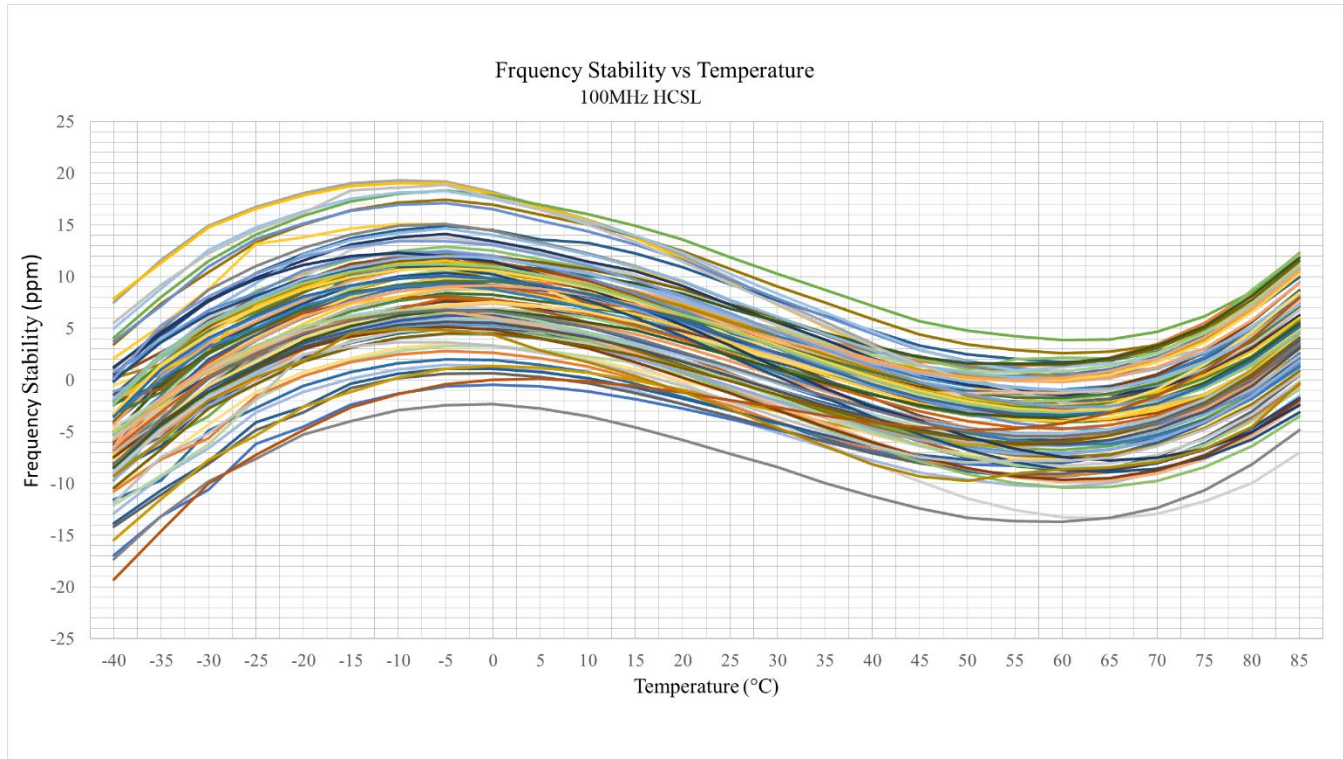


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Typical Frequency vs. Temperature Characteristics



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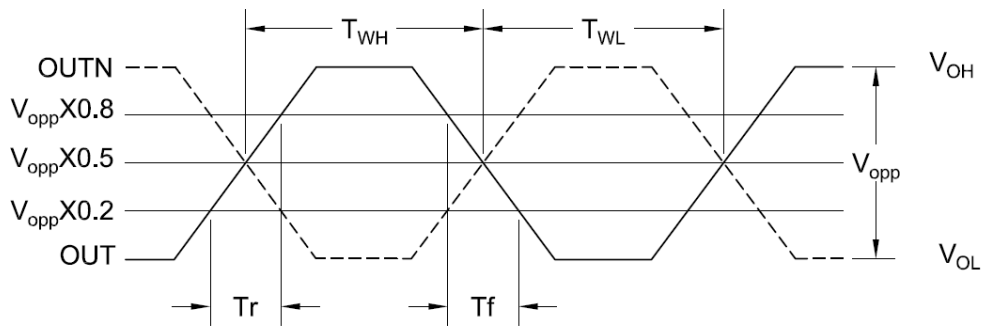
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MSL Level = N/A

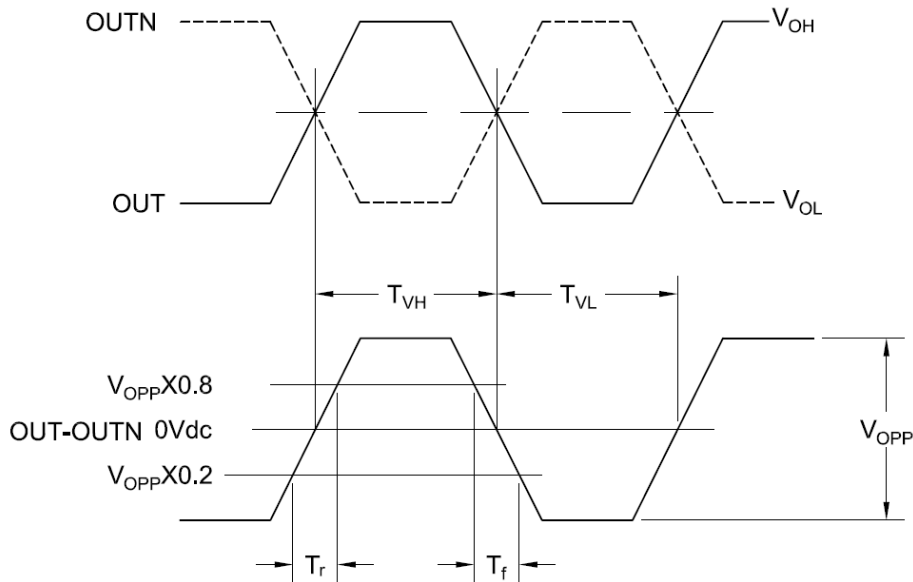
Output Waveform Diagram

LVPECL: Output Wave Form (Duty, Tr, Tf, Vopp)



$$\text{Duty Cycle} = \frac{T_{WH}}{T_{WH} + T_{WL}} \times 100\%$$

LVDS: Output Wave Form (Duty, Tr, Tf, VOH, VOL, Vopp)



$$\text{Duty} = \frac{T_{VH}}{T_{VH} + T_{VL}} \times 100\%$$

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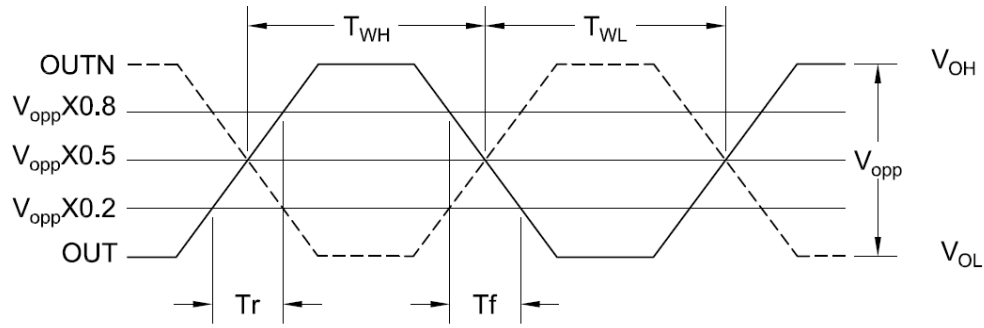


ESD Sensitive



3.2 x 2.5 x 1.0 mm
RoHS/RoHS II Compliant
MSL Level = N/A

HCSL: Output Wave Form (Duty, Tr, Tf, VOH, VOL, Vopp)



$$\text{Duty Cycle} = \frac{T_{WH}}{T_{WH} + T_{WL}} \times 100\%$$

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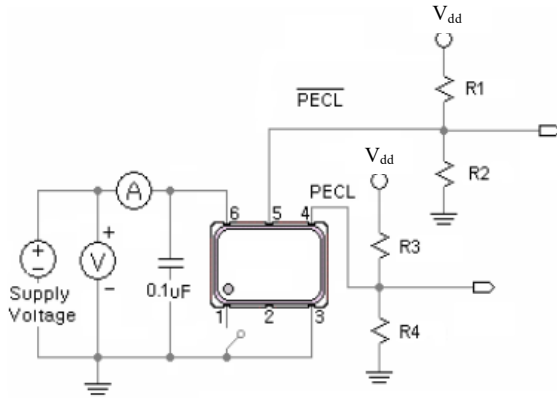
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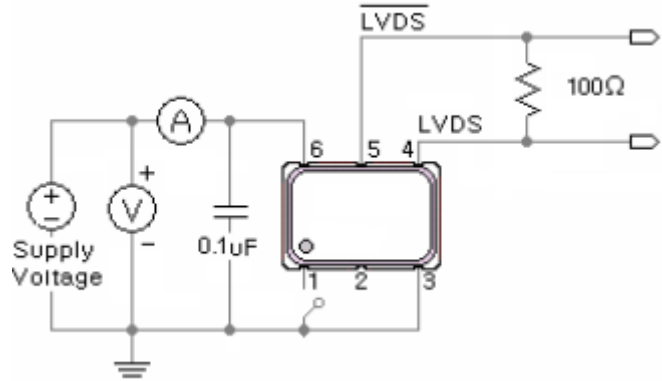
Recommended Test Circuit [\[Note 11\]](#)

LVPECL

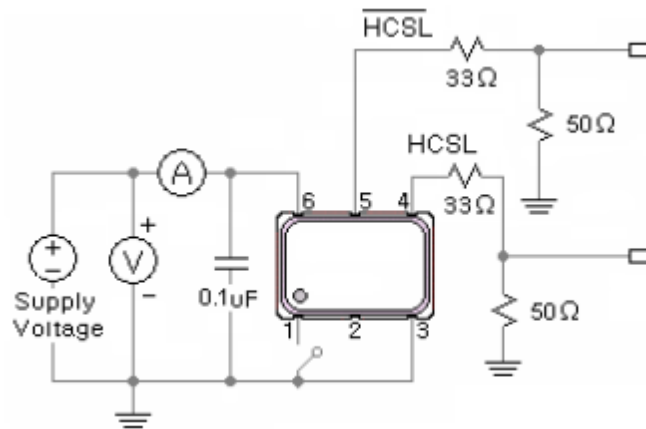


V_{dd}=3.3V: R₁=R₃=127Ω; R₂=R₄=82.5 Ω
 V_{dd}=2.5V: R₁=R₃=250Ω; R₂=R₄=62.5 Ω

LVDS



HCSL



Note 11: Recommended test circuit images are representative of when the OE Function is located on Pin 1; when the OE Function is located on Pin 2, then Pin 1=No Connect & Pin 2=OE or No Connect.

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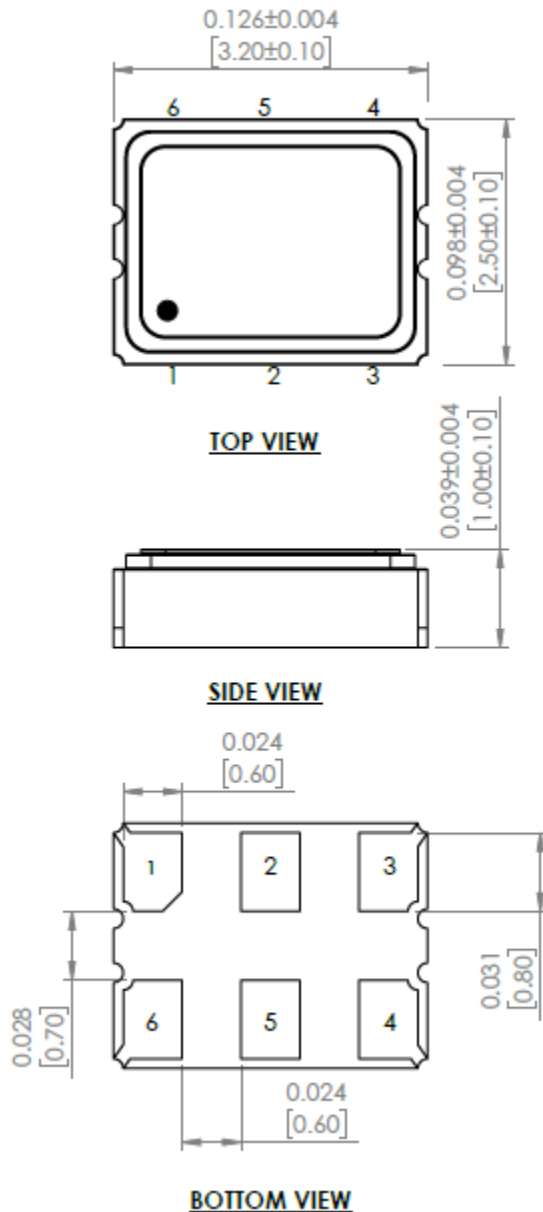


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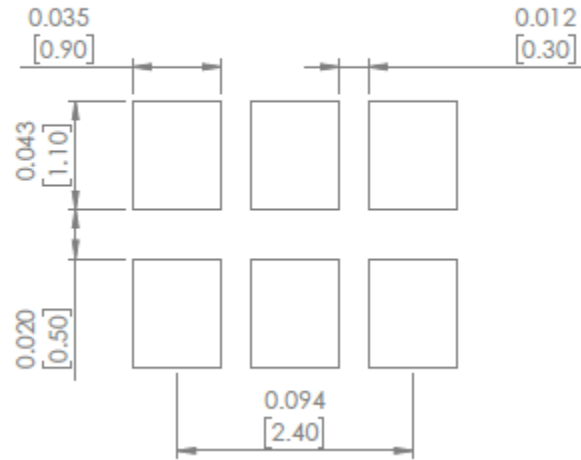


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Mechanical Dimensions



Recommended Land Pattern



Case 1 Pin #1=Output Enable/Disable Function where OE is Active HIGH		Case 2 Pin #2=Output Enable/Disable Function where OE is Active HIGH	
Pin	Description	Pin	Description
# 1	Output Enable = Logic High, "1", Vdd	# 1	No Connect
	Output Disable = Logic Low, "0", GND	# 2	Output Enable = Logic High, "1", Vdd
# 2	No Connect		Output Enable = Logic Low, "0", GND
# 3	GND	# 3	GND
# 4	Output	# 4	Output
# 5	Complementary output	# 5	Complementary output
# 6	Supply Voltage (Vdd)	# 6	Supply Voltage (Vdd)

Dimensions: inches [mm]

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Reflow Profile [JEDEC J-STD-020]

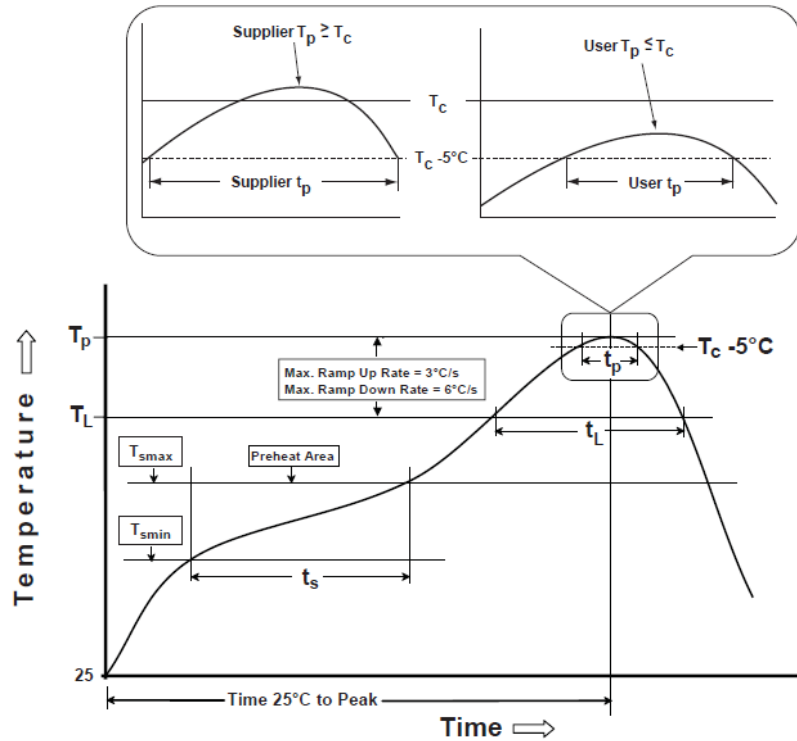


Table 1

SnPb Eutectic Process Classification Temperatures (T_c)		
Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2

Pb-Free Process Classification Temperatures (T_c)			
Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat / soak		
Temperature minimum (T_{smin})	100°C	150°C
Temperature maximum (T_{smax})	150°C	200°C
Time (T_{smin} to T_{smax}) (t_s)	60 - 120 sec.	60 - 120 sec.
Average ramp-up rate (T_{smax} to T_p)	3°C/sec. max	3°C/sec. max
Liquidous temperature (T_L)	183°C	217°C
Time at liquidous (t_L)	60 - 150 sec.	60 - 150 sec.
Peak package body temperature (T_p)*	see Table 1	see Table 2
Time (t_p)** within 5°C of the specified classification temperature (T_C)	20 sec.	30 sec.
Ramp-down rate (T_p to T_{smax})	6°C/sec. max	6°C/sec. max
Time 25°C to peak temperature	6 min. max	8 min. max
Reflow cycles	2 max	2 max

*Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

**Tolerance for time at peak profile temperature (t_p) is defined as supplier minimum and a user maximum.



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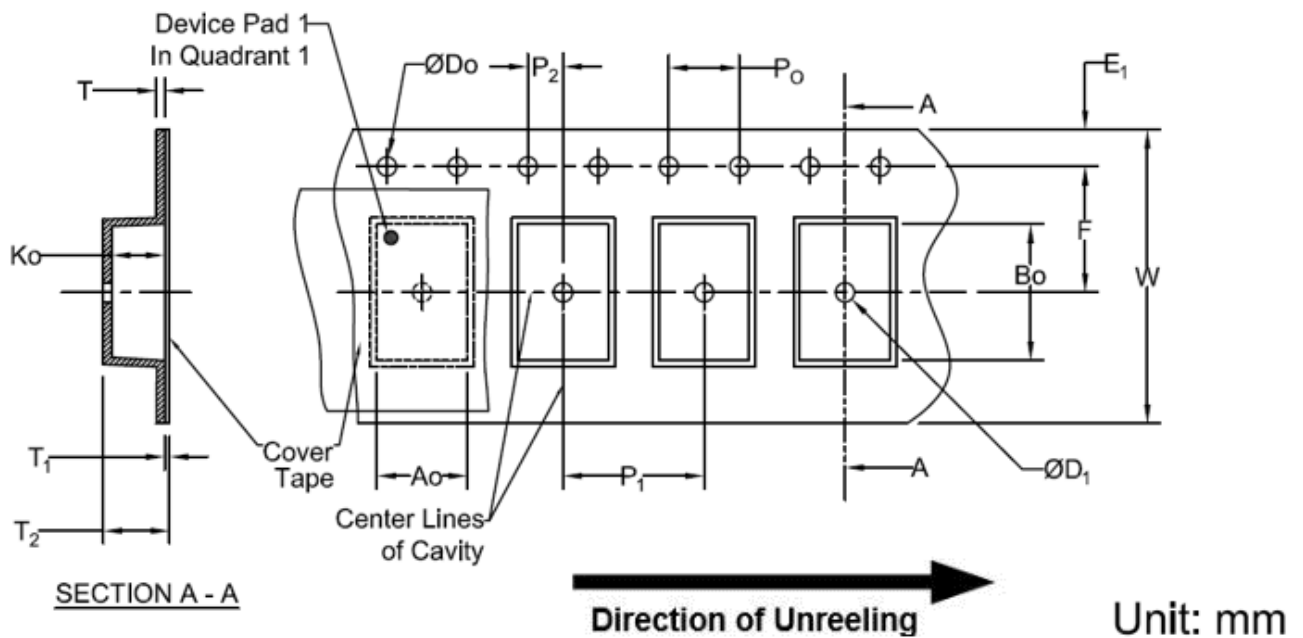
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Packaging

Blank = Bulk

T = Tape & Reel 1,000 units/reel

T3 = Tape & Reel 3,000 units/reel



Tape Specifications (mm)							
Width	Ao	Bo	Do	D ₁ (Min)	E ₁	F	Ko
8mm	*	*	1.5+0.1/-0.0	1.0	1.75±0.1	3.5±0.05	*

*Note: Compliant to EIA-481

Tape Specifications (mm)							
Width	P ₁	P ₂	P ₀	T (Max)	T ₁ (Max)	T ₂ (Max)	W (Max)
8mm	4.0±0.1	2.0±0.05	4.0±0.1	0.6	0.1	2.5	8.3

*Note: Compliant to EIA-481



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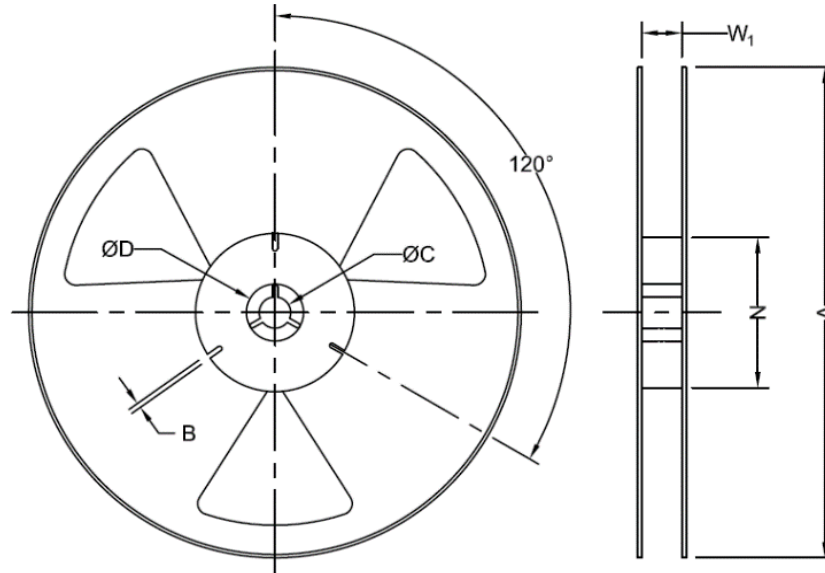
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Unit: mm

Tape Specifications (mm)							
Suffix	Qty/Reel	A (Nom)	B (Min)	C (Min)	D (Min)	N (Min)	* W_1
-T	1000	178	1.5	13.0+0.5/-0.2	20.2	50	8.4+1.5/-0.0
-T3	3000	178	1.5	13.0+0.5/-0.2	20.2	50	8.4+1.5/-0.0

*Note: Measured at Hub

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