

ClearClock™ Oscillator Family | Low Jitter | 7.0 x 5.0mm XO

AK7

Request Samples



Check Inventory



ESD Sensitive



7.0 x 5.0 x 1.8 mm
RoHS/RoHS II Compliant
MSL Level = 1

Features

- 3rd overtone solution
- Ultra-Low jitter: 75 fs typ RMS (100fs MAX, F= 156.25MHz LVPECL); spurs included
- Frequency range: 100MHz to 220MHz
- Lowest in-class power consumption (16mA Typ LVDS)
- ± 20 ppm & ± 25 ppm stability (-40 to +85°C) options available (dependent on frequency)
- 3.3V, 2.5V, 1.8V Vdd supply
- LVPECL, LVDS, & HCSL differential output options
- Output enable standard

Applications

- Networking & communications
- Gigabit Ethernet
- Fibre Channel
- SONET/SDH
- RF systems, base stations (BTS)
- Datacenter
- PCI Express
- Test & measurement

Key Electrical Specifications

Parameters		Min.	Typ.	Max.	Unit	Notes	
Frequency Range		100		220	MHz		
Standard Available Frequencies		100	122.88	125	148.5	MHz	Contact Abracon for availability of frequencies not listed
		156.25	200	212.5			
Supply Voltage (Vdd) ^[Note 1]		2.97	3.3	3.63	V	Option "A"	
		2.37	2.5	2.62		Option "B"	
		1.71	1.8	1.89		Option "C"	
Supply Current (Idd)	LVPECL		30	50	mA	@ 220MHz; @ Vdd=3.3V	
	LVDS		16	27		@ 220MHz; @ Vdd=3.3V	
	HCSL		17	30		@ 220MHz; @ Vdd=3.3V	
Operating Temperature Range		-20		+70	°C	Option "D"	
		-40		+85		Option "F" or "Q"	
Storage Temperature		-55		+150	°C		
Frequency Accuracy (Initial Set-Tolerance) ^[Note 3] at time of shipment (Pre-Reflow) @ +25°C		-10	< ± 5	+10	ppm	Relative to carrier frequency	
Frequency Stability over ^[Note 2, 3] Operating Temperature Range		-15		+15	ppm	Option "D" (-20°C to +70°C)	
		-20		+20		Option "Q" (-40°C to +85°C)	
		-25		+25		Option "F" (-40°C to +85°C)	
Aging over 20 Year Product Life ^[Note 4]		-15		+15	ppm		
All-Inclusive Frequency Accuracy (Total Stability) over 20 Year Product Life ^[Notes 4, 5]		-40		+40	ppm	Option "D" (-20°C to +70°C)	
		-45		+45		Option "Q" (-40°C to +85°C)	
		-50		+50		Option "F" (-40°C to +85°C)	



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Parameters	Min.	Typ.	Max.	Unit	Notes
Rise (Tr) / Fall (Tf) Time 20% to 80% V _{peak to peak}	LVPECL	0.2	0.4	ns	@ Vdd=3.3V, R _L =50Ω
		0.3	0.6		@ Vdd=2.5V, R _L =50Ω
	LVDS	0.15	0.4		@ Vdd=3.3V, R _L =100Ω
		0.15	0.4		@ Vdd=2.5V, R _L =100Ω
		0.3	0.5		@ Vdd=1.8V, R _L =100Ω
	HCSL	0.3	0.5		@ Vdd=3.3V, R _L =50Ω to GND
		0.3	0.5		@ Vdd=2.5V, R _L =50Ω to GND
		0.3	0.6		@ Vdd=1.8V, R _L =50Ω to GND
	Duty Cycle	45			55
Start-up Time ^[Note 2]		< 2	5.0	ms	

Note 1: Supply voltage (Vdd) = 1.8V option not available with LVPECL output

Note 2: Relative to initial measured frequency @ +25°C

Note 3: Option Q only available in select frequencies. Please contact Abracon for availability

Note 4: Relative to post-reflow frequency

Note 5: Includes temperature stability, initial frequency accuracy, load pulling, power supply variation, and 20-year aging

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Parameters		Min.	Typ.	Max.	Unit	Notes	
Differential Output High Voltage (V_{OH}) Output Low Voltage (V_{OL})	LVPECL	V_{OH}	$V_{dd}-1.03$		$V_{dd}-0.88$	V $R_L=50\Omega$ to $V_{dd}-2.0V$ $R_L=100\Omega$ between both outputs $R_L=50\Omega$ to ground on each output	
		V_{OL}	$V_{dd}-1.85$		$V_{dd}-1.60$		
	LVDS	V_{OH}		1.40	1.60		
		V_{OL}	0.90	1.10			
	HCSL	V_{OH}	0.40	0.74	0.85		
		V_{OL}	-0.15	0.00	0.15		
Output Voltage Swing		0.595	0.750	0.930	V	LVPECL	
		0.250	0.350	0.450		LVDS	
		0.620	0.700	0.780		HCSL	
Output Enable & Disable Control		$0.7*(V_{dd})$			V	Output Enable or No Connect	
				$0.3*(V_{dd})$		Output Disable (High Impedance)	
Output Enable Time			< 1	5.0	ms		
Output Disable Time				0.2	μs		
Output Disable Current Consumption				< 10	μA	$OE \leq 0.3V$	
RMS Phase Jitter [Note 6, 7, 8] @ +25°C (12kHz- 20MHz BW)	@ 200 MHz	LVPECL		70	95	fsec	@ Vdd=3.3V
				80	105		@ Vdd=2.5V
		LVDS		125	150		@ Vdd=3.3V
				150	175		@ Vdd=2.5V
		HCSL		120	145		@ Vdd=3.3V
				135	160		@ Vdd=2.5V
	@ 156.25 MHz	LVPECL		75	100	fsec	@ Vdd=3.3V
				80	105		@ Vdd=2.5V
		LVDS		90	115		@ Vdd=3.3V
				80	105		@ Vdd=2.5V
		HCSL		110	135		@ Vdd=3.3V
				115	140		@ Vdd=2.5V
	@ 148.5 MHz	LVPECL		115	140	fsec	@ Vdd=3.3V
				95	120		@ Vdd=2.5V
		LVDS		125	150		@ Vdd=3.3V
				120	145		@ Vdd=2.5V
		HCSL		130	155		@ Vdd=3.3V
				135	160		@ Vdd=2.5V
		115	140	@ Vdd=1.8V			

Note 6: Guaranteed by characterization; RMS Phase Jitter specifications are inclusive of any spurs

Note 7: Phase jitter measured with Keysight E5052B Signal Source Analyzer

Note 8: Refer to the next section for phase noise test setup and representative phase noise plots



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Parameters		Min.	Typ.	Max.	Unit	Notes	
RMS Phase Jitter [Note 6, 7, 8] @ +25°C (12kHz- 20MHz BW)	@ 125 MHz	LVPECL		100	125	fsec	@ Vdd=3.3V
				100	125		@ Vdd=2.5V
		LVDS		150	175		@ Vdd=3.3V
				110	135		@ Vdd=2.5V
		HCSL		140	165		@ Vdd=1.8V
				135	160		@ Vdd=3.3V
	@ 122.88 MHz	LVPECL		150	175	fsec	@ Vdd=3.3V
				155	180		@ Vdd=2.5V
		LVDS		130	155		@ Vdd=3.3V
				115	140		@ Vdd=2.5V
		HCSL		165	190		@ Vdd=1.8V
				135	160		@ Vdd=3.3V
	@ 100 MHz	LVDS		140	165	fsec	@ Vdd=2.5V
				125	150		@ Vdd=1.8V
		HCSL		155	180		@ Vdd=2.5V
				145	170		@ Vdd=3.3V
		HCSL		120	145		@ Vdd=2.5V
				155	180		@ Vdd=1.8V

Phase Noise Test Setup

- Keysight E5052B Signal Source Analyzer
- Integration Bandwidth = 12kHz to 20MHz
- Spurious Activity (entire plot trace) = Not omitted (Normalized in dBc/Hz)
- Specified Spur Omission Function = Not enabled
- IF Gain = 20dB
- Correlation = 5
- Average = 3

Note 6: Guaranteed by characterization; RMS phase jitter specifications are inclusive of any spurs

Note 7: RMS phase jitter measured with Keysight E5052B Signal Source Analyzer

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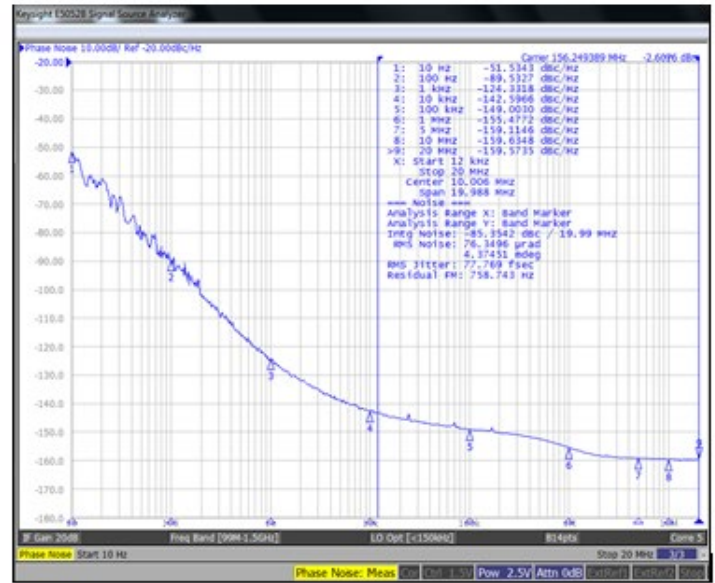
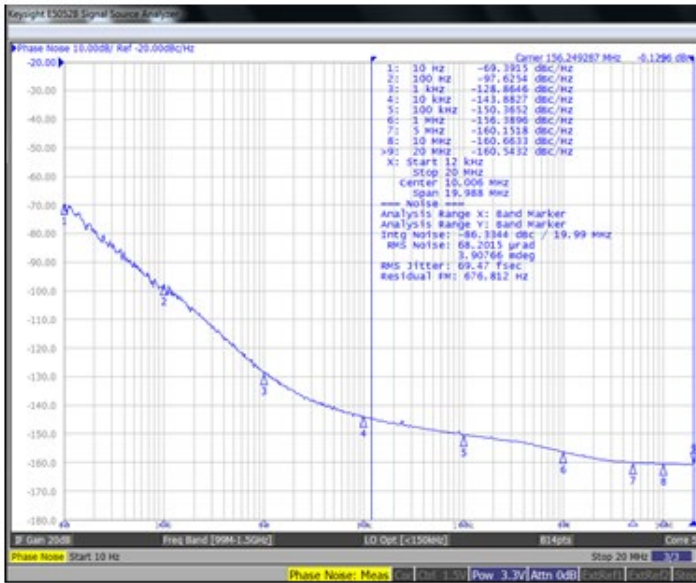
RoHS/RoHS II Compliant

MSL Level = 1

Representative Phase Noise Plots @ +25°C [Note 9]

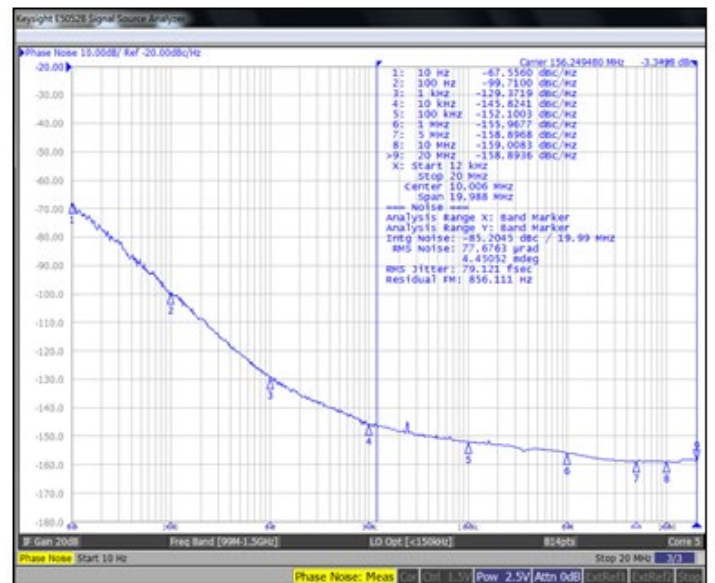
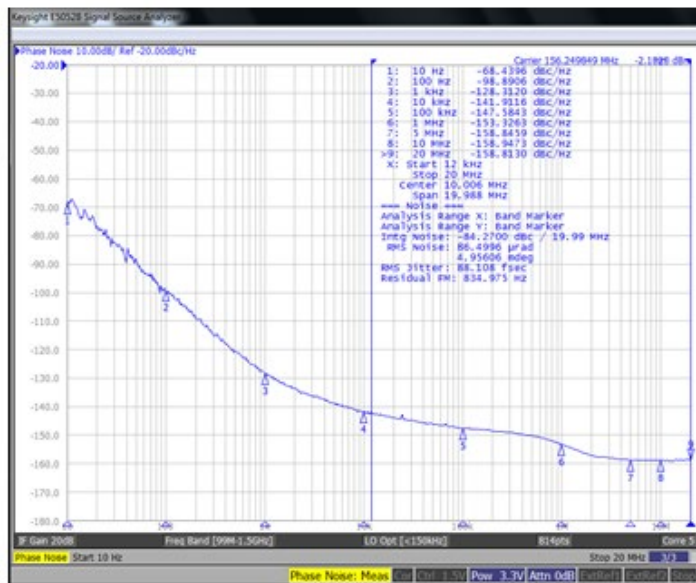
F=156.2500MHz | V_{dd}=3.3V | LVPECL
RMS Phase Jitter = 69 fsec

F=156.2500MHz | V_{dd}=2.5V | LVPECL
RMS Phase Jitter = 77 fsec



F=156.2500MHz | V_{dd}=3.3V | LVDS
RMS Phase Jitter = 88 fsec

F=156.2500MHz | V_{dd}=2.5V | LVDS
RMS Phase Jitter = 79 fsec



Note 9: Contact Abracon for phase noise plots at alternative supply voltage (V_{dd}) & differential output formats



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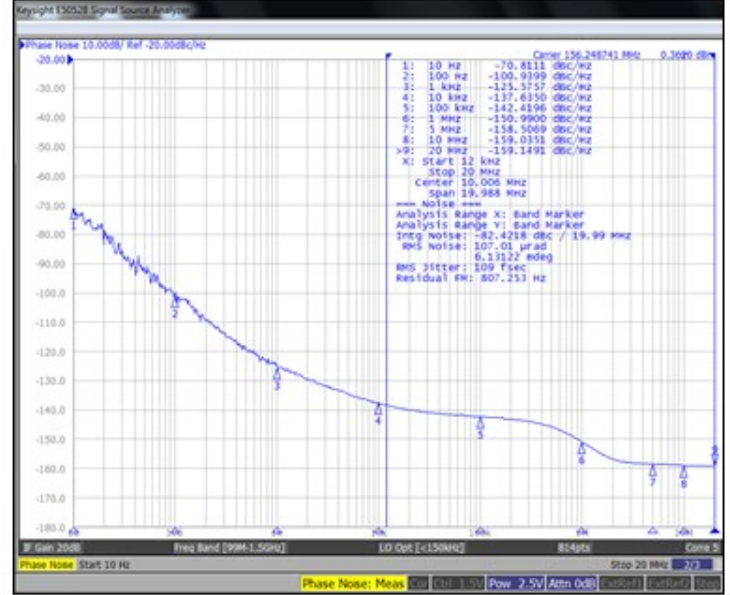
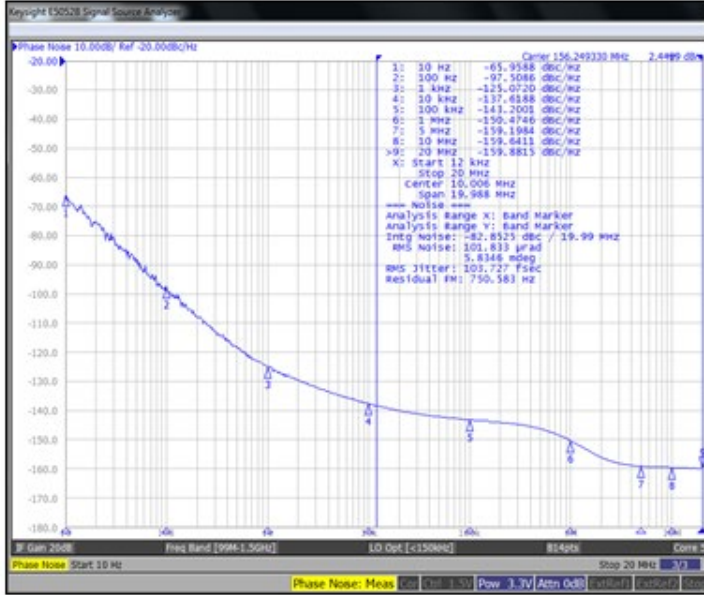
ESD Sensitive



7.0 x 5.0 x 1.8 mm
RoHS/RoHS II Compliant
MSL Level = 1

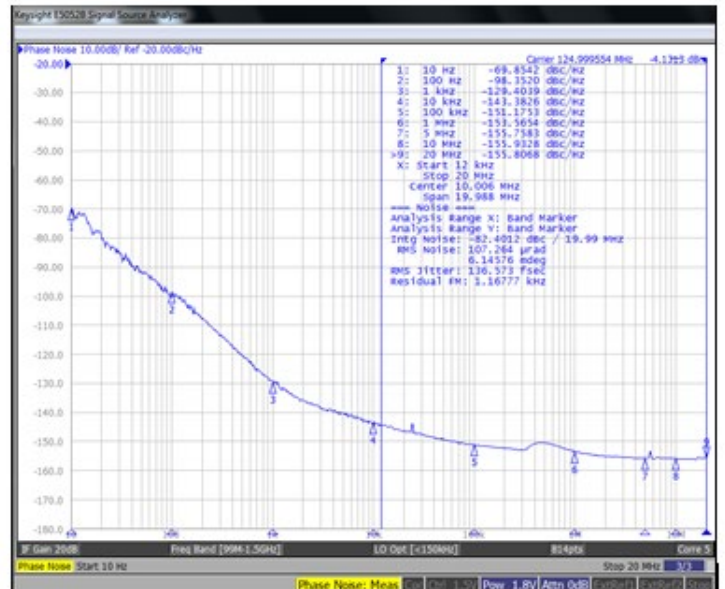
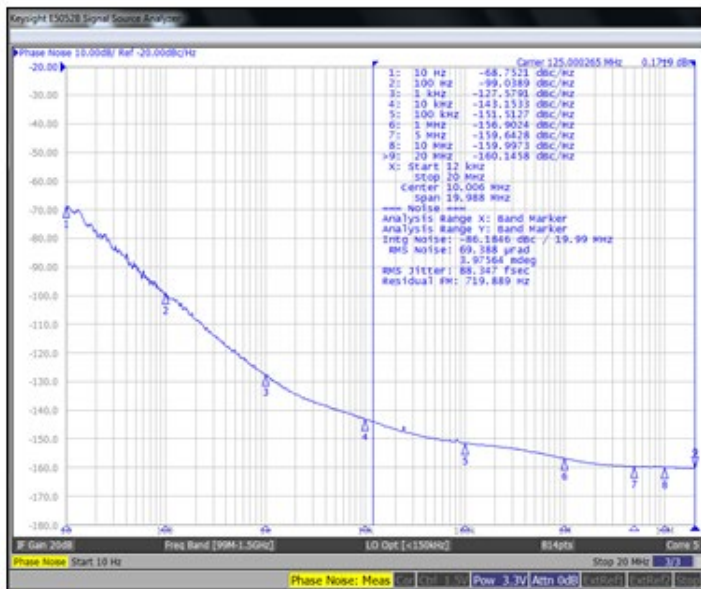
F=156.2500MHz | V_{dd}=3.3V | HCSSL
RMS Phase Jitter = 103 fsec

F=156.2500MHz | V_{dd}=2.5V | HCSSL
RMS Phase Jitter = 109 fsec



F=125.0000MHz | V_{dd}=3.3V | LVPECL
RMS Phase Jitter = 88 fsec

F=125.0000MHz | V_{dd}=1.8V | LVDS
RMS Phase Jitter = 136 fsec



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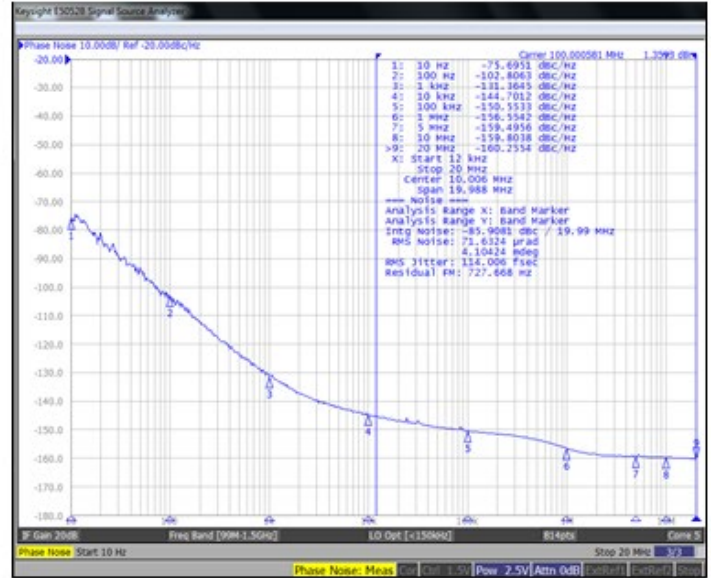
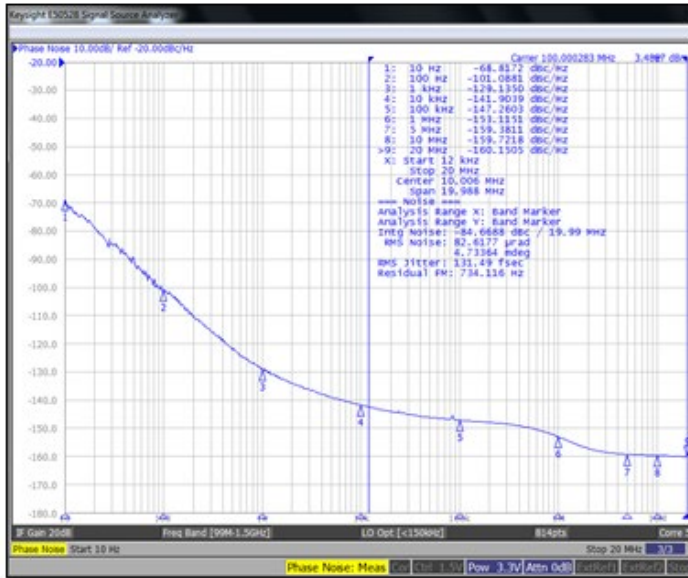
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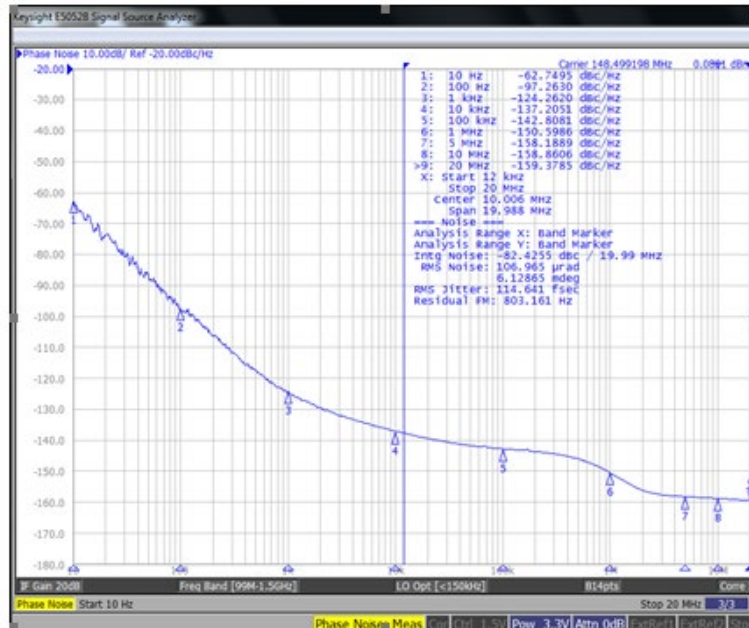
7.0 x 5.0 x 1.8 mm
RoHS/RoHS II Compliant
MSL Level = 1

F=100.0000MHz | V_{dd}=3.3V | HCSSL
RMS Phase Jitter = 131 fsec

F=100.0000MHz | V_{dd}=2.5V | HCSSL
RMS Phase Jitter = 114 fsec



F=148.5000MHz | V_{dd}=3.3V | LVPECL
RMS Phase Jitter = 114 fsec



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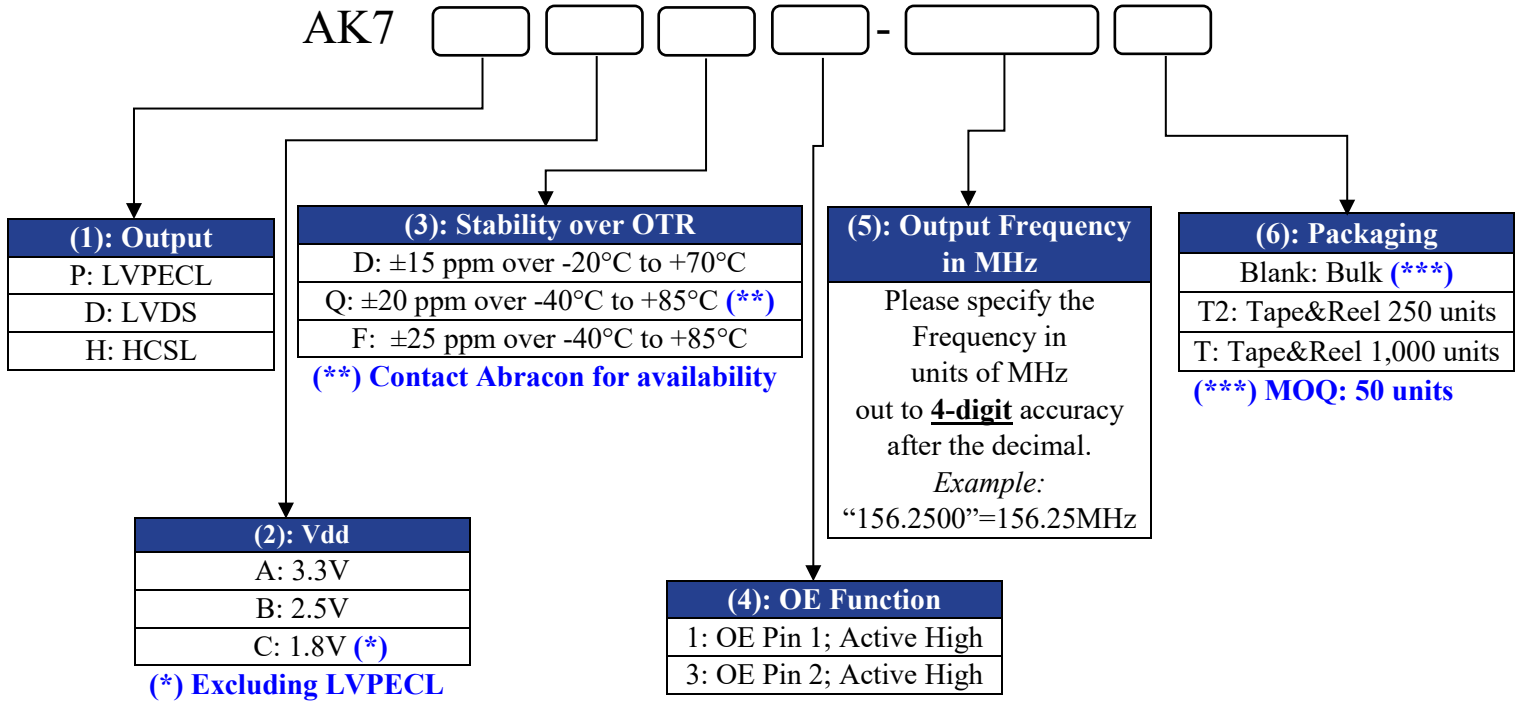


ESD Sensitive



7.0 x 5.0 x 1.8 mm
RoHS/RoHS II Compliant
MSL Level = 1

Options and Part Identification [Note 10]



Part Number Example:

AK7PAF1-156.2500

AK7PAF1-156.2500T2

AK7PAF1-156.2500T

Note 10: Contact Abracon for non-standard part number configurations and/or requests with carrier frequency callouts up to 5 & 6 digit accuracy after the decimal



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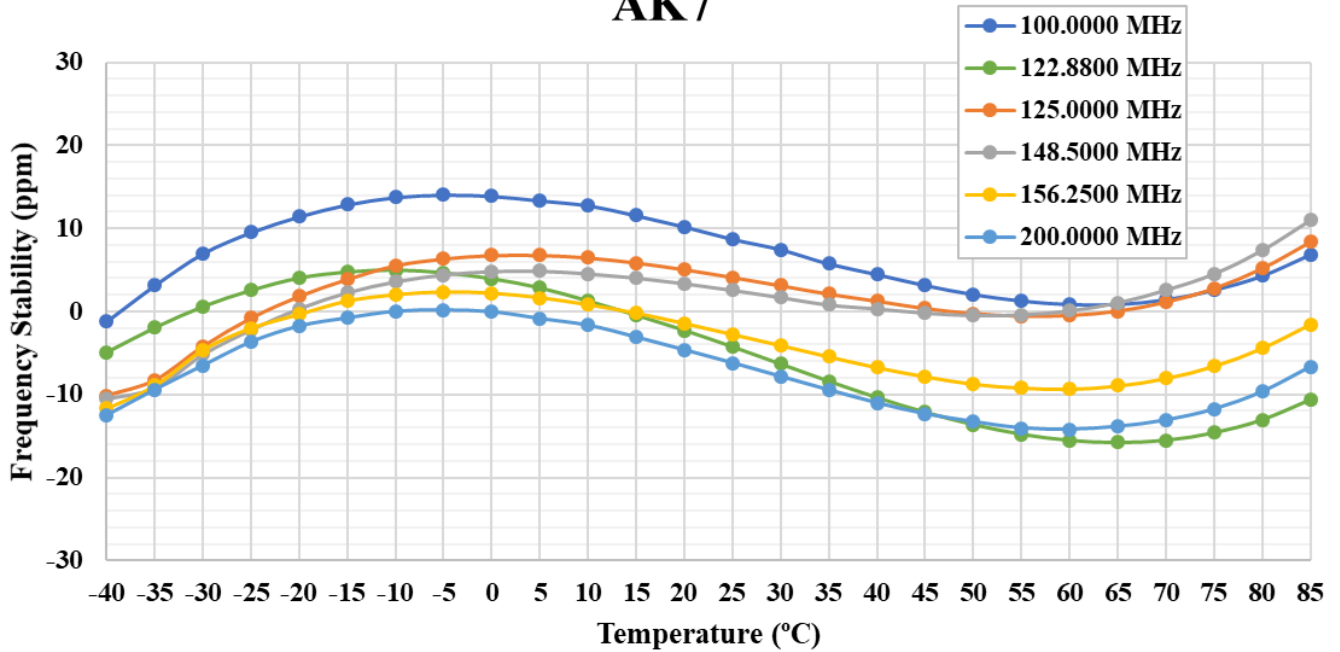
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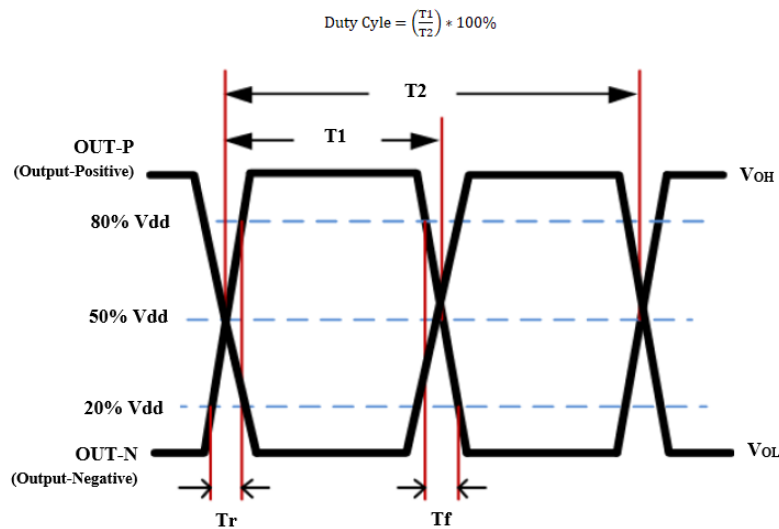
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Typical Frequency vs. Temperature Characteristics

Frequency Stability vs. Temperature AK7



Differential Output Waveform



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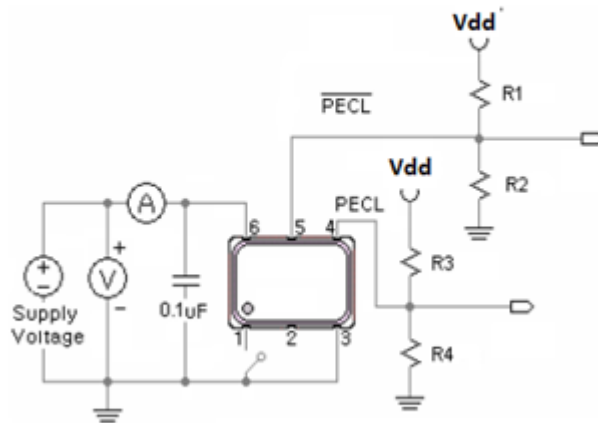
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7.0 x 5.0 x 1.8 mm
RoHS/RoHS II Compliant
MSL Level = 1

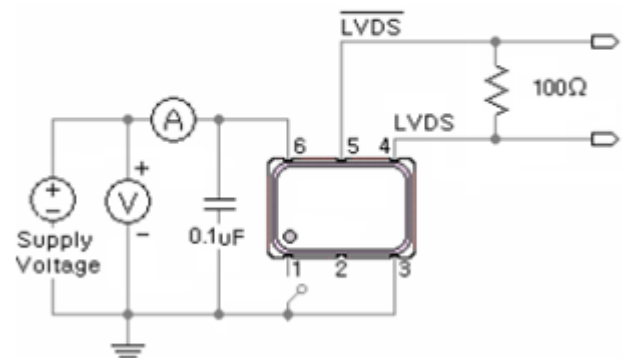
Recommended Test Circuit [\[Note 11\]](#)

LVPECL

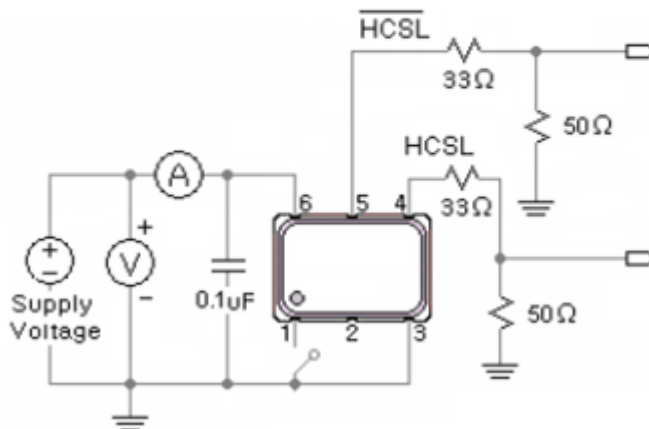


Vdd= 3.3V: R1=R3=127Ω; R2=R4=82.5Ω
Vdd= 2.5V: R1=R3=250Ω; R2=R4=62.5Ω

LVDS



HCSL



Note 11: Recommended test circuit images are representative of when the OE Function is located on Pin 1; when the OE Function is located on Pin 2, then Pin 1=No Connect & Pin 2=OE or No Connect.

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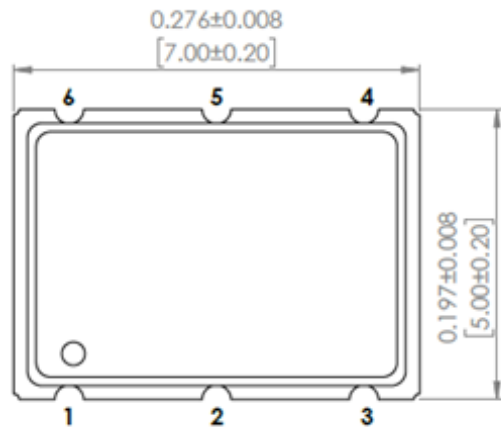


Check Inventory

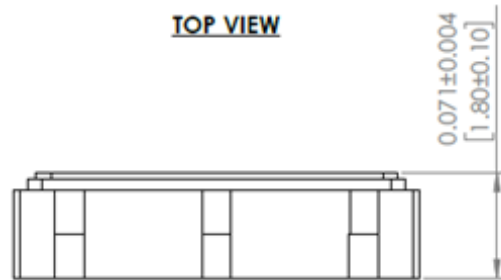


7.0 x 5.0 x 1.8 mm
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MSL Level = 1

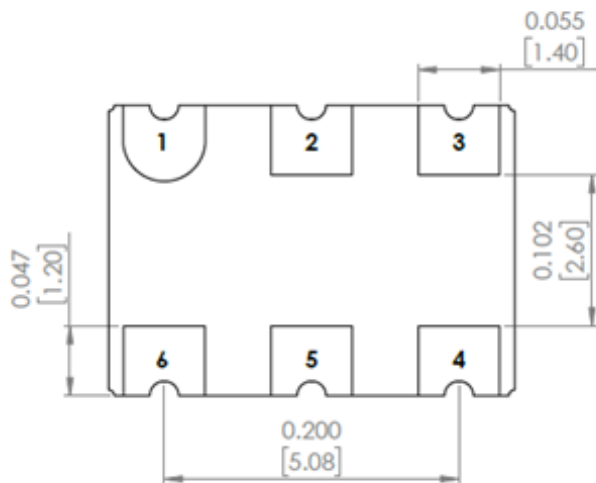
Mechanical Dimensions



TOP VIEW



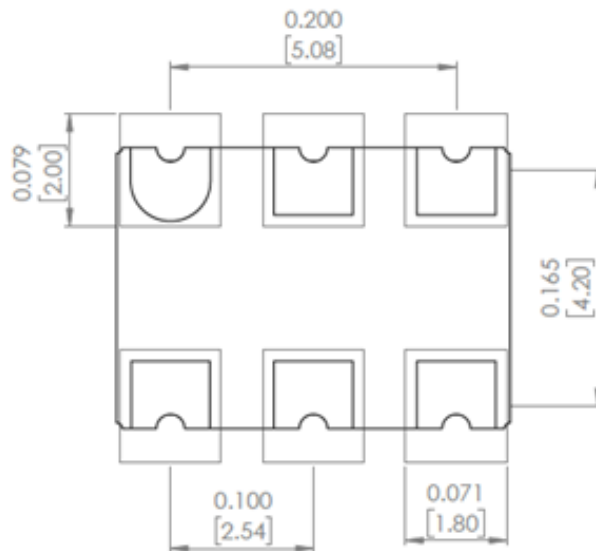
SIDE VIEW



BOTTOM VIEW

Dimensions: inches [mm]

Recommended Land Pattern



Case 1 Pin #1=Output Enable/Disable Function where OE is Active HIGH		Case 2 Pin #2=Output Enable/Disable Function where OE is Active HIGH	
Pin	Description	Pin	Description
# 1	Output Enable = Logic High, "1", Vdd	# 1	No Connect
	Output Disable = Logic Low, "0", GND	# 2	Output Enable = Logic High, "1", Vdd
# 2	No Connect		Output Enable = Logic Low, "0", GND
# 3	GND	# 3	GND
# 4	Output	# 4	Output
# 5	Complementary output	# 5	Complementary output
# 6	Supply Voltage (Vdd)	# 6	Supply Voltage (Vdd)

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Reflow Profile [JEDEC J-STD-020]

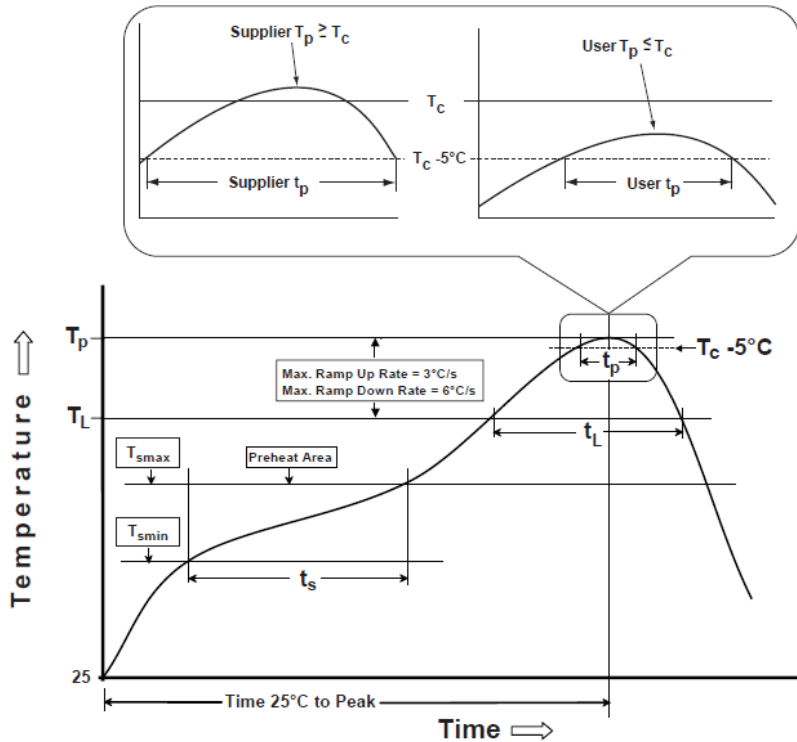


Table 1

SnPb Eutectic Process Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2

Pb-Free Process Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat / soak		
Temperature minimum (T_{smin})	100°C	150°C
Temperature maximum (T_{smax})	150°C	200°C
Time (T_{smin} to T_{smax}) (t_s)	60 - 120 sec.	60 - 120 sec.
Average ramp-up rate (T_{smax} to T_p)	3°C/sec. max	3°C/sec. max
Liquidous temperature (T_L)	183°C	217°C
Time at liquidous (t_L)	60 - 150 sec.	60 - 150 sec.
Peak package body temperature (T_p)*	see Table 1	see Table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20 sec.	30 sec.
Ramp-down rate (T_p to T_{smax})	6°C/sec. max	6°C/sec. max
Time 25°C to peak temperature	6 min. max	8 min. max
Reflow cycles	2 max	2 max

*Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

**Tolerance for time at peak profile temperature (t_p) is defined as supplier minimum and a user maximum.

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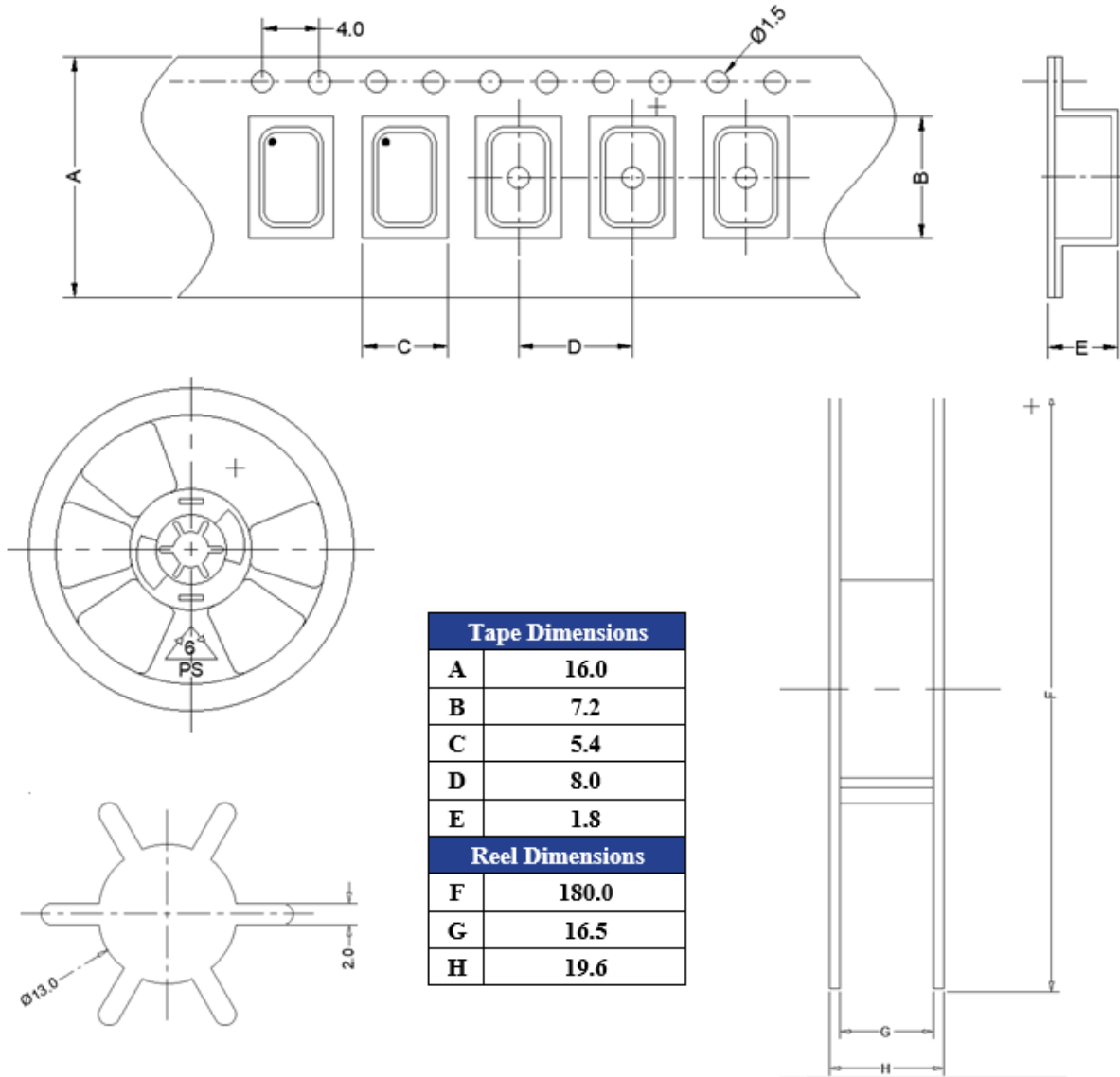


7.0 x 5.0 x 1.8 mm
RoHS/RoHS II Compliant
MSL Level = 1

Packaging

Bulk (MOQ=50 units)
T2 = Tape & Reel 250 units/reel
T = Tape & Reel 1,000 units/reel

Feeding (PULL) Direction →



Dimensions: mm

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