



ASEMP



RoHS/RoHS II compliant

Moisture Sensitivity Level – MSL 1

## FEATURES:

- Low Power Consumption for high speed communication
- Exceptional Stability Over Temp. at -40 to +85°C, ±15ppm
- Extended Automotive Grade Temp. stability at -55 to +125°C, ±25ppm
- MIL-STD-883 shock and vibration compliant
- Durable QFN Plastic Compact Packaging
- Standby or Disable Tri-state function
- Low jitter (Period jitter RMS and Phase jitter RMS)
- High power supply noise reduction, -50dBc

## APPLICATIONS:

- Storage Area Networks (SATA, SAS, Fiber Channel)
- Passive Optical Networks (EPON, 10G-EPON, GPON, 10G-PON)
- Ethernet (1G, 10GBASE-T/KR/LR/SR, FCoE)
- PCI Express
- Display port

## STANDARD SPECIFICATIONS:

### Common Key Electrical Specifications – CMOS, LVPECL, LVDS, and HCSL

Parameters	Minimum	Typical	Maximum	Units	Notes	
Frequency Range	CMOS	2.3000*		170.0000	MHz	-20 ~ +70°C -40 ~ +85°C
	CMOS	3.3000*		170.0000		-40 ~ +105°C -55 ~ +125°C
	LVPECL	2.3000*		460.0000		Commercial, Industrial temp. range
	LVDS	2.3000*		460.0000		Commercial, Industrial temp. range
	HCSL	2.3000*		460.0000		Commercial, Industrial temp. range
Operating Temperature	-20		+70	°C	See options	
Storage Temperature	-55		+150	°C		
Overall Frequency Stability	-50		+50	ppm	See options	
Supply Voltage (Vdd)	+2.25		+3.6	V		
Startup Time			5	ms		
Enable Time			20	ns	STD (Tri-state)	
			5	ms	PD option (Power Down)	
Disable Time			5	ns		
Disable Current		20	22	mA	STD (Tri-state)	
			0.095		PD option (Power Down)	
Tri-state Function (Standby/Disable)	"1" (VIH≥0.75*Vdd) or Open: Oscillation "0" (VIL<0.25*Vdd) : Hi Z			V	40kΩ pull-up resistor embedded	
Aging	-5.0		+5.0	ppm	First year	

\* For 2.3000MHz ≤ F0 ≤ 9.9999MHz, 6-8 weeks lead-time applies

### Key Electrical Specifications – CMOS

Parameters	Minimum	Typical	Maximum	Units	Notes
Supply Current (I <sub>dd</sub> )		31	35	mA	CL=15pF, 125MHz
Output Logic Level	V <sub>OH</sub>	0.9*V <sub>dd</sub>		V	I=±6mA
	V <sub>OL</sub>		0.1*V <sub>dd</sub>	V	
Rise Time		1.1	2.0	ns	CL=15pF
Fall Time		1.3	2.0	ns	20% to 80%
Duty Cycle	45		55	%	
Integrated Phase Jitter (J <sub>PH</sub> )		0.30	2	ps	200kHz ~ 20MHz@125MHz
		0.38	2		100kHz ~ 20MHz@125MHz
		1.70	2		12kHz ~ 20MHz@125MHz
Period Jitter RMS (J <sub>PER</sub> )		3.0		ps	

REVISED: 12.6.2018



## Key Electrical Specifications – LVPECL

Parameters		Minimum	Typical	Maximum	Units	Notes
Supply Current ( $I_{dd}$ )			56.5	58	mA	RL=50Ω
Output Logic Level	$V_{OH}$	$V_{dd}-1.08$			V	RL=50Ω
	$V_{OL}$			$V_{dd}-1.55$	V	
Peak to Peak Output Swing ( $V_{pp}$ )			800		mV	Single ended
Rise Time	$T_r$		250		ps	RL=50Ω , CL=0pF 20% to 80%
Fall Time	$T_f$		250			
Duty Cycle		48		52	%	Differential
Integrated Phase Jitter ( $J_{PH}$ )			0.25	2	ps	200kHz ~ 20MHz @156.25MHz
			0.38	2		100kHz ~ 20MHz @156.25MHz
			1.70	2		12kHz ~ 20MHz @156.25MHz
Period Jitter RMS ( $J_{PER}$ )			2.5		ps	

## Key Electrical Specifications – LVDS

Parameters		Minimum	Typical	Maximum	Units	Notes
Supply Current ( $I_{dd}$ )			29	32	mA	RL=100Ω
Output Offset Voltage ( $V_{OS}$ )		1.125		1.4	V	RL=100Ω differential
Delta Offset Voltage ( $\Delta V_{OS}$ )				50	mV	
Peak to Peak Output Swing ( $V_{pp}$ )			350		mV	Single ended
Rise Time	$T_r$		200		ps	RL=50Ω , CL=2pF 20% to 80%
Fall Time	$T_f$		200			
Duty Cycle		48		52	%	Differential
Integrated Phase Jitter ( $J_{PH}$ )			0.28	2	ps	200kHz ~ 20MHz @156.25MHz
			0.40	2		100kHz ~ 20MHz @156.25MHz
			1.70	2		12kHz ~ 20MHz @156.25MHz
Period Jitter RMS ( $J_{PER}$ )			2.5		ps	

## Key Electrical Specifications – HCSL

Parameters		Minimum	Typical	Maximum	Units	Notes
Supply Current ( $I_{dd}$ )			40	42	mA	RL=50Ω
Output Logic Level	$V_{OH}$	0.725			V	RL=50Ω
	$V_{OL}$			0.1	V	
Peak to Peak Output Swing ( $V_{pp}$ )			750		mV	Single ended
Rise Time	$T_r$	200		400	ps	RL=50Ω , CL=2pF 20% to 80%
Fall Time	$T_f$	200		400		
Duty Cycle		48		52	%	Differential
Integrated Phase Jitter ( $J_{PH}$ )			0.25	2	ps	200kHz ~ 20MHz @156.25MHz
			0.37	2		100kHz ~ 20MHz @156.25MHz
			1.70	2		12kHz ~ 20MHz @156.25MHz
Period Jitter RMS ( $J_{PER}$ )			2.5		ps	

REVISED: 12.6.2018



## Absolute Maximum Ratings

Item	Minimum	Maximum	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	V <sub>dd</sub> +0.3	V	
Junction Temp.		+150	°C	
Storage Temp.	-55	+150	°C	
Soldering Temp.		+260	°C	40sec max
ESD			V	
HBM		4,000		
MM		400		
CDM		1,500		

## OPTIONS AND PART IDENTIFICATION: (left blank if standard)

### Programmed Orders (Quantity > 1,000pcs)

ASEMP  -  MHz -   -  -

Output Type	Frequency in MHz	Operating Temp.	Overall Freq. Stability	Tri-state (Pin 1)	Packaging
C: CMOS	e.g. 156.2500 MHz (Maximum 4 digits after decimal)	Blank: -20°C ~ +70°C	Blank: ±50ppm	Blank: Tri-state	Blank***: Tube (110pcs / Tube)
LP: LVPECL		L: -40°C ~ +85°C	Y: ±10ppm*	PD: Power Down	T: Tape & Reel (1kpcs / reel)
LV: LVDS		X: -40°C ~ +105°C	R: ±25 ppm		T3: Tape & Reel (3kpcs / reel)
HC: HCSL		Z** : -55°C ~ +125°C			T5: Tape & Reel (5kpcs / reel)

\* Temp option L, X or -20°C ~ +70°C, only

\*\* CMOS output only

\*\*\* For Quick turn-around programmable orders < 1000pcs: Due to the immediate availability of stock and the qty of the order, the parts may be delivered as BULK: Cut Tape, Loose parts in Antistatic Bag or in Tube(s). The MOQ per the series will still apply for Tube packaging.

### Un-Programmed Orders

Blank un-programmed oscillators are available for quick turn engineering requirements. Please call ABRACON for more information

ASEMP  - BLANK -   -  -

Output Type	Operating Temp.	Overall Freq. Stability	Tri-state (Pin 1)	Packaging
C: CMOS	Blank: -20°C ~ +70°C	Blank: ±50ppm	Blank: Tri-state	Blank: Tube (110pcs / Tube)
LP: LVPECL	L: -40°C ~ +85°C	Y: ±10ppm*	PD: Power Down	T: Tape & Reel (1kpcs / reel)
LV: LVDS	X: -40°C ~ +105°C	R: ±25 ppm		T3: Tape & Reel (3kpcs / reel)
HC: HCSL	Z** : -55°C ~ +125°C			T5: Tape & Reel (5kpcs / reel)

\* Temp option L, X or -20°C ~ +70°C, only

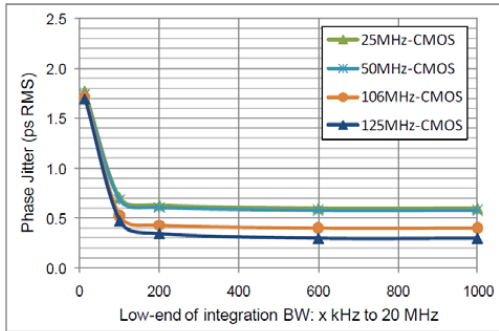
\*\* CMOS output only



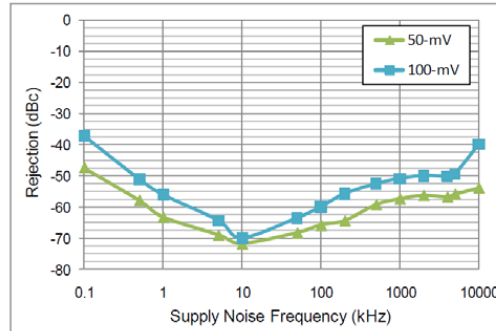
## NOMINAL PERFORMANCE PARAMETERS

(Unless specified otherwise: T=25° C, VDD=3.3 V)

### CMOS OUTPUT

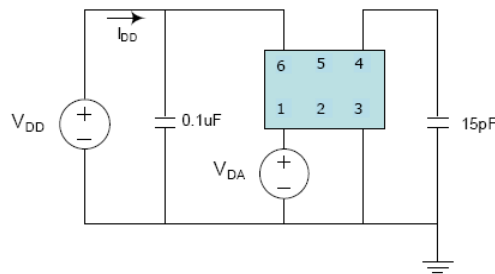


Phase jitter (integrated phase noise)

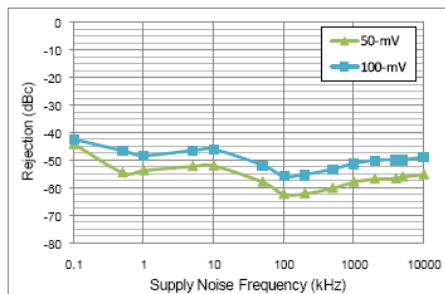


Power supply rejection ratio

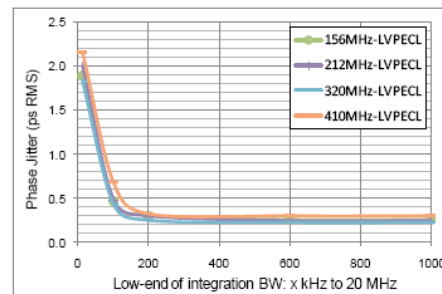
### Test Circuit



### LVPECL output

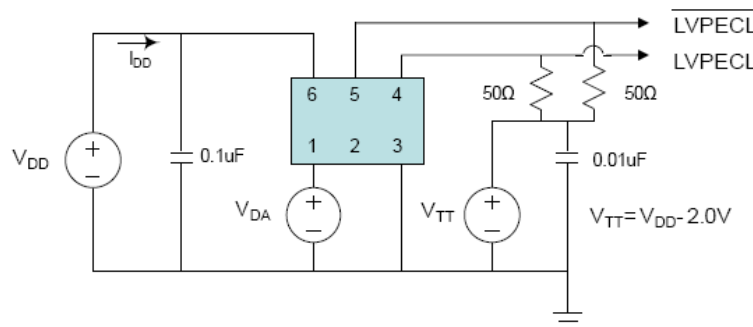


Power supply rejection ratio



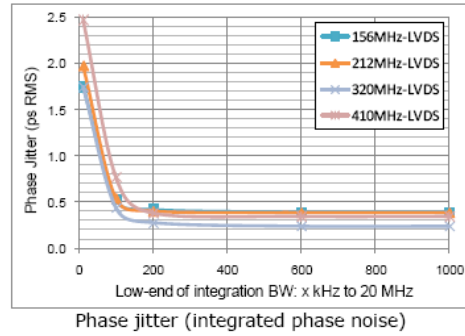
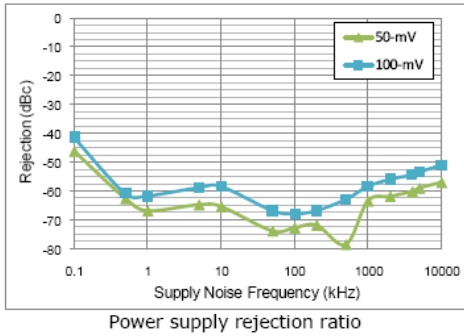
Phase jitter (integrated phase noise)

### Test Circuit

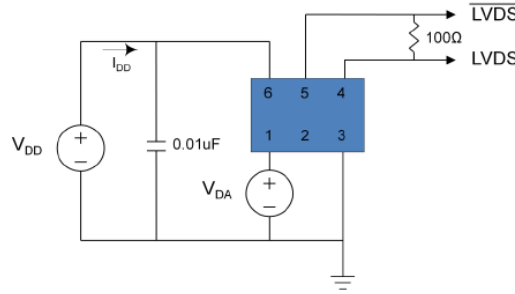




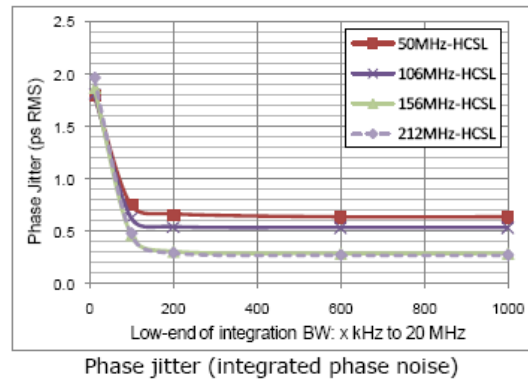
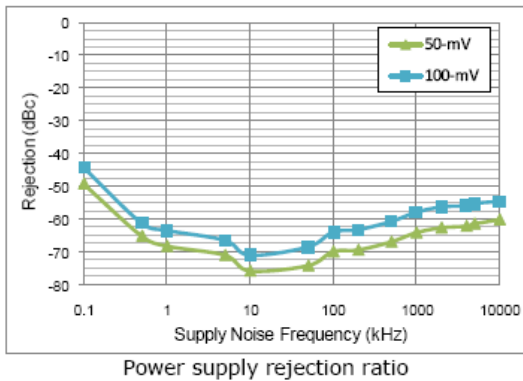
## LVDS OUTPUT



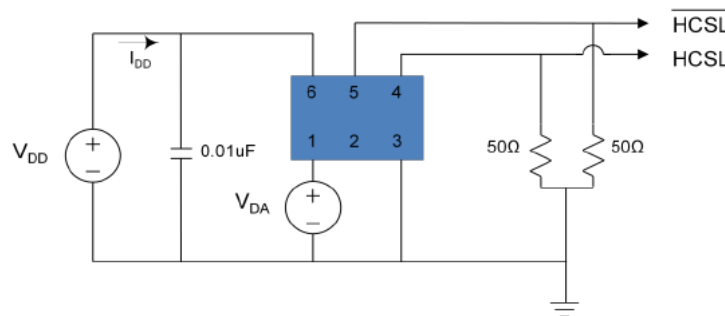
## Test Circuit



## HCSL OUTPUT



## Test Circuit





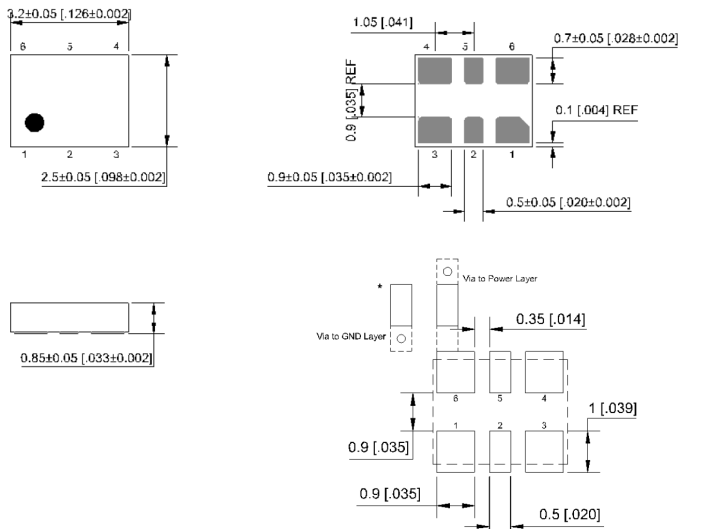
ASEMP



RoHS/RoHS II compliant

Life Size 3.2 x 2.5 x 0.85 mm

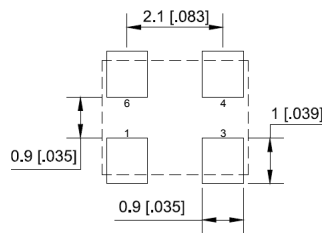
## OUTLINE DIMENSIONS:



Recommended Land Pattern for LVPECL, LVDS, HCSL

Pin #	Function
1	Tri-state
2	NC
3	GND
4	Output
5	NC (CMOS)
6	Output (LVPECL, LVDS, HCSL)
	Vdd

Note: Recommend using an approximately 0.01µF bypass capacitor between PIN 6 and 3.

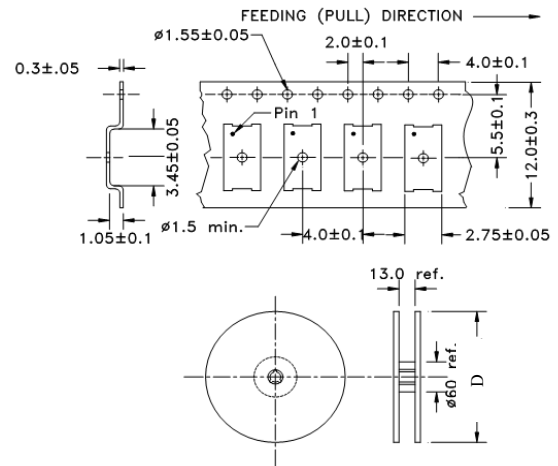


Recommended Land Pattern for CMOS

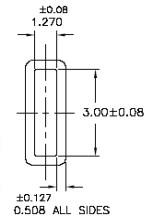
Dimensions: mm (inches)

## TAPE AND REEL:

T= 1,000pcs/reel (D=180mm)  
 T3= 3,000pcs/reel (D=180mm)  
 T5= 5,000pcs/reel (D=330mm)



Tube: 110 pcs/tube

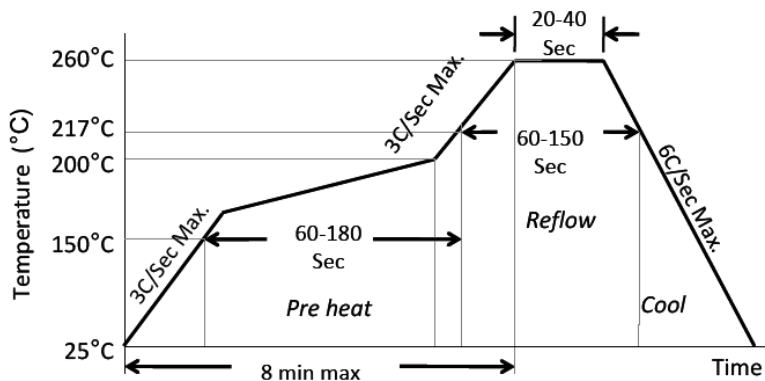


Unit orientation in tube:



Dimensions: mm

## REFLOW PROFILE:



Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec Max.
Preheat Time 150°C to 200°C	60-180 Sec
Time maintained above 217°C	60-150 Sec
Peak Temperature	255-260°C
Time within 5°C of actual Peak	20-40 Sec
Ramp-Down Rate	6°C/Sec Max.
Time 25°C to Peak Temperature	8 min Max.

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[SIT8102AI-13-18E-25.00000T](#) [8N4Q001LG-1033CDI](#) [DSC8121CL5T](#) [DS1090U-2/V+T](#) [DS1090U-32+T](#) [DSC8121AM2](#) [DSC8001AL2](#)  
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