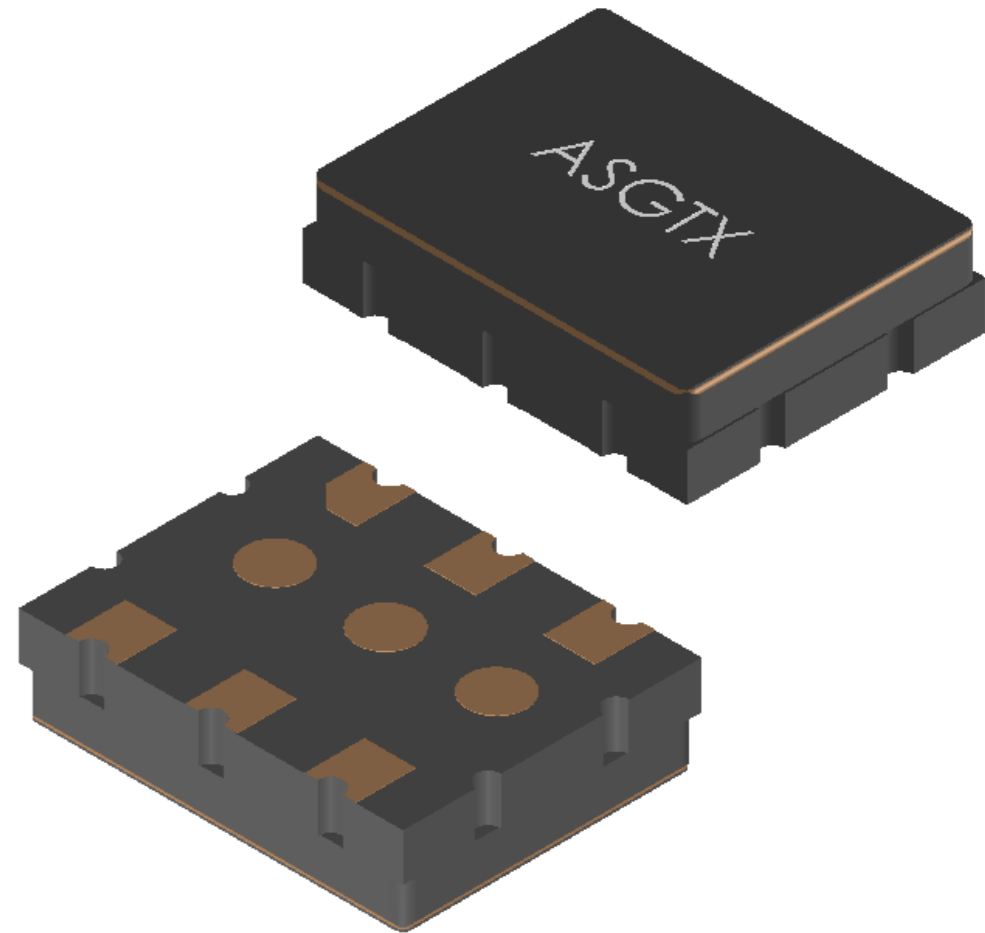
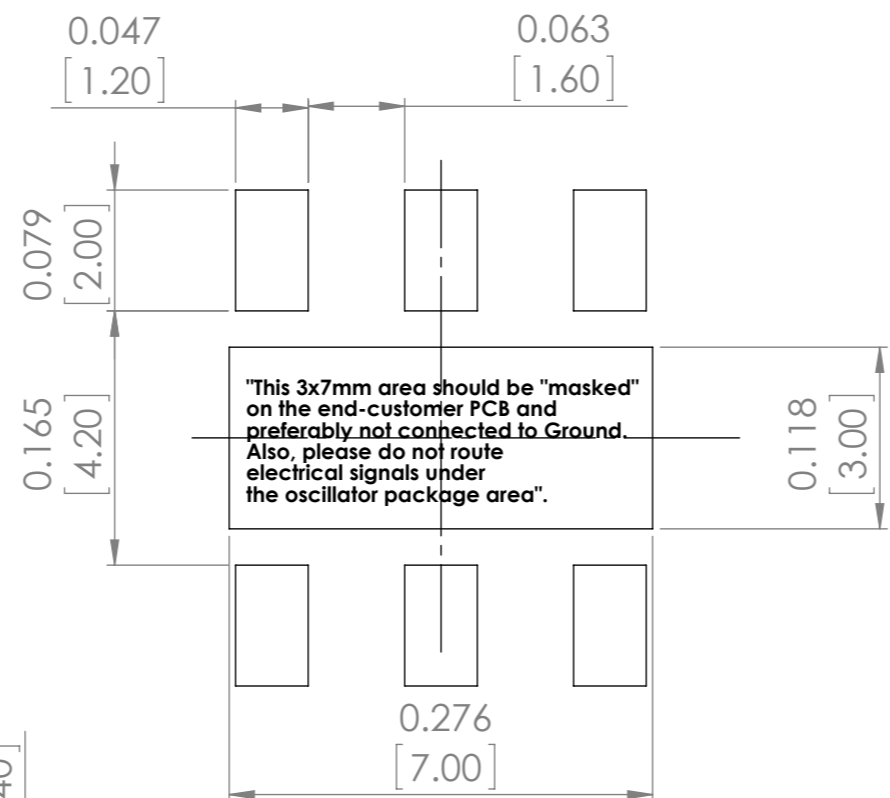



PIN #	SYMBOL	DESCRIPTION	COMMENT
1	OE	Output Enable	Active High, leave floating if not used
2	Vc	Control Voltage	0 ~ Vdd can be applied to pull frequency
3	GND	Ground	Connect to Analog Ground
4	OUT	Primary Output	LVDS/LVPECL Primary output
5	$\overline{\text{OUT}}$	Complimentary Output	LVDS/LVPECL Complimentary output
6	VDD	Bias Voltage	Apply +3.30V \pm 0.3V
	PROG, FSEL0 & FSEL1	Factory Configuration Pins	DONOT Connect, this area needs to be masked on customer PCB

Recommended land Pattern



UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MM SURFACE FINISH: TOLERANCES: LINEAR: ANGULAR:		FINISH:	DEBUR AND BREAK SHARP EDGES	DO NOT SCALE DRAWING	REVISION -
NAME	SIGNATURE	DATE		 30332 Esperanza, Rancho Santa margarita, California 92688 TITLE: - DWG NO. ASGTX SCALE: 8:1 SHEET 1 OF 1	
DRAWN SAAZVAT					
CHK'D XXXXXX					
APPV'D					
MFG					
Q.A			MATERIAL:		A3
			WEIGHT:		

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