

## REGULATORY COMPLIANCE

 <p><b>Lead Free</b> COMPLIANT</p>	 <p><b>EU RoHS</b> 2011/65 + 2015/863 COMPLIANT</p>	 <p><b>China RoHS</b> COMPLIANT</p>	 <p><b>REACH</b> SVHC COMPLIANT</p>	 <p><b>DRC</b> CONFLICT FREE</p>
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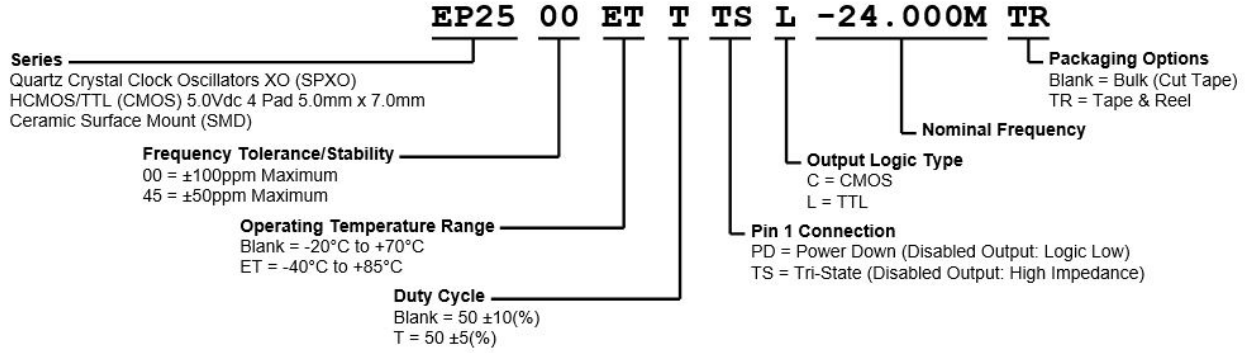
## ITEM DESCRIPTION

Quartz Crystal Clock Oscillators XO (SPXO) HCMOS/TTL (CMOS) 5.0Vdc 4 Pad 5.0mm x 7.0mm Ceramic Surface Mount (SMD)

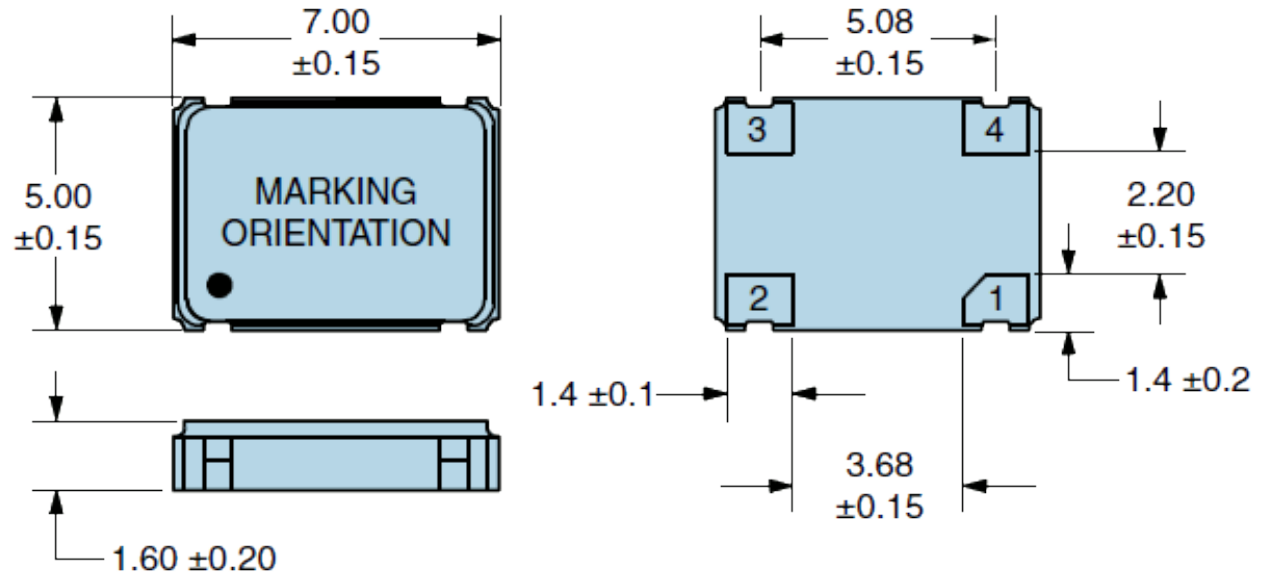
## ELECTRICAL SPECIFICATIONS

<b>Nominal Frequency</b>	1MHz to 125MHz
<b>Frequency Tolerance/Stability</b>	Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°C, Shock, and Vibration ±100ppm Maximum ±50ppm Maximum
<b>Aging at 25°C</b>	±5ppm/year Maximum
<b>Operating Temperature Range</b>	-20°C to +70°C -40°C to +85°C
<b>Supply Voltage</b>	5.0Vdc ±10%
<b>Input Current</b>	Unloaded 45mA Maximum
<b>Output Voltage Logic High (V<sub>OH</sub>)</b>	IOH = -16mA V <sub>DD</sub> -0.4Vdc Minimum at Output Logic Type of CMOS 2.4Vdc Minimum at Output Logic Type of TTL
<b>Output Voltage Logic Low (V<sub>OL</sub>)</b>	IOL = +16mA 0.4Vdc Maximum
<b>Rise/Fall Time</b>	4nSec Maximum (Measured at 20% to 80% of waveform) at Output Logic Type of CMOS 4nSec Maximum (Measured at 0.8Vdc to 2.0Vdc) at Output Logic Type of TTL
<b>Duty Cycle</b>	Measured at 1.4Vdc with TTL Load or 50% of waveform with HCMOS Load 50 ±10(%) 50 ±5(%) (Not available with TTL Output Logic Type over Nominal Frequency range of 27.000001MHz to 125MHz; Not available with CMOS Output Logic Type over Nominal Frequency range of 50.000001MHz to 125MHz)
<b>Load Drive Capability</b>	50pF HCMOS Load Maximum (over 1MHz to 50MHz at CMOS Output Logic Type) 15pF HCMOS Load Maximum (over 50.000001MHz to 125MHz at CMOS Output Logic Type) 10TTL Load Maximum over 1MHz to 40MHz at TTL Output Logic Type 5TTL Load Maximum over 40.000001MHz to 125MHz at TTL Output Logic Type
<b>Output Logic Type</b>	CMOS TTL
<b>Pin 1 Connection</b>	Power Down (Disabled Output: Logic Low) Tri-State (Disabled Output: High Impedance)
<b>Pin 1 Input Voltage (V<sub>IH</sub> and V<sub>IL</sub>)</b>	+2.0Vdc Minimum to enable output, +0.8Vdc Maximum to disable output, No Connect to enable output.
<b>Standby Current</b>	50µA Maximum (Pin 1 = Ground, Disabled Output: Logic Low)
<b>Disable Current</b>	30mA Maximum (Pin 1 = Ground, Disabled Output: High Impedance)
<b>Absolute Clock Jitter</b>	±250pSec Maximum, ±100pSec Typical over Nominal Frequency of 1MHz to 33MHz ±100pSec Maximum, ±50pSec Typical over Nominal Frequency of 33.000001MHz to 125MHz
<b>One Sigma Clock Period Jitter</b>	±50pSec Maximum over Nominal Frequency of 1MHz to 33MHz ±30pSec Maximum over Nominal Frequency of 33.000001MHz to 125MHz
<b>Start Up Time</b>	10mSec Maximum
<b>Storage Temperature Range</b>	-55°C to +125°C

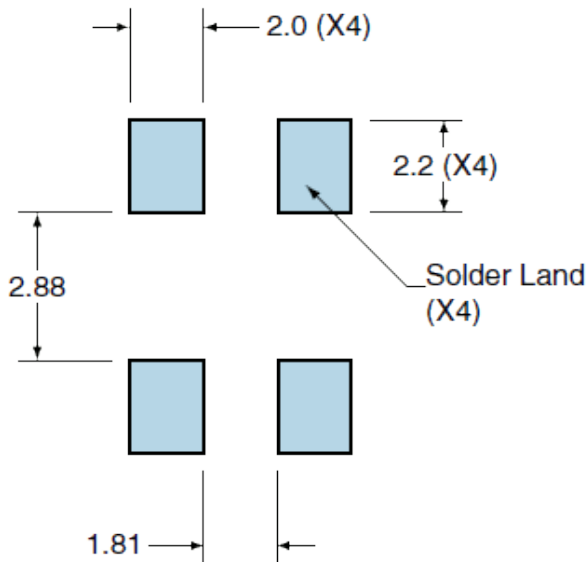
**PART NUMBERING GUIDE**



**MECHANICAL DIMENSIONS**



**SUGGESTED SOLDER PAD LAYOUT**

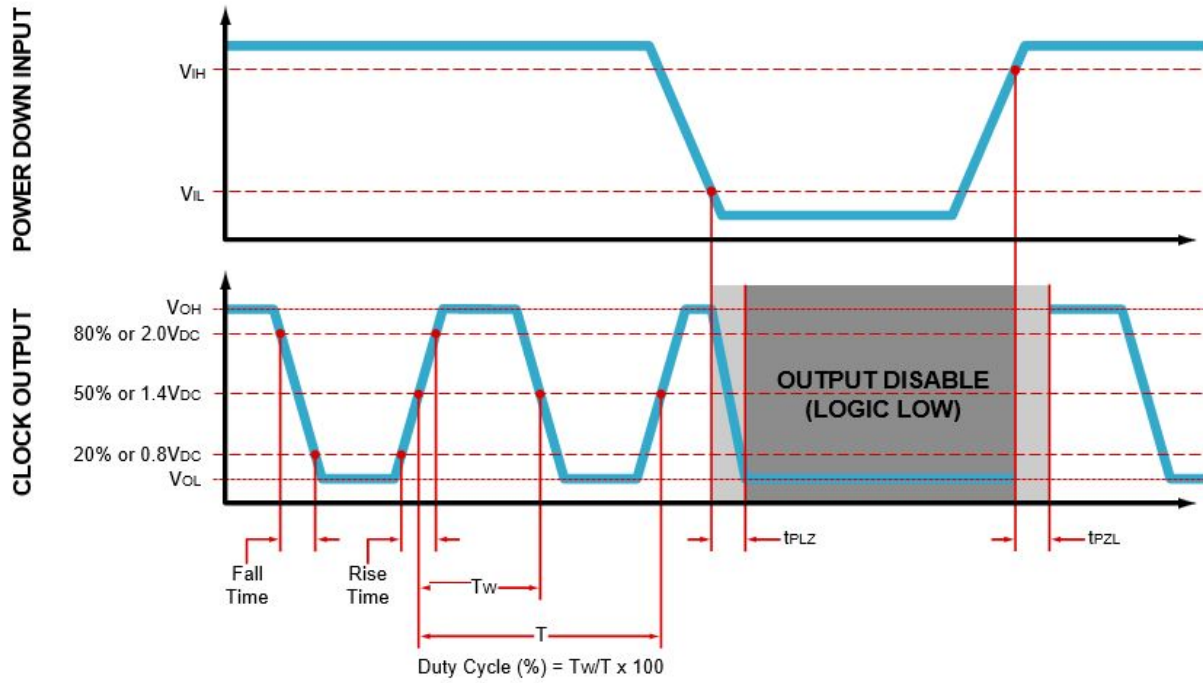


PIN	CONNECTION
1	Power Down Or Tri-State
2	Ground/Case Ground
3	Output
4	Supply Voltage

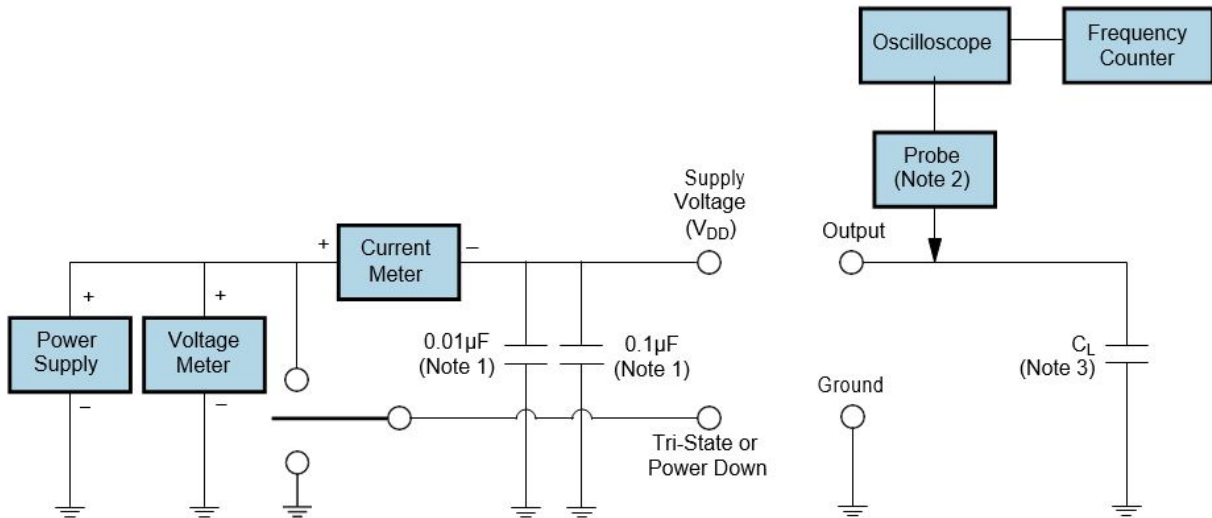
All Tolerances are  $\pm 0.1$

**All Dimensions in Millimeters**

OUTPUT WAVEFORM & TIMING DIAGRAM



TEST CIRCUIT FOR CMOS OUTPUT



**Note 1:** An external 0.01µF ceramic bypass capacitor in parallel with a 0.1µF high frequency ceramic bypass capacitor close (less Than 2mm) to the package ground and supply voltage pin is required.

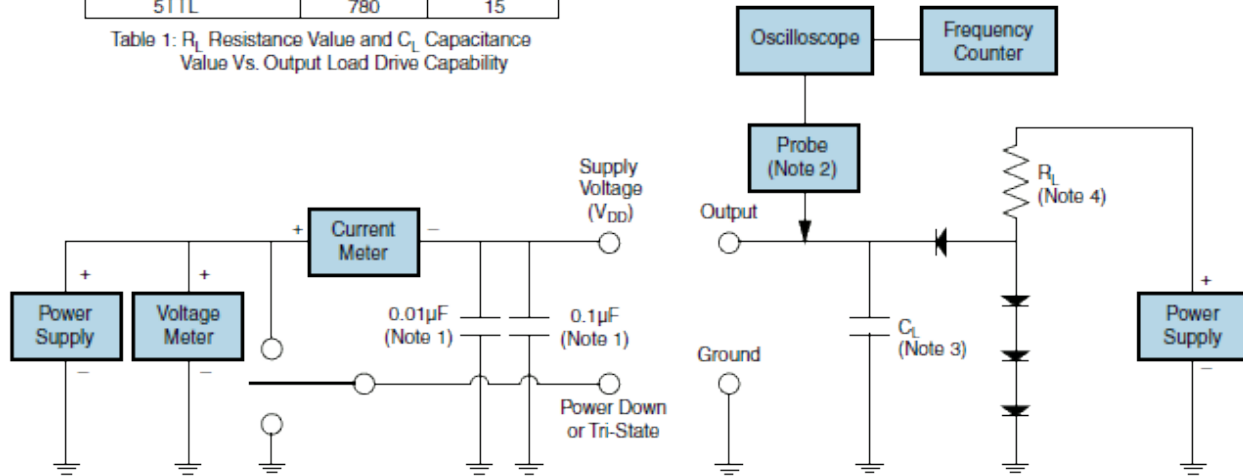
**Note 2:** A low input capacitance (<12pF), 10X Attenuation Factor, High Impedance (>10Mohms), and High bandwidth (>300MHz) Passive probe is recommended.

**Note 3:** Capacitance value C<sub>L</sub> includes sum of all probe and fixture capacitance. See applicable specification sheet for 'Load Drive Capability'.

TEST CIRCUIT FOR TTL OUTPUT

Output Load Drive Capability	$R_L$ Value (Ohms)	$C_L$ Value (pF)
10TTL	390	15
5TTL	780	15

Table 1:  $R_L$  Resistance Value and  $C_L$  Capacitance Value Vs. Output Load Drive Capability



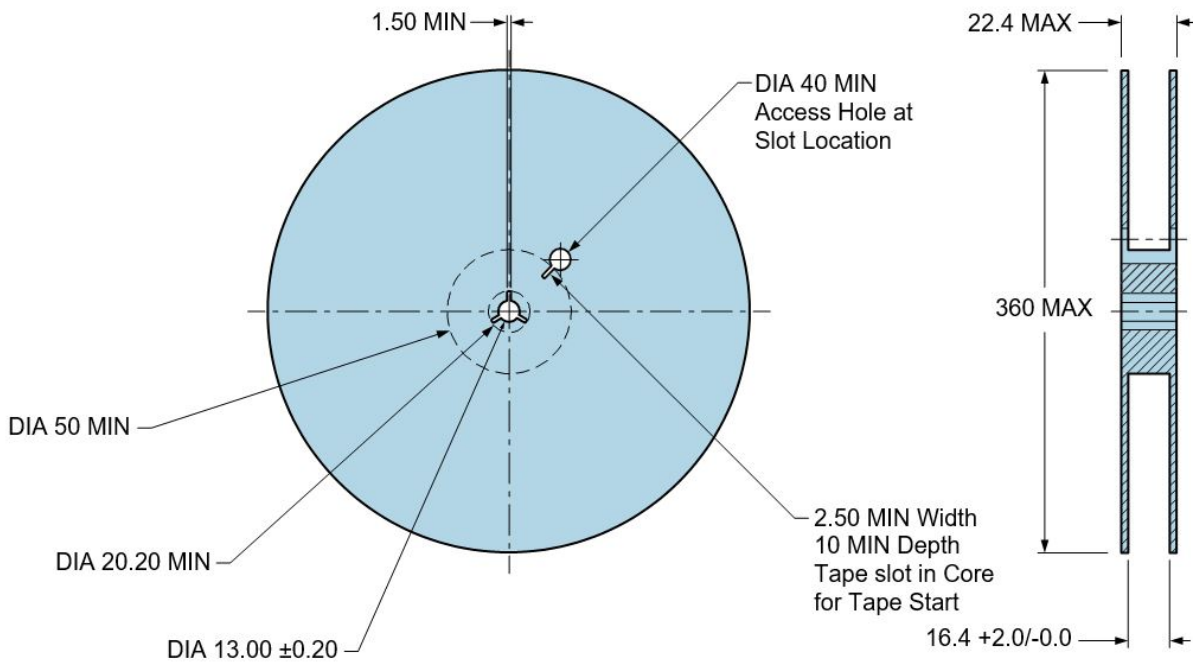
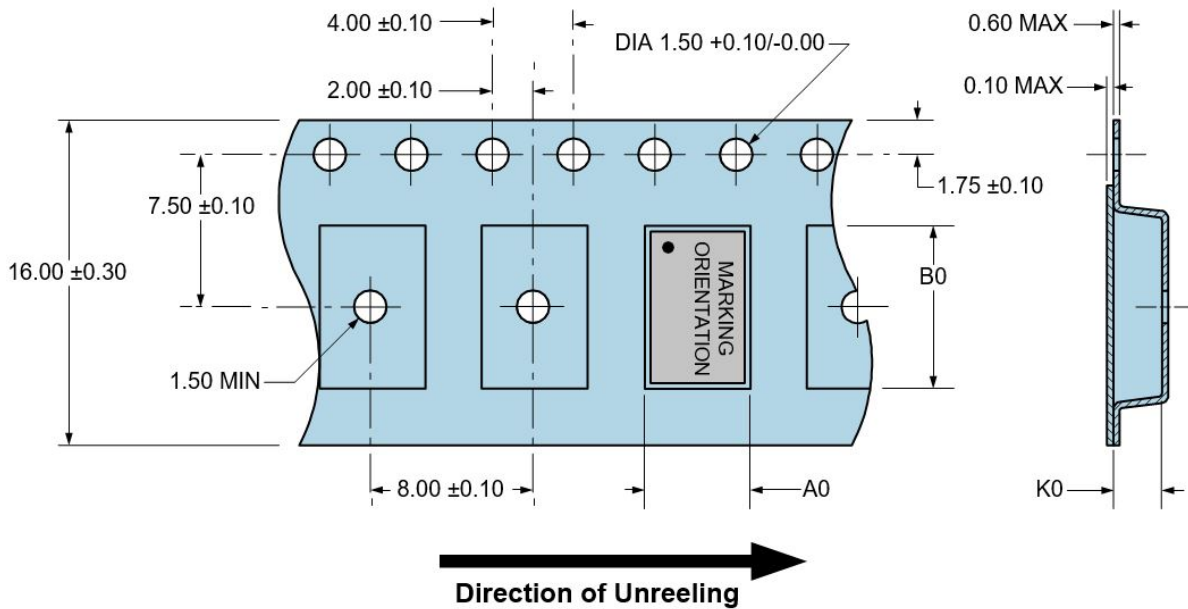
- Note 1:** An external 0.01µF ceramic bypass capacitor in parallel with a 0.1µF high frequency ceramic bypass capacitor close (less than 2mm) to the package ground and supply voltage pin is required.
- Note 2:** A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.
- Note 3:** Capacitance value CL includes sum of all probe and fixture capacitance.
- Note 4:** Resistance value RL is shown in Table 1. See applicable specification sheet for 'Load Drive Capability'.
- Note 5:** All diodes are MMBD7000, MMBD914, or equivalent.

**TAPE & REEL DIMENSIONS**

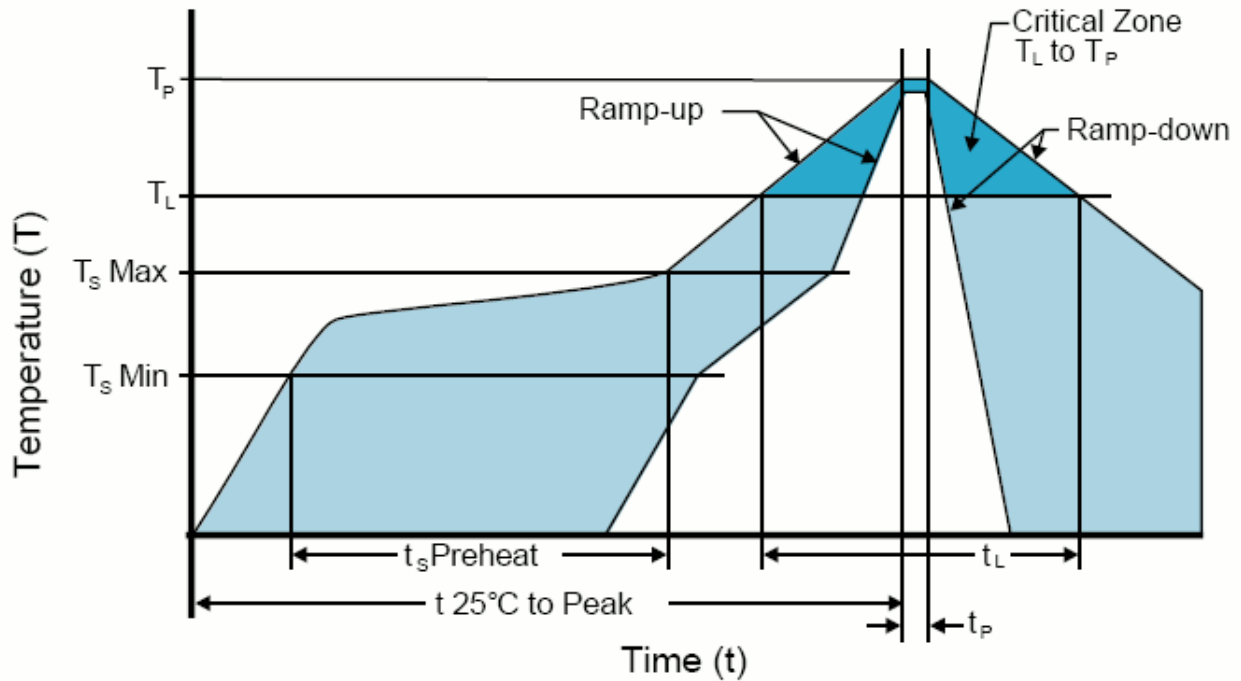
Quantity per Reel: 1,000 Units

All Dimensions in Millimeters

Compliant to EIA-481



**RECOMMENDED SOLDER REFLOW METHOD**



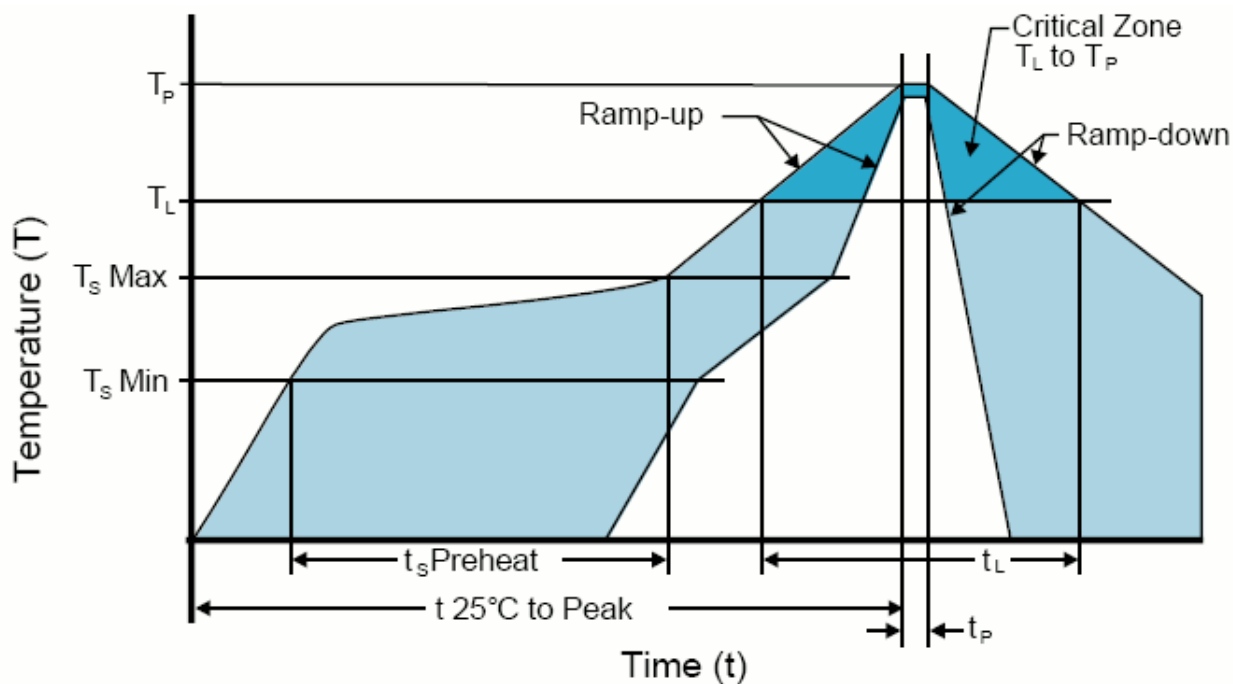
HIGH TEMPERATURE INFRARED/CONVECTION	
T <sub>S</sub> MAX to T <sub>L</sub> (Ramp-up Rate)	3°C/Second Maximum
<b>Preheat</b>	
- Temperature Minimum (T <sub>S</sub> MIN)	150°C
- Temperature Typical (T <sub>S</sub> TYP)	175°C
- Temperature Maximum(T <sub>S</sub> MAX)	200°C
- Time (t <sub>s</sub> MIN)	60 - 180 Seconds
Ramp-up Rate (T <sub>L</sub> to T <sub>P</sub> )	3°C/Second Maximum
<b>Time Maintained Above:</b>	
- Temperature (T <sub>L</sub> )	217°C
- Time (t <sub>L</sub> )	60 - 150 Seconds
Peak Temperature (T <sub>P</sub> )	260°C Maximum for 10 Seconds Maximum
Target Peak Temperature(T <sub>P</sub> Target)	250°C +0/-5°C
Time within 5°C of actual peak (t <sub>p</sub> )	20 - 40 Seconds
Ramp-down Rate	6°C/Second Maximum
Time 25°C to Peak Temperature (t)	8 Minutes Maximum
Moisture Sensitivity Level	Level 1
Additional Notes	Temperatures shown are applied to body of device.

**High Temperature Manual Soldering**

260°C Maximum for 5 Seconds Maximum, 2 times Maximum. (Temperatures shown are applied to body of device.)



RECOMMENDED SOLDER REFLOW METHOD



**LOW TEMPERATURE INFRARED/CONVECTION**

T <sub>S</sub> MAX to T <sub>L</sub> (Ramp-up Rate)	5°C/Second Maximum
<b>Preheat</b>	
- Temperature Minimum (T <sub>S</sub> MIN)	N/A
- Temperature Typical (T <sub>S</sub> TYP)	150°C
- Temperature Maximum(T <sub>S</sub> MAX)	N/A
- Time (t <sub>S</sub> MIN)	60 - 120 Seconds
Ramp-up Rate (T <sub>L</sub> to T <sub>P</sub> )	5°C/Second Maximum
<b>Time Maintained Above:</b>	
- Temperature (T <sub>L</sub> )	150°C
- Time (t <sub>L</sub> )	200 Seconds Maximum
Peak Temperature (T <sub>P</sub> )	240°C Maximum
Target Peak Temperature(T <sub>P</sub> Target)	240°C Maximum 2 Times/230°C Maximum 1Time
Time within 5°C of actual peak (t <sub>P</sub> )	10 Seconds Maximum 2 Times / 80 Seconds Maximum 1 Time
Ramp-down Rate	5°C/Second Maximum
Time 25°C to Peak Temperature (t)	N/A
Moisture Sensitivity Level	Level 1
Additional Notes	Temperatures shown are applied to body of device.

**Low Temperature Manual Soldering**

185°C Maximum for 10 Seconds Maximum, 2 times Maximum. (Temperatures shown are applied to body of device.)

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