# INTRODUCTION

PIERCE ANALYZER SYSTEM (PAS) ADVANCED BOARD CHARACTERIZATION SERVICE

Today's electronic designs include some form of timing device. Depending on the frequency accuracy requirements, some employ oscillators while others use off-the-shelf crystals in conjunction with the built-in oscillator circuit embedded in most microcontrollers and microprocessors. Due to their simple configuration and design, most embedded solutions use the Pierce Oscillator configuration integrated as part of the system on chip (SOC). The advantages of this solution include cost, size, and power compared to a stand-alone oscillator, while the key limitation is the proper matching of the quartz crystal with the on-board oscillator and feedback components.

The figure below outlines the oscillator block and the key components that influence the overall performance of the timing loop.
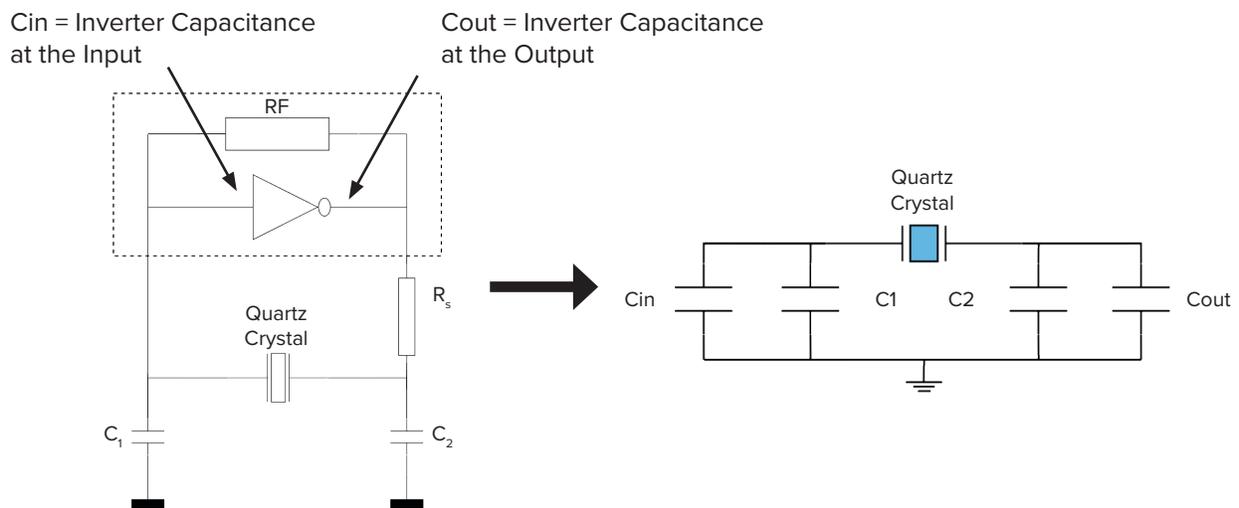
Effective Loaded Capacitance as seen by the crystal = CL

$$CL = \frac{(C_{in} + C_1)(C_2 + C_{out})}{C_{in} + C_1 + C_2 + C_{out}} + Board\ Strays$$

For example, let C1 = C2 = 27pF, Cin = 5pF, Cout = 10pF, Board Strays = 0.5pF.

$$CL = \frac{(5 + 27)(27 + 10)}{5 + 27 + 27 + 10} + 0.5 = 17.65\text{pF}$$

Therefore, specifying a crystal with 18.0 pF plating load capacitance would be the closest match for frequency accuracy.

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The reactive impedance (Xc) of the loop capacitors, in combination with the inverter amplifier's transconductance (gm), the current limiting resistor (Rs), and the presence or absence of an AGC circuit, determines the boundary condition of the oscillator loop design.

This boundary condition, commonly referred to as the safety factor (SF), is an important parameter to ensure that the product design has sufficient margin to accommodate part-to-part and lot-to-lot variations, as well as eliminating product performance uncertainty in production volume.
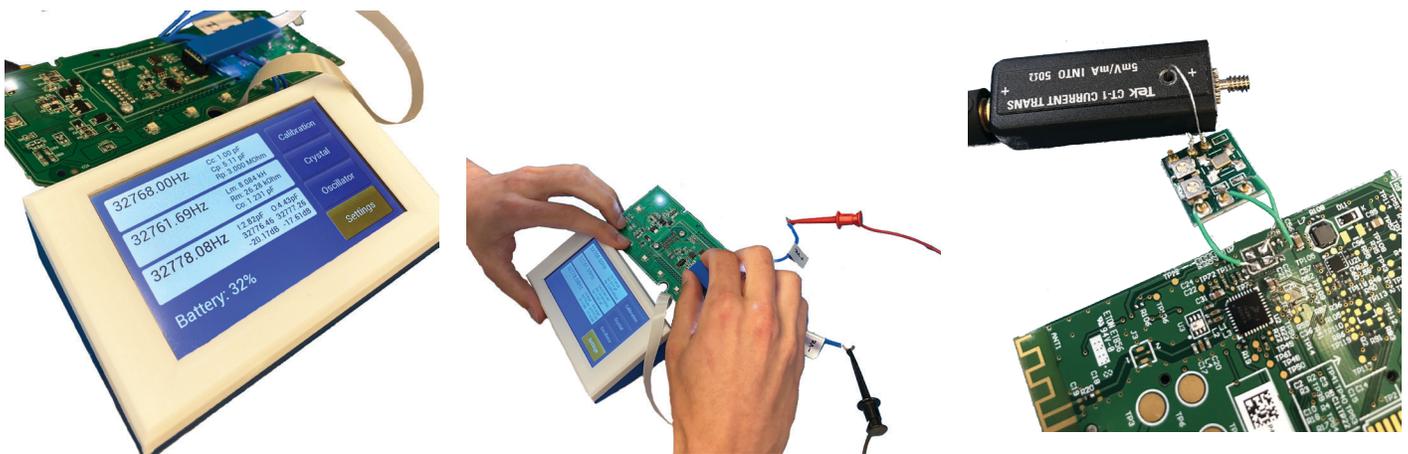
Historically, design engineers have optimized their circuit performance via trial and error, at the expense of significant investment in time. Further, to properly determine the oscillator loop dynamics, there is no other choice but to break the oscillator loop and make key measurements using specialized equipment such as a current probe.

Lastly, these measurements become increasingly sensitive if the timing loop is driven by a tuning fork (32.768kHz) crystal. These crystals are extremely sensitive to loading effects and extreme care and accuracy is essential to determine the in-circuit behavior of these components.

For instance, automotive, medical, and consumer electronics solutions typically utilize tuning fork crystals for their real-time-clocking (RTC) needs. If the selected SOC has an inadequate gain margin, there is a high probability that some percentage of these crystals will not properly start under adverse conditions, such as low operating temperature.

Another example would be a ZigBee based design which has a hard boundary condition of ±40 ppm relative to the carrier, for proper operation. If the oscillator loop is not optimized, most of the ±40 ppm can be consumed by tolerance alone potentially causing significant yield loss or timing error in the field.

In summary, a typical product launch requires a significant investment in capital and design resources. Making a very modest investment in characterizing the timing loop is a must-have to protect this investment, as well as mitigate the risk of field failures or warranty recalls.

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SOLUTION AND FEATURES
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SOLUTION
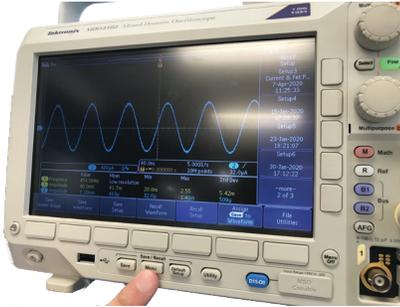
Abracon provides an accurate assessment of the oscillator loop dynamics to overcome these barriers. Abracon's Engineering Team developed a proprietary Pierce Analyzer System (PAS), which is designed to analyze both the stand-alone crystal, as well as the performance of the crystal in the customer's circuit.

FEATURES

- Circuit characterization, providing the best possible match between the quartz crystal, oscillator loop and associated feedback components
- Eliminates probability of oscillator start-up issues related to inadequate design or marginal component performance
- Eliminates production launch issues related to crystal oscillator-based timing circuits
- Solves for design margin uncertainty
- Provides a customer oscillator circuit overview in the form of a detailed report, providing a third-party assessment for the design history file or PPAP documentation.
- This report encompasses both the stand-alone crystal performance, as well as in-circuit closed loop oscillator performance.
- For additional information, please contact Abracon at: tech-support@abracon.com

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DELIVERABLES

PIERCE ANALYZER SYSTEM (PAS) ADVANCED BOARD CHARACTERIZATION SERVICE

DETAILED TEST REPORT INCLUDES:

- Project background information
- Abracon test instrumentation and equipment setup
- Customer project background information
- Customer PCB and crystal documentation
- Customer product photographs
- Quartz crystal electrical specifications
- Pierce oscillator design and theory of operation
- AC equivalent model characteristics
- Safety factor theory (non-AGC MHz oscillator loops only)
- Customer's existing oscillator design configuration performance data:
    - Stand-alone quartz crystal measurements
        - Series resonant (F_S) and parallel resonant (F_L) frequencies
        - Motional parameters (Rm, Cm, Lm)
        - Shunt capacitance (Co) and plating capacitance (Cpl)
    - Closed-loop oscillator circuit measurements (non-AGC MHz oscillator loops only)
        - Oscillator output frequency
        - Oscillator - crystal power dissipation
        - Oscillator - safety factor of oscillator loop
    - Closed-loop oscillator circuit (AGC 32.768kHz oscillator loops only)
        - Oscillator output frequency
        - Oscillator - crystal power dissipation
    - Maximum projections
        - Calculated worst-case drive level
        - Calculated worst-case safety factor of oscillator loop
- Abracon Engineering recommended oscillator design configuration
- Abracon Engineering review and conclusion

ORDERING INFORMATION

- EXPEDITED-PAS-SVC
- STANDARD-PAS-SVC

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