ACT4523A

Wide Input Sensorless CC/CV Step-Down DC/DC Converter

FEATURES

- 40V Input Voltage Surge
- 30V Steady State Operation
- Up to 3.5A Output Current
- Output Voltage up to 12V
- 250kHz Switching Frequency
- 91% Efficiency (Vout = 5V@3.5A at Vin = 12V)
- Patented ActiveCC Sensorless Constant Current Control
  - Integrated Current Control Improves Efficiency, Lowers Cost, and Reduces Component Count
- Resistor Programmable
  - Current Limit from 1.5A to 4.0A
  - Patented Cable Compensation from 0 to 0.25Ω
- ±6.5% CC Accuracy
  - Compensation of Input/Output Voltage Change
  - Temperature Compensation
  - Independent of inductance and Inductor DCR
- 2% Feedback Voltage Accuracy
- Advanced Feature Set
  - Integrated Soft Start
  - Thermal Shutdown
  - Secondary Cycle-by-Cycle Current Limit
  - Protection Against Shorted ISET Pin
- SOP-8EP Package

APPLICATIONS

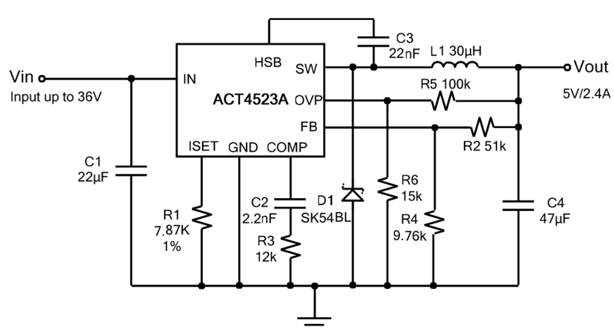
- Car Charger / Adaptor
- Rechargeable Portable Devices
- General-Purpose CC/CV Supply

GENERAL DESCRIPTION

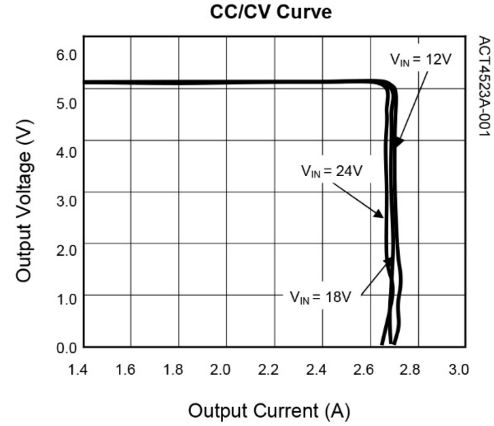
ACT4523A is a wide input voltage, high efficiency ActiveCC step-down DC/DC converter that operates in either CV (Constant Output Voltage) mode or CC (Constant Output Current) mode. ACT4523A provides up to 3.5A output current at 250kHz switching frequency.

ActiveCC is a patented control scheme to achieve highest accuracy with sensorless constant current control. ActiveCC eliminates the expensive, high accuracy current sense resistor, making it ideal for battery charging applications and adaptors with accurate current limit. The ACT4523A achieves higher efficiency than traditional constant current switching regulators by eliminating its associated power loss on the sensing resistor. ACT4523A provides OVP pin for output over voltage protection.

Protection features include cycle-by-cycle current limit, thermal shutdown, and frequency foldback at short circuit. The devices are available in a SOP-8EP package and require very few external devices for operation.



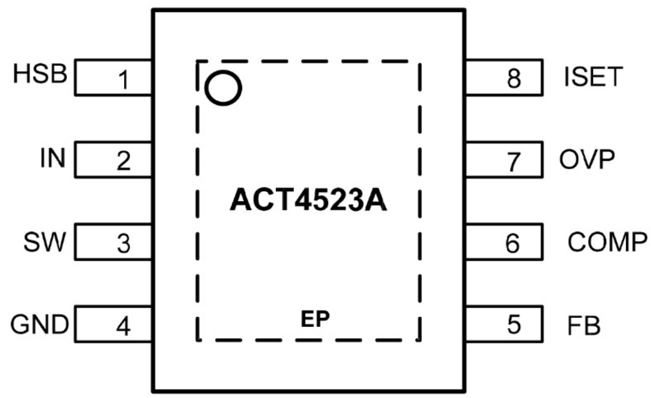
CC/CV Curve



ORDERING INFORMATION

PART NUMBER	OPERATION TEMPERATURE RANGE	PACKAGE	PINS	PACKING
ACT4523AYH-T	-40°C to 85°C	SOP-8EP	8	TAPE & REEL

PIN CONFIGURATION



SOP-8EP

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	HSB	High Side Bias Pin. This provides power to the internal high-side MOSFET gate driver. Connect a 22nF capacitor from HSB pin to SW pin.
2	IN	Power Supply Input. Bypass this pin with a 10μF ceramic capacitor to GND, placed as close to the IC as possible.
3	SW	Power Switching Output to External Inductor.
4	GND	Ground. Connect this pin to a large PCB copper area for best heat dissipation. Return FB, COMP, and ISET to this GND, and connect this GND to power GND at a single point for best noise immunity.
5	FB	Feedback Input. The voltage at this pin is regulated to 0.808V. Connect to the resistor divider between output and GND to set the output voltage.
6	COMP	Error Amplifier Output. This pin is used to compensate the converter.
7	OVP	OVP input. If the voltage at this pin exceeds 0.8V, the IC shuts down high-side switch.
8	ISET	Output Current Setting Pin. Connect a resistor from ISET to GND to program the output current.
	Exposed Pad	Heat Dissipation Pad. Connect this exposed pad to large ground copper area with copper and vias.

ABSOLUTE MAXIMUM RATING①

PARAMETER	VALUE	UNIT
IN to GND	-0.3 to 40	V
SW to GND	-1 to V_{IN} + 1	V
HSB to GND	V_{SW} - 0.3 to V_{SW} + 7	V
FB, ISET, COMP to GND	-0.3 to + 6	V
Junction to Ambient Thermal Resistance	46	°C/W
Operating Junction Temperature	-40 to 150	°C
Storage Junction Temperature	-55 to 150	°C
Lead Temperature (Soldering 10 sec.)	300	°C

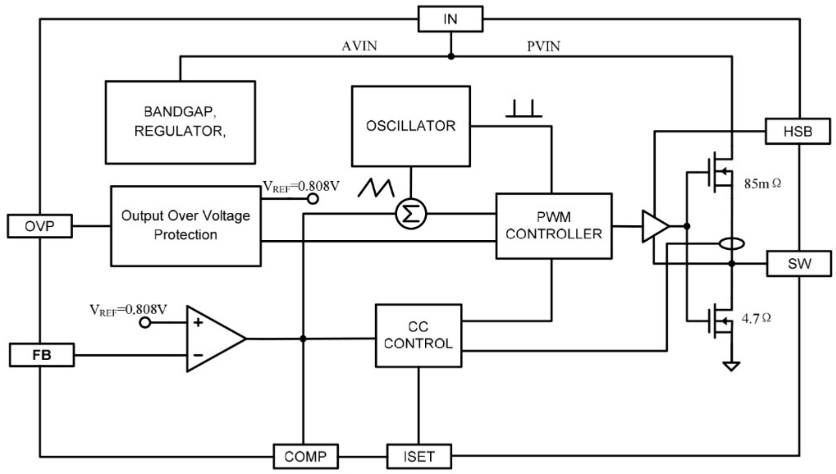
①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

ELECTRICAL CHARACTERSTICS

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input Voltage		10		36	V
Input Voltage Surge				40	V
V_{IN} UVLO Turn-On Voltage	Input Voltage Rising	9.0	9.4	9.7	V
V_{IN} UVLO Hysteresis	Input Voltage Falling		1.1		V
Standby Supply Current	V_{FB} = 1V		0.9	1.4	mA
Feedback Voltage		792	808	824	mV
Internal Soft-Start Time			400		µs
Error Amplifier Transconductance	V_{FB} = V_{COMP} = 0.8V, ΔI_{COMP} = ± 10µA		650		µA/V
Error Amplifier DC Gain			4000		V/V
Switching Frequency	V_{FB} = 0.808V		250		kHz
Foldback Switching Frequency	V_{FB} = 0V		36		kHz
Maximum Duty Cycle			85		%
Minimum On-Time			190		ns
COMP to Current Limit Transconductance	V_{COMP} = 1.2V		3.9		A/V
Secondary Cycle-by-Cycle Current Limit	Duty = 0.5		5.2		A
Slope Compensation	Duty = D_{MAX}		1.4		A
ISET Voltage			1.0		V
ISET to IOUT DC Room Temp Current Gain	IOUT / ISET, R_{ISET} = 7.87 kΩ		20000		A/A
CC Controller DC Accuracy	R_{ISET} = 7.87kΩ, V_{OUT} = 4.0V		2650		mA
OVP pin Voltage	OVP Pin Rising		0.8		V
High-Side Switch ON-Resistance			85		mΩ
SW Off Leakage Current	V_{IN} = V_{SW} = 0V		1	10	µA
Thermal Shutdown Temperature	Temperature Rising		155		°C
Thermal Shutdown Temperature Hysteresis	Temperature Falling		25		°C

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

CV/CC Loop Regulation

As seen in *Functional Block Diagram*, the ACT4523A is a peak current mode pulse width modulation (PWM) converter with CC and CV control. The converter operates as follows:

A switching cycle starts when the rising edge of the Oscillator clock output causes the High-Side Power Switch to turn on and the Low-Side Power Switch to turn off. With the SW side of the inductor now connected to IN, the inductor current ramps up to store energy in the magnetic field. The inductor current level is measured by the Current Sense Amplifier and added to the Oscillator ramp signal. If the resulting summation is higher than the COMP voltage, the output of the PWM Comparator goes high. When this happens or when Oscillator clock output goes low, the High-Side Power Switch turns off.

At this point, the SW side of the inductor swings to a diode voltage below ground, causing the inductor current to decrease and magnetic energy to be transferred to output. This state continues until the cycle starts again. The High-Side Power Switch is driven by logic using HSB as the positive rail. This pin is charged to V_{SW} + 5V when the Low-Side Power Switch turns on. The COMP voltage is the integration of the error between FB input and the internal 0.808V reference. If FB is lower than the reference voltage, COMP tends to go higher to increase current to the output. Output current will increase until it reaches the CC limit set by the ISET resistor. At this point, the device will transition from regulating output voltage to regulating output current, and the output voltage will drop with increasing load.

The Oscillator normally switches at 250kHz. However, if FB voltage is less than 0.6V, then the switching frequency decreases until it reaches a typical value of 36kHz at V_{FB} = 0.15V.

Over Voltage Protection

The ACT4523A has an OVP pin. If the voltage at this pin exceeds 0.8V, the IC shuts down high side switch.

Thermal Shutdown

The ACT4523A disables switching when its junction temperature exceeds 155°C and resumes when the temperature has dropped by 25°C.

APPLICATIONS INFORMATION

Output Voltage Setting

Figure 1:
Output Voltage Setting

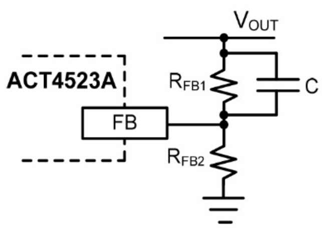


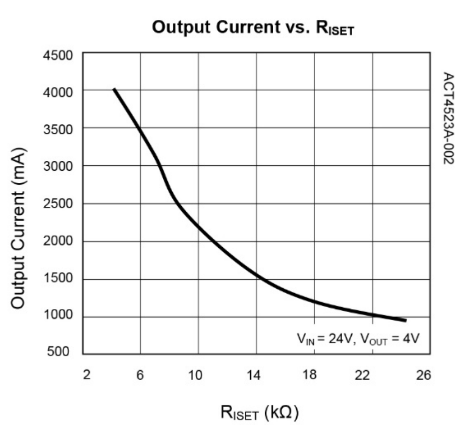
Figure 1 shows the connection for setting the output voltage. Select the proper ratio of the two feedback resistors R_{FB1} and R_{FB2} based on the output voltage. Adding a capacitor in parallel with R_{FB1} helps the system stability. Typically, use $R_{FB2} \approx 10k\Omega$ and determine $_{RFB1}$ from the following equation:

$$R_{FB1} = R_{FB2}\left(\frac{V_{OUT}}{0.808\ V} - 1\right) \quad (1)$$

CC Current Setting

ACT4523A constant current value is set by a resistor connected between the ISET pin and GND. The CC output current is linearly proportional to the current flowing out of the ISET pin. The voltage at ISET is roughly 1.1V and the current gain from ISET to output is roughly 21000 (21mA/1µA). To determine the proper resistor for a desired current, please refer to Figure 2 below

Figure 2:
Curve for Programming Output CC Current



Inductor Selection

The inductor maintains a continuous current to the output load. This inductor current has a ripple that is dependent on the inductance value:

Higher inductance reduces the peak-to-peak ripple current. The trade off for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general, select an inductance value L based on ripple current requirement:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN}\ f_{SW}\ I_{LOADMAX}\ K_{RIPPLE}} \quad (2)$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_{SW} is the switching frequency, $I_{LOADMAX}$ is the maximum load current, and K_{RIPPLE} is the ripple factor. Typically, choose K_{RIPPLE} = 30% to correspond to the peak-to-peak ripple current being 30% of the maximum load current.

With a selected inductor value the peak-to-peak inductor current is estimated as:

$$I_{LPK-PK} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{L\ \times\ V_{IN} \times f_{SW}} \quad (3)$$

The peak inductor current is estimated as:

$$I_{LPK} = I_{LOADMAX} + \frac{1}{2}\ I_{LPK-PK} \quad (4)$$

The selected inductor should not saturate at I_{LPK}. The maximum output current is calculated as:

$$I_{OUTMAX} = I_{LIM} - \frac{1}{2}\ I_{LPK-PK} \quad (5)$$

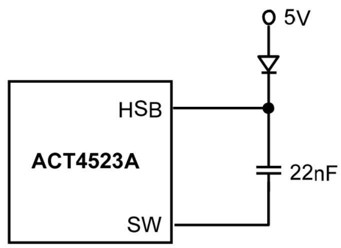
L_{LIM} is the internal current limit, which is typically 4.5A, as shown in Electrical Characteristics Table.

External High Voltage Bias Diode

It is recommended that an external High Voltage Bias diode be added when the system has a 5V fixed input or the power supply generates a 5V output. This helps improve the efficiency of the regulator. The High Voltage Bias diode can be a low cost one such as IN4148 or BAT54

APPLICATIONS INFORMATION CONT'D

Figure 3:
External High Voltage Bias Diode



This diode is also recommended for high duty cycle operation and high output voltage applications.

Input Capacitor

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.

The input capacitance needs to be higher than 10µF. The best choice is the ceramic type, however, low ESR tantalum or electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. The input capacitor should be placed close to the IN and G pins of the IC, with the shortest traces possible. In the case of tantalum or electrolytic types, they can be further away if a small parallel 0.1µF ceramic capacitor is placed right next to the IC.

Output Capacitor

The output capacitor also needs to have low ESR to keep low output voltage ripple. The output ripple voltage is:

$$V_{RIPPLE} = I_{OUTMAX}\, K_{RIPPLE}\, R_{ESR} + \frac{V_{IN}}{28 \times {f_{SW}}^2 L C_{OUT}} \qquad (6)$$

Where I_{OUTMAX} is the maximum output current, K_{RIPPLE} is the ripple factor, R_{ESR} is the ESR of the output capacitor, f_{SW} is the switching frequency, L is the inductor value, and C_{OUT} is the output capacitance. In the case of ceramic output capacitors, R_{ESR} is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used for ceramic type. In the case of tantalum or electrolytic capacitors, the ripple is dominated by R_{ESR} multiplied by the ripple current. In that case, the output capacitor is chosen to have sufficiently low ESR.

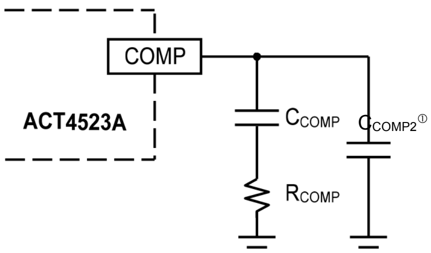
For ceramic output capacitor, typically choose a capacitance of about 22µF. For tantalum or electrolytic capacitors, choose a capacitor with less than 50mΩ ESR.

Rectifier Diode

Use a Schottky diode as the rectifier to conduct current when the High-Side Power Switch is off. The Schottky diode must have current rating higher than the maximum output current and a reverse voltage rating higher than the maximum input voltage.

STABILITY COMPENSATION

Figure 4:
Stability Compensation



①: C_{COMP2} is needed only for high ESR output capacitor

The feedback loop of the IC is stabilized by the components at the COMP pin, as shown in Figure 4. The DC loop gain of the system is determined by the following equation:

$$A_{VDC} = \frac{0.808\,V}{I_{OUT}} A_{VEA}\, G_{COMP} \tag{7}$$

The dominant pole P1 is due to C_{COMP}:

$$f_{P1} = \frac{G_{EA}}{2\pi\, A_{VEA}\, C_{COMP}} \tag{8}$$

The second pole P2 is the output pole:

$$f_{P2} = \frac{I_{OUT}}{2\pi\, V_{OUT}\, C_{OUT}} \tag{9}$$

The first zero Z1 is due to R_{COMP} and C_{COMP}:

$$f_{Z1} = \frac{1}{2\pi\, R_{COMP}\, C_{COMP}} \tag{10}$$

And finally, the third pole is due to R_{COMP} and C_{COMP2} (if C_{COMP2} is used):

$$f_{P3} = \frac{1}{2\pi\, R_{COMP}\, C_{COMP2}} \tag{11}$$

The following steps should be used to compensate the IC:

STEP 1. Set the cross over frequency at 1/10 of the switching frequency via R_{COMP}:

$$R_{COMP} = \frac{2\pi\, V_{OUT}\, C_{OUT}\, f_{SW}}{10\, G_{EA}\, G_{COMP} \times 0.808\,V} = 2.75\; x\; 10^{8}\, V_{OUT}\, C_{OUT} \quad (\Omega) \tag{12}$$

STEP 2. Set the zero f_{Z1} at 1/4 of the cross over frequency. If R_{COMP} is less than 15kΩ, the equation for C_{COMP} is:

$$C_{COMP} = \frac{1.8 \times 10^{-5}}{R_{COMP}} \quad (F) \tag{13}$$

If R_{COMP} is limited to 15kΩ, then the actual cross over frequency is 6.58 / ($V_{OUT}C_{OUT}$). Therefore:

$$C_{COMP} = 1.2 \times 10^{-5}\, V_{OUT}\, C_{OUT} \quad (F) \tag{14}$$

STEP 3. If the output capacitor's ESR is high enough to cause a zero at lower than 4 times the cross over frequency, an additional compensation capacitor C_{COMP2} is required. The condition for using C_{COMP2} is:

$$R_{ESROUT} \geq Min\left(\frac{1.1 \times 10^{-6}}{C_{OUT}}, 0.012\, V_{OUT}\right) \quad (\Omega) \tag{15}$$

And the proper value for C_{COMP2} is:

$$C_{COMP2} = \frac{C_{OUT}\, R_{ESRCOUT}}{R_{COMP}} \tag{16}$$

Though C_{COMP2} is unnecessary when the output capacitor has sufficiently low ESR, a small value C_{COMP2} such as 100pF may improve stability against PCB layout parasitic effects.

Table 1 shows some calculated results based on the compensation method above.

Table 1:
Typical Compensation for Different Output Voltages and Output Capacitors

V_{OUT}	C_{OUT}	R_{COMP}	C_{COMP}	C_{COMP2}①
2.5V	47µF Ceramic CAP	5.6kΩ	2.2nF	None
3.3V	47µF Ceramic CAP	6.2kΩ	2.2nF	None
5V	47µF Ceramic CAP	12kΩ	2.2nF	None
2.5V	220µF/10V/30mΩ	20kΩ	2.2nF	47pF
3.3V	220µF/10V/30mΩ	20kΩ	2.2nF	47pF
5V	220µF/10V/30mΩ	20kΩ	2.2nF	47pF

①: C_{COMP2} is needed for high ESR output capacitor.
C_{COMP2} ≤ 47pF is recommended.

STABILITY COMPENSATION CONT'D

CC Loop Stability

The constant-current control loop is internally compensated over the 1500mA-3000mA output range. No additional external compensation is required to stabilize the CC current.

Output Cable Resistance Compensation

To compensate for resistive voltage drop across the charger's output cable, the ACT4523A integrates a simple, user-programmable cable voltage drop compensation using the impedance at the FB pin. Use the curve in Figure 5 to choose the proper feedback resistance values for cable compensation. R_{FB1} is the high side resistor of voltage divider.

In the case of high R_{FB1} used, the frequency compensation on needs to be adjusted correspondingly. As show in Figure 6, adding a capacitor in paralleled with R_{FB1} or increasing the compensation capacitance at COMP pin helps the system stability.

Figure 5:

Cable Compensation at Various Resistor Divider Values

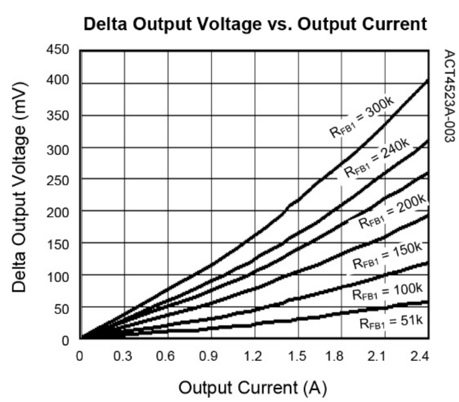
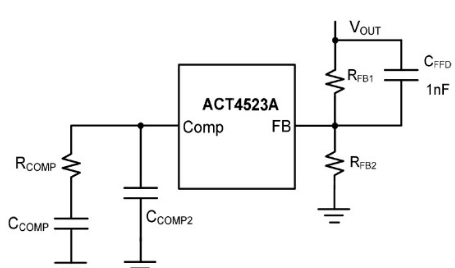


Figure 6:

Frequency Compensation for High R_{FB1}



PC Board Layout Guidance

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

1) Arrange the power components to reduce the AC loop size consisting of C_{IN}, IN pin, SW pin and the schottky diode.
2) Place input decoupling ceramic capacitor C_{IN} as close to IN pin as possible. C_{IN} is connected power GND with vias or short and wide path.
3) Return FB, COMP and ISET to signal GND pin, and connect the signal GND to power GND at a single point for best noise immunity. Connect exposed pad to power ground copper area with copper and vias.
4) Use copper plane for power GND for best heat dissipation and noise immunity.
5) Place feedback resistor close to FB pin.
6) Use short trace connecting HSB-C_{HSB}-SW loop

Figure 7 shows an example of PCB layout.

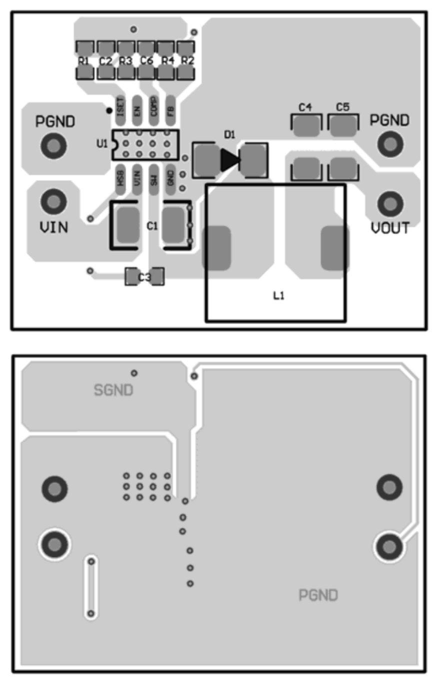


Figure 7: PCB Layout

Figure 8 gives one typical car charger application schematics and associated BOM list.

Figure 8:
Typical Application Circuit for 5V/2.4A Car Charger

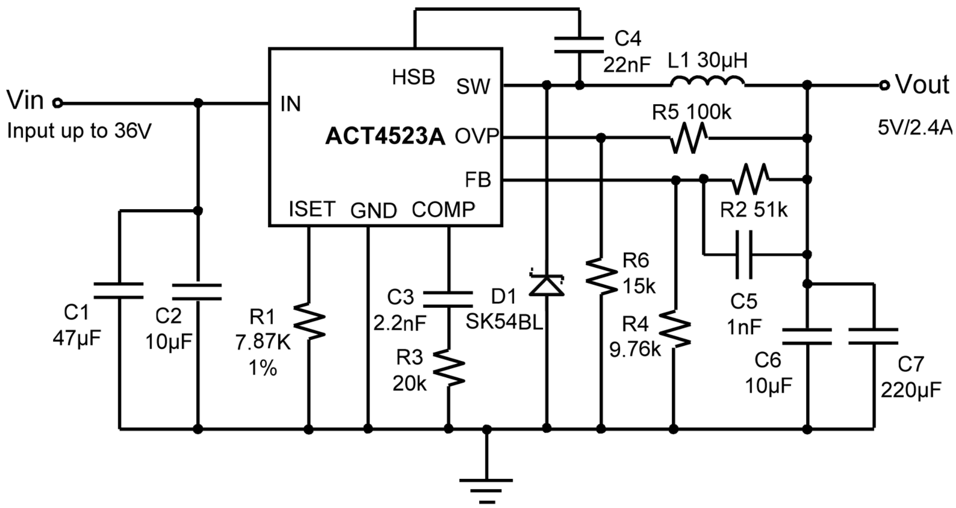
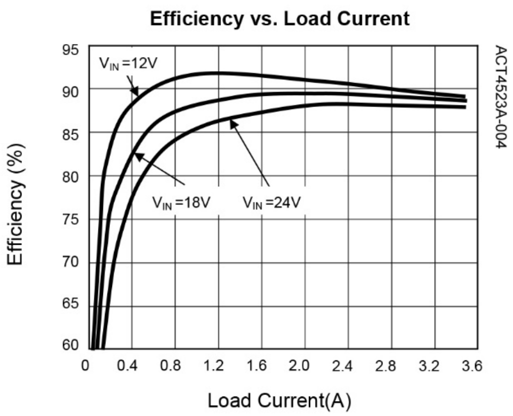


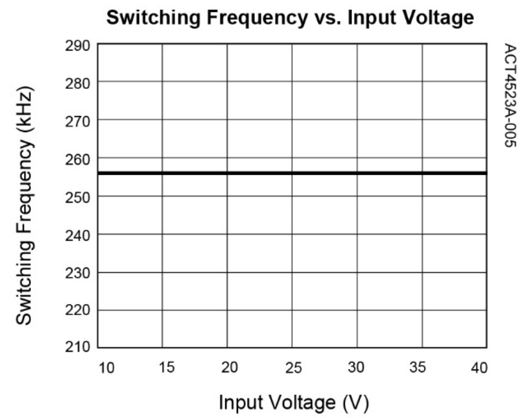
Table 2:
BOM List for 5V/2.4A Car Charger

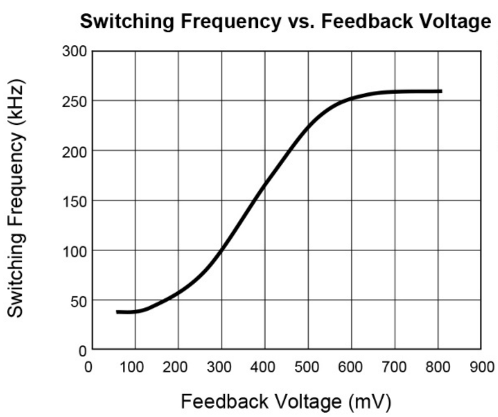
ITEM	REFERENCE	DESCRIPTION	MANUFACTURER	QTY
1	U1	IC, ACT4523AYH, SOP-8EP	Qorvo	1
2	C1	Capacitor, Electrolytic, 47µF/50V, 6.3x7mm	Murata, TDK	1
3	C2	Capacitor, Ceramic, 10µF/50V, 1206, SMD	Murata, TDK	1
4	C3	Capacitor, Ceramic, 2.2nF/6.3V, 0603, SMD	Murata, TDK	1
5	C4	Capacitor, Ceramic, 22nF/50V, 1206, SMD	Murata, TDK	1
6	C5	Capacitor, Ceramic, 1nF/10V, 0603, SMD	Murata, TDK	1
7	C6	Capacitor, Ceramic, 10uF/10V, 0603, SMD	Murata, TDK	1
8	C7	Capacitor, Electrolytic, 220uF/10V, 6.3x7mm	Murata, TDK	1
9	L1	Inductor, 30µH, 5A, 20%, SMD	Tyco Electronics	1
10	D1	Diode, Schottky, 40V/5A, SK54BL	Diodes	1
11	R1	Chip Resistor, 7.87kΩ, 0603, 1%	Murata, TDK	1
12	R2	Chip Resistor, 51kΩ, 0603, 1%	Murata, TDK	1
13	R3	Chip Resistor, 20kΩ, 0603, 5%	Murata, TDK	1
14	R4	Chip Resistor, 9.76kΩ, 0603, 1%	Murata, TDK	1
15	R5	Chip Resistor, 100kΩ, 0603, 1%	Murata, TDK	1
16	R6	Chip Resistor, 15kΩ, 0603, 1%	Murata, TDK	1

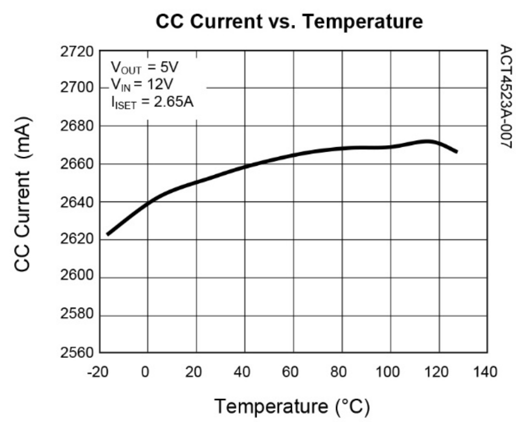
TYPICAL PERFORMANCE CHARACTERISTICS

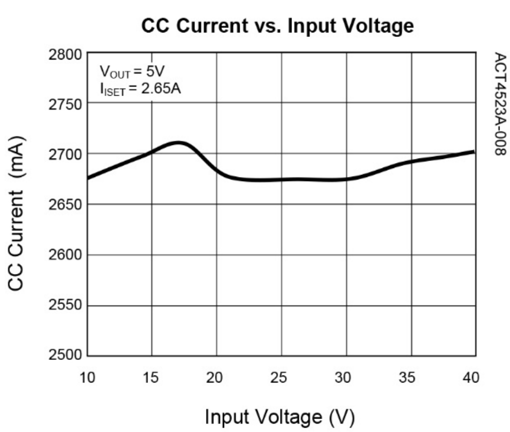
(Schematic as show in Figure 8, Ta = 25°C, unless otherwise specified)

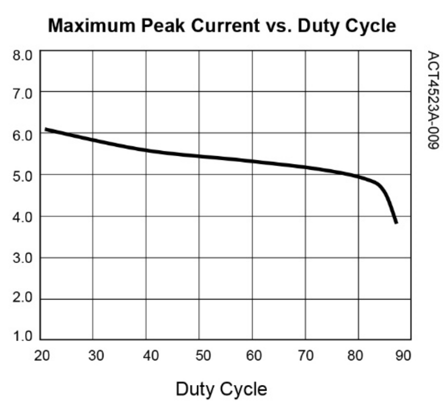








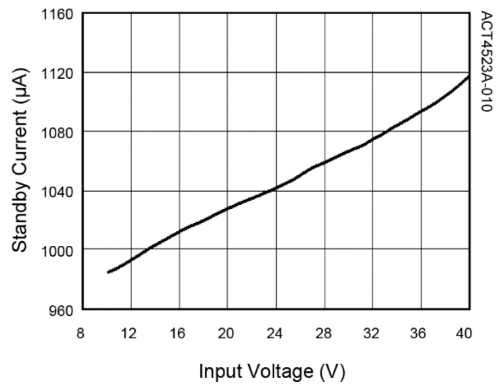




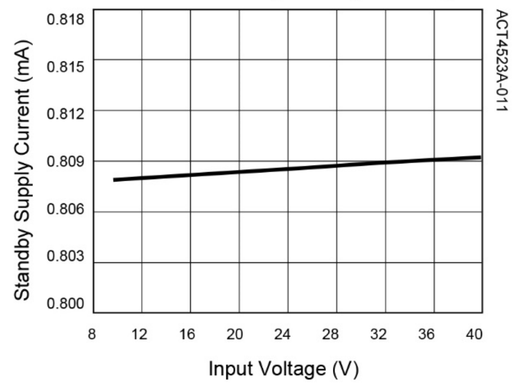
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(Schematic as show in Figure 8, Ta = 25°C, unless otherwise specified)

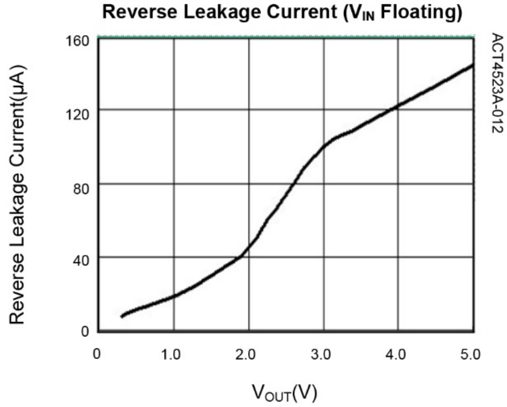
Standby Current vs. Input Voltage (FB=1V)



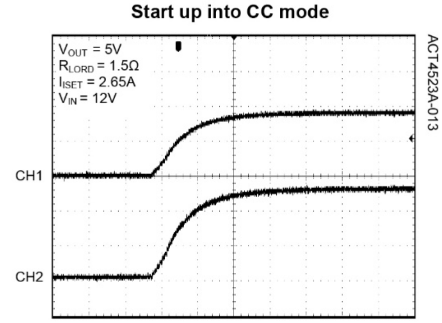
Feedback Voltage vs. Input Voltage



Reverse Leakage Current (V_{IN} Floating)

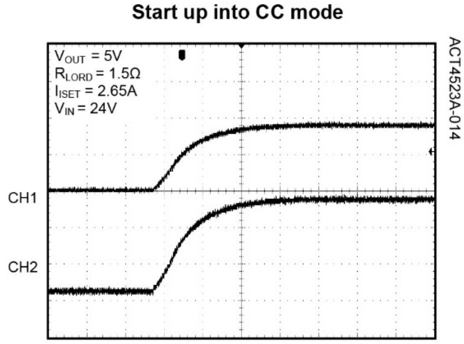


Start up into CC mode



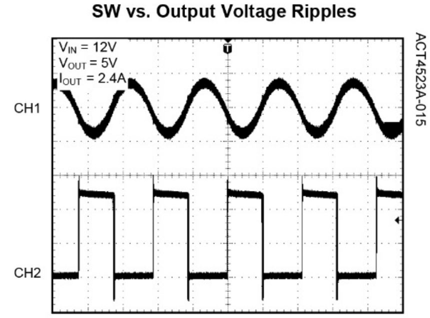
CH1: V_{OUT}, 2V/div
CH2: I_{OUT}, 1A/div
TIME: 400µs/div

Start up into CC mode



CH1: V_{OUT}, 2V/div
CH2: I_{OUT}, 1A/div
TIME: 400µs/div

SW vs. Output Voltage Ripples

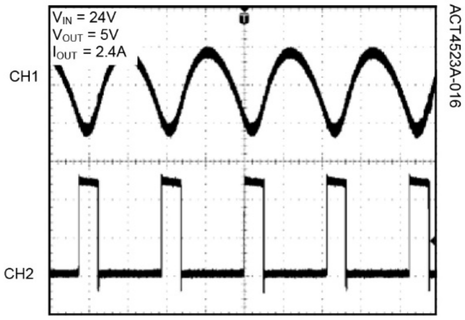


CH1: V_{OUT} Ripple, 20mV/div
CH2: SW, 5V/div
TIME: 2µs/div

TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

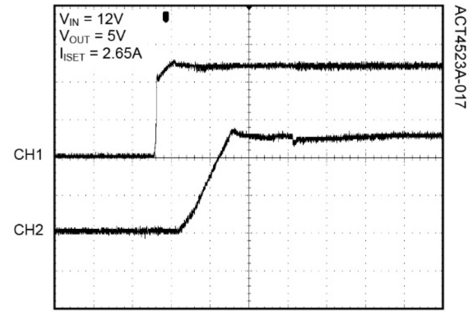
(Schematic as show in Figure 8, Ta = 25°C, unless otherwise specified)

SW vs. Output Voltage Ripple



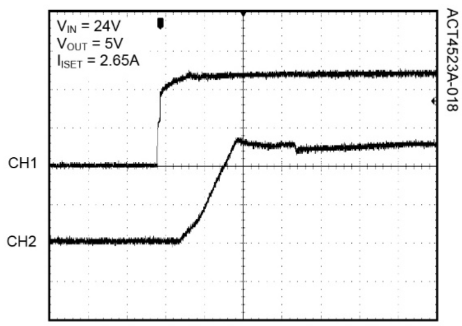
CH1: V_{RIPPLE}, 20mV/div
CH2: SW, 10V/div
TIME: 2μs/div

Start up with VIN



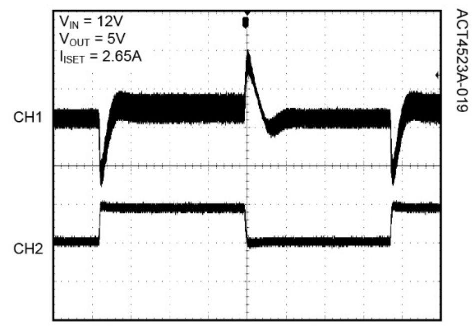
CH1: V_{IN}, 5V/div
CH2: V_{OUT}, 2V/div
TIME: 400μs//div

Start up with VIN



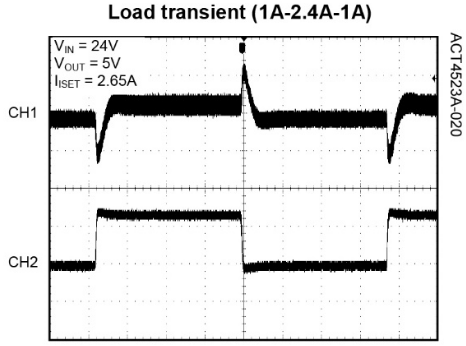
CH1: V_{IN}, 10V/div
CH2: V_{OUT}, 2V/div
TIME: 400μs//div

Load transient (80mA-1A-80mA)



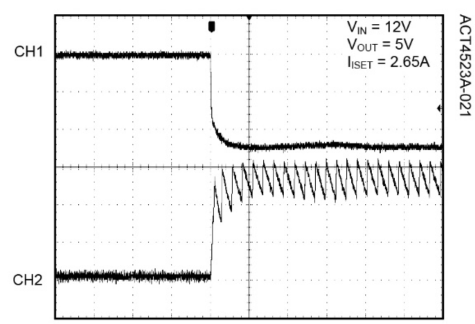
CH1: V_{OUT}, 50mV/div
CH2: I_{OUT}, 1A/div
TIME: 400μs//div

Load transient (1A-2.4A-1A)



CH1: V_{OUT}, 100mV/div
CH2: I_{OUT}, 1A/div
TIME: 400μs//div

Short Circuit

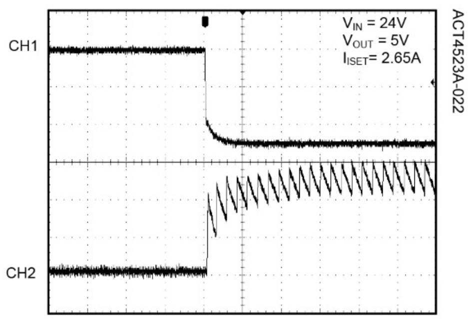


CH1: V_{OUT}, 2V/div
CH2: I_L, 1A/div
TIME: 100μs//div

TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

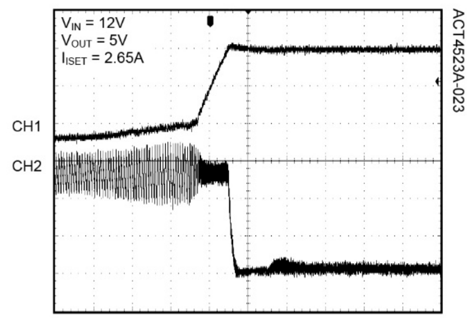
(Schematic as show in Figure 8, Ta = 25°C, unless otherwise specified)

Short Circuit



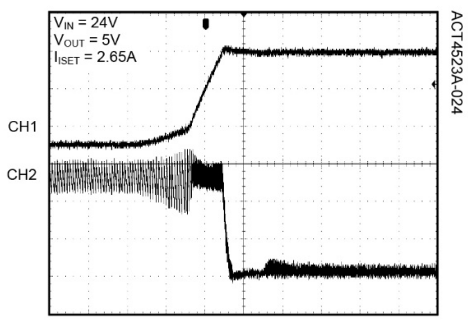
CH1: V_{OUT}, 2V/div
CH2: I_L, 1A/div
TIME: 100µs//div

Short Circuit Recovery



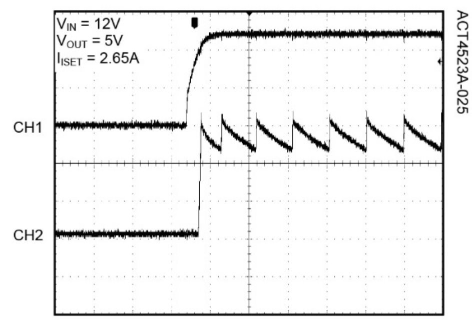
CH1: V_{OUT}, 2V/div
CH2: I_L, 1A/div
TIME: 400µs//div

Short Circuit Recovery



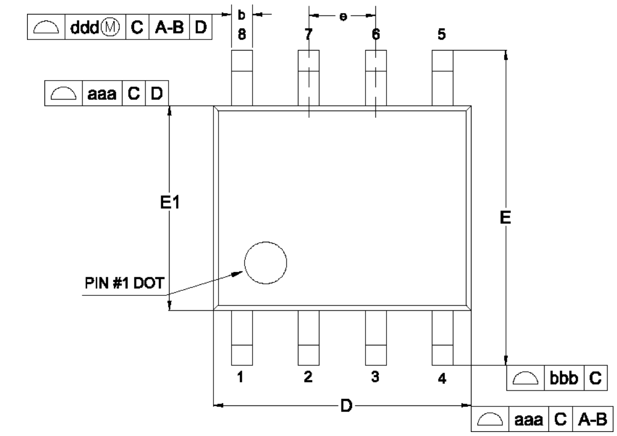
CH1: V_{OUT}, 2V/div
CH2: I_L, 1A/div
TIME: 400µs//div

OVP Circuit

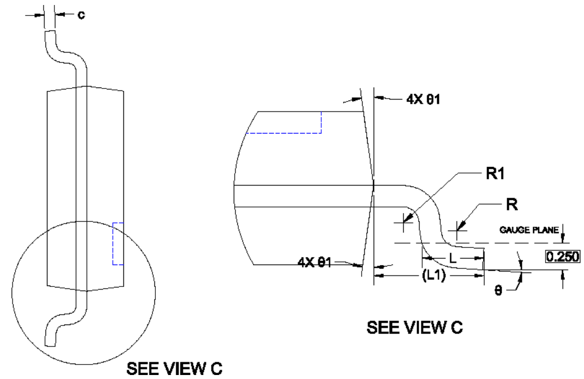


CH1: V_{IN}, 5V/div
CH2: V_{OUT}, 2V/div
TIME: 10ms//div

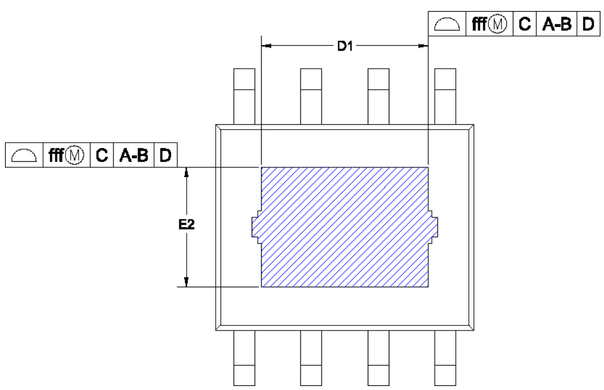
PACKAGE OUTLINE AND DIMENSIONS



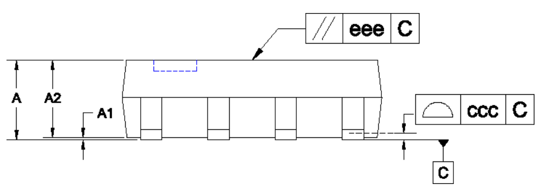
Top View



Side View



Bottom View



Side View

Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	1.300	--	1.700
A1	0.000	--	0.100
A2	1.350	--	1.550
b	0.330	--	0.510
c	0.170	--	0.250
D	4.900BSC		
E	6.000BSC		
E1	3.900BSC		
D1	3.150BSC		
E2	2.260BSC		
e	1.270 BSC		
L	0.400	--	1.270
L1	1.050REF.		
R	0.070	--	--
R1	0.070	--	--
θ	0°	--	8°
θ1	5°	--	15°
Tol. of Form&Position			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		
fff	0.15		

Notes

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5-2009.
2. All DIMENSIONS ARE IN MILLIMETERS.
3. UNILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Product Compliance

This part complies with RoHS directive 2011/65/EU as amended by (EU) 2015/863.

This part also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel: 1-844-890-8163**

Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

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