ET-UARTSWD Users Guide

Power Application Controller®

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CONTENTS

OVERVIEW

Active-Semi's ET-UARTSWD isolated communications and debugging interface unifies two modules into one. Traditionally, interfacing a PC Computer to any of Active-Semi's PAC5xxx Evaluation Modules required one module to enable UART based serial communications and a second module to allow for in-system debugging and FLASH memory programing. The ET-UARTSWD modules allow for a single board to carry all pertinent functions regarding these two interfacing methodologies, making Evaluation Module bring up much quicker and efficient.

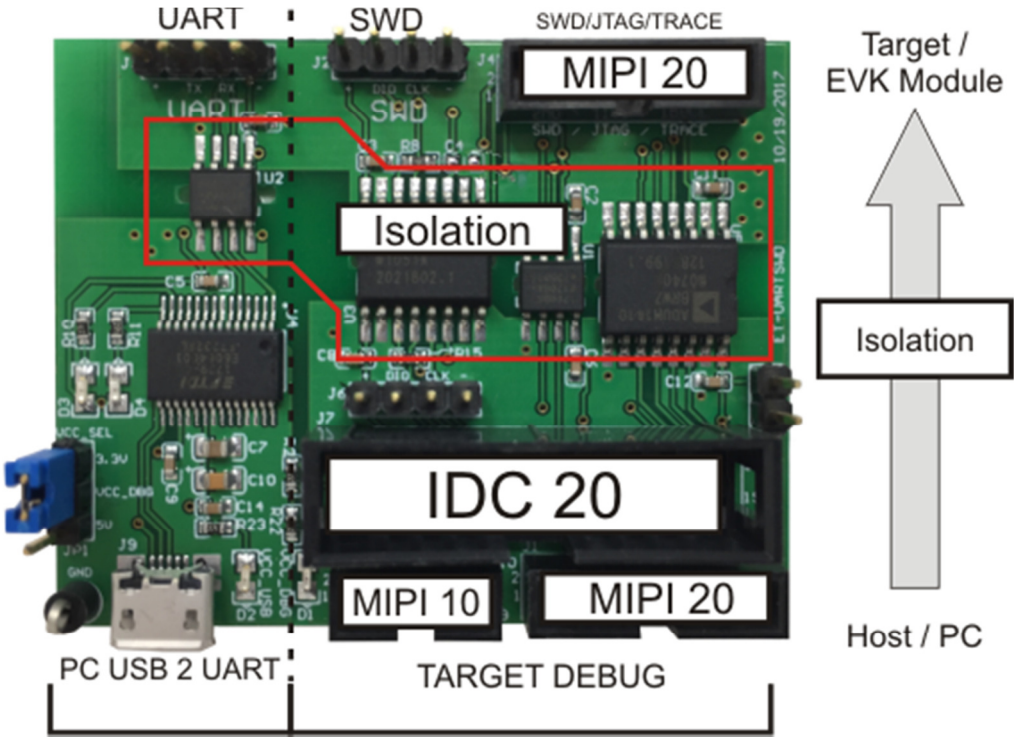


Figure 1: ET-UARTSWD Block Diagram

The module is in essence divided in two independently usable sections. One section handles all aspects of serial communications, with the subsequent section taking care of all debugging and FLASH programming resources.

To provide serial communications capability, a USB to UART FTDI chip is provided. Coupled with the user's PC Computer, this chip generates a Virtual COM Port. Said COM Port can then be used by the Graphical User Interface (GUI) commonly used to drive the application residing within the different PAC5xxx Evaluation Modules. In order to protect the PC Computer from the possible high voltages some of the PAC5xxx evaluation modules operate with, isolation chips have been placed in between the computer and the target board.

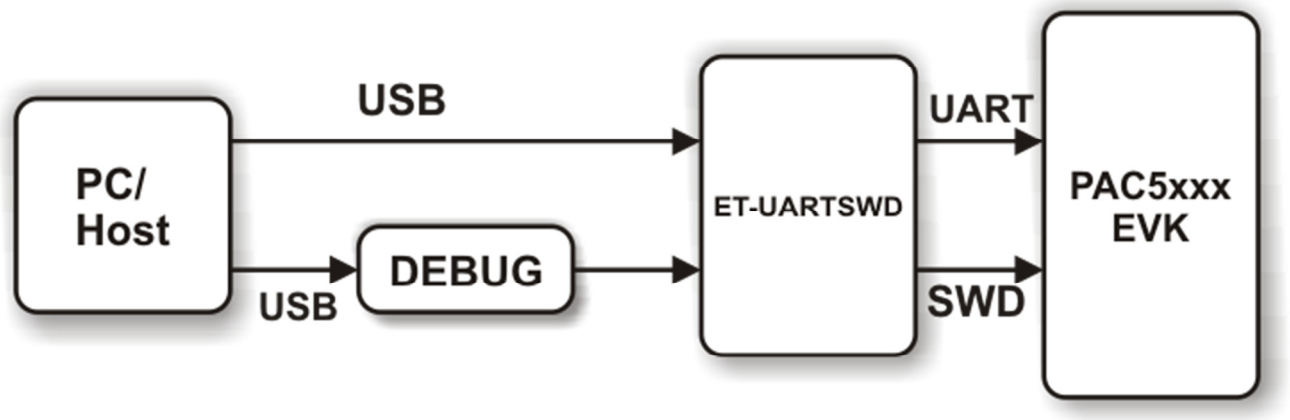


Figure 2: Typical Host To Target Connections Block Diagram

The ET-UARTSWD interfacing board was designed with the many SWD and JTAG interfaces available for different ARM RISC32 cores. In order to service the great variety of debugger modules commercially available (i.e. IAR's I-JET, Segger's J-LINK, etc.), different connectors have been incorporated. MIPI20, MIPI10 and 4 pin header connectors are included at the debugger's side. This allows the user to connect their respective debugger module to the interface board through the debugger module's factory provided ribbon cable. Note that debuggers that already include isolation are not supported. The two isolation stages will not work together.

On the target's side, a MIPI20 and 4 pin header connector are provided to ensure connectivity with any of the PAC5xxx Evaluation modules.

In between the host side and the target side, an isolator block has been provided. This ensures safety to both the user as well as the PC/debugger module, when dealing with high voltage platforms. It is recommended for any application running at anything higher than 24V to take advantage of the provided isolation feature.

Active-Semi's ET-UARTSWD isolated UART and SWD Debug module kit consists of the following:

- ET-UARTSWD Evaluation module
- USM Micro Cable (Qty = 1)
- Four pin female/female header connector cable (Qty = 2)

Solution Benefits:

- Ideal for interfacing into all PAC5xxx Evaluation Modules.
- Provides access to both serial communications as well as in-system debugging and FLASH programming.
- Isolation protects user's computer as well as any other external hardware (e.g. debugger/programmer).
- Power can be derived from the debugger module, or the computer's USB port.
- Schematics, BOM, Layout drawings available

The following sections provide information about the hardware features of Active-Semi's ET-UARTSWD turnkey solution.

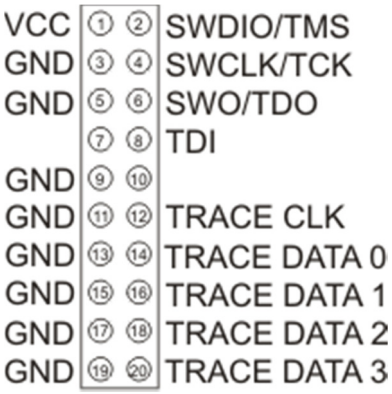
1. ET-UARTSWD RESOURCES

1.1 Provided Connectors

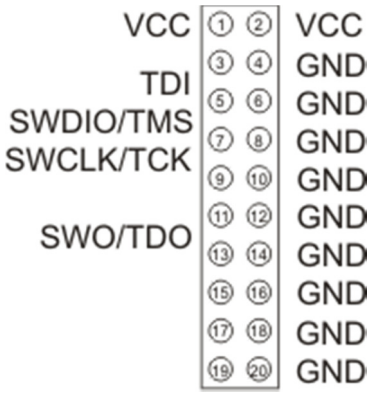
The ET-UARTSWD interface module includes the following ARM compliant Cortex-M debug connectors:

MIPI 10 Cortex Debug Connector:

MIPI20 Cortex Debug + ETM Connector:



Legacy IDC 20 JTAG IDC Connector



1.2 Pinout and Signal Connectivity

The following diagram shows the male header pinout for the ET-UARTSWD evaluation module, as seen from above:

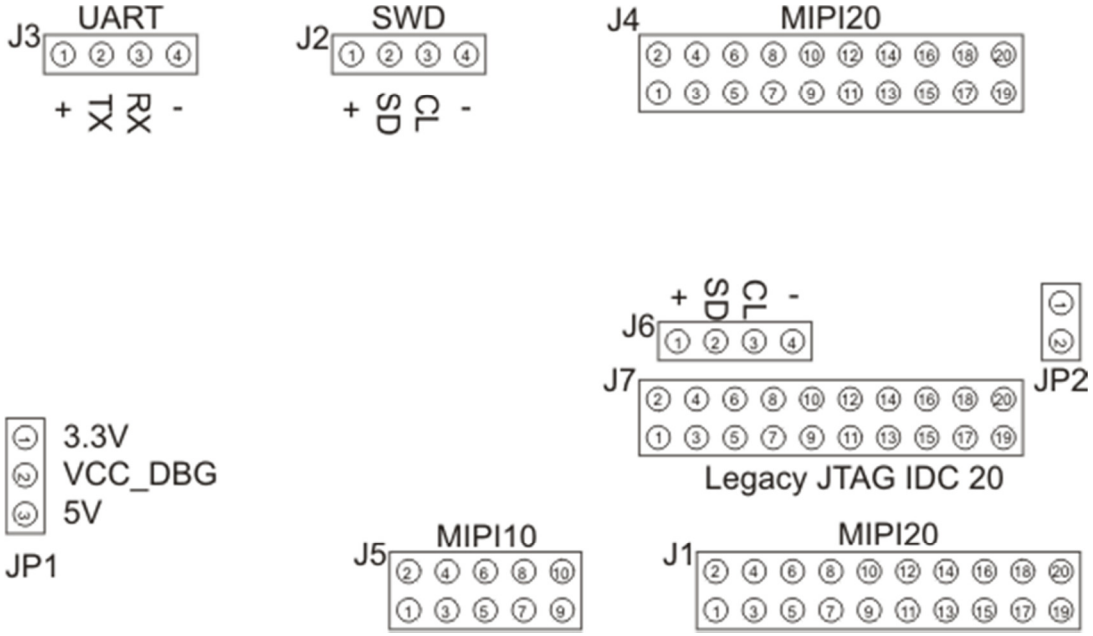


Figure 2 ET-UARTSWD Headers and Test Stakes Pinout

1.3 Power Input

Power to the ET-UARTSWD interface module is provided through the USB to UART chip (FT232) USB port. The isolation module takes advantage of the USB port device's integrated 3.3V and 5V rails. The ET-UARTSWD ships with the 3.3V rail used as the default mode of operation.

In some cases, debug modules include their own voltage rail. For such scenarios, there is no need to use the power derived from the USB resource. (Please refer to the "Jumpers" section to study the different input power combinations)

1.4 LED's

When the USB to UART device is connected to a personal computer's USB port, 5V are obtained from within the USB connection. At this point in time, LED D2 should light up.

When connecting a debugger module to the isolated interface module, if said module provides its own power (often 5V or 3.3V), then D1 will light up. In the event the debug module does not provide its own power, JP1 can be used to feed power derived from the USB connection. If this resource is employed, LED D1 will light up.

The following table shows the provided LED and its associated diagnostic function.

LED	Description
D1	VCC Debug (5V or 3.3V) indicator. Lights up when power to the debugger side is provided.
D2	5V rail indicator. Light up when the USB connector J9 is connected to a personal computer USB port.
D3	UART Port TX Indicator
D4	UART Port RX Indicator

1.5 Jumpers

Two jumpers are provided to configure the isolated debug interface block with different power options. Depending on the debug module being employed, different power levels may need to be provided.

Jumper	Description
JP1	Place a 2 pin shunt when the debug module requires either 5V or 3.3V provided at pin 1 on any of the input connectors. **NOTE: When JP1 jumper is shunted, JP2 should be left open.**
JP1:1-2	(**DEFAULT**) Debug Module VCC is 3.3V.
JP1:2-3	Debug Module VCC is 5V.
JP2	Place a 2 pin shunt when pin a debug module connected to the IDC20 connector provides power on pin 19. **NOTE: When JP2 jumper is shunted, JP1 should be left open.**

1.6 Input SWD / JTAG Connectors

Input connectors are considered those connectors before the isolator. In these header connectors, the user will connect a 4 pin 0.1" pitch single line connector, or a 10 or 20 pin ribbon cable based debug module.

Serial Wire Debug (SWD)

Connector J7 is a 4 pin 0.1" pitch header provided to interface to simple 4 wire based debug modules.

J7 Pins	Terminal	Description
1	+	VCC (powered from the target side – either 5V or 3.3V)
2	SD	SWD Serial Data
3	CL	SWD Serial Clock
4	-	GND (System Ground)

MIPI 10 Cortex Debug Connector

Connector J5 is a 10 pin MIPI10 Cortex-M Debug Connector provided to interface to MIPI10 based debug modules.

J5 Pins	Terminal	Description
1	VCC	VCC Power
2	SWDIO/TMS	Serial Wire Debug Data Input Output / JTAG Test Mode Select
3	GND	GND (System GND)
4	SWCLK/TCK	Serial Wire Debug Clock / JTAG Clock
5	GND	GND (System GND)
6	SWO/TDO	Serial Wire Debug Output / JTAG Data Output
7	NC	Not Connected
8	TDI	JTAG Data Input
9	GND	GND (System GND)
10	NC	Not Connected

MIPI20 Cortex Debug + ETM Connector

Connector J1 is a 20 pin MIPI20 Cortex-M Debug Connector provided to interface to MIPI20 based debug modules.

J1 Pins	Terminal	Description
1	VCC	VCC Power
2	SWDIO/TMS	Serial Wire Debug Data Input Output / JTAG Test Mode Select
3	GND	GND (System GND)
4	SWCLK/TCK	Serial Wire Debug Clock / JTAG Clock
5	GND	GND (System GND)
6	SWO/TDO	Serial Wire Debug Output / JTAG Data Output
7	NC	Not Connected
8	TDI	JTAG Data Input
9	GND	GND (System GND)

10	NC	Not Connected
11	GND	GND (System GND)
12	TRACE CLK	ETM Trace Clock
13	GND	GND (System GND)
14	TRACE DATA 0	ETM Trace Data 0
15	GND	GND (System GND)
16	TRACE DATA 1	ETM Trace Data 1
17	GND	GND (System GND)
18	TRACE DATA 2	ETM Trace Data 2
19	GND	GND (System GND)
20	TRACE DATA 3	ETM Trace Data 3

Legacy IDC 20 JTAG IDC Connector

Connector J7 is a 20 pin shrouded header connector provided to interface to Legacy IDC 20 JTAG based debug modules.

J7 Pins	Terminal	Description
1	VCC	VCC Power
2	VCC	VCC Power (Optional)
3	NC	Not Connected
4	GND	GND (System GND)
5	TDI	JTAG Data Input
6	GND	GND (System GND)
7	SWDIO/TMS	Serial Wire Debug Data Input Output / JTAG Test Mode Select
8	GND	GND (System GND)
9	SWCLK/TCK	Serial Wire Debug Clock / JTAG Clock
10	GND	GND (System GND)
11	NC	Not Connected
12	GND	GND (System GND)
13	SWO/TDO	Serial Wire Debug Output / JTAG Data Output
14	GND	GND (System GND)
15	NC	Not Connected
16	GND	GND (System GND)
17	NC	Not Connected
18	GND	GND (System GND)
19	VCC	VCC Power (Optional)
20	GND	GND (System GND)

1.7 Output UART / SWD / JTAG Connectors

Output connectors are considered those connectors after the isolation stage. In these header connectors, the user will connect a 10 or 20 pin ribbon cable based debug module..

Serial Wire Debug (SWD)

Connector J2 offers access to the isolated SWD port lines.

J2 Pins	Terminal	Description
1	+	VCC (powered from the target side – either 5V or 3.3V)
2	SD	SWD Serial Data
3	CL	SWD Serial Clock
4	-	GND (System Ground)

Serial Communications

Connector J3 offers access to the isolated UART port lines.

J3 Pin	Terminal	Description
1	+	VCC (powered from the target side – either 5V or 3.3V)
2	TX	MCU Transmit Line
3	RX	MCU Receive Line
4	-	GND (System Ground)

MIPI20 Cortex Debug + ETM Connector

Connector J4 offers access to the isolated 20 pin MIPI20 Cortex-M Debug Connector.

J1 Pins	Terminal	Description
1	VCC	VCC Power
2	SWDIO/TMS	Serial Wire Debug Data Input Output / JTAG Test Mode Select
3	GND	GND (System GND)
4	SWCLK/TCK	Serial Wire Debug Clock / JTAG Clock
5	GND	GND (System GND)
6	SWO/TDO	Serial Wire Debug Output / JTAG Data Output
7	NC	Not Connected
8	TDI	JTAG Data Input
9	GND	GND (System GND)
10	NC	Not Connected
11	GND	GND (System GND)
12	TRACE CLK	ETM Trace Clock
13	GND	GND (System GND)
14	TRACE DATA 0	ETM Trace Data 0
15	GND	GND (System GND)
16	TRACE DATA 1	ETM Trace Data 1
17	GND	GND (System GND)
18	TRACE DATA 2	ETM Trace Data 2
19	GND	GND (System GND)
20	TRACE DATA 3	ETM Trace Data 3

2. TYPICAL ET-UARTSWD SETUP

The setup for the ET-UARTSWD evaluation module requires up to four simple connections. The following guidelines assume both UART and SWD/JTAG debug functionalities are being employed.

1. Connect J9 USB 2 UART input to a PC using the provided USB Micro cable. This will power up the module with D2 powering up.
2. Connect the selected debug module to the respective 10 or 20 pin header connector.
    a. NOTE: Debug Modules which already include an isolation stage are not supported. Two isolation stages will introduce a conflictive behavior.
3. Connect one of the provided four pin female header cables to the UART isolated output on J3. The other side of this cable must be connected to the PAC5xxx Evaluation Module's UART port.
    a. NOTE: Polarity must be observed.
4. Connect the second four pin female header cable to the SWD isolated output on J2. The other side of this cable must be connected to the PAC5xxx Evaluation Module's SWD port.
    a. NOTE: Polarity must be observed.

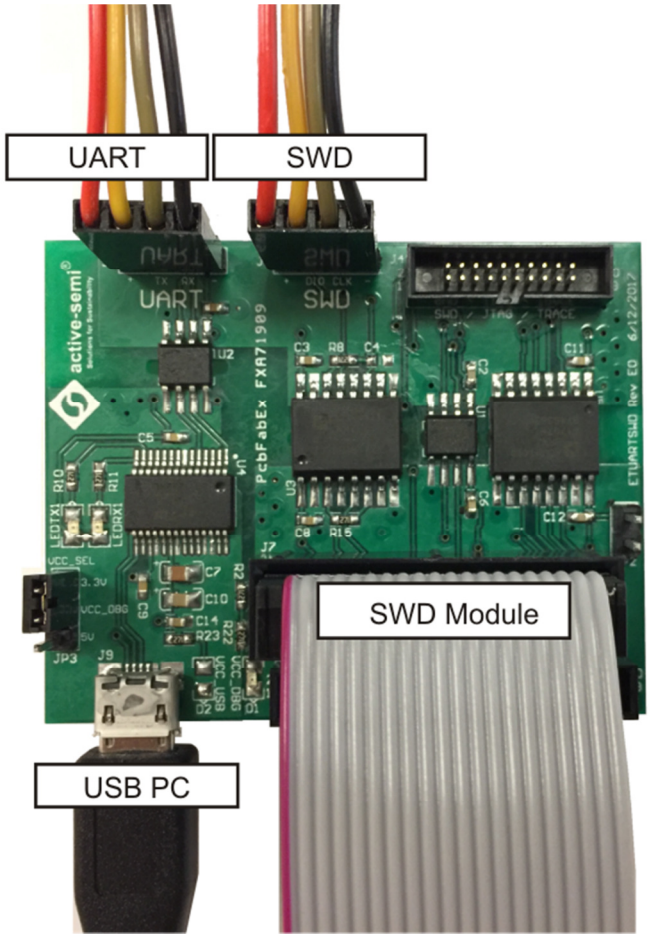


Figure 3: ET-UARTSWD interface Module Connections

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