adesto® TECHNOLOGIES

ATXP032

266 Mbyte/s High-Performance 32Mbit XiP System Accelerating Memory

ADVANCE INFORMATION
SUMMARY DATASHEET

Features

- Optimized for eXecute-in-Place (XiP) operations
  - Reduces average latency for improving CPU performance
  - Enables 40% higher CPU performance than the basic Octal SPI protocol
- 133MHz Maximum Operating Frequency
  - Up to 266-Mbytes per second data transfer in Octal DTR mode
- Concurrent Read and Write
  - Simultaneous execution of Read and Write operations
  - No additional delay executing Read commands issued during Program or Erase
  - Flexible boundary between Data Storage Area and Read While Write Area
  - Each area can have any size from 0 to 32 Mbits in 4 Mbit steps
- Single 1.8V Supply
- Serial Peripheral Interface (SPI) Compatible
  - Supports SPI Modes 0 and 3 (1-1-1)
  - Supports QPI Mode (4-4-4)
  - Supports Octal Mode (8-8-8)
  - Supports Dual Transfer Rate (DTR) for QPI and Octal modes
- Flexible, Optimized Erase Architecture for Code + Data Storage Applications
  - Uniform 4-Kbyte Block Erase
  - Uniform 32-Kbyte Block Erase
  - Uniform 64-Kbyte Block Erase
  - Full Chip Erase
- Hardware Controlled Locking of Protected Sectors via $\overline{WP}$ Pin
- 256-byte, One-Time Programmable (OTP) Security Register
  - 128 bytes factory programmed with a unique identifier
  - 128 bytes user programmable
- Flexible Programming
  - Byte/Page Program (1 to 256 Bytes)
  - Single, Quad and Octal-Input Byte/Page Program (1 to 256 Bytes)
  - Write to Buffer and Write Buffer to Memory Commands
  - Active Status Interrupt when Program or Erase operation has finished
- Power Optimized Program and Erase Control
  - Automatic Deep Power-Down or Ultra-Deep Power-Down upon the completion of Program or Erase operation
- Automatic Checking and Reporting of Program/Erase Failures
- Software Controlled Reset
- Hardware Reset Pin
- JEDEC Standard Hardware Reset
- JEDEC Standard Manufacturer and Device ID Read Methodology
- Support for Serial Flash Discoverable Parameters (SFDP)
- Low Power Dissipation
  - 200nA Ultra-Deep Power-Down current (Typical)

- 4µA Deep Power-Down Current (Typical)
- 20µA Standby current (Typical, for SPI Mode)
- 35µA Standby current (Typical, for QPI and Octal mode)
- 1.0mA + 30µa/MHz Active Read Current (KGD, Typical, for SPI Mode@ 1pF load)
- 1.0mA + 65µa/MHz Active Read Current (KGD, Typical, for QPI Single Transfer Rate @ 1pF load)
- 1.0mA + 91µa/MHz Active Read Current (KGD, Typical, for QPI Dual Transfer Rate @ 1pF load)
- 1.0mA + 142µa/MHz Active Read Current (KGD, Typical, for Octal Mode Dual Transfer Rate @ 1pF load)

- Programmable I/O drive strength
- Endurance: 100,000 Program/Erase Cycles
- Data Retention: 20 Years
- Complies with Full Industrial Temperature Range
  - -40°C - 85°C for packaged parts
  - -40°C - 105°C for Known Good Die [KGD]
- Industry Standard Green (Pb/Halide-free/RoHS Compliant) Package Options
  - 24-ball BGA
  - WLCSP
  - Known Good Die [KGD]

1. Description

The Adesto® ATXP032 is a high speed serial interface Flash memory device designed for use in a wide variety of high-volume consumer based applications in which program code is executed directly from Flash memory (XiP) or shadowed from Flash memory into embedded or external RAM for execution. The ATXP032 allows writing to the flash array at the same time as code is being fetched from a different part of the array. This enables firmware updates and data logging without the need for additional data storage devices in the system.

The ATXP032 is specifically optimized for eXecute-in-Place (XiP) operations. While being backwards compatible with existing XiP protocols, the ATXP032 includes additional improvements that reduce significantly the latency of fetching the next cache line(s). The improved command protocol may enable more than 40% faster execution than the standard XiP protocol running at the same clock frequency.

In addition to standard SPI (1-1-1) Operation, the ATXP032 supports QPI Mode (4-4-4) and Octal Mode (8-8-8).

For even higher data throughput, the ATXP032 Supports Dual Transfer Rate (DTR) for QPI and Octal modes.

For faster transfer of data from the device, the ATXP032 provides a Data Strobe (DS) output signal. DS serves as a source-synchronous clock to the output data. This enables much faster clock rates for both DTR and STR modes than can be achieved by using SCK as the clock signal for incoming data.

The ATXP032 is optimized for low power system operation. In addition to the inherently low power consumption of the device it supports programmable strength IO drivers that can be matched to the required operating capacitive load. The ATXP032 supports 3 low-power operation modes and an option to automatically switch to low power mode upon completion of a program or erase operation

The erase block sizes of the ATXP032 have been optimized to meet the needs of today's code and data storage applications. By optimizing the size of the erase blocks, the memory space can be used much more efficiently. Because certain code modules and data storage segments must reside by themselves in their own erase regions, the wasted and unused memory space that occurs with large sectored and large block erase Flash memory devices can be greatly reduced. This increased memory space efficiency allows additional code routines and data storage segments to be added while still maintaining the same overall device density.

The device also contains a specialized OTP (One-Time Programmable) Security Register that can be used for purposes such as unique device serialization, system-level Electronic Serial Number (ESN) storage and locked key storage.

Specifically designed for use in many different systems, the ATXP032 supports read, program, and erase operations with a single 1.8V supply voltage. No separate voltage is required for programming and erasing.

2. Pin Descriptions and Pinouts

All I/O pins and DS will be in tri-state mode when not actively driven. To reduce power consumption, it is recommended to not leave pins floating, but have internal pull downs in the host controller that will ensure that all pins have a valid logic level at all times.

Table 2-1. Pin Descriptions

Symbol	Name and Function	Asserted State	Type
$\overline{CS}$	**CHIP SELECT:** Asserting the $\overline{CS}$ pin selects the device. When the $\overline{CS}$ pin is deasserted, the device will be deselected and normally be placed in standby mode (not Deep Power-Down mode), and the output pins will be in a high-impedance state. When the device is deselected, data will not be accepted on the SI pin. A high-to-low transition on the $\overline{CS}$ pin is required to start an operation, and a low-to-high transition is required to end an operation. When ending an internally self-timed operation such as a program or erase cycle, the device will not enter the standby mode until the completion of the operation.	Low	Input
SCK	**SERIAL CLOCK:** This pin is used to provide a clock to the device and is used to control the flow of data to and from the device. In Single Transfer Rate modes, command, address, and input data present on the I/O pins are always latched in on the rising edge of SCK, while output data on the I/O pins is always clocked out on the falling edge of SCK. In the Double Transfer Rate Modes, address and input data present on the I/O pins data are latched on both clock edges. For more accurate operation at high speeds, SCK is returned as DS synchronous to output data.	-	Input
SI (I/O_0)	**SERIAL INPUT:** In SPI Mode, the SI pin is used to shift data into the device. The SI pin is used for all data input including command and address sequences. In Single Transfer Rate modes, command, address, and input data present on the SI pin is always latched in on the rising edge of SCK. In the Double Transfer Rate Modes, address and input data present on the SI pin is latched on both edges of SCK. In QPI and Octal modes, the SI Pin becomes an I/O pin (I/O_0) in conjunction with other pins. In Single Transfer Rate modes this allows four or eight bits of command, address, or input data on I/O_{3-0} or I/O_{7-0} to be clocked in on the rising edge of SCK, or four or eight bits clocked out on the falling edge of SCK. In Double Transfer Rate modes this allows four or eight bits of address or input data on I/O_{3-0} or I/O_{7-0} to be clocked in on every edge of SCK, or four or eight bits clocked out on every edge of SCK. Commands are clocked on the rising edge of SCK, requiring a whole clock cycle also in the Double Transfer Rate modes. To maintain consistency with the SPI nomenclature, the SI (I/O_0) pin will be referenced as the SI pin unless specifically addressing the Multi-I/O modes in which case it will be referenced as I/O_0. Data present on the SI pin will be ignored whenever the device is deselected ($\overline{CS}$ is deasserted).	-	Input/ Output

Table 2-1. Pin Descriptions (Continued)

Symbol	Name and Function	Asserted State	Type
SO (I/O_1)	**SERIAL OUTPUT:** The SO pin is used to shift data out from the device. In the Single Transfer Rate modes, Data on the SO pin is always clocked out on the falling edge of SCK. In the Double Data Rate modes, Data on the SO pin is clocked out on both edges of SCK In QPI and Octal modes, the SO Pin becomes an I/O pin (I/O_1) in conjunction with other pins. In Single Transfer Rate modes this allows four or eight bits of command, address, or input data on I/O_{3-0} or I/O_{7-0} to be clocked in on the rising edge of SCK, or four or eight bits clocked out on the falling edge of SCK. In Double Transfer Rate modes this allows four or eight bits of address or input data on I/O_{3-0} or I/O_{7-0} to be clocked in on every edge of SCK, or four or eight bits clocked out on every edge of SCK. Commands are clocked on the rising edge of SCK, requiring a whole clock cycle also in the Double Transfer Rate modes. To maintain consistency with the SPI nomenclature, the SO (I/O_1) pin will be referenced as the SO pin unless specifically addressing the Multi-I/O modes in which case it is referenced as I/O_1. The SO pin will be in a high-impedance state whenever the device is deselected ($\overline{CS}$ is deasserted).	-	Input/ Output
$\overline{WP}$ (I/O_2)	**WRITE PROTECT:** The $\overline{WP}$ pin controls the hardware locking feature of the device. Please refer to "Protection Commands and Features" on page 45 for more details on protection features and the $\overline{WP}$ pin. The $\overline{WP}$ pin is internally pulled-high and may be left floating if hardware controlled protection will not be used. However, it is recommended that the $\overline{WP}$ pin also be externally connected to V_{CC} whenever possible. In QPI and Octal modes, I/O_2 is used together with I/O_{3-0} or I/O_{7-0} as a bidirectional I/O pin. pin. In these modes, the I/O_2 pin will be in a high-impedance state whenever the device is deselected ($\overline{CS}$ is deasserted).	Low	Input/ Output
$\overline{HOLD}$ (I/O_3)	**HOLD:** The $\overline{HOLD}$ pin is used to temporarily pause serial communication without deselecting or resetting the device. While the $\overline{HOLD}$ pin is asserted, transitions on the SCK pin and data on the SI pin will be ignored, and the SO pin will be in a high-impedance state. The $\overline{CS}$ pin must be asserted, and the SCK pin must be in the low state in order for a Hold condition to start. A Hold condition pauses serial communication only and does not have an effect on internally self-timed operations such as a program or erase cycle. Please refer to "Hold" on page 94 for additional details on the Hold operation.The $\overline{HOLD}$ pin is internally pulled-high and may be left floating if the Hold function will not be used. However, it is recommended that the $\overline{HOLD}$ pin also be externally connected to V_{CC} whenever possible. In QPI and Octal modes, I/O_3 is used together with I/O_{3-0} or I/O_{7-0} as a bidirectional I/O pin. In these modes, the I/O_3 pin will be in a high-impedance state whenever the device is deselected ($\overline{CS}$ is deasserted).	Low	Input/ Output

Table 2-1. Pin Descriptions (Continued)

Symbol	Name and Function	Asserted State	Type
DS	**DATA STROBE:** DS is the return of the SCK clock, synchronized to the return data. It is available in all modes, and will make it easier to achieve high clock speeds in a system. DS is required to achieve maximum clock speeds. DS is in a high-impedance state when the device is receiving commands, address, or data, and will be driven low prior to data output from the device. In Single Transfer Rate mode, DS is driven low in the first half of the data output cycle, and high in the second half. In Dual Transfer Rate mode, DS changes value at the edge of each data bit. DS will basically be the same value as SCK, but with a delay. Achieving high clock rates in systems without DS will require a short signal path between the SPI master and the memory device, and careful layout of all signal lines to minimize signal delays. Data Strobe is driven t_{RPRE} prior to the first Data Strobe rising edge and t_{RPST} after the last falling edge.	-	Output
I/O_7, I/O_6, I/O_5, I/O_4	**SERIAL I/O:** In Octal Mode, I/O_{7-4} are used together with I/O_{3-0} as bidirectional I/O pins.In these modes, the I/O_{7-4} pins (as well as the I/O_{3-0} pins) will be in a high-impedance state whenever the device is deselected ($\overline{CS}$ is deasserted). In other modes, the I/O_{7-4} pins are always in a high-impedance state. These I/O lines are not available in 8-pin packages.	-	Input/ Output
V_{CC},V_{CC} I/O	**DEVICE POWER SUPPLY:** The V_{CC} and V_{CC} I/O pins are used to supply the source voltage to the device. The V_{CC} and V_{CC} I/O pins have to be connected to the same supply voltage. Each V_{CC} and V_{CC} I/O pin requires a separate decoupling capacitor to GND. 1 µF ceramic capacitors are recommended. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.	-	Power
GND, GND I/O	**GROUND:** The ground reference for the power supply. GND and GND I/O should be connected to the system ground.	-	Power
$\overline{RESET}$	**RESET:** A low state on the reset pin ($\overline{RESET}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{RESET}$ pin. Normal operation can resume once the $\overline{RESET}$ pin is brought back to a high level. See Section 12.11 for details about the device operation when $\overline{RESET}$ pin is engaged. The device incorporates an internal power-on reset circuit, so there are no restrictions on the $\overline{RESET}$ pin during power-on sequences. If this pin and feature is not utilized, then it is recommended that the $\overline{RESET}$ pin is driven high externally. The $\overline{RESET}$ pin is not required for operation of the device. The JEDEC Standard Hardware Reset function described in Section 12.10 provides the same functions without requiring a dedicated pin. The $\overline{RESET}$ pin is included for compatibility with older systems. For new designs, the JEDEC Standard Hardware Reset is recommended. The $\overline{RESET}$ pin may not be included in all package options.	Low	Input

Figure 2-1. 24-pad 6x8 mm BGA Pinout

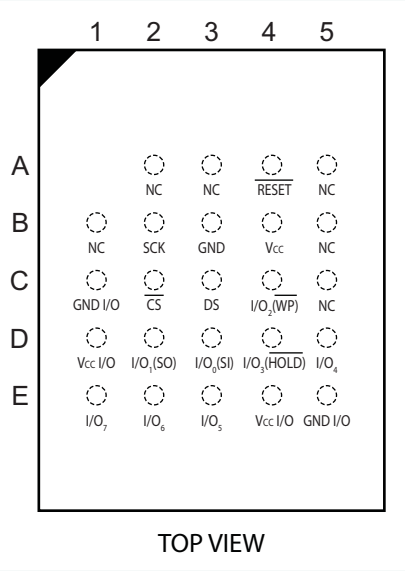


Figure 2-2. WLCSP Pinout

Contact Adesto for pinout

Figure 2-3. QFN Pinout

Figure 2-4. 19-pad 6 x 5 mm BGA Pinout

Possible future package offering

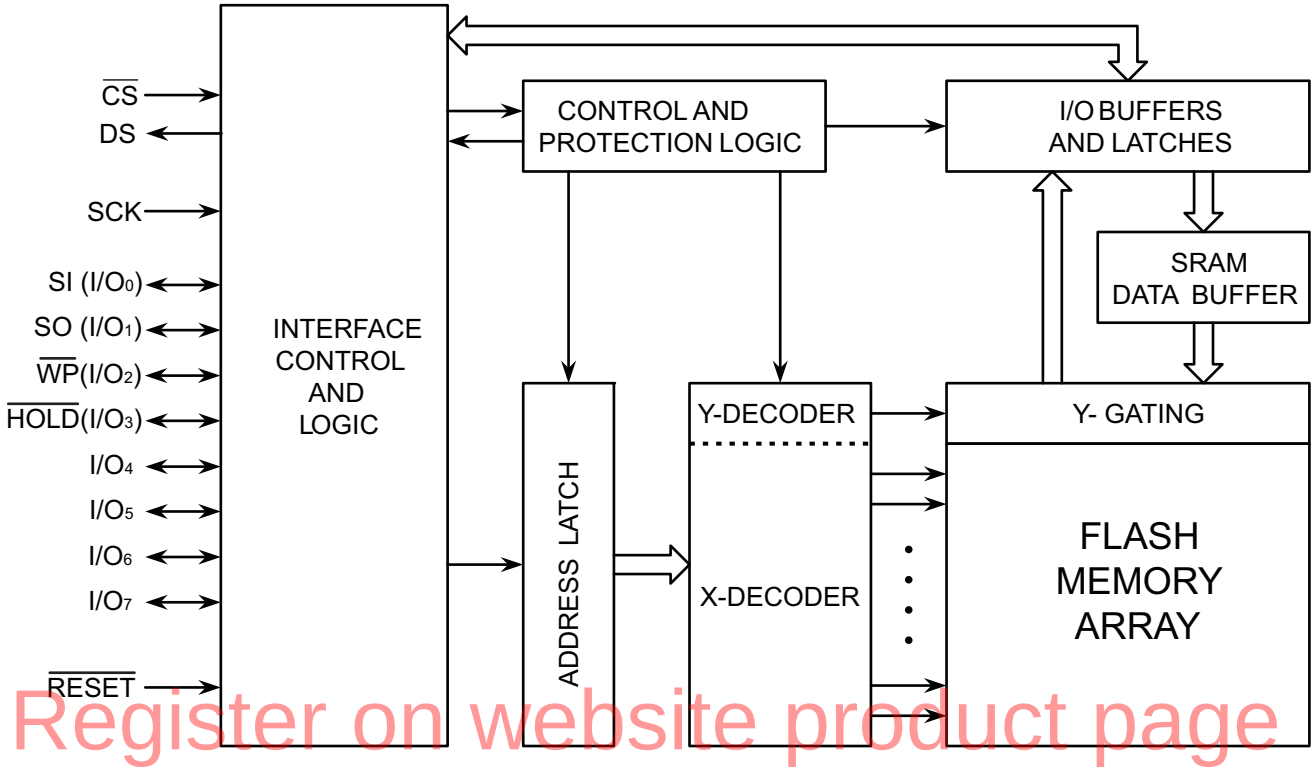
Contact Adesto for pinout and availability09/201609/2016

Possible future package offering

Contact Adesto for pinout and availability

3. Block Diagram

Figure 3-1. Block Diagram



4. Memory Array

To provide the greatest flexibility, the memory array of the ATXP032 memory array is divided into three levels of granularity comprising of sectors, blocks, and pages. The size of the erase blocks is optimized for both code and data storage applications, allowing both code and data segments to reside in their own erase regions. Figure 4-1, Memory Architecture Diagram, illustrates the breakdown of each level and details the number of pages per sector and block. Program operations to the memory array can be done at the full page level or at the byte level (a variable number of bytes). The erase operations can be performed at the chip level or at 3 different block size levels.

4.1 Read-While-Write memory banks

For Read-While-Write operations, the memory array is divided into 2 banks of 0-32 Mbit each as shown in Figure 4-2, Read-While-Write Memory Banks. While an Erase or Program operation is taking place in one bank, a Read operation can take place in the other.

See Section 7.3, Read-While-Write, for more details about using Read-While-Write operations.

Figure 4-1. Memory Architecture Diagram

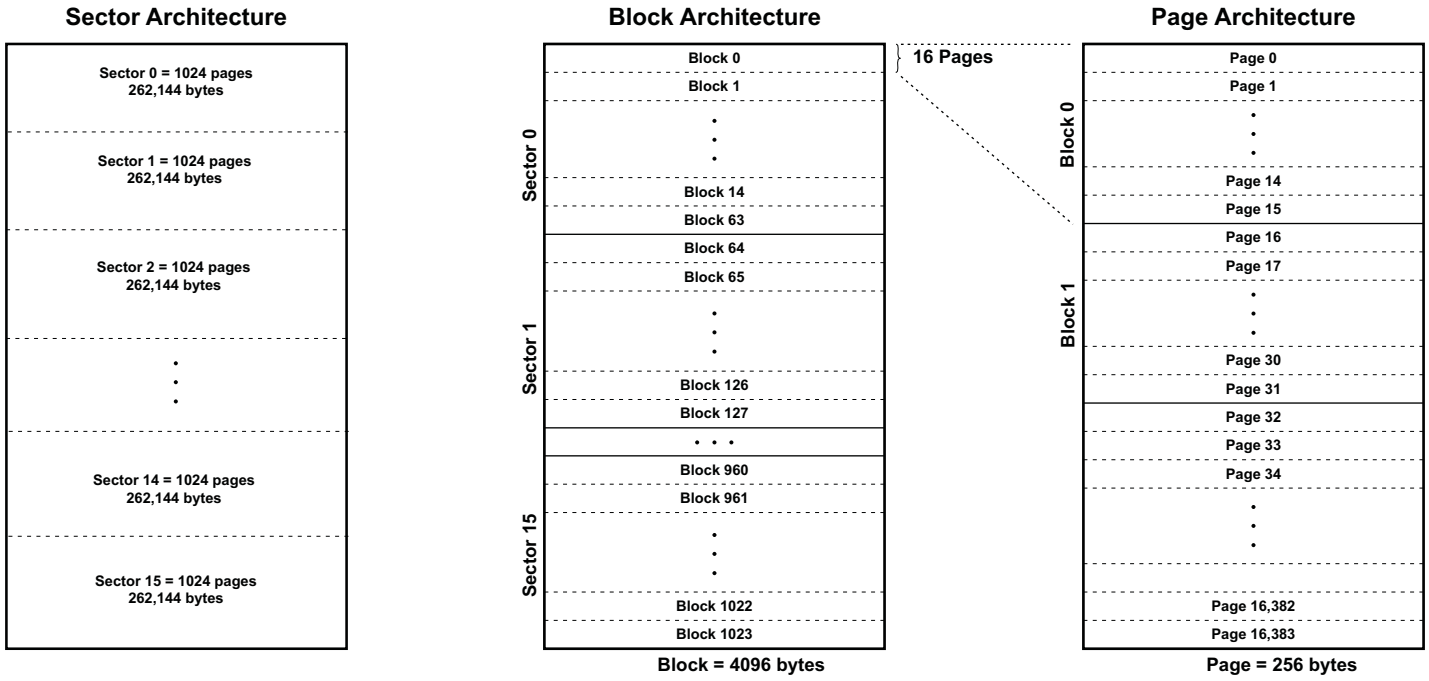
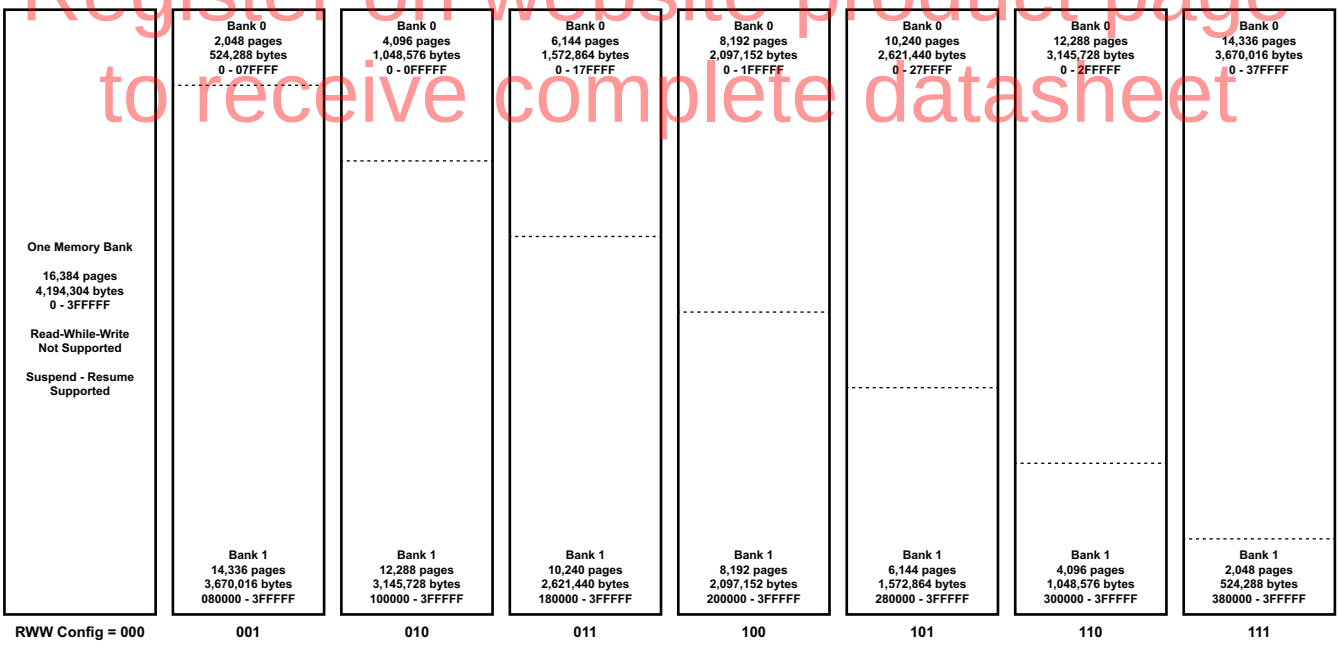
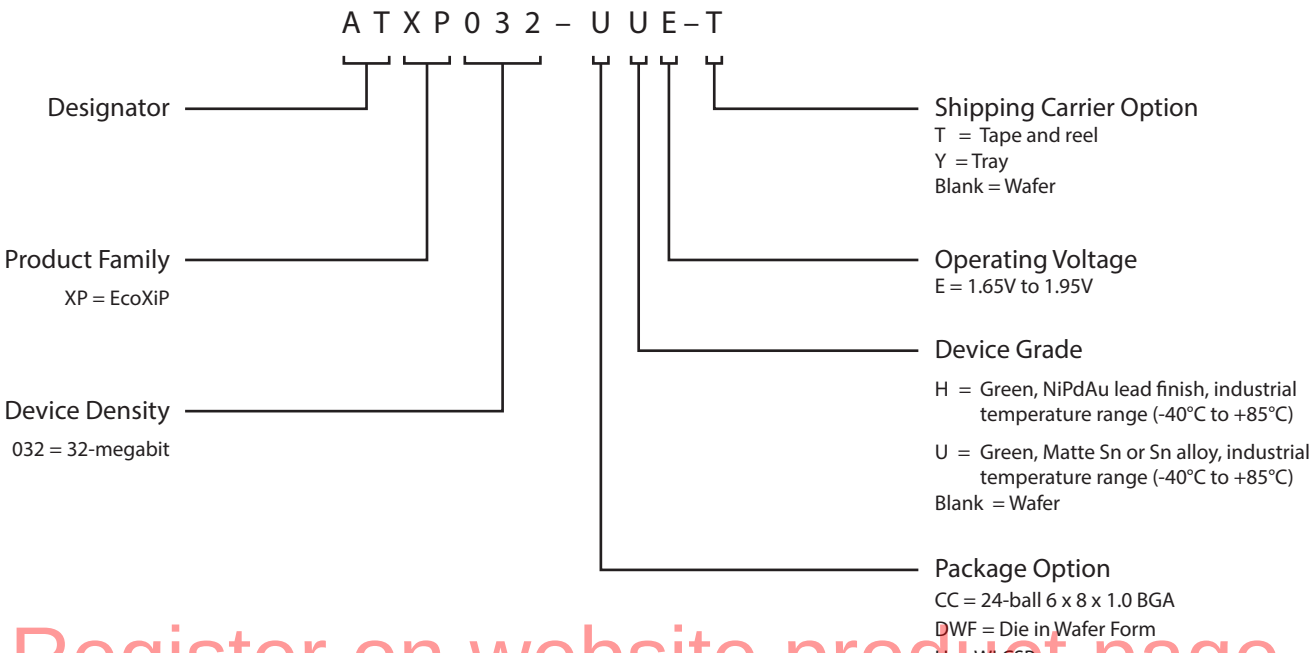


Figure 4-2. Read-While-Write Memory Banks



5. Ordering Information

5.1 Ordering Code Detail



Ordering Code [1]	Package	Lead Finish	Operating Voltage	Max. Freq. (MHz)	Operation Range
ATXP032-CCUE-Y	24CBGA	SnAgCu	1.65V to 1.95V	133	Industrial (-40°C to +85°C)
ATXP032-CCUE-T					
ATXP032-UUE-T [2]	WLCSP				
ATXP032-DWF[2]	DWF	N/A			

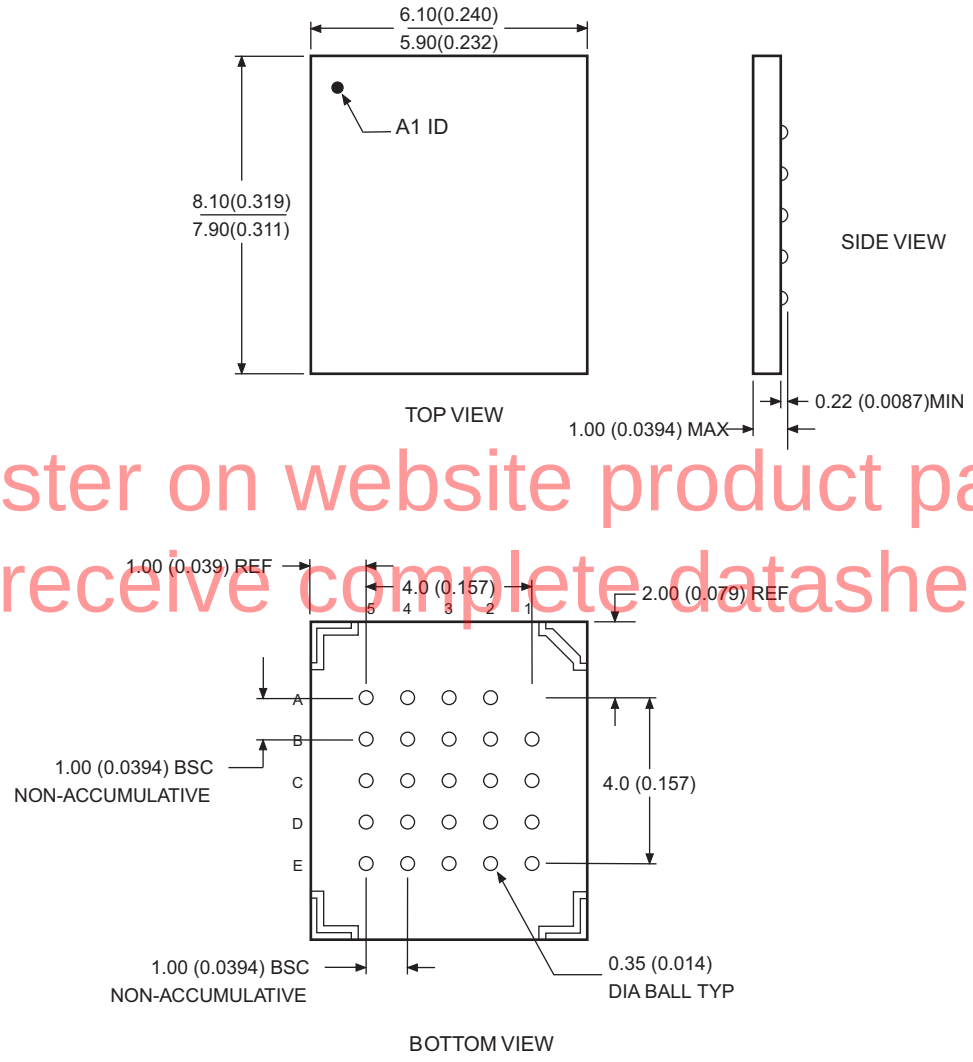
1. The shipping carrier option code is not marked on the device.
2. Contact Adesto for mechanical drawing or Die Sales information.

Package Type	
24CBGA	24C2, 24-ball (5 x 5 Array), 6 x 8 x 1.0mm Body, 1.0 mm Ball Pitch Chip-scale Ball Grid Array Package (CBGA)
WLCSP	Wafer Level CSP / die Ball Grid Array (dBGA)
DWF	Die in Wafer Form

6. Packaging Information

Figure 6-1. 24C2 - 24-ball CBGA

Dimensions in Millimeters and (Inches).
Controlling dimension: Millimeters.



06/2016

adesto TECHNOLOGIES Package Drawing Contact : contact@adestotech.com	TITLE	DRAWING NO.	REV.
	24C2, 24-ball (5 x 5 Array), 6 x 8 x 1.0 mm Body, 1.0 mm Ball Pitch Chip-scale Ball Grid Array Package (CBGA)	24C2	B

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