TS256MSK72V3N-I(TS7L8MDS0-0000) 204Pin DDR3 1333 Industrial ECC SO-DIMM
TS512MSK72V3N-I(TS8L8MDS0-0000) 2GB~4GB Based on 256Mx8

Description

DDR3 Industrial ECC SO-DIMM is high-speed, low power memory module that use 256Mx8bits DDR3 SDRAM in FBGA package and a 2048 bits serial EEPROM on a 204-pin printed circuit board. DDR3 Industrial ECC SO-DIMM is a Dual In-Line Memory Module and is intended for mounting into 204-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

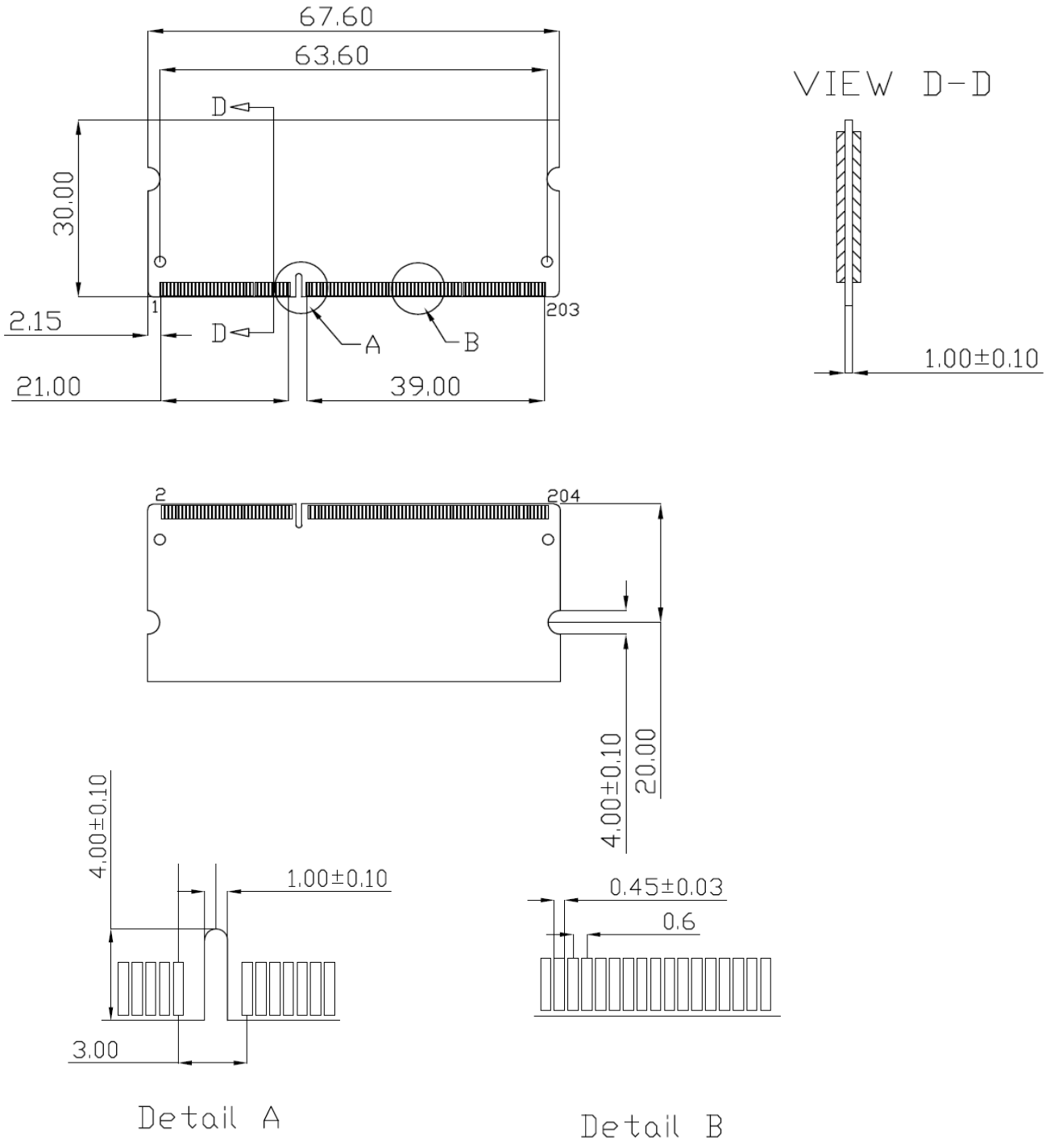
Features

- Operating Temperature : -40°C to +85°C
- RoHS compliant products.
- JEDEC standard 1.5V ± 0.075V Power supply
- VDDQ=1.5V ± 0.075V
- Clock Freq: 667MHZ for 1333Mb/s/Pin.
- Programmable CAS Latency: 5, 6, 7, 8, 9
- Programmable Additive Latency (Posted /CAS): 0,CL-2 or CL-1 clock
- Programmable /CAS Write Latency (CWL) = 7(DDR3-1333)
- 8 bit pre-fetch
- Burst Length: 4, 8
- Bi-directional Differential Data-Strobe
- Internal calibration through ZQ pin
- On Die Termination with ODT pin
- Serial presence detect with EEPROM
- On DIMM thermal Sensor
- Asynchronous reset

Pin Identification

Symbol	Function
A0~A14, BA0~BA2	Address/Bank input
DQ0~DQ63	Data Input / Output.
DQS0~DQS8	Data strobes
/DQS0~/DQS8	Differential Data strobes
CB0~CB7	DIMM ECC check bits
CK0, /CK0,CK1, /CK1	Clock Input. (Differential pair)
CKE0, CKE1	Clock Enable Input.
ODT0, ODT1	On-die termination control line
/CS0, /CS1	DIMM Rank Select Lines.
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
DM0~DM8	Data masks/high data strobes
VDD	Voltage power supply
VDDQ	Voltage Power Supply for DQS
$V_{REF}DQ$/ $V_{REF}CA$	Power Supply for Reference
VDDSPD	SPD EEPROM Power Supply
SA0~SA1	I2C serial bus address select for EEPROM
SCL	I2C serial bus clock for EEPROM
SDA	I2C serial bus data for EEPROM
VSS	Ground
/RESET	Set DRAMs Known State
VTT	SDRAM I/O termination supply
NC	No Connection

Dimensions (Unit: millimeter)



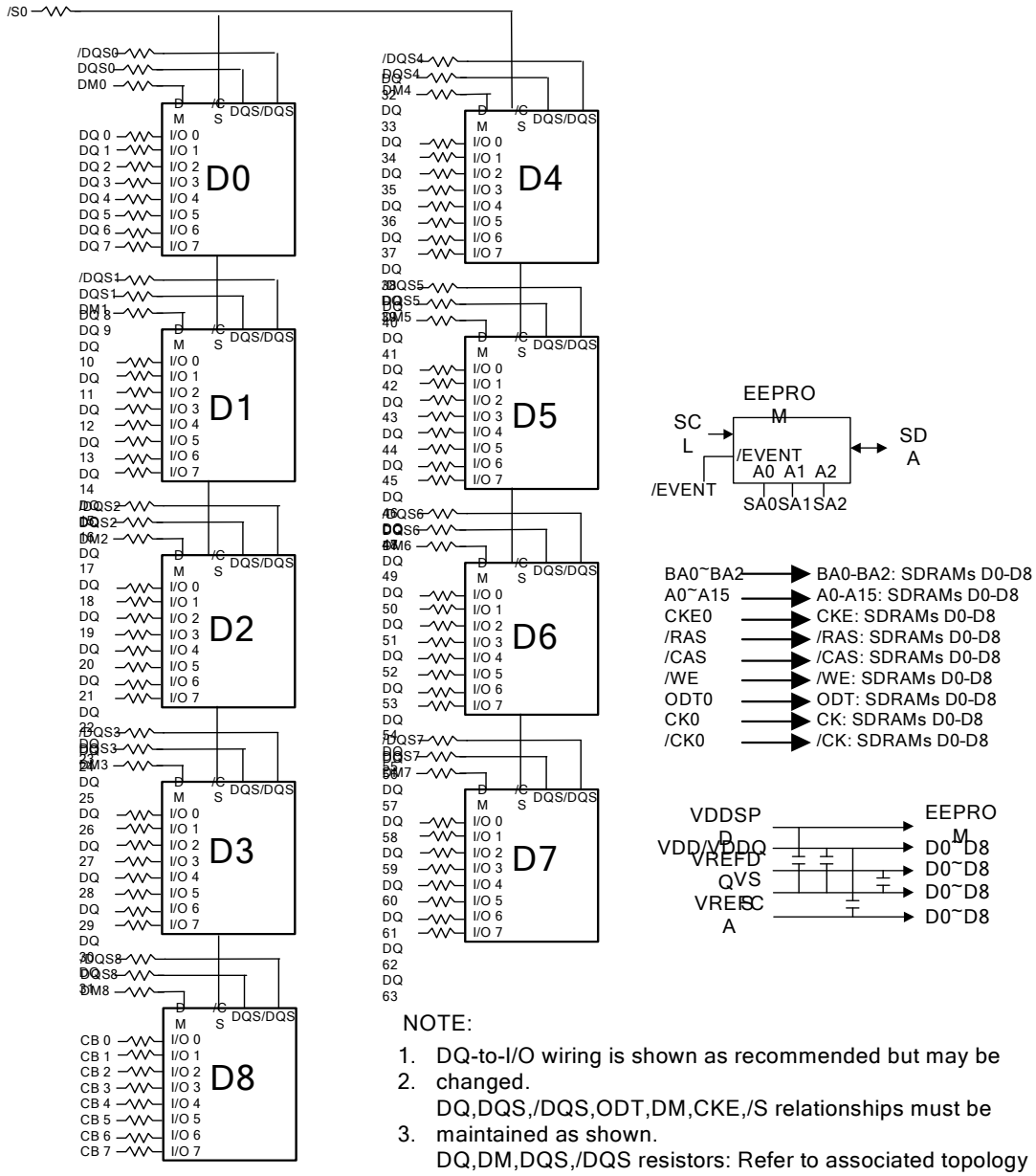
Note:
1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.

Pin Assignments

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	VREFDQ	69	CB0	137	VSS	02	VSS	70	VSS	138	VSS
03	VSS	71	CB1	139	/DQS4	04	DQ4	72	CB4	140	DM4
05	DQ0	73	VSS	141	DQS4	06	DQ5	74	CB5	142	DQ38
07	DQ1	75	/DQS8	143	VSS	08	VSS	76	DM8	144	DQ39
09	VSS	77	DQS8	145	DQ34	10	/DQS0	78	VSS	146	VSS
11	DM0	79	VSS	147	DQ35	12	DQS0	80	CB6	148	DQ44
13	DQ2	81	CB2	149	VSS	14	VSS	82	CB7	150	DQ45
15	DQ3	83	CB3	151	DQ40	16	DQ6	84	VREFCA	152	VSS
17	VSS	85	VDD	153	DQ41	18	DQ7	86	VDD	154	/DQS5
19	DQ8	87	CKE0	155	VSS	20	VSS	88	NC	156	DQS5
21	DQ9	89	CKE1	157	DM5	22	DQ12	90	A14	158	VSS
23	VSS	91	BA2	159	DQ42	24	DQ13	92	A9	160	DQ46
25	/DQS1	93	VDD	161	DQ43	26	VSS	94	VDD	162	DQ47
27	DQS1	95	A12	163	VSS	28	DM1	96	A11	164	VSS
29	VSS	97	A8	165	DQ48	30	/RESET	98	A7	166	DQ52
31	DQ10	99	A5	167	DQ49	32	VSS	100	A6	168	DQ53
33	DQ11	101	VDD	169	VSS	34	DQ14	102	VDD	170	VSS
35	VSS	103	A3	171	/DQS6	36	DQ15	104	A4	172	DM6
37	DQ16	105	A1	173	DQS6	38	VSS	106	A2	174	DQ54
39	DQ17	107	A0	175	VSS	40	DQ20	108	BA1	176	DQ55
41	VSS	109	VDD	177	DQ50	42	DQ21	110	VDD	178	VSS
43	/DQS2	111	CK0	179	DQ51	44	DM2	112	CK1	180	DQ60
45	DQS2	113	/CK0	181	VSS	46	VSS	114	/CK1	182	DQ61
47	VSS	115	VDD	183	DQ56	48	DQ22	116	VDD	184	VSS
49	DQ18	117	A10/AP	185	DQ57	50	DQ23	118	NC	186	/DQS7
51	DQ19	119	BA0	187	VSS	52	VSS	120	NC	188	DQS7
53	VSS	121	/WE	189	DM7	54	DQ28	122	/RAS	190	VSS
55	DQ24	123	VDD	191	DQ58	56	DQ29	124	VDD	192	DQ62
57	DQ25	125	/CAS	193	DQ59	58	VSS	126	ODT0	194	DQ63
59	DM3	127	/CS0	195	VSS	60	/DQS3	128	ODT1	196	VSS
61	VSS	129	/CS1	197	SA0	62	DQS3	130	A13	198	/EVENT
63	DQ26	131	VDD	199	VDDSPD	64	VSS	132	VDD	200	SDA
65	DQ27	133	DQ32	201	SA1	66	DQ30	134	DQ36	202	SCL
67	VSS	135	DQ33	203	Vtt	68	DQ31	136	DQ37	204	Vtt

/CS1,ODT1,CKE1：Used for dual-rank SO-DIMMs; NC on single-rank SO-DIMMs.
CK1 and /CK1：Used for dual-rank SO-DIMMs; not used on single-rank SO-DIMMs but terminated.

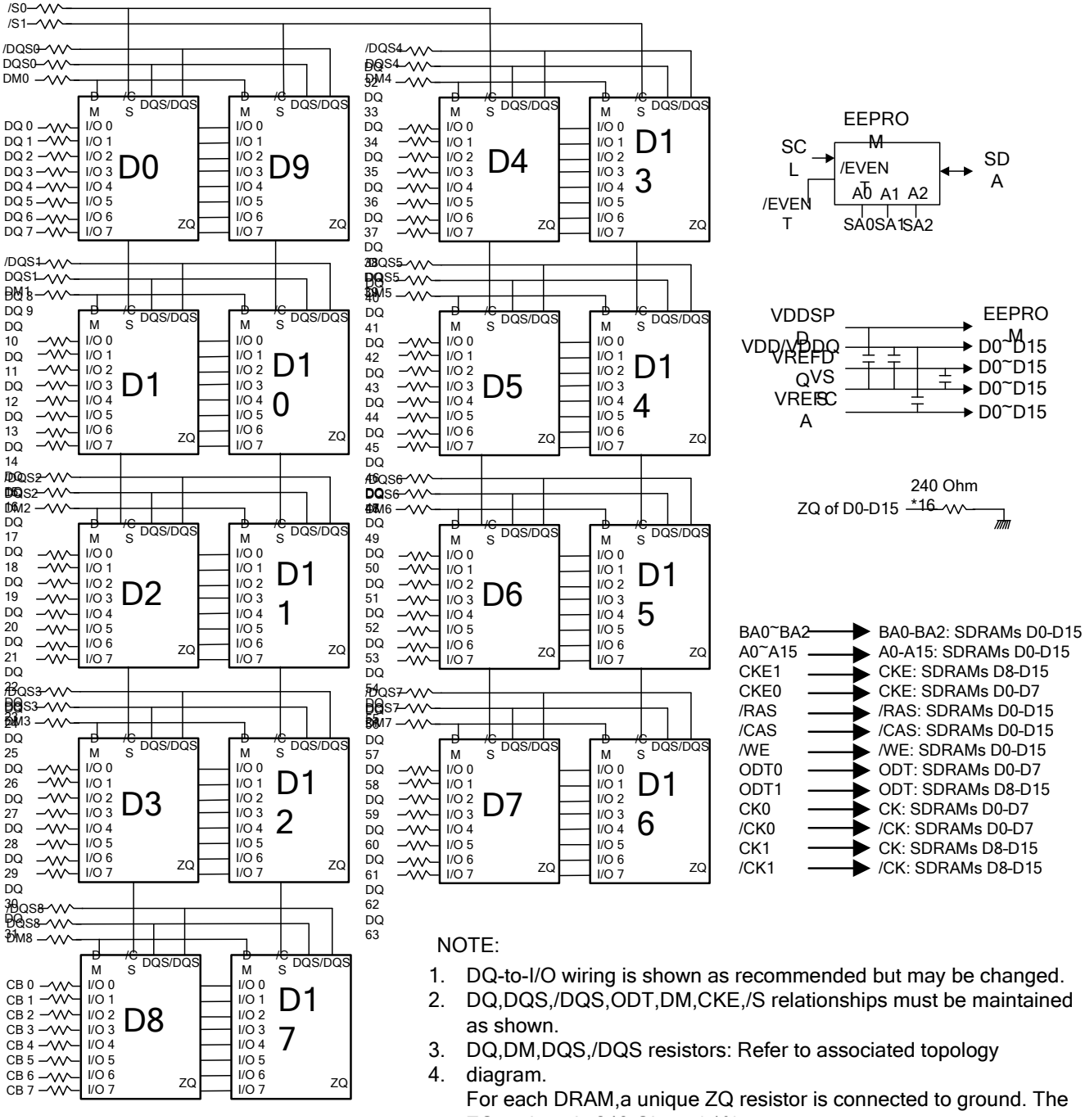
Block Diagram
2GB, 256Mx72 Module(1 Rank x8)



NOTE:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ,DQS,/DQS,ODT,DM,CKE,/S relationships must be maintained as shown.
3. DQ,DM,DQS,/DQS resistors: Refer to associated topology diagram.
4. For each DRAM, a unique ZQ resistor is connected to ground. The ZQ resistor is 240ohm +/- 1%.

Block Diagram
4GB, 512Mx72 Module(2 Rank x8)



NOTE:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ,DQS,/DQS,ODT,DM,CKE,/S relationships must be maintained as shown.
3. DQ,DM,DQS,/DQS resistors: Refer to associated topology
4. diagram.
   For each DRAM,a unique ZQ resistor is connected to ground. The

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	-40 to 85	°C	1,2

Note: 1. Operating Temperature is the ambient temperature.
2. At -40 ~ 85°C, operation temperature range are the temperature which all DRAM specification will be supported.

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on V_{DD} relative to Vss	VDD	-0.4 ~ 1.975	V	1
Voltage on V_{DDQ} pin relative to Vss	VDDQ	-0.4 ~ 1.975	V	1
Voltage on any pin relative to Vss	VIN, VOUT	-0.4 ~ 1.975	V	1
Storage temperature	T_{STG}	-55~+100	°C	1,2

Note:
1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC operating conditions (SSTL –1.5)

Parameter	Symbol	Rating			Unit	Note
		Min	Typ.	Max		
Supply voltage	VDD	1.425	1.5	1.575	V	1, 2
Supply voltage for Output	VDDQ	1.425	1.5	1.575	V	1, 2
I/O Reference Voltage (DQ)	$VREF_{DQ}$(DC)	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	3
I/O Reference Voltage (CMD/ADD)	$VREF_{CA}$(DC)	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	3
AC Input Logic High	$V_{IH(AC)}$	VREF+0.175	-	-	V	
AC Input Logic Low	$V_{IL(AC)}$	-	-	VREF-0.175	V	
DC Input Logic High	$V_{IH(DC)}$	V_{REF}+0.1	-	VDD	V	
DC Input Logic Low	$V_{IL(DC)}$	VSS	-	V_{REF}-0.1	V	

Note: There is no specific device VDD supply voltage requirement for SSTL-1.5 compliance.
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD, AC parameters are measured with VDD and VDDQ tied together.
3. Peak to peak AC noise on VREF may not allow deviate from VREF(DC) by more than +/-1% VDD.

AC Input Level for Differential Signals

Parameter	Symbol	Value		Unit	Note
Differential Input Logical High	V_{IHdiff}	+200	-	mV	
Differential Input Logical Low	V_{ILdiff}	-	-200		

IDD Specification parameters Definition(IDD values are for full operating range of Voltage and Temperature)

2GB, 256Mx72 Module(1 Rank x8)

Parameter	Symbol	DDR3 1333 CL9	Unit
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands;Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	450	mA
Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1	540	mA
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	135	mA
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	270	mA
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N	270	mA
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD3P	135	mA
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	315	mA
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD4R	855	mA
Operating burst write current; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R	IDD4W	855	mA
Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD5	1395	mA
Self refresh current; CK and /CK at 0V; CKE ≒ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD6	108	mA
Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), Trc = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS is HIGH between valid commands;Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;	IDD7	1215	mA

Note: 1.Module IDD was calculated on the specific brand DRAM component IDD and can be differently measured according to DQ loading capacitor.

4GB, 512Mx72 Module(2 Rank x8)

Parameter	Symbol	DDR3 1333 CL9	Unit
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands;Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	720	mA
Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1	810	mA
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	270	mA
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	540	mA
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N	540	mA
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD3P	270	mA
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	630	mA
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD4R	1125	mA
Operating burst write current; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R	IDD4W	1125	mA
Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD5	1665	mA
Self refresh current; CK and /CK at 0V; CKE ≒ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD6	216	mA
Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), Trc = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS is HIGH between valid commands;Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;	IDD7	1485	mA

Note: 1.Module IDD was calculated on the specific brand DRAM component IDD and can be differently measured according to DQ loading capacitor.

Timing Parameters & Specifications

Speed		DDR3 1333		Unit
Parameter	Symbol	Min	Max	
Average Clock Period	tCK	1.5	<1.875	ns
CK high-level width	tCH	0.47	0.53	tCK
CK low-level width	tCL	0.47	0.53	tCK
DQS, /DQS to DQ skew, per group, per access	tDQSQ	-	125	ps
DQ output hold time from DQS, /DQS	tQH	0.38	-	tCK
DQ low-impedance time from CK, /CK	tLZ(DQ)	-500	250	ps
DQ high-impedance time from CK, /CK	tHZ(DQ)	-	250	ps
Data setup time to DQS, /DQS reference to Vih(ac)Vil(ac) levels	tDS	30	-	ps
Data hold time to DQS, /DQS reference to Vih(ac)Vil(ac) levels	tDH	65	-	ps
DQ and DM input pulse width for each input	tDIPW	400	-	ps
DQS, /DQS Read preamble	tRPRE	0.9	-	tCK
DQS, /DQS differential Read postamble	tRPST	0.3	-	tCK
DQS, /DQS Write preamble	tWPRE	0.9	-	tCK
DQS, /DQS Write postamble	tWPST	0.3	-	tCK
DQS, /DQS low-impedance time	tLZ(DQS)	-500	250	ps
DQS, /DQS high-impedance time	tHZ(DQS)	-	250	ps
DQS, /DQS differential input low pulse width	tDQSL	0.45	0.55	tCK
DQS, /DQS differential input high pulse width	tDQSH	0.45	0.55	tCK
DQS, /DQS rising edge to CK, /CK rising edge	tDQSS	-0.25	+0.25	tCK
DQS, /DQS falling edge setup time to CK, /CK rising edge	tDSS	0.2	-	tCK
DQS, /DQS falling edge hold time to CK, /CK rising edge	tDSH	0.2	-	tCK
Delay from start of Internal write transaction to Internal read command	tWTR	Max (4tck, 7.5ns)	-	
Write recovery time	tWR	15	-	ns
Mode register set command cycle time	tMRD	4	-	tCK
/CAS to /CAS command delay	tCCD	4	-	nCK
Auto precharge write recovery + precharge time	tDAL	tWR+tRP/tck		nCK
Active to active command period for 1KB page size	tRRD	Max (4tck, 6ns)	-	ns
Active to active command period for 2KB page size	tRRD	Max (4tck, 7.5ns)	-	

Speed		DDR3 1333		Unit
Parameter	Symbol	Min	Max	
Four Activate Window for 1KB page size	tFAW	30	-	ns
Four Activate Window for 2KB page size products	tFAW	45	-	ns
Power-up and RESET calibration time	tZQinitl	512	-	tCK
Normal operation Full calibration time	tZQoper	256	-	tCK
Normal operation short calibration time	tZQcs	64	-	tCK
Exit self refresh to commands not requiring a locked DLL	tXS	Max (5tCK, tRFC+10)	-	
Exit self refresh to commands requiring a locked DLL	tXSDLL	tDLL(min)	-	tCK
Internal read to precharge command delay	tRTP	Max (4tCK, 7.5ns)	-	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCK(min)+1tCK	-	
Exit power down with DLL to any valid command: Exit Precharge Power Down with DLL	tXP	Max (3tCK, 6ns)	-	
CKE minimum pulse width (high and low pulse width)	tCKE	Max (3tCK,5.625ns)		
Asynchronous RTT turn-on delay (Power-Down mode)	tAONPD	2	8.5	ns
Asynchronous RTT turn-off delay (Power-Down mode)	tAOFPD	2	8.5	ns
ODT turn-on	tAON	-250	250	ps
ODT turn-off	tAOF	0.3	0.7	tCK

SERIAL PRESENCE DETECT SPECIFICATION

TS256MSK72V3N-I(TS7L8MDS0-0000) Serial Presence Detect			
Byte No.	**Function Described**	**Standard Specification**	**Vendor Part**
0	Number of SPD Bytes written / SPD device size / CRC coverage during module production	CRC:0-116Byte SPD Byte use: 176Byte SPD Byte total: 256Byte	92
1	SPD Revision	Version 1.0	10
2	Key Byte / DRAM Device Type	DDR3 SDRAM	0B
3	Key Byte / Module Type	ECC SODIMM	08
4	SDRAM Density and Banks	2GB 8banks	03
5	SDRAM Addressing	ROW:15, Column:10	19
6	Reserved	-	00
7	Module Organization	1Rank / x8	01
8	Module Memory Bus Width	ECC, 72bit	0B
9	Fine Timebase Dividend and Divisor	2.5ps	52
10	Medium Timebase Dividend	0.125ns	01
11	Medium Timebase Divisor	0.125ns	08
12	SDRAM Minimum Cycle Time (tCKmin)	1.5ns	0C
13	Reserved	-	00
14	CAS Latencies Supported, Least Significant Byte	5, 6, 7, 8, 9	3E
15	CAS Latencies Supported, Most Significant Byte	5, 6, 7, 8, 9	00
16	Minimum CAS Latency Time (tAAmin)	13.125ns	69
17	Minimum Write Recovery Time (tWRmin)	15ns	78
18	Minimum /RAS to /CAS Delay Time (tRCDmin)	13.125ns	69
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	6ns	30
20	Minimum Row Precharge Time (tRPmin)	13.125ns	69
21	Upper Nibble for tRAS and tRC	-	11
22	Minmum Active to Precharge Time (tRASmin)	36ns	20
23	Minmum Active to Active/Refresh Time (tRCmin)	49.125ns	89
24	Minmum Refresh Recovery Time (tRFCmin), Least Significant Byte	160ns	00
25	Minmum Refresh Recovery Time (tRFCmin), Most Significant Byte	160ns	05
26	Minmum Internal Write to Read Command Delay Time (tWTmin)	7.5ns	3C
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5ns	3C
28	Upper Nibble for tFAW	30ns	00
29	Minmum Four Active Window Delay Time	30ns	F0

	(tFAWmin)							
30	SDRAM Optional Features	DLL off Mode, RZQ/6, RZQ/7	83					
31	SDRAM Thermal and Refresh Options	No ODTs, No ASR	01					
32	DDR3-MODULE THERMAL SENSOR	Support TS	80					
33-59	Reserved	-	00					
60	Module Nominal Height	30mm	0F					
61	Module Max Thickness	Planar Double Sides	11					
62	Reference Raw Card Used	No Jedec Raw Card	1F					
63	Address Mapping from Edge Connector to DRAM	Standard	00					
64-116	Reserved	-	00					
117	Module Manufacturer ID Code, Least Significant Byte	Transcend	01					
118	Module Manufacturer ID Code, Most Significant Byte	Transcend	4F					
119	Module Manufacturing Location	Taipei	54					
120-121	Module Manufacturing Date	-	00					
122-125	Module Serial Number	-	00					
126-127	Cyclical Redundancy Code	-	70,53					
128-145	Module Part Number	TS256MSK72V3N-I(TS7L8MDS0-0000)	54	53	32	35	36	4D
			53	4B	37	32	56	33
			4E	2D	49	20	20	20
146-147	Revision Code	-	00					
148-149	DRAM Manufacturer ID Code	By Manufacturer	Variable					
150-175	Manufacturer Specific Data	By Manufacturer	Variable					
176-255	Open for customer use	Undefined	00					

TS512MSK72V3N-I(TS8L8MDS0-0000) Serial Presence Detect			
Byte No.	**Function Described**	**Standard Specification**	**Vendor Part**
0	Number of SPD Bytes written / SPD device size / CRC coverage during module production	CRC:0-116Byte SPD Byte use: 176Byte SPD Byte total: 256Byte	92
1	SPD Revision	Version 1.0	10
2	Key Byte / DRAM Device Type	DDR3 SDRAM	0B
3	Key Byte / Module Type	ECC SODIMM	08
4	SDRAM Density and Banks	2GB 8banks	03
5	SDRAM Addressing	ROW:15, Column:10	19
6	Reserved	-	00
7	Module Organization	2Rank / x8	09
8	Module Memory Bus Width	ECC, 72bit	0B
9	Fine Timebase Dividend and Divisor	2.5ps	52
10	Medium Timebase Dividend	0.125ns	01
11	Medium Timebase Divisor	0.125ns	08
12	SDRAM Minimum Cycle Time (tCKmin)	1.5ns	0C
13	Reserved	-	00
14	CAS Latencies Supported, Least Significant Byte	5, 6, 7, 8, 9	3E
15	CAS Latencies Supported, Most Significant Byte	5, 6, 7, 8, 9	00
16	Minimum CAS Latency Time (tAAmin)	13.125ns	69
17	Minimum Write Recovery Time (tWRmin)	15ns	78
18	Minimum /RAS to /CAS Delay Time (tRCDmin)	13.125ns	69
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	6ns	30
20	Minimum Row Precharge Time (tRPmin)	13.125ns	69
21	Upper Nibble for tRAS and tRC	-	11
22	Minmum Active to Precharge Time (tRASmin)	36ns	20
23	Minmum Active to Active/Refresh Time (tRCmin)	49.125ns	89
24	Minmum Refresh Recovery Time (tRFCmin), Least Significant Byte	160ns	00
25	Minmum Refresh Recovery Time	160ns	05

	(tRFCmin), Most Significant Byte		
26	Minmum Internal Write to Read Command Delay Time (tWTmin)	7.5ns	3C
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5ns	3C
28	Upper Nibble for tFAW	30ns	00
29	Minmum Four Active Window Delay Time (tFAWmin)	30ns	F0
30	SDRAM Optional Features	DLL off Mode, RZQ/6, RZQ/7	83
31	SDRAM Thermal and Refresh Options	No ODTs, No ASR	01
32	DDR3-MODULE THERMAL SENSOR	Support TS	80
33-59	Reserved	-	00
60	Module Nominal Height	30mm	0F
61	Module Max Thickness	Planar Double Sides	11
62	Reference Raw Card Used	No Jedec Raw Card	1F
63	Address Mapping from Edge Connector to DRAM	Standard	00
64-116	Reserved	-	00
117	Module Manufacturer ID Code, Least Significant Byte	Transcend	01
118	Module Manufacturer ID Code, Most Significant Byte	Transcend	4F
119	Module Manufacturing Location	Taipei	54
120-121	Module Manufacturing Date	-	00
122-125	Module Serial Number	-	00
126-127	Cyclical Redundancy Code	-	AB, 7F
128-145	Module Part Number	TS512MSK72V3N-I(TS8L8MDS0-0000)	54 53 35 31 32 4D 53 4B 37 32 56 33 4E 2D 49 20 20 20
146-147	Revision Code	-	00
148-149	DRAM Manufacturer ID Code	By Manufacturer	Variable
150-175	Manufacturer Specific Data	By Manufacturer	Variable
176-255	Open for customer use	Undefined	00

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