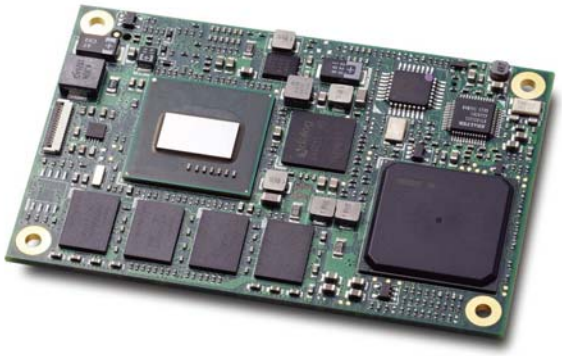
COM Express

COM.0 Rev. 2.0 Type 10

nanoX-TC

User's Manual



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ADLINK TECHNOLOGY INC.

Revision History

Release	Date	Change
2.00	2011/07/11	Initial release
2.01	2013/04/01	Correct PCIe port used for EG20T PCH

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Preface

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Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

Additional information, aids, and tips that help users perform tasks.

Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

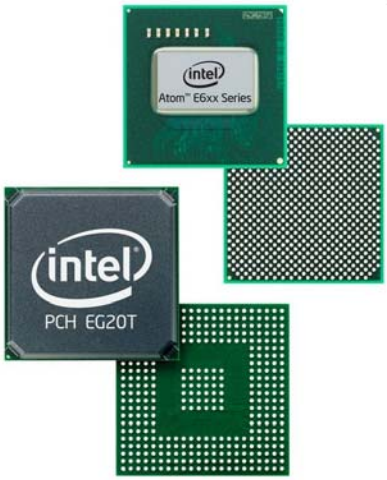
Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

1 Introduction

1.1 Description

No bigger in size than a business card, the nanoX-TC is a COM Express™ Mini form factor Type 10 computer-on-module that targets battery powered, mobile and handheld system designs. The new Mini size form factor with a footprint of just 55 mm x 84 mm is the smallest size in ADLINK's COM Express product lineup, next to the Basic size (125 mm x 95 mm) and Compact size (95x95) form factors.

The nanoX-TC is based on the Intel® Atom™ Processor E6xx with less than 3.9 W thermal design power (TDP). These new 45nm Intel architecture processors implement ground-breaking power management techniques, making them ideal for thermally constrained and fanless embedded applications. The Processor E6xx series offers an integrated 2D/3D graphics engine with hardware encode/decode, LVDS and SDVO output, HD Audio, PCI Express, and support for Intel® Hyper-Threading and Intel® Virtualization Technology.



The Intel® EG20T Platform Controller Hub (PCH) provides additional I/O flexibility with SATA, UART, CAN bus, Gigabit Ethernet and USB host/client support.

The nanoX-TC allows for innovative designs in mobile and "light" computing, including portable and mobile equipment for the automotive and test and measurement industries, visual communication and in the medical field. Using the Intel® Atom™ Processor E6xx and Intel® EG20T PCH chipset, the nanoX-TC allows developers to utilize a wide variety of mainstream software applications and middleware familiar to end users that will run unmodified with full functionality on this platform.

2 Specifications

2.1 Core system

- **CPU**

  - Intel® Atom™ E680, 1.6 GHz, 3.9 W TDP
  - Intel® Atom™ E660, 1.3 GHz, 3.3 W TDP
  - Intel® Atom™ E640, 1.0 GHz, 3.3 W TDP
  - Intel® Atom™ E620, 600 MHz, 2.7 W TDP

All processors support Intel® Hyper-Threading and Intel® Virtualization Technology

- **L2 Cache**: 512 KB on all processors
- **Memory:** Soldered 512 MB or 1 GB unbuffered DDR2 at 800 MHz
- **BIOS:** AMI UEFI BIOS
- **Hardware Monitor**: Supply voltages and CPU temperature
- **Debug Interface:** XDP SFF-26 extension for ICE debug
- **Embedded Features:** Instant on with Intel Bootloader support, OEM BIOS settings, Board Info & Statistics, ACPI 3.0, Smart Battery Management support, Watchdog with programmable timer ranges.
- **Expansion Busses to carrier board:**
  - 4 PCI Express x1 (0/1/2/3, port 0 is optionally used for EG20T PCH; no PCIe x4 support)
  - LPC Bus, SMBus (system) , I2C (user)
  - 4 GPI and 4 GPO (shared with SDIO on optional EG20T)
  - SPI (supports BIOS only)

2.2 Video

- **2D/3D Graphics Engine:** Integrated in Intel® Atom™ E6xx Processor
- **Decoding** MPEG2, MPEG4, VC1, WMV9, H.264 and DivX
- **Encoding** MPEG4, H.264 (baseline at L3)

- **LVDS Interface:** Single channel 18- or 24-bit pixel color depths with maximum resolution of up to 1280x768 @ 60 Hz. Pixel clock rate between 19.75 MHz (minimum) and 80 MHz (maximum)
- **SDVO:** Serial digital video output supporting devices for DVI, TV-out, analog VGA. Maximum resolution of up to 1280x1024 @ 85 Hz and pixel clock rate up to 160 MHz.

2.3 Audio

- **Chipset:** Integrated in Intel® Atom™ Processor E6xx
- **Type**: Multi-channel audio stream, 32-bit sample depth, sample rate up to 192 kHz

2.4 LAN

- **GbE MAC:** Integrated in Intel® EG20T PCH
- **PHY:** Realtek RTL8211CL
- **Speed**: 10/100/1000 Mbps

2.5 Multi I/O

- **Chipset:** Integrated in Intel® PCH EG20T
- **USB:** Six USB 1.1/2.0 host ports and one USB 1.1/2.0 client port
- **SATA:** Two ports supporting SATA 1.5 Gb/s and 3 Gb/s
- **SDIO Port:** SDIO/MMC supporting SDHC speed class 6 (shared with GPIO)
- **SDIO Storage:** TBD
- **Serial and CAN:** One RS-232 (RX/TX) and one CAN (AX/RX) port (optional 2x RS-232 w/o CAN)

2.6 Super I/O

- Connected to LPC bus on carrier if needed (standard support for Winbond W83627DHG)

2.7 SDIO/MMC Extension

- **Chipset:** Integrated in Intel® Controller Hub
- **Type**: Single port SDIO/MMC supports SDIO specification 1.1 and MMC specification 4.0
- **Connection**: Multiplexed over GPIO signals to carrier

2.8 Operating Systems

- **Standard Support**
  - Windows 7
  - Linux 2.6.x
- **Extended Support (BSP)**
  - Linux BSP
  - AIDI I2C Library for Windows and Linux
  - WinCE 6.0 / 7.0
  - Windows XP Embedded

2.9 Mechanical and Environmental

- **Standard Operating Temperature:** 0°C to 60°C
- **Relative Humidity:** up to 90% at 55°C
- **Form Factor and Type:** PICMG COM.0, COM Express™ Type 10 compatible
- **Dimensions:** 85 x 55 mm

2.10 Power Specifications

- **Input Power:** 4.75 V – 21 V wide range, supports AT mode and ATX mode (with additional 5 Vsb)
- **Power States:** Supports S0, S3, S4, S5
- **Power Consumption:** 6W at 5V typical, 5W idle
- **Smart Battery Support:** Yes

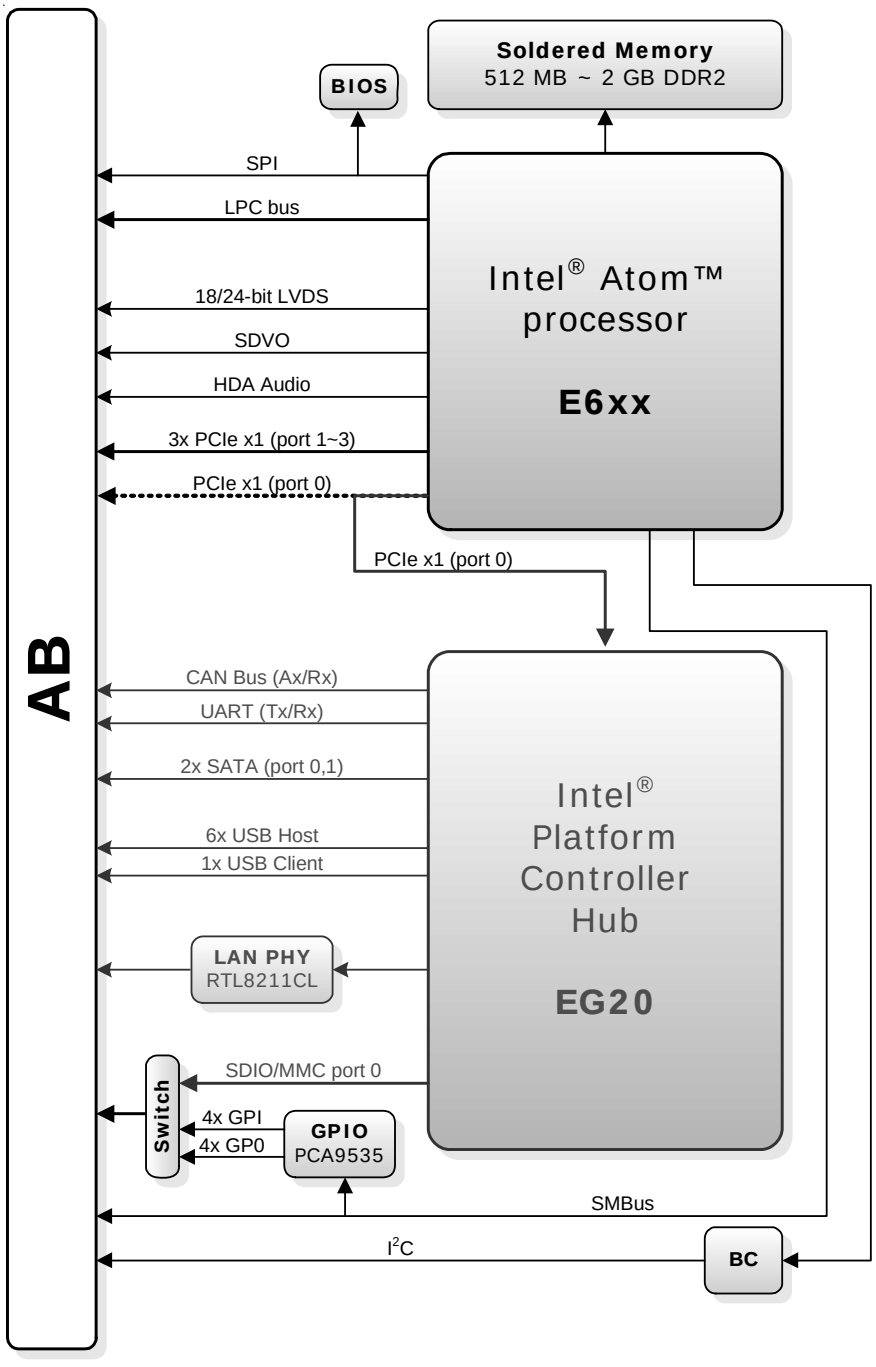
2.11 Power Consumption

	Power Consumption [W]				
	12V	12V	12V	5Vsb	5Vsb
	Idle WinXP Login	**Max Load** WinXP Burnin/Kpower	**S1** Standby Powered On	**S3** Suspend to RAM	**S5** Soft Off
nanoX-TC-E620 (2G)	4.5	5.5	N/A	1.3	0.4
nanoX-TC-E640 (2G)	4.7	6.3	N/A	1.4	0.4
nanoX-TC-E660 (2G)	5.0	6.6	N/A	1.4	0.4
nanoX-TC-E680 (2G)	5.2	7.4	N/A	1.3	0.4

2.12 Ordering Codes

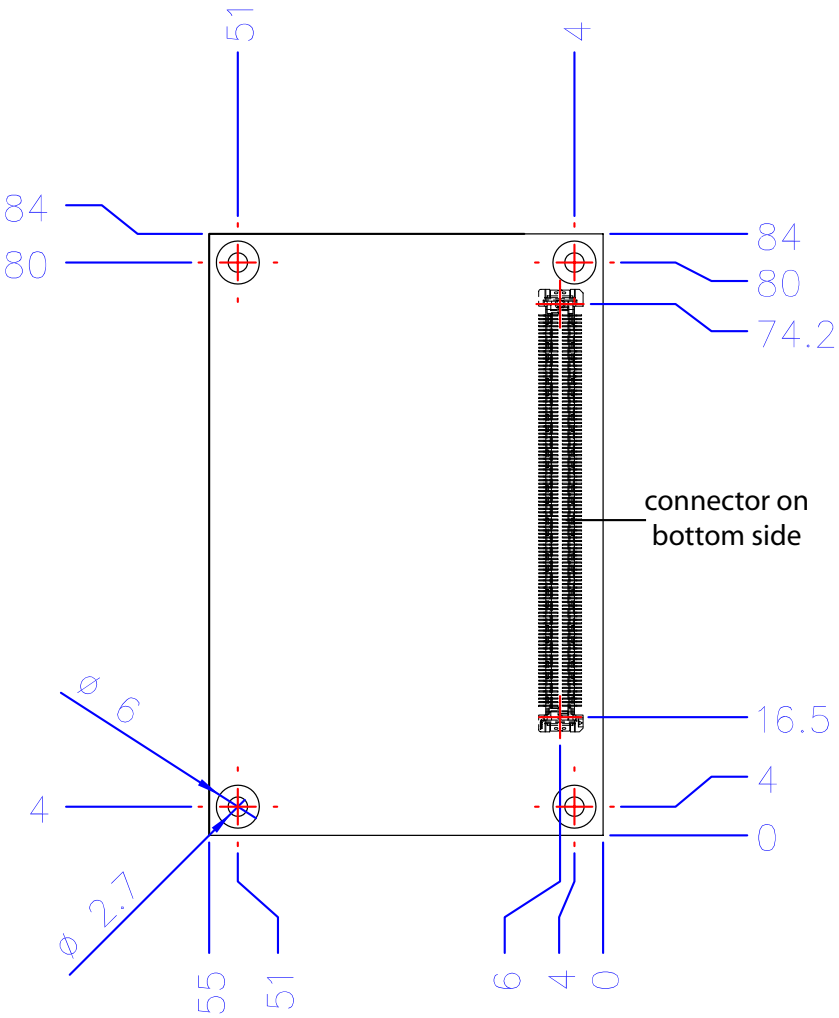
- **nanoX-TC-E680-1G:** Mini size COM Express Type 10 Module with Intel® Atom™ E680 processor at 1.6GHz, PCH EG20T and 1 GB DDR2 SDRAM
- **nanoX-TC-E660-1G:** Mini size COM Express Type 10 Module with Intel® Atom™ E660 processor at 1.3GHz, PCH EG20T, and 1 GB DDR2 SDRAM
- **nanoX-TC-E640-1G:** Mini size COM Express Type 10 Module with Intel® Atom™ E640 processor at 1.1GHz, PCH EG20T, and 1 GB DDR2 SDRAM
- **nanoX-TC-E620-1G:** Mini size COM Express Type 10 Module with Intel® Atom™ E620 processor at 600 MHz, PCH EG20T, and 1 GB DDR2 SDRAM

3 Functional Diagram

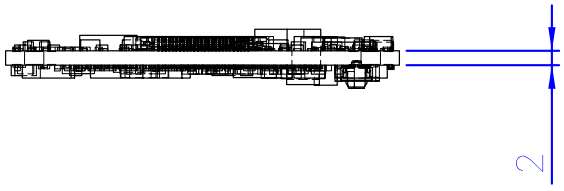


4 Mechanical Dimensions

Top View



Side View



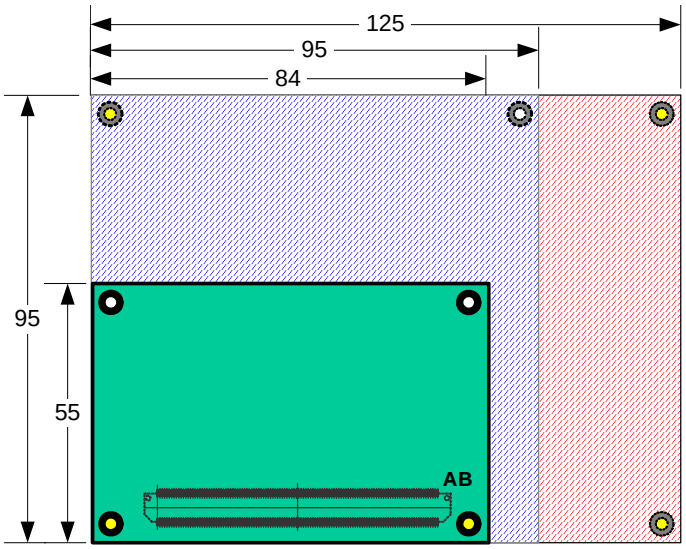
All ∅ tolerances ± 0.05 mm
Other tolerances ± 0.2 mm

5 Pinout and Signal Descriptions

5.1 COM Express™ Type 10 Pinout

All pinouts on AB connector of the nanoX-TC comply with pin-out and signal descriptions used in the "**PICMG® COM.0 R2.0: COM Express® Module Base Specification Type 2"**. This chapter details pinouts, signal descriptions, and mechanical characteristics of the nanoX-TC.

An additional document, the **"PICMG COM Express Design Guide"** gives a general introduction to carrier board designs for COM Express™ modules.



- Gigabit Ethernet port
- LPC interface
- 4 Serial ATA channels
- AC'97 or High Definition Audio
- 6 USB 2.0 ports
- 6 PCI Express x1 Lanes
- Dual 24-bit LVDS channels
- SDVO
- GPIO / SDIO
- Keyboard
- I²C / SMBus
-SPI support
- Primary power input: +12V, +5V standby and 3.3V RTC

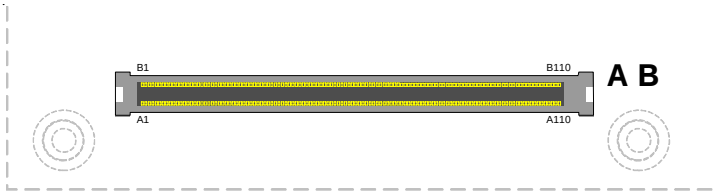
AB Connector

Dimensions in mm

NOTE: The above function mappings are a generic description of COM Express pinouts, and not necessarily supported on the module described in this manual.

5.2 Pin Definitions

Pinouts comply with COM Express Type 10



Pin	Row A	Row B
1	GND(FIXED)	GND(FIXED)
2	GBE0_MDI3-	GBE0_ACT#
3	GBE0_MDI3+	LPC_FRAME#
4	GBE0_LINK100#	LPC_AD0
5	GBE0_LINK1000#	LPC_AD1
6	GBE0_MDI2-	LPC_AD2
7	GBE0_MDI2+	LPC_AD3
8	GBE0_LINK#	~~LPC_DRQ0#~~
9	GBE0_MDI1-	~~LPC_DRQ1#~~
10	GBE0_MDI1+	LPC_CLK
11	GND(FIXED)	GND(FIXED)
12	GBE0_MDI0-	PWRBTN#
13	GBE0_MDI0+	SMB_CK
14	~~GBE0_CTREF~~	SMB_DAT
15	SUS_S3#	SMB_ALERT#
16	SATA0_TX+	SATA1_TX+
17	SATA0_TX-	SATA1_TX-
18	SUS_S4#	~~SUS_STAT#~~
19	SATA0_RX+	SATA1_RX+
20	SATA0_RX-	SATA1_RX-
21	GND(FIXED)	GND(FIXED)
22	RSVD	RSVD
23	RSVD	RSVD
24	SUS_S5#	PWR_OK
25	RSVD	RSVD
26	RSVD	RSVD
27	BATLOW#	WDT
28	(S)ATA_ACT#	~~AC/HDA_SDIN2~~
29	AC/HDA_SYNC	AC/HDA_SDIN1
30	AC/HDA_RST#	AC/HDA_SDIN0
31	GND(FIXED)	GND(FIXED)
32	AC/HDA_BITCLK	SPKR
33	AC/HDA_SDOUT	I2C_CK
34	BIOS_DIS0#	I2C_DAT
35	THRMTRIP#	THRM#
36	USB6-	USB7-
37	USB6+	USB7+
38	USB_6_7_OC#	USB_4_5_OC#
39	USB4-	USB5-
40	USB4+	USB5+
41	GND(FIXED)	GND(FIXED)
42	USB2-	USB3-
43	USB2+	USB3+
44	USB_2_3_OC#	USB_0_1_OC#
45	USB0-	USB1-
46	USB0+	USB1+
47	VCC_RTC	~~EXCD1_PERST#~~
48	~~EXCD0_PERST#~~	~~EXCD1_CPPE#~~
49	~~EXCD0_CPPE#~~	SYS_RESET#
50	LPC_SERIRQ	CB_RESET#
51	GND(FIXED)	GND(FIXED)
52	RSVD	RSVD
53	RSVD	RSVD
54	GPI0	GPO1
55	RSVD	RSVD

Pin	Row A	Row B
56	RSVD	RSVD
57	GND	GPO2
58	PCIE_TX3+	PCIE_RX3+
59	PCIE_TX3-	PCIE_RX3-
60	GND(FIXED)	GND(FIXED)
61	PCIE_TX2+	PCIE_RX2+
62	PCIE_TX2-	PCIE_RX2-
63	GPI1	GPO3
64	PCIE_TX1+	PCIE_RX1+
65	PCIE_TX1-	PCIE_RX1-
66	GND	WAKE0#
67	GPI2	WAKE1#
68	PCIE_TX0+	PCIE_RX0+
69	PCIE_TX0-	PCIE_RX0-
70	GND(FIXED)	GND(FIXED)
71	LVDS_A0+	DDI0_PAIR0+
72	LVDS_A0-	DDI0_PAIR0-
73	LVDS_A1+	DDI0_PAIR1+
74	LVDS_A1-	DDI0_PAIR1-
75	LVDS_A2+	DDI0_PAIR2+
76	LVDS_A2-	DDI0_PAIR2-
77	LVDS_VDD_EN	DDI0_PAIR4+
78	LVDS_A3+	DDI0_PAIR4-
79	LVDS_A3-	LVDS_BKLT_EN
80	GND(FIXED)	GND(FIXED)
81	LVDS_A_CK+	DDI0_PAIR3+
82	LVDS_A_CK-	DDI0_PAIR3-
83	LVDS_I2C_CK	LVDS_BKLT_CTRL
84	LVDS_I2C_DAT	VCC_5V_SBY
85	GPI3	VCC_5V_SBY
86	RSVD	VCC_5V_SBY
87	RSVD	VCC_5V_SBY
88	PCIE_CLK_REF+	BIOS_DIS1#
89	PCIE_CLK_REF-	~~DD0_HPD~~
90	GND(FIXED)	GND(FIXED)
91	SPI_POWER	DDI0_PAIR5+
92	SPI_MISO	DDI0_PAIR5-
93	GPO0	DDI0_PAIR6+
94	SPI_CLK	DDI0_PAIR6-
95	SPI_MOSI	DDI0_DDC_AUX_SEL
96	TPM_PP	RSVD
97	TYPE10#	SPI_CS#
98	SER0_TX	DDI0_CTRLCLK_AUX+
99	SER0_RX	DDI0_CTRLDATA_AUX-
100	GND(FIXED)	GND(FIXED)
101	SER1_TX	FAN_PWMOUT
102	SER1_RX	FAN_TACHIN
103	LID#	SLEEP#
104	VCC_12V	VCC_12V
105	VCC_12V	VCC_12V
106	VCC_12V	VCC_12V
107	VCC_12V	VCC_12V
108	VCC_12V	VCC_12V
109	VCC_12V	VCC_12V
110	GND(FIXED)	GND(FIXED)

NOTE: ~~XXX~~ Strikethrough pin names indicates that the signal is not supported on this module.

5.3 Signal Descriptions

Row A

Pin	Signal	Description	Type	PU/PD	Comment
A1	GND(FIXED)	Ground	PWR	-	-
A2	GBE0_MDI3-	Ethernet Media Dependent Interface -	I/O - DP	-	-
A3	GBE0_MDI3+	Ethernet Media Dependent Interface +	I/O - DP	-	-
A4	GBE0_LINK100#	Ethernet 100 Mbit/sec Link Indicator	OD	-	On at 100Mb/s
A5	GBE0_LINK1000#	Ethernet 1000 Mbit/sec Link Indicator	OD	-	On at 1000Mb/s
A6	GBE0_MDI2-	Ethernet Media Dependent Interface -	I/O - DP	-	-
A7	GBE0_MDI2+	Ethernet Media Dependent Interface +	I/O - DP	-	-
A8	GBE0_LINK#	Ethernet Llink Indicator (all speeds)	O-3.3	-	-
A9	GBE0_MDI1-	Ethernet Media Dependent Interface -	I/O - DP	-	-
A10	GBE0_MDI1+	Ethernet Media Dependent Interface +	I/O - DP	-	-
A11	GND(FIXED)	Ground	PWR	-	-
A12	GBE0_MDI0-	Ethernet Media Dependent Interface -	I/O - DP	-	-
A13	GBE0_MDI0+	Ethernet Media Dependent Interface +	I/O - DP	-	-
A14	~~GBE0_CTREF~~	~~Ethernet center tap reference voltage~~	NC	-	not supported
A15	SUS_S3#	S3 Suspend to RAM inidcator	O-3.3	-	-
A16	SATA0_TX+	SATA 0 Transmit Data +	O - DP	-	-
A17	SATA0_TX-	SATA 0 Transmit Data -	O - DP	-	-
A18	SUS_S4#	S4 Hibernation inidcator	O-3.3	-	-
A19	SATA0_RX+	SATA 0 Receive Data +	I - DP	-	-
A20	SATA0_RX-	SATA 0 Receive Data -	I - DP	-	-
A21	GND(FIXED)	Ground	PWR	-	-
A22	RSVD	Clock sync signal to Dialog	CLK IN	-	-
A23	RSVD		NC	-	-
A24	SUS_S5#	S5 Soft Off inidcator	O-3.3	-	-
A25	RSVD		NC	-	-
A26	RSVD		NC	-	-
A27	BATLOW#	Battery Low Input	I-3.3	-	-
A28	(S)ATA_ACT#	SATA LED	O-3.3	PU 10k 3.3V	-
A29	AC/HDA_SYNC	HDA Sync	O-3.3	-	-
A30	AC/HDA_RST#	HDA Reset	O-3.3	-	-
A31	GND(FIXED)	Ground	PWR	-	-
A32	AC/HDA_BITCLK	HDA Clock	O-3.3	-	-
A33	AC/HDA_SDOUT	HDA Data	O-3.3	-	-
A34	BIOS_DIS0#	LPC_BIOS boot device selection	I-3.3	PU 10k 3.3V	-
A35	THRMTRIP#	CPU Thermal shudown inidcator	O-3.3	PU 1k 3.3V	-
A36	USB6-	USB Data - Port6	I/O - DP	-	-
A37	USB6+	USB Data + Port6	I/O - DP	-	-
A38	USB_6_7_OC#	USB OverCurrent Port 6/7	I-3.3	PU 10k 3.3Vsb	-
A39	USB4-	USB Data - Port4	I/O - DP	-	-
A40	USB4+	USB Data + Port4	I/O - DP	-	-
A41	GND(FIXED)	Ground	PWR	-	-
A42	USB2-	USB Data - Port2	I/O - DP	-	-
A43	USB2+	USB Data + Port2	I/O - DP	-	-
A44	USB_2_3_OC#	USB OverCurrent Port 2/3	I-3.3	PU 10k 3.3Vsb	-
A45	USB0-	USB Data - Port0	I/O - DP	-	-
A46	USB0+	USB Data + Port0	I/O - DP	-	-
A47	VCC_RTC	External RTC battery power	PWR	-	-
A48	~~EXCD0_PERST#~~	~~Express Card Support [0]	card reset~~	O-3.3	PU 10k 3.3V	not supported
A49	~~EXCD0_CPPE#~~	~~Express Card Support [0]	cap. card req.~~	I-3.3	PU 10k 3.3V	not supported
A50	LPC_SERIRQ	LPC INT_SERIRQ	Serial Interrupt Request	IO-3.3	PU 10k 3.3V	-
A51	GND(FIXED)	Ground	PWR	-	-
A52	RSVD		NC	-	-
A53	RSVD		NC	-	-
A54	GPI0	GPI0 or SDIO controller 0 data 0	IO-3.3	PU 10k 3.3V	BIOS select
A55	RSVD		NC	-	-

~~XXX~~ Strikethrough pin names indicates that the signal is not supported on this module.

Signal Descriptions (cont'd)

Row A

Pin	Signal	Description	Type	PU/PD	Comment
A56	RSVD		NC	-	-
A57	GND	Ground	PWR	-	-
A58	PCIE_TX3+	PCIe 3 TX+ (port 0 of CPU, occupied)	O - DP	-	used for PCH EG20T
A59	PCIE_TX3-	PCIe 3 TX- (port 0 of CPU, occupied)	O - DP	-	used for PCH EG20T
A60	GND(FIXED)	Ground	PWR	-	-
A61	PCIE_TX2+	PCIe 2 TX+ (port 3 of CPU)	O - DP	-	-
A62	PCIE_TX2-	PCIe 2 TX- (port 3 of CPU)	O - DP	-	-
A63	GPI1	GPI1 or SDIO controller 0 data 1	IO-3.3	PU 10k 3.3V	BIOS select
A64	PCIE_TX1+	PCIe 1 TX+ (port 2 of CPU)	O - DP	-	-
A65	PCIE_TX1-	PCIe 1 TX- (port 2 of CPU)	O - DP	-	-
A66	GND	Ground	PWR	-	-
A67	GPI2	GPI2 or SDIO controller 0 data 2	IO-3.3	PU 10k 3.3V	BIOS select
A68	PCIE_TX0+	PCIe 0 TX+ (port 1 of CPU)	O - DP	-	-
A69	PCIE_TX0-	PCIe 0 TX- (port 1 of CPU)	O - DP	-	-
A70	GND(FIXED)	Ground	PWR	-	-
A71	LVDS_A0+	LVDS Channel A	O - DP	-	-
A72	LVDS_A0-	LVDS Channel A	O - DP	-	-
A73	LVDS_A1+	LVDS Channel A	O - DP	-	-
A74	LVDS_A1-	LVDS Channel A	O - DP	-	-
A75	LVDS_A2+	LVDS Channel A	O - DP	-	-
A76	LVDS_A2-	LVDS Channel A	O - DP	-	-
A77	LVDS_VDD_EN	LVDS VDD Panel Power	O-2,5	PD 10k	-
A78	LVDS_A3+	LVDS Channel A	O - DP	-	-
A79	LVDS_A3-	LVDS Channel A	O - DP	-	-
A80	GND(FIXED)	Ground	PWR	-	-
A81	LVDS_A_CK+	LVDS Channel A Clock	O - DP	-	-
A82	LVDS_A_CK-	LVDS Channel A Clock	O - DP	-	-
A83	LVDS_I2C_CK	LVDS I2C Clock	IO-3.3	PU 2.2k 3.3V	-
A84	LVDS_I2C_DAT	LVDS I2C Data	IO-3.3	PU 2.2k 3.3V	-
A85	GPI3	GPI3 or SDIO controller 0 data 3	IO-3.3	PU 10k 3.3V	BIOS select
A86	RSVD		NC	-	-
A87	RSVD		NC	-	-
A88	PCIE_CLK_REF+	PCI Express Clock Reference	O - DP	-	-
A89	PCIE_CLK_REF-	PCI Express Clock Reference	O - DP	-	-
A90	GND(FIXED)	Ground	PWR	-	-
A91	SPI_POWER	Power source for SPI devices on carrier	PWR	-	-
A92	SPI_MISO	Data in to Module from Carrier SPI	I-3.3	-	
A93	GPO0	GPO0 or SDIO controller 0 clock	O-3.3	PU 10k 3.3V	BIOS select
A94	SPI_CLK	Clock from Module to Carrier SPI	O-3.3	-	
A95	SPI_MOSI	Data out from Module to Carrier SPI	O-3.3	-	
A96	TPM_PP	(TPM) Physical Presence pin	I-3.3	-	
A97	TYPE10#	Rev 2.0 / Type 10 indicator to carrier	STO	PD 4.7k	-
A98	SER0_TX	Serial 0 port transmitter	O-5	-	
A99	SER0_RX	Serial 0 port receiver	I-5	-	
A100	GND(FIXED)	Ground	PWR	-	-
A101	SER1_TX	Serial 1 port transmitter / or CAN CAN_AX	O-5	-	
A102	SER1_RX	Serial 1 port receiver / or CAN CAN_RX	I-5	-	
A103	LID#	ACPI type LID switch	I-3.3	PU 4.7k 3.3V	
A104	VCC_12V	Power 12V	PWR	-	-
A105	VCC_12V	Power 12V	PWR	-	-
A106	VCC_12V	Power 12V	PWR	-	-
A107	VCC_12V	Power 12V	PWR	-	-
A108	VCC_12V	Power 12V	PWR	-	-
A109	VCC_12V	Power 12V	PWR	-	-
A110	GND(FIXED)	Ground	PWR	-	-

~~XXX~~ Strikethrough pin names indicates that the signal is not supported on this module.

Signal Descriptions (cont'd)

Row B

Pin	Signal	Description	Type	PU/PD	Comment
B1	GND(FIXED)	Ground	PWR	-	-
B2	GBE0_ACT#	Ethernet Activity LED	OD	-	-
B3	LPC_FRAME#	LPC Frame Indicator	O-3.3	-	-
B4	LPC_AD0	LPC multiplexed Adress &DATA Bus	IO-3.3	-	-
B5	LPC_AD1	LPC multiplexed Adress &DATA Bus	IO-3.3	-	-
B6	LPC_AD2	LPC multiplexed Adress &DATA Bus	IO-3.3	-	-
B7	LPC_AD3	LPC multiplexed Adress &DATA Bus	IO-3.3	-	-
B8	~~LPC_DRQ0#~~	~~LPC Serial DMA Request 0~~	I-3.3	-	not supported
B9	~~LPC_DRQ1#~~	~~LPC Serial DMA Request 1~~	I-3.3	-	not supported
B10	LPC_CLK	LPC Clock	O-3.3	-	-
B11	GND(FIXED)	Ground	PWR	-	-
B12	PWRBTN#	Power Button	I-3.3	PU 10K 3.3Vsb	-
B13	SMB_CK	SMBus Clock	IO-3.3	PU 2k2 3.3Vsb	-
B14	SMB_DAT	SMBus Data	IO-3.3	PU 2k2 3.3Vsb	-
B15	SMB_ALERT#	System Management Bus Alert for SMI	I-3.3	PU 10k 3.3V	
B16	SATA1_TX+	SATA 1 Transmit Data +	O - DP	-	-
B17	SATA1_TX-	SATA 1 Transmit Data -	O - DP	-	-
B18	~~SUS_STAT#~~	~~Imminent suspend operation inidcator~~	O-3.3	-	not supported
B19	SATA1_RX+	SATA 1 Receive Data +	I - DP	-	-
B20	SATA1_RX-	SATA 1 Receive Data -	I - DP	-	-
B21	GND(FIXED)	Ground	PWR	-	-
B22	RSVD		NC	-	-
B23	RSVD		NC	-	-
B24	PWR_OK	Power OK from main power supply	I-3.3	-	always reserve pull up
B25	RSVD		NC	-	-
B26	RSVD		NC	-	-
B27	WDT	Watch Dog Event occurred indicator	O-3.3	PU 10K 3.3Vsb	
B28	~~AC/HDA_SDIN2~~	~~Serial TDM data input 2~~	I-3.3	-	not supported
B29	AC/HDA_SDIN1	Serial TDM data input 1	I-3.3	-	-
B30	AC/HDA_SDIN0	Serial TDM data input 0	I-3.3	-	-
B31	GND(FIXED)	Ground	PWR	-	-
B32	SPKR	Output for audio enunciator (PC Beep)	O-3.3	-	-
B33	I2C_CK	General purpose I2C port clock output	IO-3.3	PU 4k7 3.3V	
B34	I2C_DAT	General purpose I2C port data I/O line	IO-3.3	PU 4k7 3.3V	
B35	THRM#	Off module over temperature indicator	I-3.3	PU 1k2 3.3V	-
B36	USB7-	USB Data - Port7	I/O - DP	-	client port
B37	USB7+	USB Data + Port7	I/O - DP	-	client port
B38	USB_4_5_OC#	USB OverCurrent Port 4,5	I-3.3	PU 10k 3.3Vsb	-
B39	USB5-	USB Data- Port5	I/O - DP	-	-
B40	USB5+	USB Data+ Port5	I/O - DP	-	-
B41	GND(FIXED)	Ground	I-3.3	-	-
B42	USB3-	USB Data- Port3	I/O - DP	-	-
B43	USB3+	USB Data+ Port3	I/O - DP	-	-
B44	USB_0_1_OC#	USB OverCurrent Port 0,1	I-3.3	PU 10k 3.3Vsb	-
B45	USB1-	USB Data- Port1	I/O - DP	-	-
B46	USB1+	USB Data+ Port1	I/O - DP	-	-
B47	~~EXCD1_PERST#~~	~~PCI Express Card Reset signal~~	O-3.3	-	not supported
B48	~~EXCD1_CPPE#~~	~~PCI Express capable card request~~	O-3.3	-	not supported
B49	SYS_RESET#	Reset Button Input	I-3.3	none 3.3Vsb	
B50	CB_RESET#	Reset output from Module to Carrier Board	O-3.3	-	-
B51	GND(FIXED)	Ground	PWR	-	-
B52	RSVD		NC	-	-
B53	RSVD		NC	-	-
B54	GPO1	GPO1 or SDIO contr. 0 Command/Response	IO-3.3	PU 10k 3.3V	BIOS select
B55	RSVD		NC	-	-

~~XXX~~ Strikethrough pin names indicates that the signal is not supported on this module.

Signal Descriptions (cont'd)

Row B

Pin	Signal	Description	Type	PU/PD	Comment
B56	RSVD		NC	-	-
B57	GPO2	GPO2 or SDIO controller 0 Write Protect	IO-3.3	PU 10k 3.3V	BIOS select
B58	PCIE_RX3+	PCIe 3 RX+ (port 0 of CPU, occupied)	I - DP	-	used for PCH E G20T
B59	PCIE_RX3-	PCIe 3 RX- (port 0 of CPU, occupied)	I - DP	-	used for PCH E G20T
B60	GND(FIXED)	Ground	PWR	-	-
B61	PCIE_RX2+	PCIe 2 RX+ (port 3 of CPU)	I - DP	-	-
B62	PCIE_RX2-	PCIe 2 RX- (port 3 of CPU)	I - DP	-	-
B63	GPO3	GPO3 or SDIO controller 0 Card Detect	IO-3.3	PU 10k 3.3V	BIOS select
B64	PCIE_RX1+	PCIe 1 RX+ (port 2 of CPU)	I - DP	-	remove LAN to use
B65	PCIE_RX1-	PCIe 1 RX- (port 2 of CPU)	I - DP	-	remove LAN to use
B66	WAKE0#	PCI Express wake up signal.	I-3.3	none 3.3Vsb	connected to WAKE1#
B67	WAKE1#	General Purpose wake up signal	I-3.3	none 3.3Vsb	connected to WAKE0#
B68	PCIE_RX0+	PCIe 0 RX+ (port 1 of CPU)	I - DP	-	
B69	PCIE_RX0-	PCIe 0 RX- (port 1 of CPU)	I - DP	-	
B70	GND(FIXED)	Ground	PWR	-	-
B71	DDI0_PAIR0+	SDVOB_RED+	O - DP	-	-
B72	DDI0_PAIR0-	SDVOB_RED-	O - DP	-	-
B73	DDI0_PAIR1+	SDVOB_GRN+	O - DP	-	-
B74	DDI0_PAIR1-	SDVOB_GRN-	O - DP	-	-
B75	DDI0_PAIR2+	SDVOB_BLU+	O - DP	-	-
B76	DDI0_PAIR2-	SDVOB_BLU-	O - DP	-	-
B77	DDI0_PAIR4+	SDVOB_INT+	I - DP	-	-
B78	DDI0_PAIR4-	SDVOB_INT-	I - DP	-	-
B79	LVDS_BKLT_EN	LVDS panel backlight enable	O-3.3	PD 100k	-
B80	GND(FIXED)	Ground	PWR	-	-
B81	DDI0_PAIR3+	SDVOB_CK+	O - DP	-	-
B82	DDI0_PAIR3-	SDVOB_CK	O - DP	-	-
B83	LVDS_BKLT_CTRL	LVDS panel backlight brightness control	O-3.3	PD 10k	-
B84	VCC_5V_SBY	5V Standby Input	PWR	-	-
B85	VCC_5V_SBY	5V Standby Input	PWR	-	-
B86	VCC_5V_SBY	5V Standby Input	PWR	-	-
B87	VCC_5V_SBY	5V Standby Input	PWR	-	-
B88	BIOS_DIS1#	SPI BIOS boot device selection	I-3.3	PU 10k 3.3Vsb	-
B89	~~DD0_HPD~~	~~Digital Display Interface Hot-Plug Detect~~	I-3.3	PU 10k 3.3V	not needed on SDVO
B90	GND(FIXED)	Ground	PWR	-	-
B91	DDI0_PAIR5+	SDVO_TVCLKIN+	I - DP	-	-
B92	DDI0_PAIR5-	SDVO_TVCLKIN-	I - DP	-	-
B93	DDI0_PAIR6+	SDVO_FLDSTALL+	I - DP	-	-
B94	DDI0_PAIR6-	SDVO_FLDSTALL-	I - DP	-	-
B95	DDI0_DDC_AUX_SEL	Select function of DDI(0) CTRL_CLK_AUX+	IO-3.3	-	-
B96	RSVD		NC	-	-
B97	SPI_CS#	Chip select for Carrier Board SPI	O-3.3	none 3.3Vsb	-
B98	DDI0_CTRLCLK_AUX+	SDVO I2C Clock	IO-2.5		
B99	DDI0_CTRLDATA_AUX-	SDVO I2C Data	IO-2.5		
B100	GND(FIXED)	Ground	PWR	-	-
B101	FAN_PWMOUT	Fan speed control output	O-3.3	PU 1.2K 3.3Vsb	
B102	FAN_TACHIN	Fan tachometer input	I-3.3	PD 10k	-
B103	SLEEP#	sleep	I-3.3	-	-
B104	VCC_12V	Power 12V	PWR	-	-
B105	VCC_12V	Power 12V	PWR	-	-
B106	VCC_12V	Power 12V	PWR	-	-
B107	VCC_12V	Power 12V	PWR	-	-
B108	VCC_12V	Power 12V	PWR	-	-
B109	VCC_12V	Power 12V	PWR	-	-
B110	GND(FIXED)	Ground	PWR	-	-

~~XXX~~ Strikethrough pin names indicates that the signal is not supported on this module.

Signal Description Legend

Signal Type Legend	
IO-2,5	Bi-directional 2,5 V Input/Output
IO-3,3	Bi-directional 3,3 V Input/Output
IO-5	Bi-directional 5 V Input/Output
I-3,3	3,3 V Input
I-5	5 V Input
O-2,5	2,5 V Output
O-3,3	3,3 V Output
O-5	5 V Output
IO	Input/Output
OA	Analog Output
OD	Digital Output
I/O - DP	Differential Pair Input/Output
O - DP	Differential Pair Output
I - DP	Differential Pair Input
PWR	Power or Ground
STO	Strapping Output
PU	Pull Up Resistor
PD	Pull Down Resistor
NC	Not Connected / Reserved

6 Embedded Functions

All embedded board functions on ADLINK's Computer on Modules are supported at the operating system level using the ADLINK Intelligent Device Interface (AIDI) library. The AIDI API programming interface is compatible and identical across all ADLINK Computer on Modules and all supported operating systems. The AIDI library includes a demo program to demonstrate the library's functionallity.

6.1 Watchdog Timer

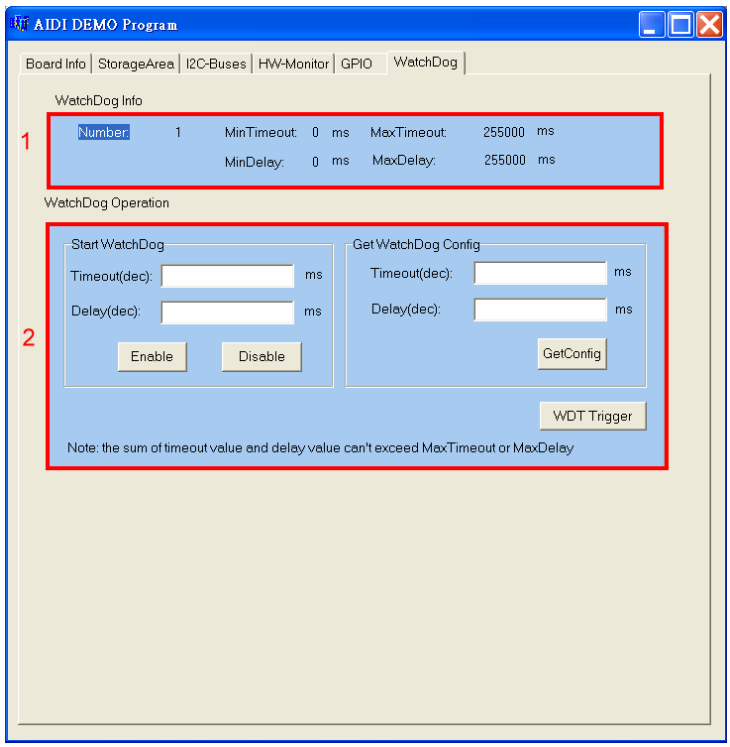
The nanoX-TC implements a watchdog timer that can be used to automatically detect software execution problems or system hangs and reset the board if necessary. The watchdog timer consists of a counter that counts down from an initial value to zero. When the system is operating normally, the software that sets the intial value periodically resets the counter so that the it never reaches zero. If the counter reaches zero before the software resets it, the system is presumed to be malfunctioning and a reset signal is asserted.

The AIDI Library Watchdog Functions support watchdog control of the board. If the watchdog begins countdown and reaches zero, it will access the CPU's RESET signal to reset the system. The watchdog application must call another function named AidiWDogTrigger that restarts the Watchdog timer in order to prevent system reset.

AIDI Demo Program - Watchdog Tab

The AIDI Demo Program allows retrieval of the current watchdog status and updating of the watchdog settings

If the watchdog is enabled, the user can click the *WDT Trigger* button to manually reset the counter and prevent the system from resetting



6.2 GPIO

The COM.0 Rev 2.0 Type 10 standard specification allows for optional SDIO signals to be carried over the GPIO pins. On the nanoX-TC, the output mode is set to either SDIO or GPIO by BIOS setup. The nanoX-BASE has no special setting for this and will either output the GPIO signals to the GPIO header or the SDIO signals to the standard SDIO socket.

NOTE: If SDIO mode is selected in BIOS, the GPIO pins below cannot be used.

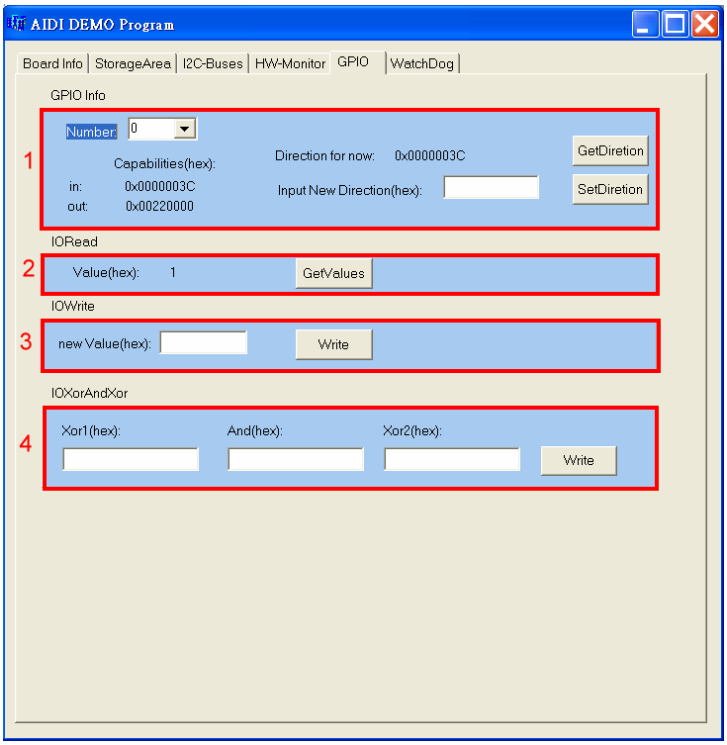
Pin	Signal Type #	AIDI ID (bit)	Remark
A54	GPI0	0	Not supported in SDIO mode
A63	GPI1	1	Not supported in SDIO mode
A67	GPI2	2	Not supported in SDIO mode
A85	GPI3	3	Not supported in SDIO mode
A93	GPO0	4	Not supported in SDIO mode
B54	GPO1	5	Not supported in SDIO mode
B57	GPO2	6	Not supported in SDIO mode
B63	GPO3	7	Not supported in SDIO mode

AIDI Demo Program - GPIO Tab

The AIDI Demo Program displays current GPI or GPO status and allows reading of GPI and writing to GPO.

The table above links logical port numbers in AIDI to physical port numbers on the COM Express board-to-board connector.

For boards that support *multi-direction* the "SetDirection" button can configure the port for either GPI or GPO



6.3 Hardware Monitoring

To ensure system health of your embedded system ADLINK's COM Express modules come with built in support for monitoring and control of CPU and system temperatures, fan speed and critical module voltage levels.

The AIDI Library provides simple APIs at the application level to support these functions and adds alarm functions when voltage or temperature levels exceeds the upper or lower limit set by the user.

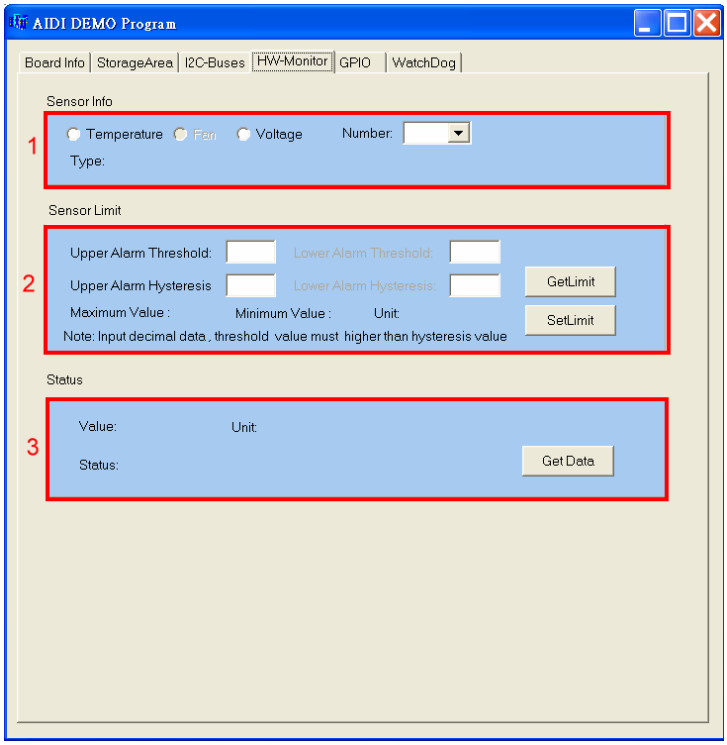
On the nanoX-TC the following monitored values can be read from the module: CPU temperature, system temperature, Vcore, 1.8 V, 5 V, 3.3 V and 12 V.

AIDI Demo Program - HW Monitor Tab

Field 1 displays detected sensors (number).

Field 2 allows setting of upper and lower alarm limits.

Field 3 displays read out information of sensors.



7 System Resources

7.1 System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
(4GB- 512KB)	FFF80000 – FFFFFFFF	512 KB	High BIOS area
(4GB-16MB) – (4GB-16MB-48KB)	FEFD4000 –FED4BFFF	48 KB	TPM 1.2
(4GB-19MB) – (4GB-18MB-1KB)	FED00000 – FED003FF	1 KB	HPET
(4GB-20MB) – (4GB-19MB-64Byte)	FEC00000 – FEC00040	64 Byte	APIC configuration space
960 K – 1024 K	F0000 – FFFFF	64 KB	System BIOS area
896 K – 960 K	E0000 – EFFFF	64 KB	Extended System BIOS area
768 K – 896 K	C0000 – DFFFF	128 KB	PCI expansion ROM area C0000-CEFFF: Onboard VGA BIOS D0000 – D33FF: PXE option ROM when onboard LAN boot ROM is enabled."
640 K – 768 K	A0000 – BFFFF	128 KB	Video Buffer & SMM space
0 K – 640 K	00000 – 9FFFF	640 KB	DOS area

7.2 Direct Memory Access Channels

Channel Number	Data Width	System Resource	Comment
0	8-bits	Open	
1	8-bits	Open	
2	8-bits	Open	
3	8-bits	Open	
4		Reserved - cascade channel	
5	16-bits	Open	
6	16-bits	Open	
7	16-bits	Open	

7.3 Legacy I/O Map

Address (hex)	Size	Description	Comment
0000 - 001F	32 bytes	DMA controller	
0020 - 0021	2 bytes	Interrupt controller	
0024 - 0025	2 bytes	Interrupt controller	
0028 - 0029	2 bytes	Interrupt controller	
002C - 002D	2 bytes	Interrupt controller	
002E - 002F	2 bytes	LPC SIO	
0030 - 0031	2 bytes	Interrupt controller	
0034 - 0035	2 bytes	Interrupt controller	
0038 - 0039	2 bytes	Interrupt controller	
003C - 003D	2 bytes	Interrupt controller	
0040 - 0043	4 bytes	Counter/Timer	
0044 - 0047	4 bytes	System reserved	
004E - 004F	2 bytes	TPM configuration port	
0050 - 0053	4 bytes	Counter/Timer	
0054 - 005F	12 bytes	System reserved	
0060	1 byte	Keyboard controller	
0061	1 byte	NMI, speaker control	
0063	1 byte	NMI controller	
0064	1 byte	Keyboard controller	
0065	1 byte	NMI controller	
0067	1 byte	NMI controller	
0070 - 0071	2 bytes	Real time clock controller	
0072 - 0073	2 bytes	Real time clock controller	
0074 - 0075	2 bytes	Real time clock controller	
0076 - 0077	2 bytes	Real time clock controller	
0080 - 0091	18 bytes	DMA controller	
0092	1 bytes	Reset Generator	
0093 - 009F	13 bytes	DMA controller	
00A0 - 00A1	2 bytes	Interrupt controller	
00A4 - 00A5	2 bytes	Interrupt controller	
00A8 - 00A9	2 bytes	Interrupt controller	
00AC - 00AD	2 bytes	Interrupt controller	
00B0 - 00B1	2 bytes	Interrupt controller	
00B2 - 00B3	2 bytes	Power Management	
00B4 - 00B5	2 bytes	Interrupt controller	
00B8 - 00B9	2 bytes	Interrupt controller	
00BC - 00BD	2 bytes	Interrupt controller	
00C0 - 00DF	32 bytes	DMA controller	
00E0 - 00EF	16 bytes	System reserved	
00F0 - 00FF	16 bytes	Numeric processor	
02F8 - 02FF	8 bytes	COM2***	Note (***)
03B0 - 03BB	12 bytes	Video (monochrome)	
03F0 - 03F5, 03F7	7 bytes	Diskette controller	

Legacy I/O Map (cont'd)

Address (hex)	Size	Description	Comment
03F8 - 03FF	8 bytes	COM1***	Note (***)
0400 - 041F	32 bytes	Onboard SMBus control registers	
0480 - 04BF	64 bytes	GPIO control registers	
04D0 - 04D1	2 bytes	Interrupt controller	
0900 - 090F	16bytes	ACPI control registers	
0900 - 091F	16bytes	Power managermant registers	
09C0 - 09FF	64bytes	General Purpose Event Block Registers	
0CF8 - 0CFF*	8 bytes	PCI configuration registers	Note (*)
0CF9**	1 byte	Reset control register	Note (**)
04700 - 0470F	16 bytes	TPM control registers	
E000-E01F	32 byte	EG20T SATA AHCI Controller	
E020-E03F	32 byte	EG20T Gigabit Ethernet Controller	
E040-E047	8 bytes	EG20T UART Controller	
E050-E057	8 bytes	EG20T UART Controller	
E060-E067	8 bytes	EG20T UART Controller	
E070-E077	8 bytes	EG20T UART Controller	

NOTE:

(*) DWORD access only
(**) Byte access only
(***) Available when onboard device is disabled

7.4 Interrupt Request (IRQ) Lines

PIC Mode

IRQ#	Typical Interrupt Resource	Connected	Available
0	Counter 0	N/A	No
1	Keyboard controller	N/A	No
2	Cascade interrupt from slave PIC	N/A	No
3	Serial Port 2 (COM2) / PCI	IRQ3 via SERIRQ	Note (1)
4	Serial Port 1 (COM1) / PCI	IRQ4 via SERIRQ	Note (1)
5	AHCI SATA controller	AHCI SATA controller	No
6	N/A	N/A	Yes
7	N/A	N/A	Yes
8	Real-time clock	Internal RTC	No
9	SCI / PCI	IRQ9 via SERIRQ	Note (1)
10	PCI	N/A	No
11	PCI	N/A	No
12	PS/2 Mouse / PCI	IRQ12 via SERIRQ	Note (1)
13	Math Processor	N/A	No
14	N/A	N/A	No
15	N/A	N/A	No

NOTE: **(1)** These IRQs can be used for PCI devices when onboard device is disabled.

APIC Mode

IRQ#	Typical Interrupt Resource	Connected	Available
0	Counter 0	N/A	No
1	Keyboard controller	N/A	No
2	Cascade interrupt from slave PIC	N/A	No
3	Serial Port 2 (COM2) / PCI	IRQ3 via SERIRQ	Note (1)
4	Serial Port 1 (COM1) / PCI	IRQ4 via SERIRQ	Note (1)
5	EG20T DMA controller	EG20T DMA controller #2	No
6	N/A	N/A	No
7	N/A	N/A	No
8	Real-time clock	Internal RTC	No
9	SCI / PCI	IRQ9 via SERIRQ	Note (1)
10	N/A	N/A	Yes
11	Embedded Media and Graphics extension	Embedded Media and Graphics extension	No
12	PS/2 Mouse / PCI	IRQ12 via SERIRQ	Note (1)
13	Math Processor	N/A	No
14	N/A	N/A	No

APIC Mode (cont'd)

IRQ#	Typical Interrupt Resource	Connected	Available
15	N/A	N/A	No
16	N/A	PCI-E Slot #0, 1, 2, 3, VGA controller, High Definition Audio controller, USB controller #1,2,3, Gigabit Ethernet, I2C controller, IEEE1588 controller, GPIO controller, CAN controller, EHCI controller #1	Yes (2)
17	N/A	SATA AHCI controller	Yes (2)
18	N/A	SD Host controller #1, 2	Yes (2)
19	N/A	USB controller #4, 5, 6, USB Client Controller, UART controller, EHCI controller #2, EG20T DMA controller #1	Yes (2)
20	N/A	N/A	Yes
21	N/A	N/A	Yes
22	N/A	N/A	Yes
23	N/A	N/A	Yes

NOTE:

(1) These IRQs can be used for PCI devices when onboard device is disabled.
(2) These devices from are from the PCH EG20T.

7.5 PCI Configuration Space Map

Bus #	Device #	Function #	Routing	Description	Notes
00h	00h	00h	N/A	Host Bridge (1)	
00h	01h	00h	N/A	Host Bridge (1)	
00h	02h	00h	Internal	Intel Integrated Graphics Device(1)	
00h	03h	00h	Internal	Intel Video controller (1)	
00h	17h	00h	Internal	PCIE Port #0 (1)	
00h	18h	00h	Internal	PCIE Port #1 (1)	
00h	19h	00h	Internal	PCIE Port #2 (1)	
00h	1Ah	00h	Internal	PCIE Port #3 (1)	
00h	1Bh	00h	Internal	Intel HD Audio Device (1)	
00h	1Fh	00h	Internal	Intel LPC Interface Bridge (1)	
01h	00h	00h	Internal	Intel PCI to PCI Bridge (2)	
02h	00h	00h	Internal	Intel EG20T Packet Hub Controller (2)	
02h	00h	01h	Internal	Intel EG20T Ethernet Controller (2)	
02h	00h	02h	Internal	Intel EG20T GPIO Controller (2)	
02h	02h	00h	Internal	Intel EG20T OHCI USB Controller (2)	
02h	02h	01h	Internal	Intel EG20T OHCI USB Controller (2)	
02h	02h	02h	Internal	Intel EG20T OHCI USB Controller (2)	
02h	02h	03h	Internal	Intel EG20T EHCI USB Controller (2)	
02h	02h	04h	Internal	Intel EG20T USB Client (2)	
02h	04h	01h	Internal	Intel EG20T SDIO #0 Controller (2)	
02h	04h	02h	Internal	Intel EG20T SDIO #1 Controller (2)	
02h	06h	00h	Internal	Intel EG20T SATA AHCI Controller (2)	
02h	08h	00h	Internal	Intel EG20T OHCI USB Controller (2)	
02h	08h	01h	Internal	Intel EG20T OHCI USB Controller (2)	
02h	08h	02h	Internal	Intel EG20T OHCI USB Controller (2)	
02h	08h	03h	Internal	Intel EG20T EHCI USB Controller (2)	
02h	0Ah	00h	Internal	Intel EG20T Shared DMA Controller (2)	
02h	0Ah	01h	Internal	Intel EG20T UART Controller (2)	
02h	0Ah	02h	Internal	Intel EG20T UART Controller (2)	
02h	0Ah	03h	Internal	Intel EG20T UART Controller (2)	
02h	0Ah	04h	Internal	Intel EG20T UART Controller (2)	
02h	0Ch	00h	Internal	Intel EG20T Shared DMA Controller (2)	
02h	0Ch	01h	Internal	Intel EG20T SPI Controller (2)	
02h	0Ch	02h	Internal	Intel EG20T I2C bus Controller (2)	
02h	0Ch	03h	Internal	Intel EG20T CAN bus Controller (2)	
02h	0Ch	04h	Internal	Intel EG20T IEEE1588 Controller (2)	

NOTE:

(1) These devices are from the CPU.
(2) These devices are from the PCH EG20T.

8 BIOS Setup Utility

The following chapter describes basic navigation for the AMIBIOS8 BIOS setup utility.

8.1 Starting the BIOS

To enter the setup screen, follow these steps:

1. Power on the motherboard
2. Press the < Delete > key on your keyboard when you see the following text prompt:

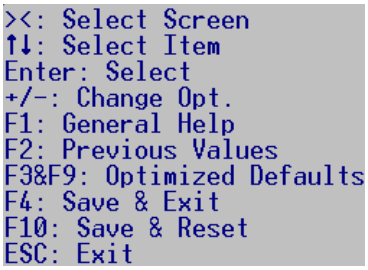
   < Press DEL or Delete to run Setup >

3. After you press the < Delete > key, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu, such as Chipset and Power menus.

NOTE: In most cases, the < Delete > key is used to invoke the setup screen. There are several cases that use other keys, such as < F1 >, < F2 >, and so on.

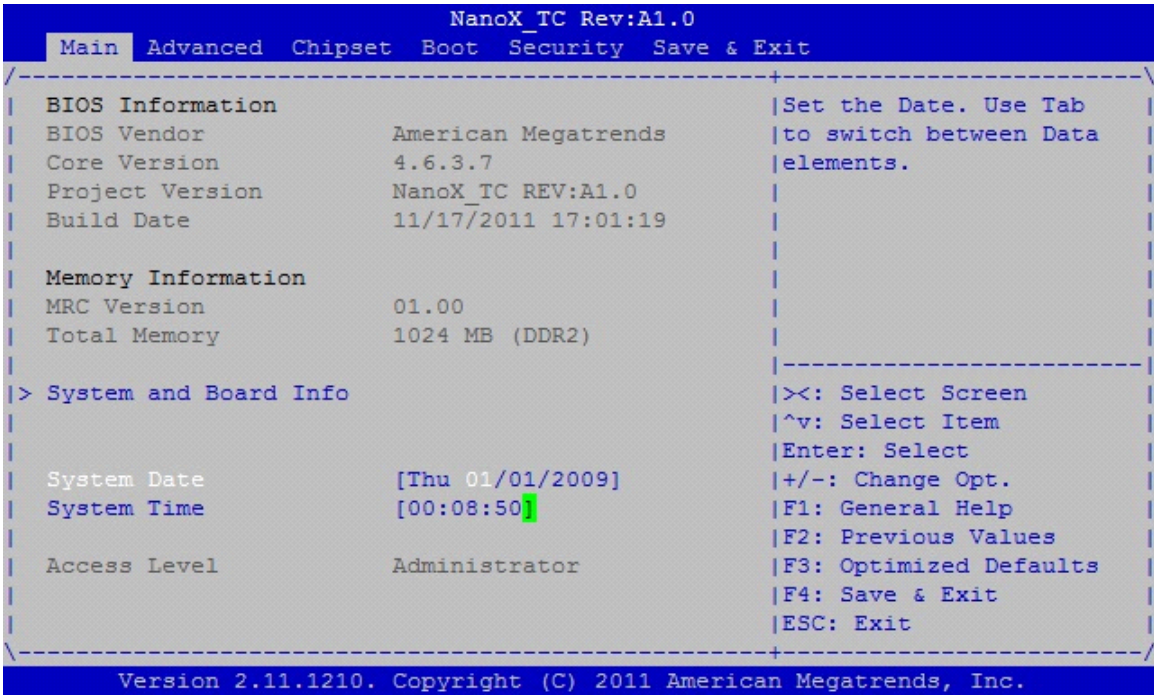
8.2 UEFI BIOS Setup Navigation

The UEFI BIOS Setup Utility is a text-based basic input and output system that provides advance UEFI functionality with a familiar BIOS interface. The UEFI BIOS Setup Utility keyboard-based navigation can be accomplished using a combination of keys:



<ENTER>	The Enter key allows the user to select an option to edit its value or access a sub menu.
<Left>/<Right>	The Left and Right <Arrow> keys allow you to select an Aptio TSE screen. For example: Main screen, Advanced screen, Chipset screen, and so on.
<Up>/<Down>	The Up and Down <Arrow> keys allow you to select an Aptio TSE item or sub-screen.
<Plus>/<Minus>	The Plus and Minus <Arrow> keys allow you to change the field value of a particular setup item. For example: Date and Time.
<Tab>	The <Tab> key allows you to select Aptio TSE fields.
<F1>	This key displays the general help window for the user.
<F2>	This key enables users to load pervious values in TSE
<F3>&<F9>	This key enables users to load optimized default values in TSE
<F4>	This key enables users to save the current configuration and exit TSE.
<F10>	This key enables users to save the current configuration and Reset.
<ESC>	The <Esc> key allows you to discard any changes you have made and exit the Aptio TSE. Press the <Esc> key to exit the Aptio TSE without saving your changes. The following screen will appear: Press the <Enter> key to discard changes and exit. You can also use the<Arrow> key to select Cancel and then press the <Enter> key to abort this function and return to the previous screen.

8.3 Main Setup



System and Board Information

The Main BIOS setup screen reports processor, memory and board information.

Project Version: Displays the current BIOS version.

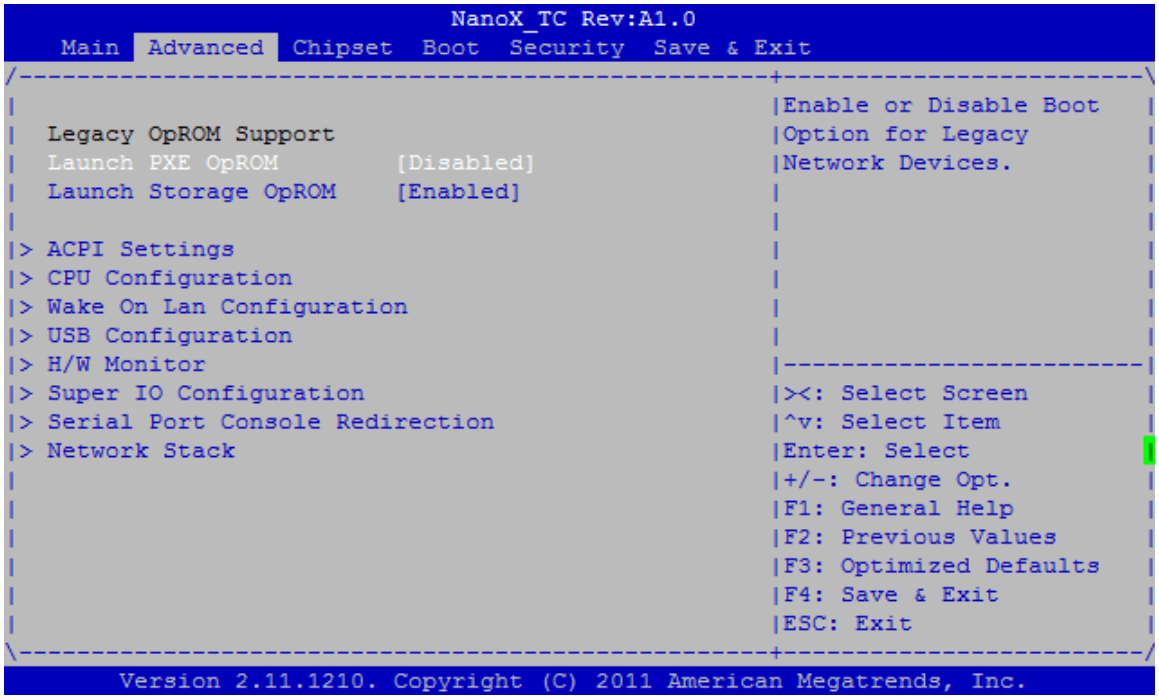
Build Data: Displays the BIOS build data.

Total Memory: Displays the total memory.

8.4 Advanced BIOS Setup

Select the *Advanced* tab from the setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the < Arrow > keys. The Advanced BIOS Setup screen is shown below.

The sub menus are described on the following pages.



Setting incorrect or conflicting values in Advanced BIOS Setup may cause system malfunctions.

Launch PXE OpROM

Boot Option for Legacy Network Devices. Set this value to Enabled/Disabled.

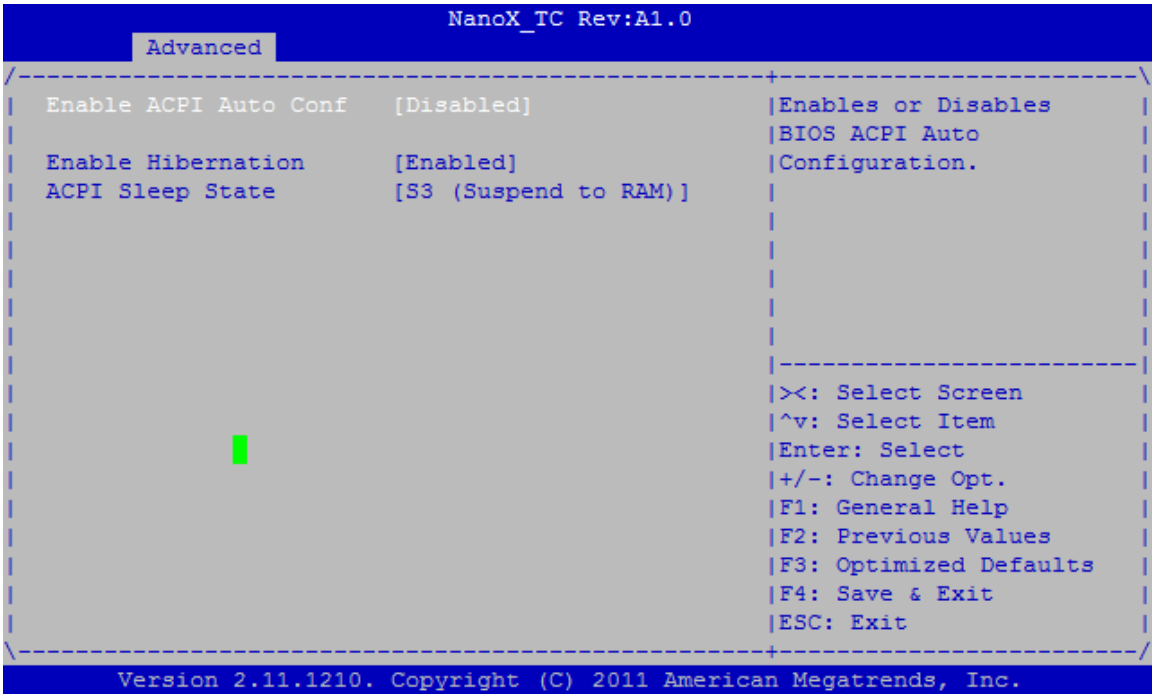
Launch Storage OpROM

Boot Option for Legacy Mass Storage Devices. Set this value to Enabled/Disabled.

8.4.1 ACPI Settings

CPU Configuration Settings

You can use this screen to select options for the ACPI Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the *ACPI Configuration* screen is shown below.



Enable APIC Auto Configuration

BIOS ACPI Auto Configuration. Set this value to Enabled/Disabled.

Enable Hibernation

System ability to Hibernate (OS/S4 Sleep State). Set this value to Enabled/Disabled.

ACPI Sleep State

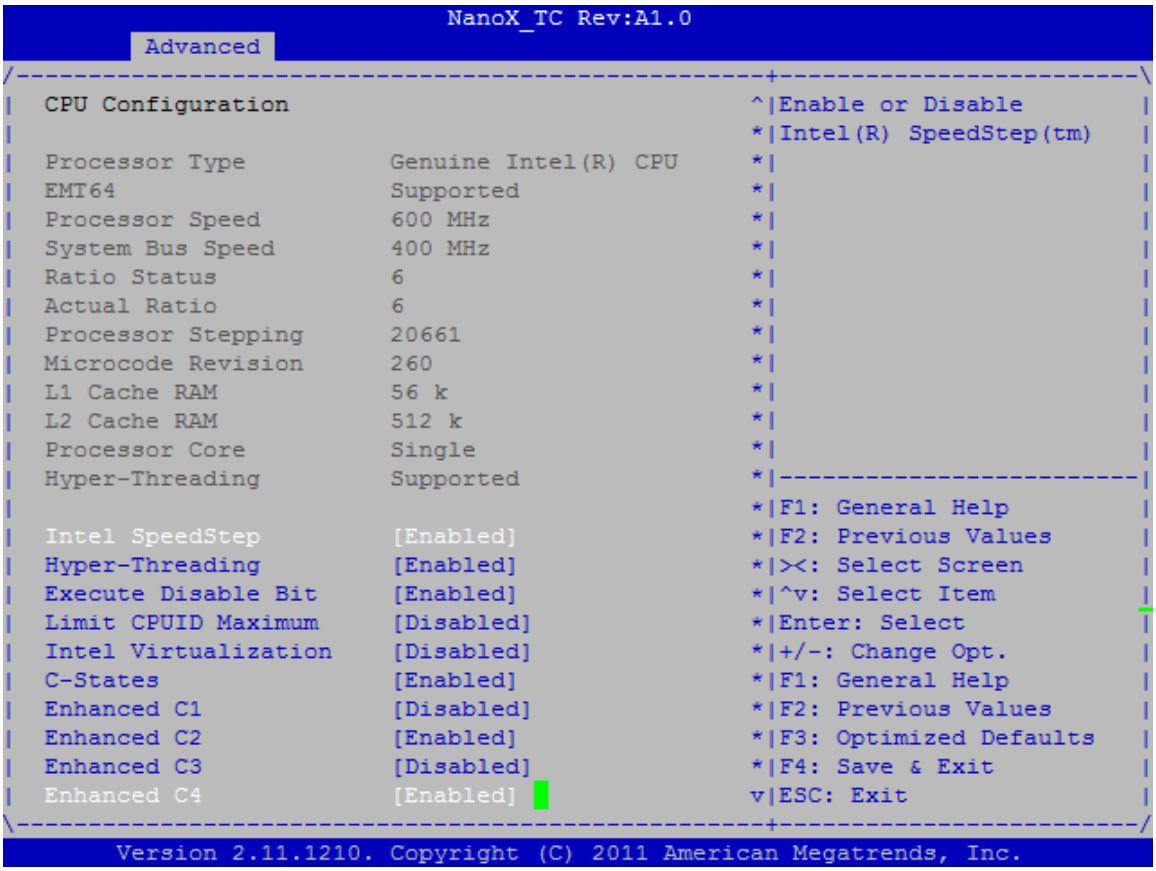
Selects the highest ACPI sleep state the system will enter, when the SUSPEND button is pressed. Set this value to S3/Suspend Disable.

S3 Suspend to RAM (STR) - Under this setting the system enters a low power state instead of being completely shut off. This allows the computer system to boot up in a few seconds.

8.4.2 CPU Configuration

CPU Configuration Settings

You can use this screen to select options for the CPU Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the *CPU Configuration* screen is shown below.



Hyper-Threading Technology

This option enables/disables Intel® Hyper-Threading Technology.

Intel® SpeedStep tech

This option enables or disables Intel® SpeedStep® technology.

Execute Disable Bit Capability

This is an Intel hardware-based security feature that can help reduce system exposure to viruses and malicious code. It allows the processor to classify areas in memory where application code can or cannot execute. When a malicious worm attempts to insert code in the buffer, the processor disables its code execution, preventing damage and worm propagation. To use Execute Disable Bit you must have a PC or server with a processor with Execute Disable Bit capability and a supporting operating system.

Limit CPUID Maximum

When the computer is boots, the operating system executes its CPUID instruction to identify the processor and its capabilities. Before it can do so, it must first query the processor to find out the highest input value the CPUID recognizes. This determines the kind of basic information CPUID can provide the operating system. This option allows you to circumvent problems with older operating systems.

When Enabled, the processor will limit the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. When Disabled, the processor will return the actual maximum CPUID input value of the processor when queried.

Intel® Virtualization Tech

Intel® Virtualization Technology is a set of platform features that supports virtualization of platform hardware and multiple software environmentss. When enabled, it offers data center managers the ability to consolidate multiple workloads on one physical server system.

Intel® C-STATE tech

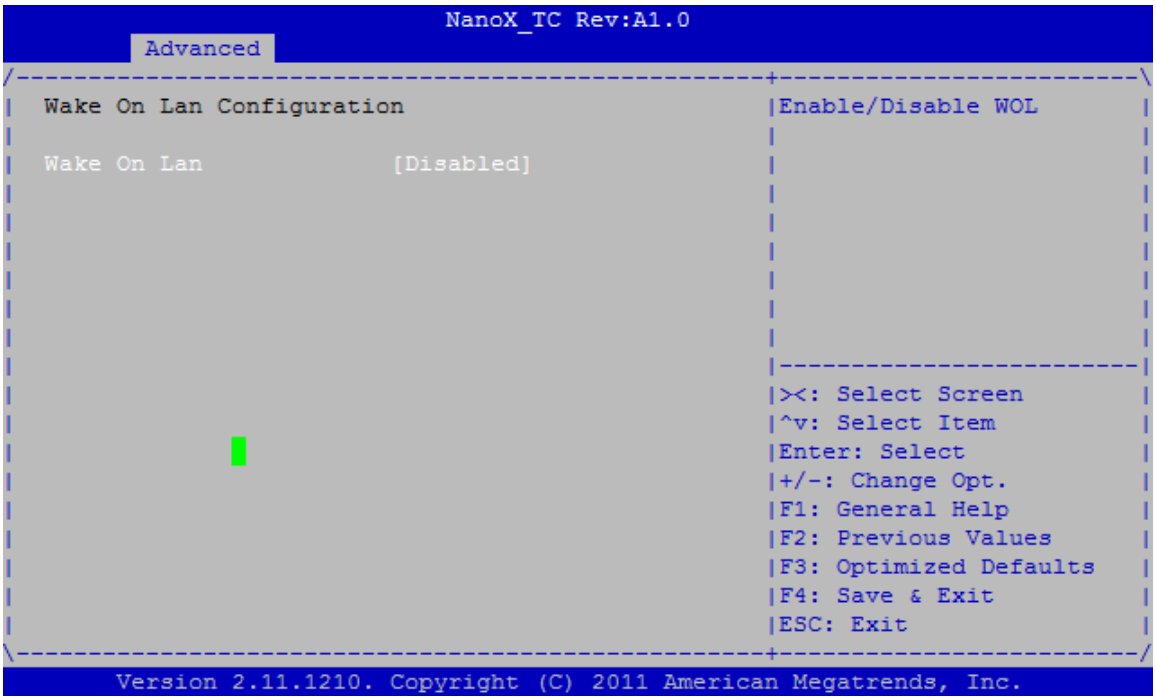
This item allows you to Enable/Disable the C-STATE function. C-STATE make the power and thermal control unit part of the core logic and not part of the chipset as before.

Enhanced C1~C4

Enable or Disable Enhanced C1~C4 state. Set this value to Enabled/Disabled.

8.4.3 Wake On LAN Configuration

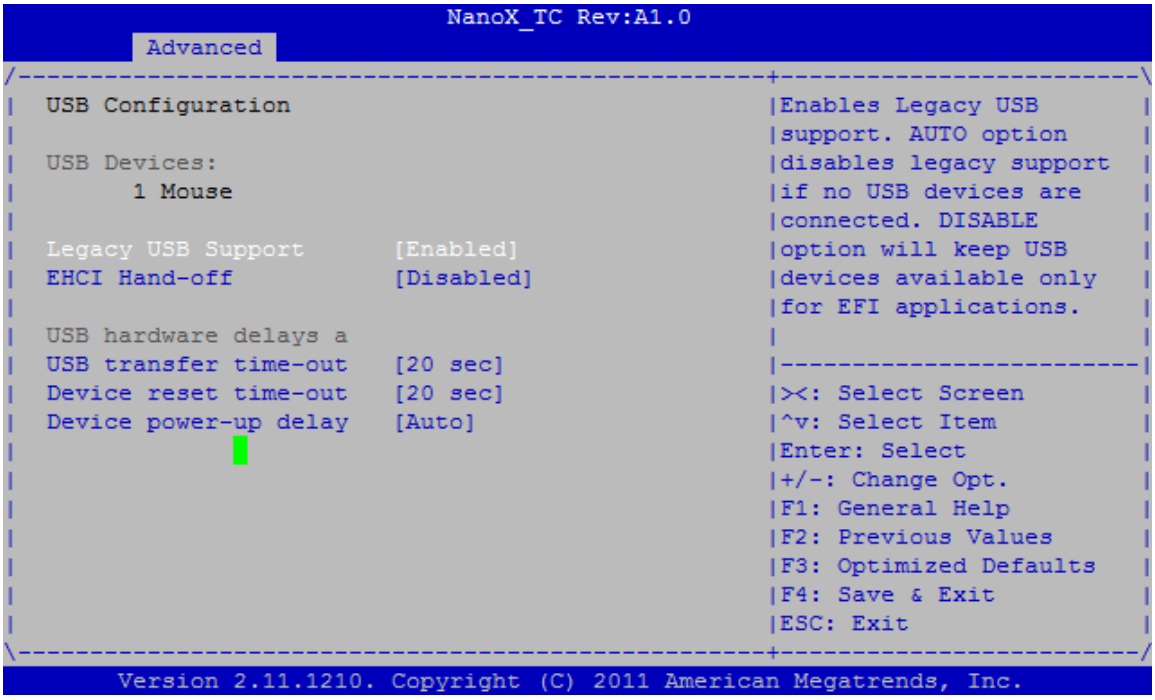
You can use this screen to select options for the WOL Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the WOL Configuration screen is shown below.



Wake On LAN

Enables/disables Wake On LAN. Set this value to Enabled/Disabled.

8.4.4 USB Configuration



Legacy USB Support

Enables legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications. Set this value to Enabled/Disabled/Auto.

EHCI Hand-off

This is a workaround for OS without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver. Set this value to Enabled/Disabled.

USB transfer time-out

The time-out value for control, bulk, and interrupt transfers.Set this value to 1 sec / 5 sec / 10 sec / 20 sec.

Device reset time-out

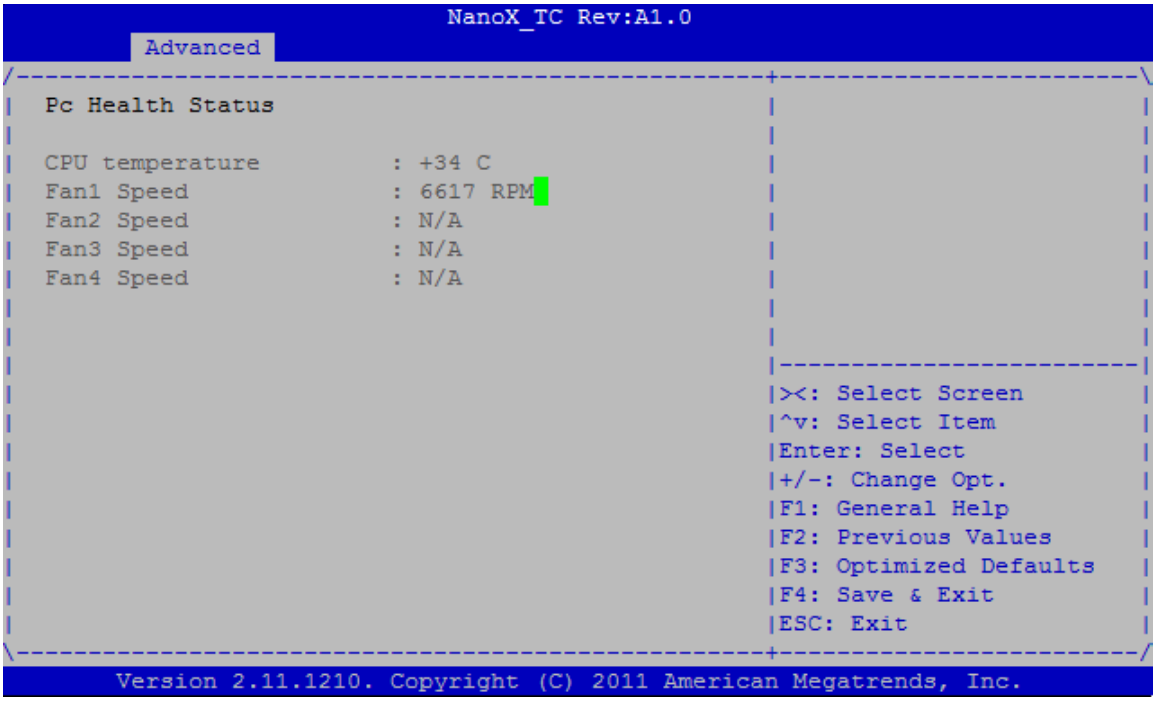
USB mass storage device start unit command time-out. Set this value to 10 sec / 20 sec / 30 sec / 40 sec.

Device power-up delay

Maximum time the device will take before it properly reports itself to the host controller. 'Auto' uses default value: for a root port it is 100 ms, for a hub port the delay is taken from hub descriptor. Set this value to Auto/Manual.

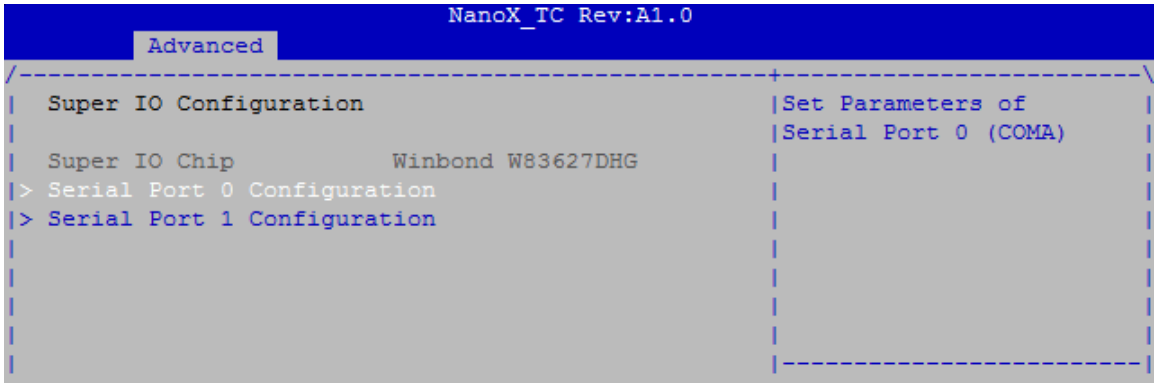
8.4.5 H/W Monitor

Use this screen to check system health status.



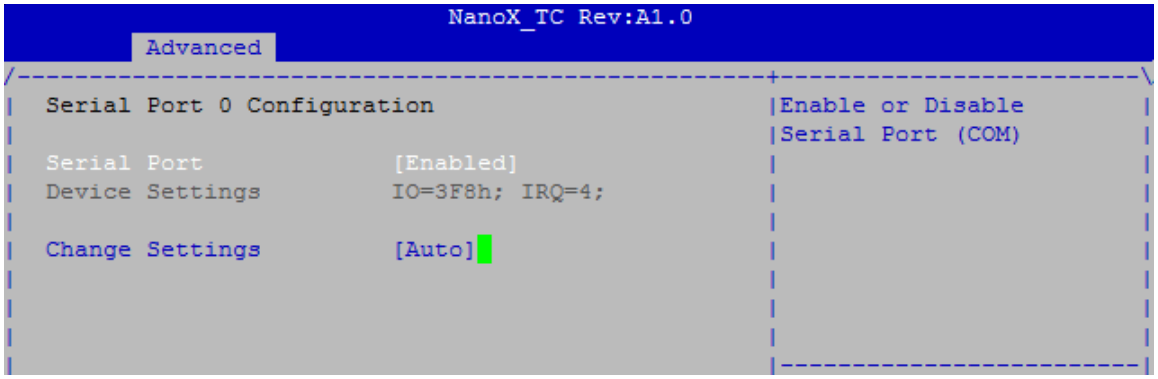
8.4.6 Super IO Configuration

You can use this screen to select options for the Super IO settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



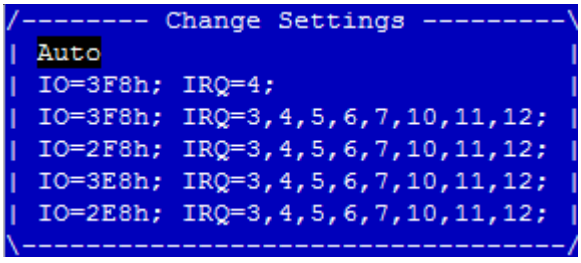
Serial Port 0,1 Configuration

Set Parameters of Serial Port 0,1. Set this value to Enabled/Disabled.

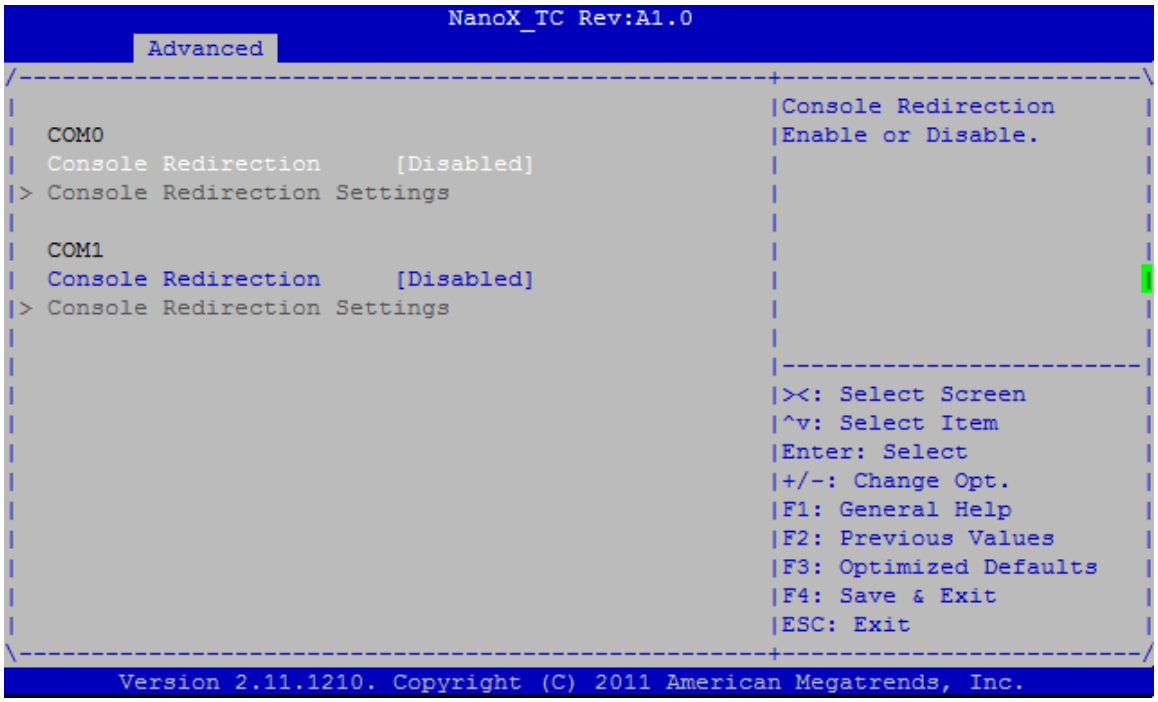


Change Settings

This option specifies the base I/O port address and interrupt request address of serial port 0,1. Options shown below.



8.4.7 Serial Port Console Redirection

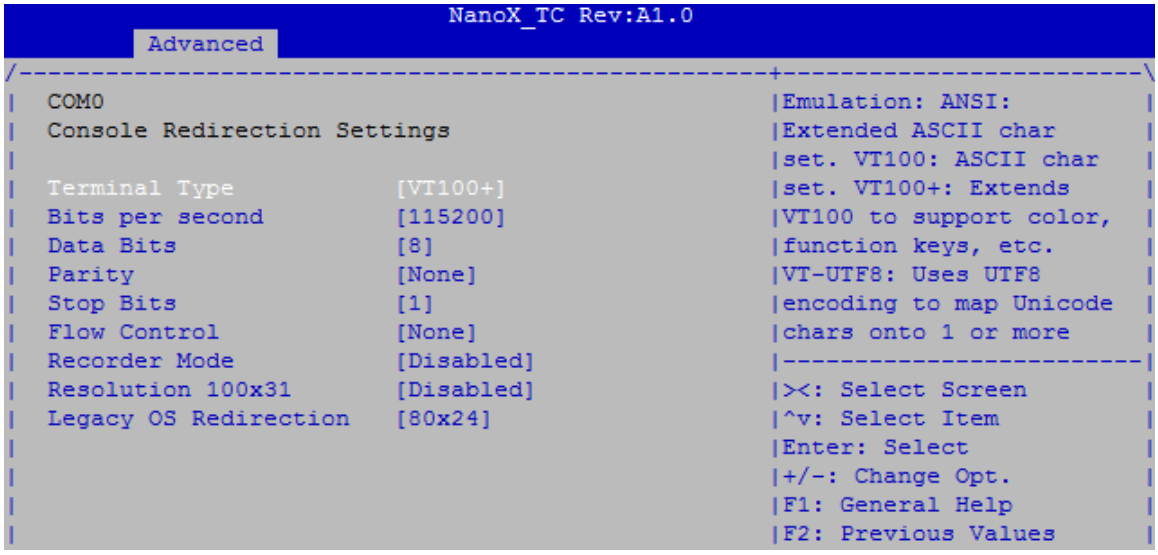


Console Redirection

Set this value to enable/disable console redirection.

Console Redirection Settings

The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.



Terminal Type

VT100+ is the preferred terminal type for out-of-band management. Configuration options: VT100, VT100+, VT-UTF8 , ANSI.

Bits per second

Select the bits per second you want the serial port to use for console redirection. The options are 115200, 57600, 38400, 19200, 9600.

Data Bits

Select the data bits you want the serial port to use for console redirection. Set this value to 7 / 8.

Parity

Set this option to select Parity for console redirection. The settings for this value are None, Even, Odd, Mark, Space.

Stop Bits

Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit. Set this value to 1 and 2.

Flow Control

Set this option to select Flow Control for console redirection. The settings for this value are None, Hardware RTS/CTS.

Recorder Mode

Enabled this mode, only text will be sent. This is to capture terminal data.Set this value to Enabled/Disabled.

Resolution 100x31

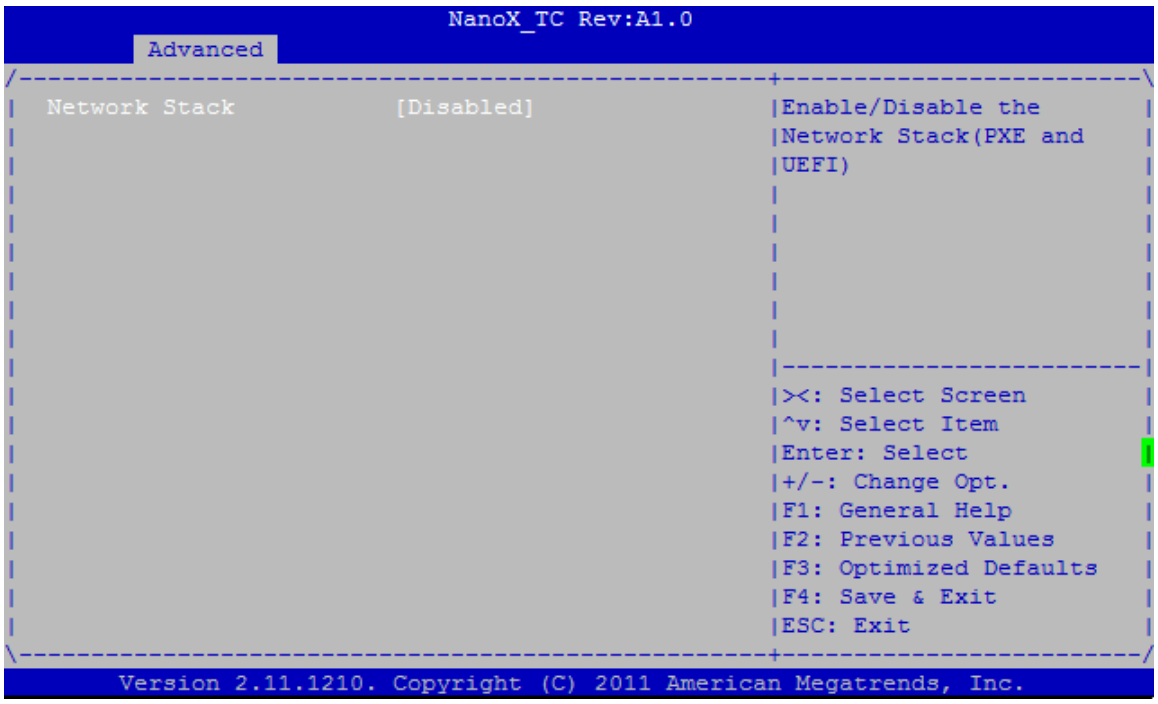
Set this option to extended terminal resolution. Set this value to Enabled/Disabled.

Legacy OS Redirection

On Legacy OS, the number of rows and columns supported redirection. Set this value to 80x24 / 80x25.

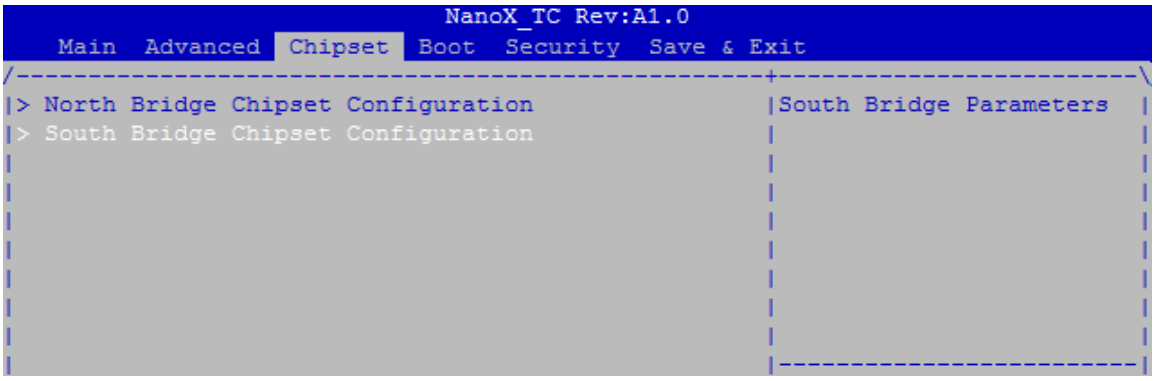
8.4.8 Network Stack

Enable / Disable the network stack (PXE and UEFI). An example of the Network Stack screen is shown below.

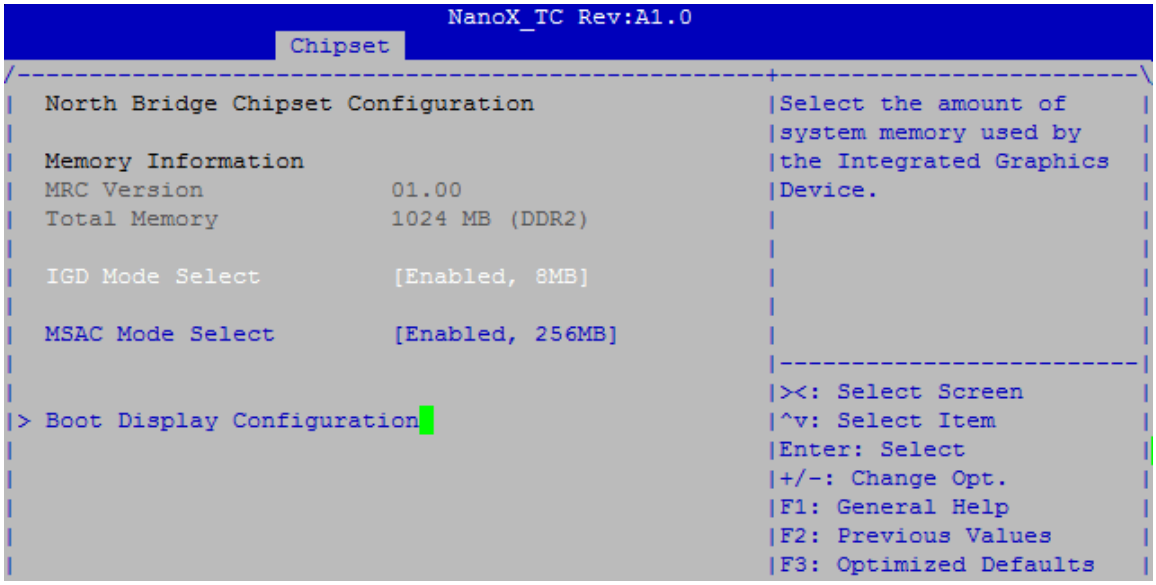


8.5 Chipset Configuration

Select the Chipset tab from the setup screen to enter the Chipset BIOS Setup screen. You can select any of Chipset BIOS Setup options by highlighting it using the < Arrow > keys. The Chipset BIOS Setup screen is shown below.



8.5.1 North Bridge Chipset Configuration



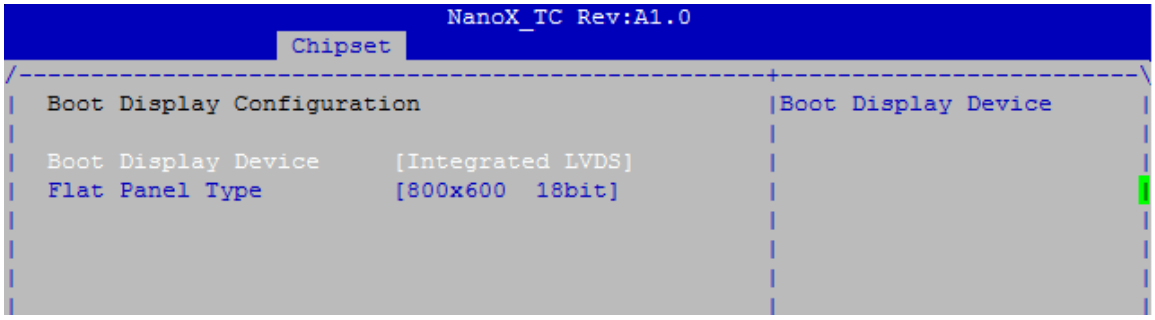
IGD Mode Select

Select the amount of system memory used by the integrated graphics device. Options: Disable/1M/4M/8M/16M/32M/48M/64M.

MSAC Mode Select

Select the size of the graphics memory aperture and untrusted space. Used by the integrated graphics device. Options: 512M/256M/128M.

Boot Display Configuration

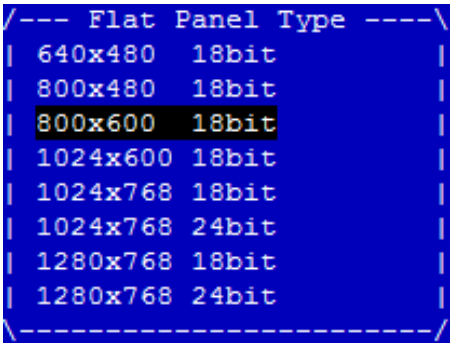


Boot Display Device

Select the boot display device. Options: Auto, Integrated LVDS, or External DVI/HDMI (SDVO).

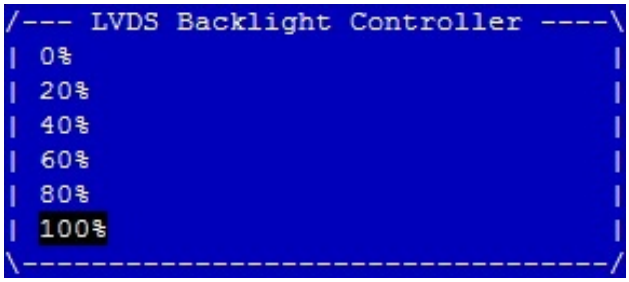
Flat Panel Type

When LVDS is selected from Boot Display Device, this option allows you to select resolution settings as below:

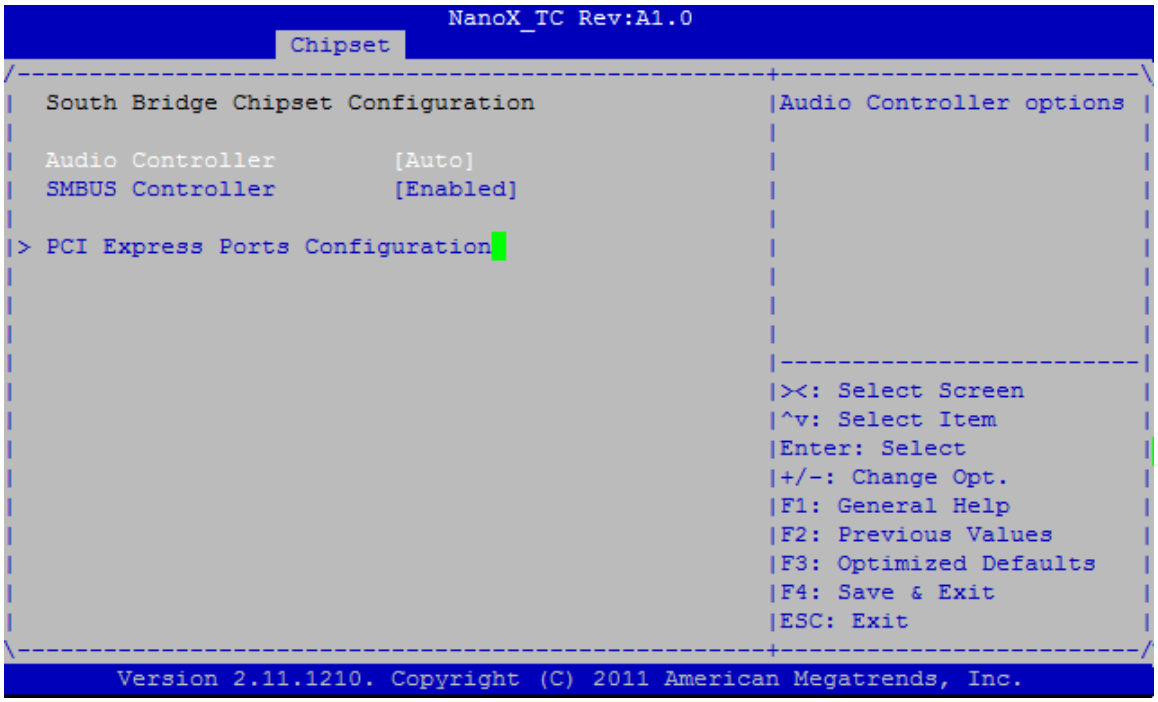


LVDS Backlight Control

When LVDS is selected from Boot Display Device, this option allows you to select LVDS Backlight settings as below:



8.5.2 South Bridge Chipset Configuration



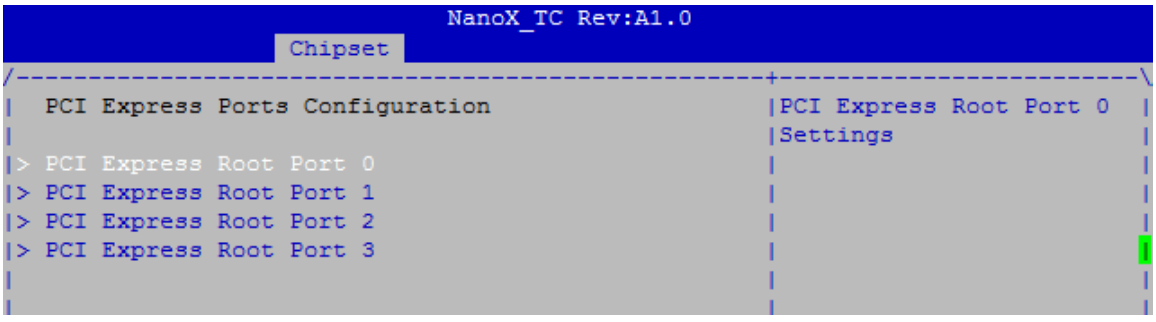
Audio Controller

The audio controller. Set this value to Enabled/Disabled/Auto.

SMBus Controller

The SMBus controller. Set this value to Enabled/Disabled.

PCI Express Ports Configuration

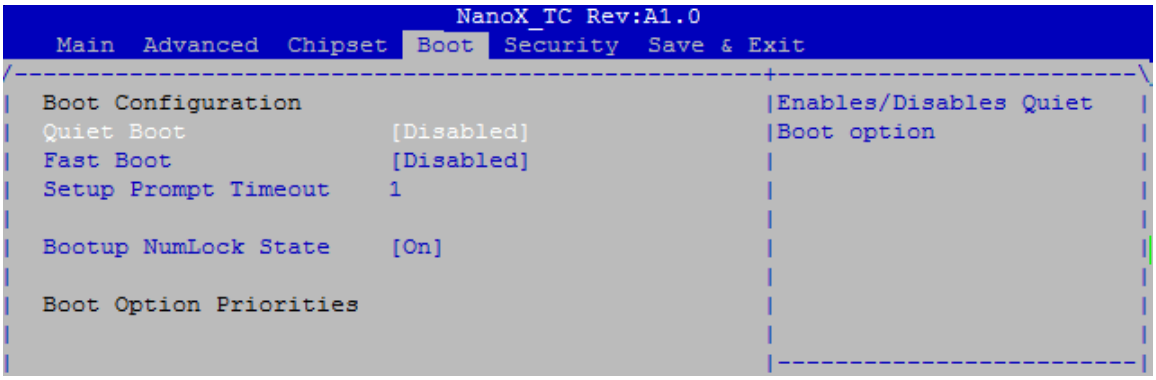


PCI Express Root Ports

Options: Enable, Disable.

8.6 Boot Setup

Select the Boot tab from the setup screen to enter the Boot Setup screen.



Quiet Boot

Disabled - Set this value to allow the computer system to display the POST messages.
Enabled - Set this value to allow the computer system to display the OEM logo.

Fast Boot

Disabled - Set this value to allow the BIOS to perform all POST tests.
Enabled - Set this value to allow the BIOS to skip certain POST tests to boot faster.

Setup Prompt Timeout

Number of seconds to wait for setup activation key. 65535 (0xFFFF) means wait indefinitely.

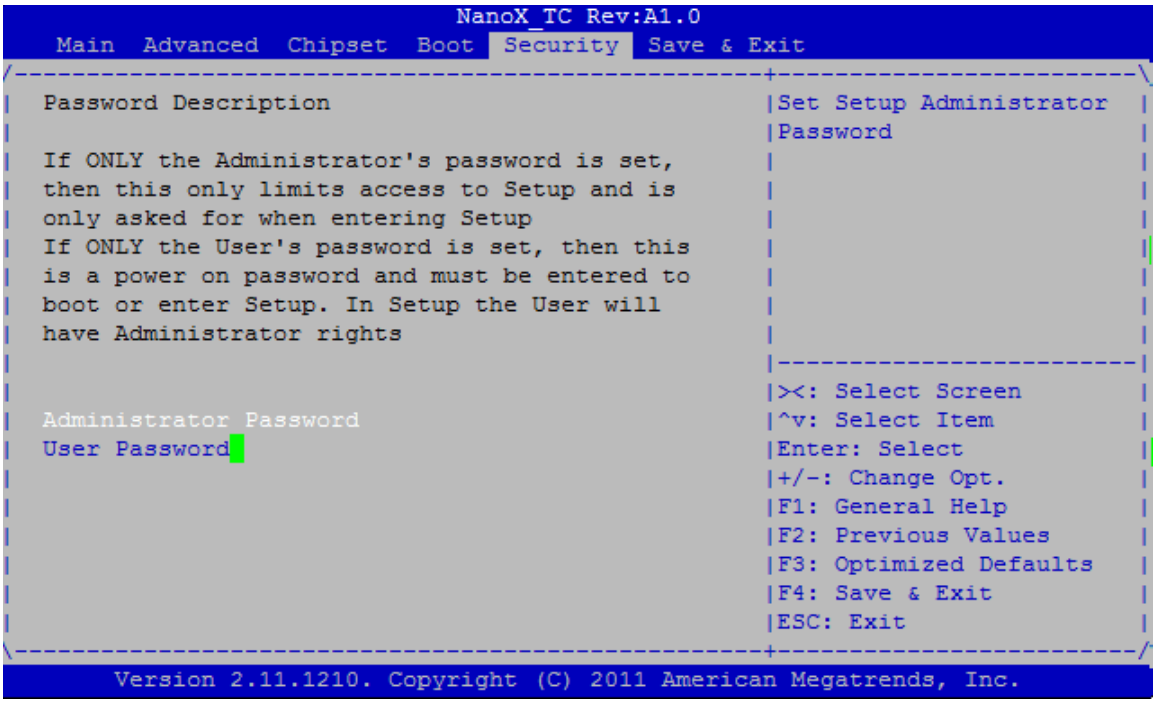
Bootup Num-Lock

Set this value to allow the Number Lock setting to be modified during boot up.
Off - This option does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad. The Number Lock LED on the keyboard will light up when the Number Lock is engaged.
On - Set this value to allow the Number Lock on the keyboard to be enabled automatically when the computer system is boot up. This allows the immediate use of 10-keys numeric keypad located on the right side of the keyboard. To confirm this, the Number Lock LED light on the keyboard will be lit.

Boot Option Priorities

This option sets the priorities of the boot options. The user can change the priorities by selecting the particular boot option. The device selected in Boot option #1 will be the first priority, followed by second, third and so on.

8.7 Security Setup



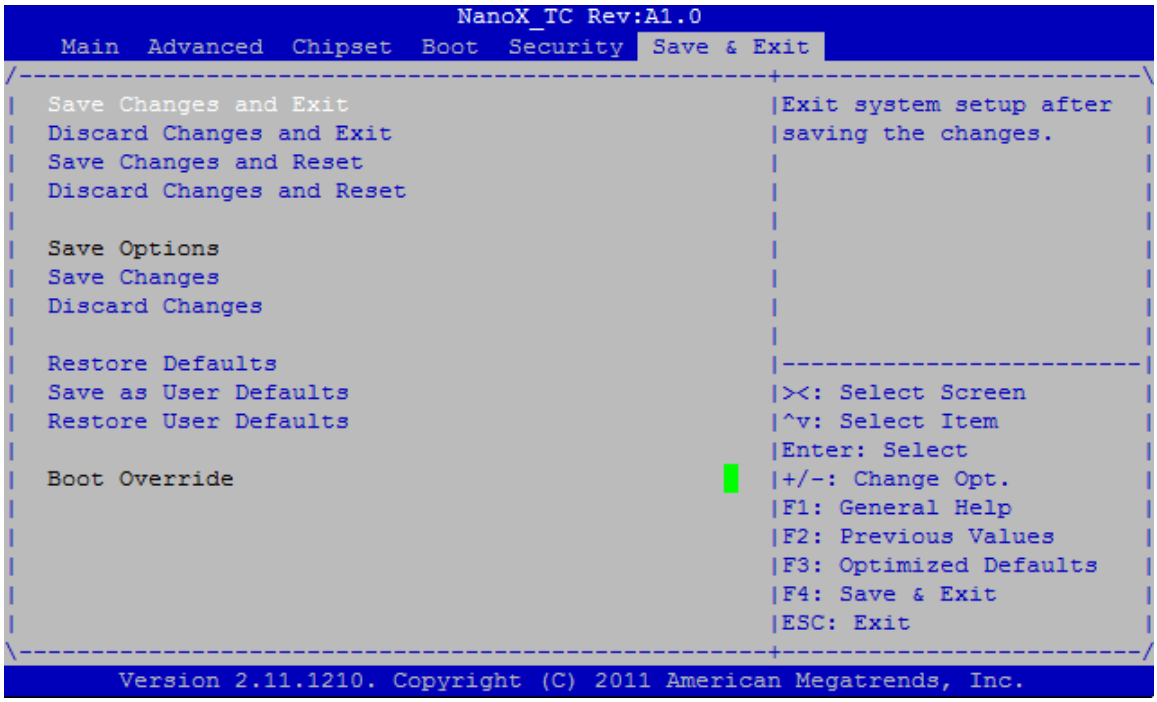
Administrator Password

Use this option to set a password for administrators with full control of the BIOS setup utility.

User Password

Use this option to set a password for users with limited access to the BIOS setup utility.

8.8 Save & Exit



Save Changes and Exit

When you have completed the system configuration changes, select this option to save changes and continue booting the system. New configuration parameters will take effect after the next system restart.

Discard Changes and Exit

Select this option to quit Setup without saving changes to the system configuration and continue booting.

Save Changes and Reset

Reset the system after saving the changes.

Discard Changes and Reset

Reset system setup without saving any changes.

Save Options

Save changes made so far to any of the setup options.

Save Changes

When you have completed the system configuration changes, select this option to save your system configuration and continue. For some of the options it required to reset the system to take effect. Select YES to Save Changes and continue.

Discard Changes

Discard any unsaved changes

Restore Defaults

Restore standard default values for all the setup options.

Save as User Defaults

Save the changes made so far as User Defaults.

Restore User Defaults

Restore the User Defaults to all the setup options.

Boot Override

Use the up/down arrow keys to highlight a boot device or "Launch EFI Shell" to immediately exit the BIOS Setup and boot from the selected device.

9 BIOS Checkpoints, Beep Codes

This section of this document lists checkpoints and beep codes generated by AMIBIOS. The checkpoints defined in this document are inherent to the AMIBIOS generic core, and do not include any chipset or board specific checkpoint definitions.

Checkpoints and Beep Codes Definition

A checkpoint is either a byte or word value output to I/O port 80h. The BIOS outputs checkpoints throughout bootblock and Power-On Self Test (POST) to indicate the task the system is currently executing. Checkpoints are very useful for debugging problems that occur during the preboot process.

Beep codes are used by the BIOS to indicate a serious or fatal error. They are used when an error occurs before the system video has been initialized, and generated by the system board speaker.

Viewing BIOS Checkpoints

Viewing all checkpoints generated by the BIOS requires a checkpoint card, also referred to as a “POST Card” or “POST Diagnostic Card”. These are PCI add-in cards that show the value of I/O port 80h on a LED display.

Some computers display checkpoints in the bottom right corner of the screen during POST. This display method is limited, since it only displays checkpoints that occur after the video card has been activated.

Keep in mind that not all computers using AMIBIOS enable this feature. In most cases, a checkpoint card is the best tool for viewing AMIBIOS checkpoints.

9.1 Status Code Ranges

Status Code Range	Description
0x01 – 0x0F	SEC Status Codes & Errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0xCF	DXE execution up to BDS
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

9.2 Standard Status Codes

SEC Status Codes

Status Code	Description
0x0	Not used
Progress Codes	
0x1	Power on. Reset type detection (soft/hard).
0x2	AP initialization before microcode loading
0x3	North Bridge initialization before microcode loading
0x4	South Bridge initialization before microcode loading
0x5	OEM initialization before microcode loading
0x6	Microcode loading
0x7	AP initialization after microcode loading
0x8	North Bridge initialization after microcode loading
0x9	South Bridge initialization after microcode loading
0xA	OEM initialization after microcode loading
0xB	Cache initialization
SEC Error Codes	
0xC – 0xD	Reserved for future AMI SEC error codes
0xE	Microcode not found
0xF	Microcode not loaded

SEC Beep Codes

None.

PEI Status Codes

Status Code	Description
0x0	Not used
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started

PEI Status Codes (cont'd)

PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
S3 Resume Error Codes	
0xE8	S3 Resume Failed in PEI
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
7	Reset PPI is not available
4	Recovery failed
4	S3 Resume failed

DXE Status Codes

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)
0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started

DXE Status Codes (cont'd)

Status Code	Description
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes

DXE Status Codes (cont'd)

DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

DXE Beep Codes

# of Beeps	Description
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
1	Invalid password
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

ACPI/ASL Status Codes

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

9.3 OEM-Reserved Status Code Ranges

Status Code	Description
0x5	OEM SEC initialization before microcode loading
0xA	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

Important Safety Instructions

For user safety, please read and follow all instructions, **warnings**, **cautions**, and **notes** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:

  - Turn off power and unplug any power cords/cables.

- To avoid electrical shock and/or damage to equipment:

  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.
- A Lithium-type battery may be provided for uninterrupted, backup or emergency power.

Risk of explosion if battery is replaced by an incorrect type. Dispose of used batteries according to the instructions.

- Equipment must be serviced by authorized technicians when:

  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

Getting Service

Contact us should you require any service or assistance.

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