에이디반도체

TS20

20-Ch Auto Sensitivity Calibration Capacitive Touch Sensor

SPECIFICATION

VER. 1.9

TS20 (20-CH Auto Sensitivity Calibration Capacitive Touch Sensor)

General

The TS20 is 20-Channel capacitive sensor with auto sensitivity calibration. And the supply voltage range is from 2.5 to 5.0V.

The TS20 offers LED drivers with 16 steps dimming controller. The CS1~CS20 ports can be used for PWM output for LED dimming control.

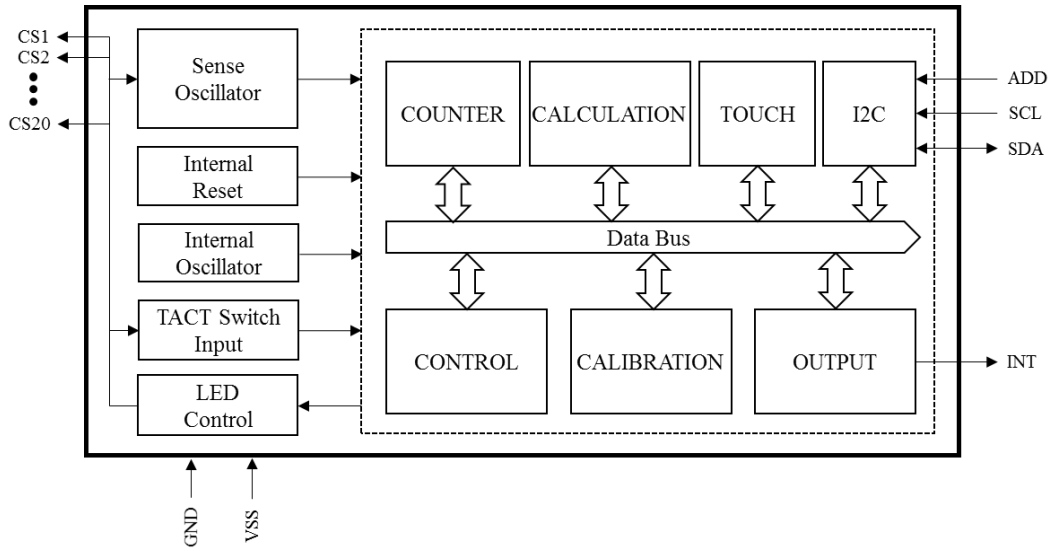
The TS20 offers a tact switch input. The CS1~CS20 ports can be used for a tact switch input.

The result of touch sensing can be checked by the I^2C serial interface.

Feature

■ 20-Channel capacitive sensor with auto sensitivity calibration
■ I2C serial interface
■ Selectable output operation (single mode / multi-mode)
■ Independently adjustable in 16 steps (2 mode) sensitivity
■ Adjustable response time by the control registers
■ Embedded common and normal noise elimination circuit
■ Available LED PWM drive ports up to 20 channels
■ Available tact switch input up to 20 channels
■ Typical current consumption in slow mode
85 uA (@3.3V)
■ Clock-off mode to reduce the current consumption
9uA (@3.3V)
■ RoHS compliant 28QFN and 28TSSOP package

Block Diagram



Application

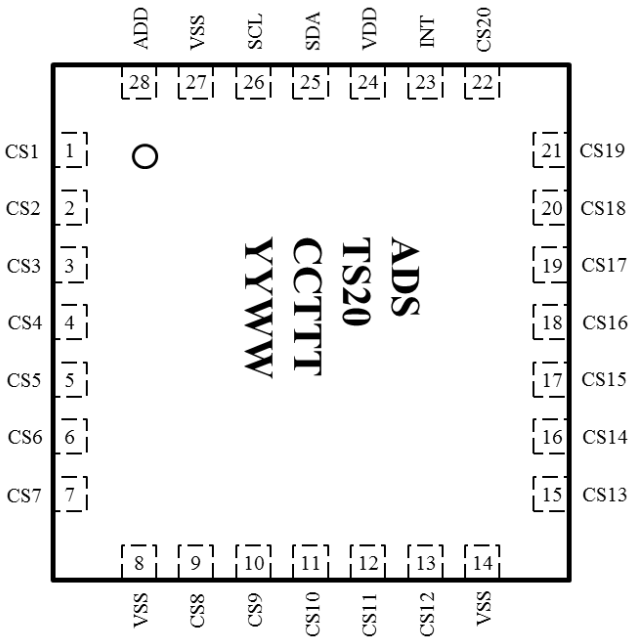
■ Mobile application (mobile phone, PDA, PMP, MP3, Car navigation)
■ Membrane switch replacement
■ Sealed control panels, keypads
■ Door key-lock matrix application
■ Touch screen replacement application

Ordering Information

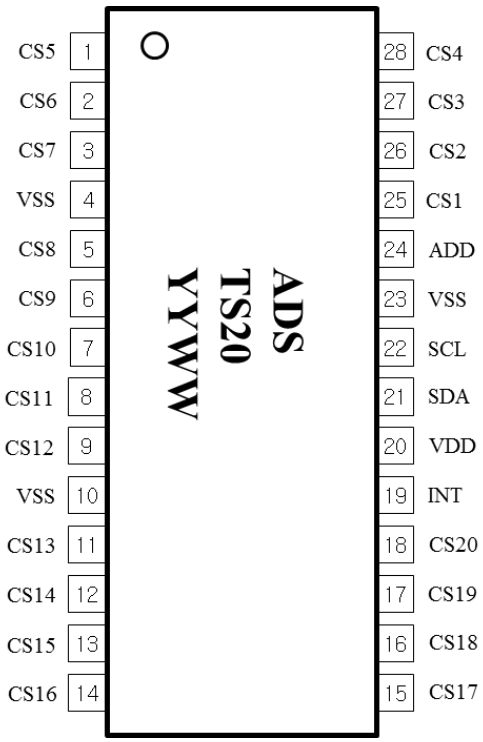
Part No.	Package
TS20-Q	28QFN
TS20	28TSSOP

Content

1 Pin Configuration



[28-QFN]



[28-TSSOP]

2 Pin Description

VDD, VSS
Supply voltage and ground pin.

CS1~CS20
Capacitive sensor input pins. CS1 ~ CS20 port can be changed tact switch input port or LED PWM drive output port with using the "Port_CTRL1~Port_CTRL6[1]" registers. And the luminance of LED is possible to control with using the "Sensitivity/PWM1~Sensitivity/PWM11[2]" register.

SCL, SDA
SCL is I2C clock input pin and SDA is I2C data input-output pin.

INT
Touch sensing interrupt output pin.

ADD
Slave address selection pin.

[1] Refer to chapter 8.2.5 Ports Control Register.
[2] Refer to chapter 8.2.1 Sensitivity Control Register.

2.1 TS20-Q (28QFN package)

PIN No.	Name	I/O	Description	Protection
1	CS1	Analog Input /Digital Output	Capacitive sensor input 1 Tact switch input[3] 1 LED Drive output[4] 1 (Open drain)	VDD/GND
2	CS2	Analog Input /Digital Output	Capacitive sensor input 2 Tact switch input 2 LED Drive output 2 (Open drain)	VDD/GND
3	CS3	Analog Input /Digital Output	Capacitive sensor input 3 Tact switch input 3 LED Drive output 3 (Open drain)	VDD/GND
4	CS4	Analog Input /Digital Output	Capacitive sensor input 4 Tact switch input 4 LED Drive output 4 (Open drain)	VDD/GND
5	CS5	Analog Input /Digital Output	Capacitive sensor input 5 Tact switch input 5 LED Drive output 5 (Open drain)	VDD/GND
6	CS6	Analog Input /Digital Output	Capacitive sensor input 6 Tact switch input 6 LED Drive output 6 (Open drain)	VDD/GND
7	CS7	Analog Input /Digital Output	Capacitive sensor input 7 Tact switch input 7 LED Drive output 7 (Open drain)	VDD/GND
8	VSS	Ground	Supply ground	VDD
9	CS8	Analog Input /Digital Output	Capacitive sensor input 8 Tact switch input 8 LED Drive output 8 (Open drain)	VDD/GND
10	CS9	Analog Input /Digital Output	Capacitive sensor input 9 Tact switch input 9 LED Drive output 9 (Open drain)	VDD/GND
11	CS10	Analog Input /Digital Output	Capacitive sensor input 10 Tact switch input 10 LED Drive output 10 (Open drain)	VDD/GND
12	CS11	Analog Input /Digital Output	Capacitive sensor input 11 Tact switch input 11 LED Drive output 11 (Open drain)	VDD/GND
13	CS12	Analog Input /Digital Output	Capacitive sensor input 12 Tact switch input 12 LED Drive output 12 (Open drain)	VDD/GND
14	VSS	Ground	Supply ground	VDD
15	CS13	Analog Input /Digital Output	Capacitive sensor input 13 Tact switch input 13 LED Drive output 13 (Open drain)	VDD/GND
16	CS14	Analog Input /Digital Output	Capacitive sensor input 14 Tact switch input 14 LED Drive output 14 (Open drain)	VDD/GND
17	CS15	Analog Input	Capacitive sensor input 15	VDD/GND

[3] Refer to chapter 8.2 CS implementation for Tact switch input.
[4] Refer to chapter 8.3 CS implementation for LED drive output.

		/Digital Output	Tact switch input 15 LED Drive output 15 (Open drain)	
18	CS16	Analog Input /Digital Output	Capacitive sensor input 16 Tact switch input 16 LED Drive output 16 (Open drain)	VDD/GND
19	CS17	Analog Input /Digital Output	Capacitive sensor input 17 Tact switch input 17 LED Drive output 17 (Open drain)	VDD/GND
20	CS18	Analog Input /Digital Output	Capacitive sensor input 18 Tact switch input 18 LED Drive output 18 (Open drain)	VDD/GND
21	CS19	Analog Input /Digital Output	Capacitive sensor input 19 Tact switch input 19 LED Drive output 19 (Open drain)	VDD/GND
22	CS20	Analog Input /Digital Output	Capacitive sensor input 20 Tact switch input 20 LED Drive output 20 (Open drain)	VDD/GND
23	INT	Digital Output	Interrupt output (Open drain)	VDD/GND
24	VDD	Power	Power (2.5V~5.0V)	GND
25	SDA	Digital Input/Output	I2C data input-output (Open drain)	VDD/GND
26	SCL	Digital Input	I2C clock input	VDD/GND
27	VSS	Ground	Supply ground	VDD
28	ADD	Digital Input	I2C slave ID selection input[5]	VDD/GND

[5] Refer to chapter 8. I2C Interface

2.2 TS20 (28TSSOP package)

PIN No.	Name	I/O	Description	Protection
1	CS5	Analog Input /Digital Output	Capacitive sensor input 5 Tact switch input 5 LED Drive output 5 (Open drain)	VDD/GND
2	CS6	Analog Input /Digital Output	Capacitive sensor input 6 Tact switch input 6 LED Drive output 6 (Open drain)	VDD/GND
3	CS7	Analog Input /Digital Output	Capacitive sensor input 7 Tact switch input 7 LED Drive output 7 (Open drain)	VDD/GND
4	VSS	Ground	Supply ground	VDD
5	CS8	Analog Input /Digital Output	Capacitive sensor input 8 Tact switch input 8 LED Drive output 8 (Open drain)	VDD/GND
6	CS9	Analog Input /Digital Output	Capacitive sensor input 9 Tact switch input 9 LED Drive output 9 (Open drain)	VDD/GND
7	CS10	Analog Input /Digital Output	Capacitive sensor input 10 Tact switch input 10 LED Drive output 10 (Open drain)	VDD/GND
8	CS11	Analog Input /Digital Output	Capacitive sensor input 11 Tact switch input 11 LED Drive output 11 (Open drain)	VDD/GND
9	CS12	Analog Input /Digital Output	Capacitive sensor input 12 Tact switch input 12 LED Drive output 12 (Open drain)	VDD/GND
10	VSS	Ground	Supply ground	VDD
11	CS13	Analog Input /Digital Output	Capacitive sensor input 13 Tact switch input 13 LED Drive output 13 (Open drain)	VDD/GND
12	CS14	Analog Input /Digital Output	Capacitive sensor input 14 Tact switch input 14 LED Drive output 14 (Open drain)	VDD/GND
13	CS15	Analog Input /Digital Output	Capacitive sensor input 15 Tact switch input 15 LED Drive output 15 (Open drain)	VDD/GND
14	CS16	Analog Input /Digital Output	Capacitive sensor input 16 Tact switch input 16 LED Drive output 16 (Open drain)	VDD/GND
15	CS17	Analog Input /Digital Output	Capacitive sensor input 17 Tact switch input 17 LED Drive output 17 (Open drain)	VDD/GND
16	CS18	Analog Input /Digital Output	Capacitive sensor input 18 Tact switch input 18 LED Drive output 18 (Open drain)	VDD/GND
17	CS19	Analog Input /Digital Output	Capacitive sensor input 19 Tact switch input 19 LED Drive output 19 (Open drain)	VDD/GND

18	CS20	Analog Input /Digital Output	Capacitive sensor input 20 Tact switch input 20 LED Drive output 20 (Open drain)	VDD/GND
19	INT	Digital Output	Interrupt output (Open drain)	VDD/GND
20	VDD	Power	Power (2.5V~5.0V)	GND
21	SDA	Digital Input/Output	I2C data input-output (Open drain)	VDD/GND
22	SCL	Digital Input	I2C clock input	VDD/GND
23	VSS	Ground	Supply ground	VDD
24	ADD	Digital Input	I2C slave ID selection input	VDD/GND
25	CS1	Analog Input /Digital Output	Capacitive sensor input 1 Tact switch input 1 LED Drive output 1 (Open drain)	VDD/GND
26	CS2	Analog Input /Digital Output	Capacitive sensor input 2 Tact switch input 2 LED Drive output 2 (Open drain)	VDD/GND
27	CS3	Analog Input /Digital Output	Capacitive sensor input 3 Tact switch input 3 LED Drive output 3 (Open drain)	VDD/GND
28	CS4	Analog Input /Digital Output	Capacitive sensor input 4 Tact switch input 4 LED Drive output 4 (Open drain)	VDD/GND

3 Absolute Maximum Rating

Maximum supply voltage	5.5V
Maximum voltage on any pin	VDD+0.3
Maximum current on any PAD	100mA
Power Dissipation	800mW
Storage Temperature	-50 ~ 150℃
Operating Temperature	-20 ~ 75℃
Junction Temperature	150℃

Note Unless any other command is noted, all above are operated in normal temperature.

4 ESD & Latch-up Characteristics

4.1 ESD Characteristics

Mode	Polarity	Minimum Level	Reference
H.B.M	Pos / Neg	8000V	VDD
		8000V	GND
		8000V	P to P
M.M	Pos / Neg	625V	VDD
		625V	GND
		500V	P to P
C.D.M	-	1000V	Field Induced Charge

4.2 Latch-up Characteristics

Mode	Polarity	Minimum Level	Reference
I Test	Positive	100mA	JESD78A
	Negative	-100mA	
V supply over 5.0V	Positive	8.0V	

5 Electrical Characteristics

▪ V_{DD}=3.3V, T_A = 27℃

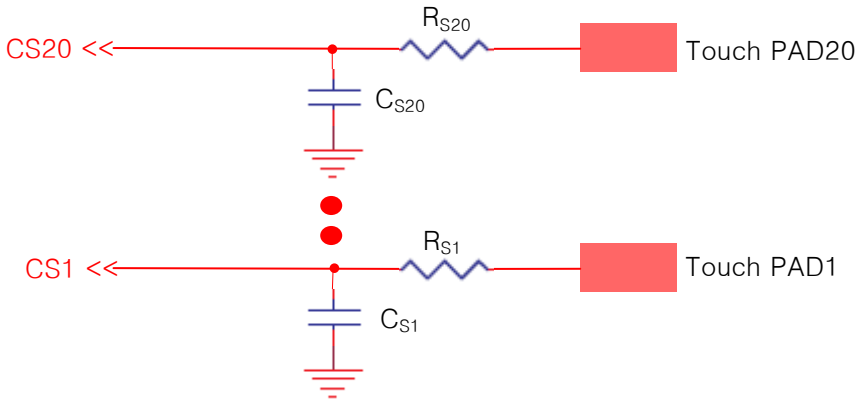
Characteristics	Symbol	Test Condition		Min	Typ	Max	Units
Operating supply voltage	V_{DD}			2.5	3.3	5.0	V
Current consumption[6]	I_{DD}	Slow mode[7]	V_{DD}= 3.3V	-	85	-	μA
			V_{DD}= 5.0V	-	120	-	
		Normal mode	V_{DD}= 3.3V	-	130	180	
			V_{DD}= 5.0V		180	240	
		Fast mode	V_{DD}= 3.3V		190	-	
			V_{DD}= 5.0V	-	250	-	
		Clock-off mode	V_{DD}= 3.3V	-	9	-	
			V_{DD}= 5.0V	-	11	-	
	I_{DD_I2C}	V_{DD}= 3.3V (2M Bps)		-	1.8	2.2	mA
		V_{DD}= 5.0V (2M Bps)		-	2.8	3.4	
Digital output maximum sink current	I_{OUT}	T_A = 25℃ (Normal I2C Output)		-	-	4.0	mA
LED drive output sink current per 1channel	I_{LED_OUT}	T_A = 25℃ (LED Drive Output)		-	-	8.0	mA
LED drive output total sink current	I_{LED_TOT}	T_A = 25℃ (LED Drive Output)		-	-	30.0	mA
Tact switch interface input internal pull-up current	I_{TACT}	V_{DD}= 5.0V, T_A = 25℃		-	5.6	-	μA
Start supply voltage for internal reset	V_{DD_RST}	T_A = 25℃		-	-	$0.3 \cdot V_{DD}$	V
Sense input capacitance range	C_S			-	-	50	pF
Minimum detective capacitance difference	ΔC_{MIN}			0.1	-	-	pF
Output impedance (open drain)	Zo	$\Delta C > \Delta C_{MIN}$		-	12	-	Ω
		$\Delta C < \Delta C_{MIN}$		-	30M	-	
Self calibration time after system reset	T_{CAL}	Slow calibration speed		-	100	-	ms
		Normal calibration speed		-	80	-	
		Fast calibration speed		-	60	-	
Sense input resistance	R_S	-		-	200	1000	Ω
Internal reset pulse duration	T_{RST}			2.5	-	-	usec
SCL, SDA rising delay	T_{SCL}, T_{SDA}			0	-	1	usec
Minimum power on SCL, SDA high time	T_{H_SCL}, T_{H_SDA}			100	-	-	msec

[6] Maximum communication speed is 2Mbps.
[7] Refer to chapter 8.2.3 General Control Register.

6 TS20 Implementation

6.1 CS implementation

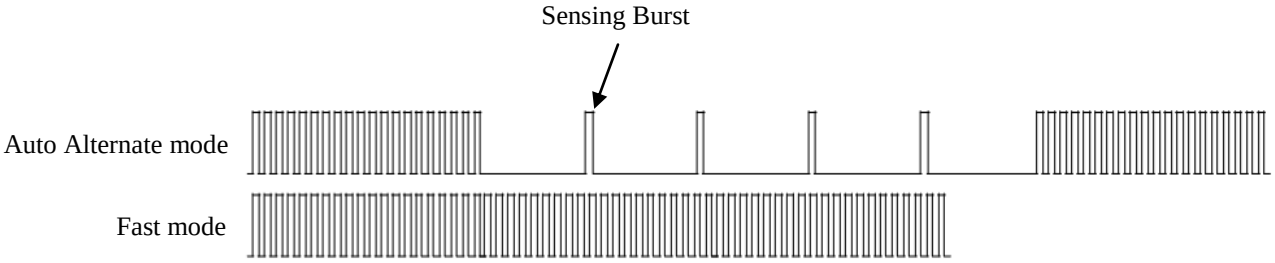
TS20 has 2 sensitivity modes and each mode has 16 step selections of the sensitivity. And Sensitivity of each sensing channel (CS) can be independently controlled by TS20 Control Register (I2C interface). External components of CS pin such as series resistor or parallel capacitor isn't necessary. The parallel parasitic capacitance of CS pins caused by touch line, touch pad and adjacent GND or other pattern may affect sensitivity. The sensitivity will be decreased when bigger parallel parasitic capacitance of CS pin is added.
Sensitivity mediation is required to complement sensitivity difference between channels. Parallel capacitor ($C_{S1\sim S20}$) of CS pin is useful in case of detail sensitivity mediation. The sensitivity would be increased when smaller value of C_S is used. Under 50pF capacitor can be used as sensitivity meditation capacitor and a few pF is usually used. The R_S, serial connection resistor of CS pins, may be used to avoid mal-function from external surge and ESD. (It might be optional.) From 200Ω to 1kΩ is recommended for R_S. Refer to below CS pins application figure.



The TS20 has twenty independent touch sensor inputs from CS1 to CS20. The internal touch decision process of each channel is separated from others. Therefore twenty channel touch key board application can be designed by using only one TS20 without coupling problems.
The size and shape of PAD might have influence on the sensitivity. The sensitivity will be optimal when the size of PAD is approximately an half of the first knuckle (it's about 10 ㎜ x 7 ㎜). The connection line of CS to touch PAD is recommended to be routed as short as possible to prevent from abnormal touch detect caused by connection line. And it must not touch the PAD directly without any case.
The unused CS channel must be hold with the ports control registers[8]. And the unused CS pin must be connected with the ground to prevent the unpredictable mal-function that occurred in the floating CS pin.
The CSX[9] port goes the low impedance except sensing period when the "IMP_SEL" register[10] is set by '0'. And if the "IMP_SEL" register is set by '1', the CSX port is to be always high impedance.
The TS20 has two operation modes[11] that are the auto alternate mode and fast mode.

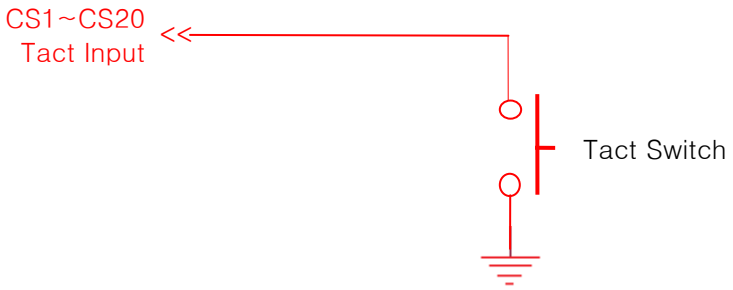
[8] Refer to chapter 8.2.5 Ports Control Register.
[9] X = 1 to 20
[10] Refer to chapter 8.2.3 General Control Register 2.
[11] Refer to chapter 8.2.2 General Control Register 1.

Operation Mode Figure



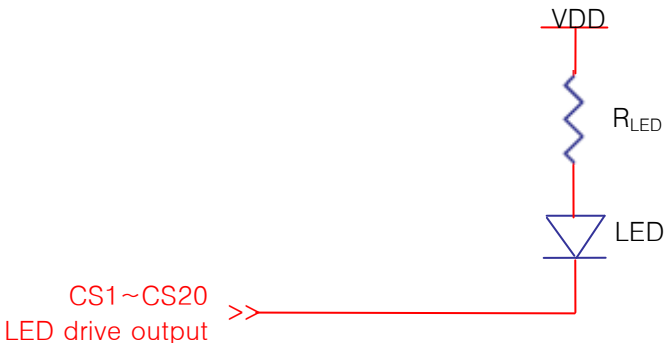
The auto alternate mode is helpful to reduce the current consumption. And the fast mode is very good for noisy environment.

6.2 CS implementation for tact switch input



CS input ports are possible to change to tact switch input by setting the Port Control Register[12] through I2C interface. The number of possible tact switch input is 20. And user can get the output data from output registers (Chapter 8.9). When the CS is used for tact switch input, the internal pull-up current source makes it possible without external pull-up resistors. Typical internal pull-up current is 5.6uA independent to external condition

6.3 CS implementation for LED drive output



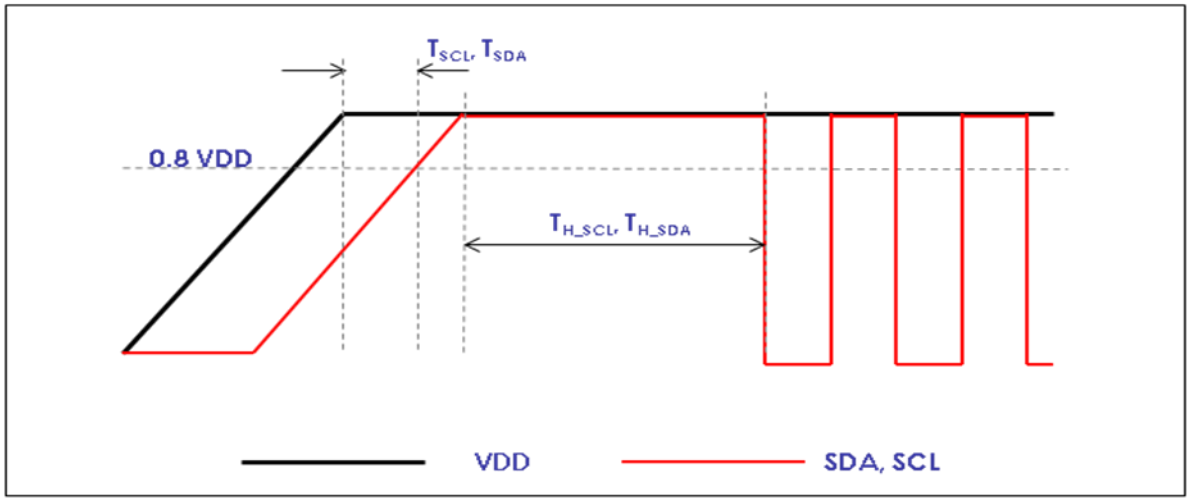
[12] Refer to chapter 8.2.5 Ports Control Register

CS input ports are possible to change to LED drive output by setting the Port Control Register[13] through I2C interface. The number of possible LED drive output channel is 20. Each channel has 16 steps of LED dimming. Each LED dimming step is controlled by setting Port Control Register through I2C interface. The maximum current that is sunk by CS is 8mA when the CS is used for LED drive output port.

6.4 Internal reset operation

The TS20 has stable internal reset circuit to offer reset pulse to digital block. The supply voltage for a system start or restart should be under $0.3 \cdot V_{DD}$ of normal operation V_{DD}. No external components required for TS20 power reset, that helps simple circuit design and to realize the low cost application.

6.5 Power on sequence for SCL & SDA



Timing Diagram

Items	Description	min	typ	max	unit
T_{SCL}	Settling time for SCL voltage rising to 0.8 VDD	0	-	1.0	usec
T_{SDA}	Settling time for SDA voltage rising to 0.8 VDD	0	-	1.0	usec
T_{H_SCL}, T_{H_SDA}	SCL SDA high pulse remain time for power on	100	-	-	msec

[13] Refer to chapter 8.2.5 Ports Control Register

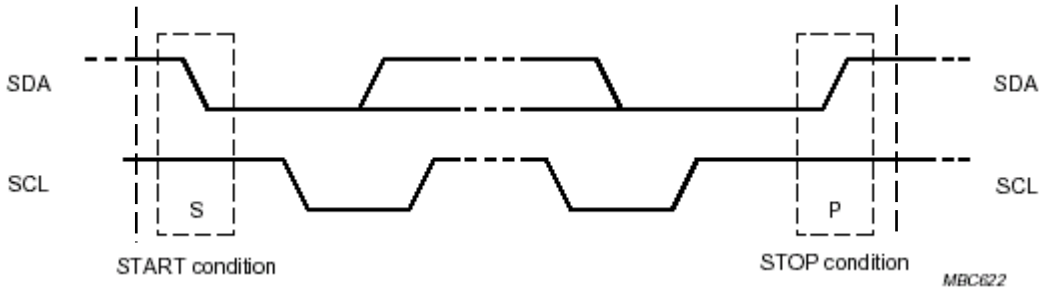
7 I2C Interface

7.1 I2C Enable / Disable

If the SDA or SCL signal goes to low, I2C control block is enabled automatically. And if the SDA and SCL signal maintain high during about 2 us, I2C control block is disabled automatically also.

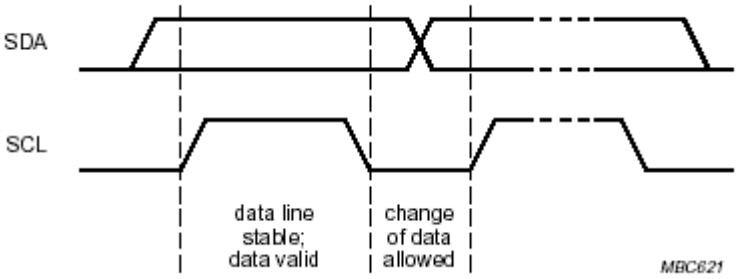
7.2 Start & Stop Condition

- Start Condition (S)
- Stop Condition (P)
- Repeated Start (Sr)



7.3 Data validity

The SDA should be stable when the SCL is high and the SDA can be changed when the SCL is low.

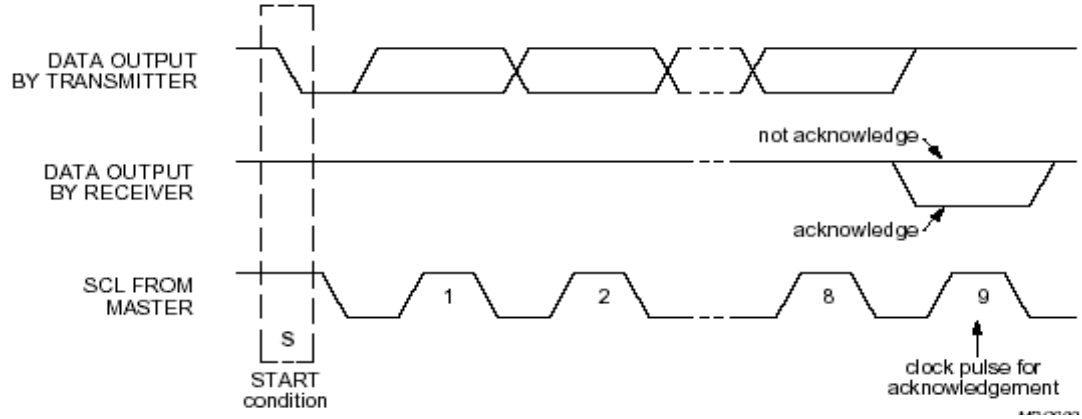


7.4 Byte Format

The byte structure is composed with 8Bit data and an acknowledge signal.

7.5 Acknowledge

It is a check bit whether the receiver gets the data from the transmitter without error or not. The receiver will write '0' when it received the data successfully and '1' if not.



7.6 First Byte

7.6.1 Slave Address

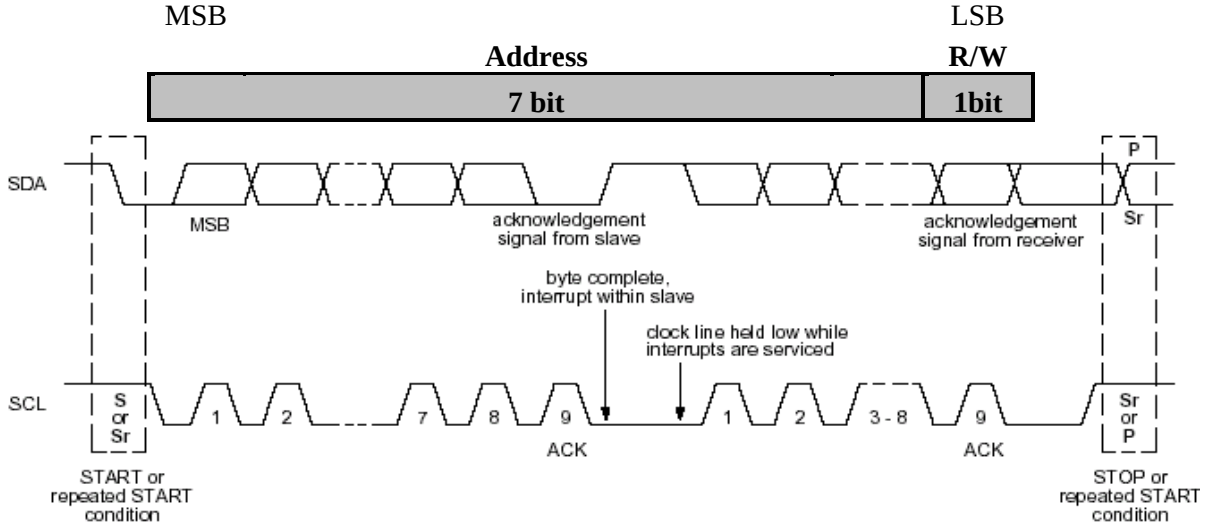
It is the first byte from the start condition. It is used to access the slave device.

TS20 Chip Address : 7bit

ADD	Address
GND	0xD4
VDD	0xF4

7.6.2 R/$\overline{W}$

The direction of data is decided by the bit and it follows the address data.

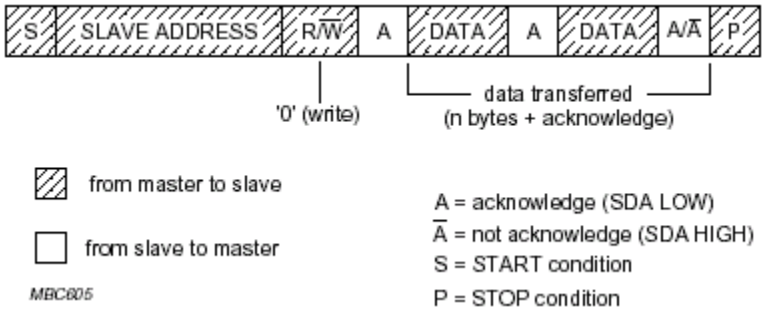


7.7 Transferring Data

7.7.1 Write Operation

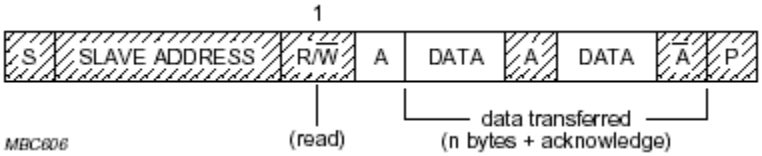
The byte sequence is as follows:

1. The first byte gives the device address plus the direction bit (R/W = 0).
2. The second byte contains the internal address of the first register to be accessed.
3. The next byte is written in the internal register. Following bytes are written in successive internal registers.
4. The transfer lasts until stop conditions are encountered.
5. The TS20 acknowledges every byte transfer.

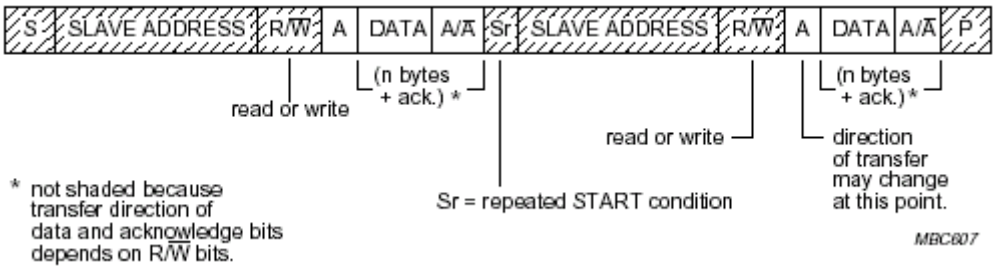


7.7.2 Read Operation

The address of the first register to read is programmed in a write operation without data, and terminated by the stop condition. Then, another start is followed by the device address and R/W= 1. All following bytes are now data to be read at successive positions starting from the initial address.



7.7.3 Read/Write Operation



7.8 I2C write and read operations in normal mode

The following figure represents the I^2C normal mode write and read registers.

☞ Write register 0x00 to 0x01 with data AA and BB

Start	Device Address 0xD4	ACK	Register Address 0x00	ACK	Data AA	ACK	Data BB	ACK	Stop

Read register 0x00 and 0x01

Start	Device Address 0xD4	ACK	Register Address 0x00	ACK	Stop

Start	Device Address 0xD5	ACK	Data Read AA	ACK	Data Read BB	$\overline{\text{ACK}}$	Stop

From Master to Slave From Slave to Master

8 TS20 Control Register List

◂ Note 1 : The unused bits (defined as reserved) in I2C register must be kept to the reset value or refer to the details.

◂ Note 2 : The empty bits (defined as '-') in I2C register are zero at read operation. So the empty bits are recommended as zero at write operation.

8.1 I2C Register Map

Name	Addr. (Hex)	Reset Value (Bin)	Register Function and Description							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Sensitivity/PWM1	00H	0101 0101	SEN_PWM_CH2				SEN_PWM_CH1			
Sensitivity/PWM2	01H	0101 0101	SEN_PWM_CH4				SEN_PWM_CH3			
Sensitivity/PWM3	02H	0101 0101	SEN_PWM_CH6				SEN_PWM_CH5			
Sensitivity/PWM4	03H	0101 0101	Reserved				SEN_PWM_CH7			
Sensitivity/PWM5	04H	0101 0101	SEN_PWM_CH9				SEN_PWM_CH8			
Sensitivity/PWM6	05H	0101 0101	SEN_PWM_CH11				SEN_PWM_CH10			
Sensitivity/PWM7	06H	0101 0101	SEN_PWM_CH13				SEN_PWM_CH12			
Sensitivity/PWM8	07H	0101 0101	SEN_PWM_CH15				SEN_PWM_CH14			
Sensitivity/PWM9	08H	0101 0101	SEN_PWM_CH17				SEN_PWM_CH16			
Sensitivity/PWM10	09H	0101 0101	SEN_PWM_CH19				SEN_PWM_CH18			
Sensitivity/PWM11	0AH	---- 0101	-				SEN_PWM_CH20			
GTRL1	0BH	-100 1010	-	SSC	MS	FTC		RTC		
GTRL2	0CH	0001 0010	VPM	Reserved	S/M_SEL	IMP_SEL	SRST	CLK_OFF	RB_EL	
Cal_CTRL	0DH	1111 1010	BF_UP		BF_DOWN		BS_UP		BS_DOWN	
Port_CTRL1	0EH	0000 0000	CH4		CH3		CH2		CH1	
Port_CTRL2	0FH	0000 0000	Reserved		CH7		CH6		CH5	
Port_CTRL3	10H	0000 0000	CH11		CH10		CH9		CH8	
Port_CTRL4	11H	0000 0000	CH15		CH14		CH13		CH12	
Port_CTRL5	12H	0000 0000	CH19		CH18		CH17		CH16	
Port_CTRL6	13H	---- --00	-		-		-		CH20	
Cal_Hold1	14H	0000 0000	CH7	CH6	CH5	CH4	CH3	CH2	CH1	DUMMY
Cal_Hold2	15H	0000 0000	CH14	CH13	CH12	CH11	CH10	CH9	CH8	Reserved
Cal_Hold3	16H	--00 0000	-	-	CH20	CH19	CH18	CH17	CH16	CH15
Err_CTRL	17H	---0 1101	-			ERROR_COUNT			ERROR_PERCENT	

Name	Addr. (Hex)	Reset Value (Bin)	Register Function and Description							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Output1	20H	Read Only	Reserved	CH7	CH6	CH5	CH4	CH3	CH2	CH1
Output2	21H	Read Only	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Output3	22H	Read Only	-	-	ND	CH20	CH19	CH18	CH17	CH16
Ref_wr_H	23H	--00 0000	-	-	REF_COUNT[13:8]					
Ref_wr_L	24H	0000 0000	REF_COUNT[7:0]							
Ref_wr_CH1	25H	0000 0000	CH6	CH5	CH4	CH3	CH2	CH1	DUMMY	-
Ref_wr_CH2	26H	0000 0000	CH13	CH12	CH11	CH10	CH9	CH8	Reserved	CH7
Ref_wr_CH3	27H	0000 0000	CTRL	CH20	CH19	CH18	CH17	CH16	CH15	CH14
Sen_RD_CTRL	28H	---0 0000	-	-	-	SEN_RD_CHANNEL				
Sensitivity_RD	29H	Read Only	SEN_DATA							
Rd_CH1	30H	Read Only	CH6	CH5	CH4	CH3	CH2	CH1	DUMMY	CTRL
Rd_CH2	31H	Read Only	CH13	CH12	CH11	CH10	CH9	CH8	Reserved	CH7
Rd_CH3	32H	Read Only	-	CH20	CH19	CH18	CH17	CH16	CH15	CH14
Sen_H	33H	Read Only	-	-	SENSE_COUNT[13:8]					
Sen_L	34H	Read Only	SENSE_COUNT[7:0]							
Ref_H	35H	Read Only	-	-	REFERENCE_COUNT[13:8]					
Ref_L	36H	Read Only	REFERENCE _COUNT[7:0]							
Rd_CH4	37H	Read Only	CH6	CH5	CH4	CH3	CH2	CH1	DUMMY	-
Rd_CH5	38H	Read Only	CH13	CH12	CH11	CH10	CH9	CH8	Reserved	CH7
Rd_CH6	39H	Read Only	-	CH20	CH19	CH18	CH17	CH16	CH15	CH14

8.2 Details

8.2.1 Sensitivity Control Register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	Sensitivity/PWM1	SEN_PWM_CH2				SEN_PWM_CH1			
01h	Sensitivity/PWM2	SEN_PWM_CH4				SEN_PWM_CH3			
02h	Sensitivity/PWM3	SEN_PWM_CH6				SEN_PWM_CH5			
03h	Sensitivity/PWM4	Reserved				SEN_PWM_CH7			
04h	Sensitivity/PWM5	SEN_PWM_CH9				SEN_PWM_CH8			
05h	Sensitivity/PWM6	SEN_PWM_CH11				SEN_PWM_CH10			
06h	Sensitivity/PWM7	SEN_PWM_CH13				SEN_PWM_CH12			
07h	Sensitivity/PWM8	SEN_PWM_CH15				SEN_PWM_CH14			
08h	Sensitivity/PWM9	SEN_PWM_CH17				SEN_PWM_CH16			
09h	Sensitivity/PWM10	SEN_PWM_CH19				SEN_PWM_CH18			
0Ah	Sensitivity/PWM11	-				SEN_PWM_CH20			

Description

The sensitivity of channel is possible to adjust by the "Sensitivity/PWMx[14]" register. The following table show detail information of sensitivity. The sensitivity means the threshold for touching output. If the ratio of the changes between the total capacitance of the CSX before touching and the total capacitance of the CSX after touching is over sensitivity(the value of this register), the touching output of CSX is appeared with the "Output1~Output3" registers[15].

The lower value of these register TS20 has, the higher sensitivity TS20 has. And if user wants to set higher sensitivity over 0.75%, it is recommended to refer to the application note (TS20_Application_Note_R02.pdf – Q&A).

[Bit7:Bit4] of the register address 03h and the value of the unused CS channel are strongly recommended that you set to "1111".

Bit name	Reset	Function	
SEN_PWM_CH1 ~ SEN_PWM_CH20	0101	Port Control bits of Port_CTRLX[16] are "00"	Sensitivity of each channel (SSC[17] bit is '1'). Sensitivity of CSX channel : {SEN_PWM_CHX[3:0] * 0.2} + 0.15%
			Sensitivity of each channel (SSC[18] bit is '0'). Sensitivity of CSX channel : {SEN_PWM_CHX[3:0] * 0.1} + 0.05%
		"10"	LED dimming controllable up to 16 steps. 0000 : The minimum luminance(Almost Off) 1111 : The maximum luminance

[14] x = 1 to 6
[15] Refer to chapter 8.2.8 Output Register
[16] Refer to chapter 8.2.5 Ports Control Register
[17] Refer to chapter 8.2.2 General Control Register 1
[18] Refer to chapter 8.2.2 General Control Register 1

8.2.2 General Control Register 1

Type: R/W

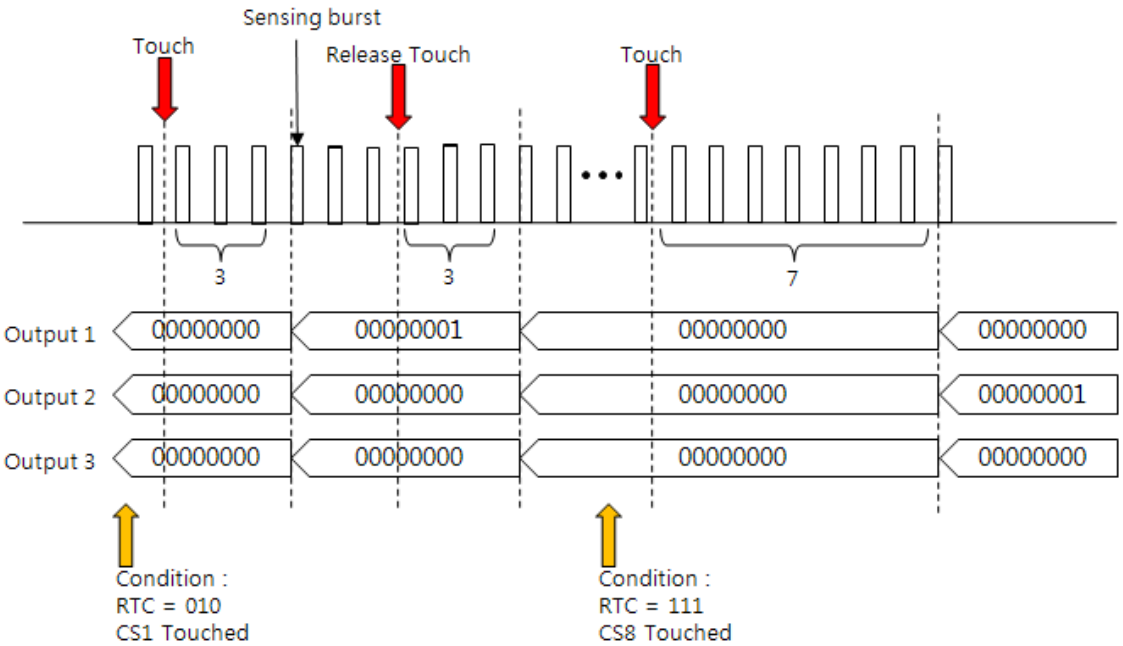
Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Bh	GTRL1	-	SSC	MS	FTC			RTC	

Description

The calibration speed just after power on reset is very high during the time which is defined by the "FTC" to have a good adoption against unstable external environment.

Bit name	Reset	Function
RTC	010	Response Time Control. Refer to the below figure - Response period = RTC[2:0] + 1 - Response period = 7, when RTC[2:0] value is "111".
FTC	01	First Touch Control - 00 : 13 * 16 * 1-Period[19] (ms) - 01 : 25 * 16 * 1-Period (ms) - 10 : 50 * 16 * 1-Period (ms) - 11 : 100 * 16 * 1-Period (ms)
MS	0	Operation Mode Selection - 0 : Auto alternate (Burst Fast/Burst Slow) mode - 1 : Fast mode(Burst Fast mod)
SSC	1	Sensitivity Step Control - 0 : Fine steps - 1 : Normal steps

RTC(Response Time Control) Figure



[19] 1-Period means that the time from the current sensing burst to the next sensing burst.

8.2.3 General Control Register 2

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Ch	GTRL2	VPM	Reserved	S/M_SEL	IMP_SEL	SRST	CLK_OFF	RB_SEL	

Description

If the "SRST" bit is set by '1', digital block is reset except analog and I2C block.
The "CLK_OFF" function allows getting very low current consumption when it is set by '1'.
The internal system frequency is controlled by the "RB_SEL" registers. The slower system frequency speed IC has, the lower current consumption IC has. The faster system frequency speed IC has, the higher current consumption IC has. It is recommended in noisy application or noisy environment. For example, refrigerator, air conditioner, CS noise environment and so on. And the change of the internal system frequency affects the sensitivity. The slow frequency has higher sensitivity than the fast frequency. For more details of RB_SEL register is refer to our application note (TS20_Application_Note_R02.pdf – Q&A).
And user can see the typical current consumption at the electrical characteristics.
It is possible to reduce the period of sensing burst if VPM bit is set by '1'. When user makes CS tact switch input or LED drive or channel hold, the period of sensing burst is calculated without that CS channel. And the "Bit6" must be zero.

Bit name	Reset	Function
RB_SEL	10	Internal System Frequency Speed Control - 00,01 : Fast - 10 : Normal - 11 : Slow
CLK_OFF	0	Clock Off Mode Enable - 0 : Disable Clock Off Mode - 1 : Enable Clock Off Mode
SRST	0	Software Reset - 0 : Disable Software Reset - 1 : Enable Software Reset
IMP_SEL	1	Impedance Select - 0 : Low Impedance - 1 : High Impedance
S/M_SEL	0	Single/Multi Output Mode Select - 0 : Multi Mode - 1 : Single Mode
VPM	0	Variable Period Mode[20] - 0 : Disable - 1 : Enable

[20] Refer to Chapter 8.2.5 Ports Control Register

8.2.4 Calibration Speed Control Register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Dh	Cal_CTRL	BF_UP		BF_DOWN		BS_UP		BS_DOWN	

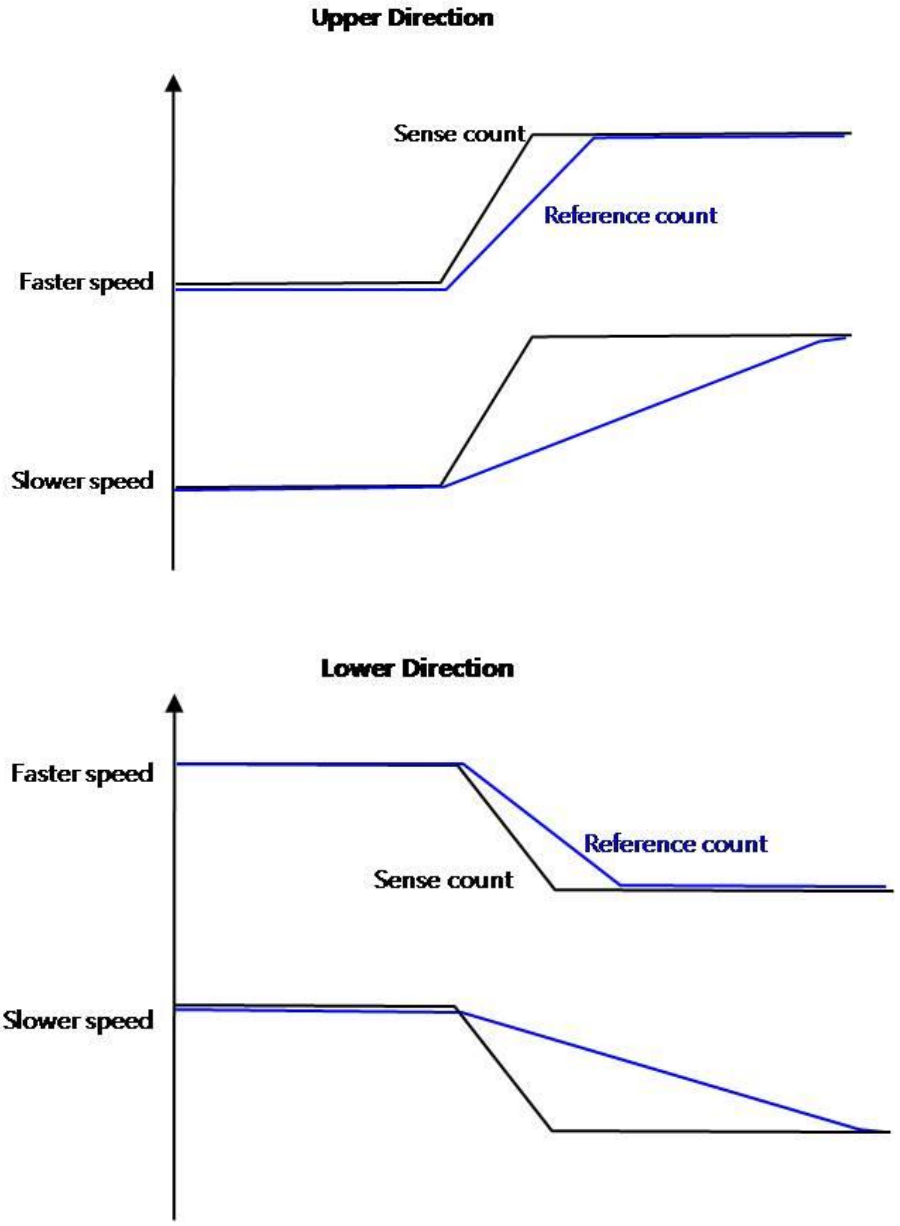
Description

There are the reference counter and the sense counter in TS20. The sense counter translates the total capacitance of CSX[21] port into the number. The reference counter is a point of reference for comparing with sense counter. The bigger total capacitance CSX port have, the smaller number the sense counter is to be. And the reference counter updated according to the changes of the capacitance of CSX port. If the sense counter has bigger number than the reference counter, the reference counter is calibrated with upper direction according to the calibration speed by itself. And the calibration speed might be controlled on each operation mode by the "Cal_CTRL" register. If the "BS_DOWN" is set "11", all calibration speed is followed this case and other register settings are ignored.

Bit name	Reset	Function
BS_DOWN	10	Calibration speed control lower direction in BS mode - 00 : Fastest - 01 : Fast - 10 : Normal - 11 : The reference count is to be previous sense count
BS_UP	10	Calibration speed control upper direction in BS mode - 00 : Fastest - 01 : Fast - 10 : Normal - 11 : Slow
BF_DOWN	11	Calibration speed control lower direction in BF mode - 00 : Fastest - 01 : Fast - 10 : Normal - 11 : Slow
BF_UP	11	Calibration speed control upper direction in BF mode - 00 : Fastest - 01 : Fast - 10 : Normal - 11 : Slow

[21] X = 1 to 20

Calibration Speed Figure



8.2.5 Ports Control Register

Type: R/W

Address	Register Name	Bit7 Bit6	Bit5 Bit4	Bit3 Bit2	Bit1 Bit0
0Eh	**Port_CTRL1**	CH4	CH3	CH2	CH1
0Fh	**Port_CTRL2**	Reserved	CH7	CH6	CH5
10h	**Port_CTRL3**	CH11	CH10	CH9	CH8
11h	**Port_CTRL4**	CH15	CH14	CH13	CH12
12h	**Port_CTRL5**	CH19	CH18	CH17	CH16
13h	**Port_CTRL6**	-			CH20

Description

CS1 ~ CS20 ports have a specific operation with the “Port_CTRL1~6” registers. The following table shows the detail information about specific operation.

Channel Hold operation is no working mode in specific channel.

And it is recommended to apply software reset when a port goes from other modes to sense.

The reserved bits, [Bit7:Bit6] of the register address 0Fh, and the value of the unused CS channels are strongly recommended that you set to "01".

Bit name	Reset	Function
CH1 ~ CH20	00	Port Operation - 00 : Sense - 01 : Channel Hold - 10 : LED driver - 11 : Tact switch input

8.2.6 Channel Calibration Control Register

Type: R/W

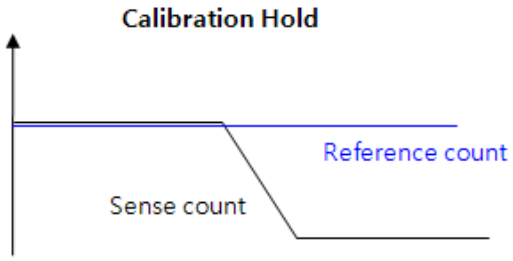
Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
14h	**Cal_Hold1**	CH7	CH6	CH5	CH4	CH3	CH2	CH1	DUMMY
15h	**Cal_Hold2**	CH14	CH13	CH12	CH11	CH10	CH9	CH8	Reserved
16h	**Cal_Hold3**	-	-	CH20	CH19	CH18	CH17	CH16	CH15

Description

The calibration of each channel is independently available to control. The reference counter is not updated even if the sense counter is changed such as below figure. Each channel is working even if a bit is set. The reserved bit, [Bit0] of the register address 15h, is don't care.

Bit name	Reset	Function
DUMMY, CH1 ~ CH20	0	Calibration Enable Control 0 : Enable reference calibration (sensing + calibration) 1 : Disable reference calibration (sensing + No calibration)

Calibration Hold Figure



8.2.7 Noise Environment Overcome Control Register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
17h	**Err_CTRL**	-	-	-	ERR_COUNT			ERR_PERCENT	

Description

The "Err_CTRL" register is set by I2C interface. And this bit can control the detective noise level and count. It is possible to prevent malfunction by rapid changes of environment.

Bit name	Reset	Function
ERR_PERCENT	01	Error detective level decision 00 : 0.3% 01 : 0.4% 10 : 0.5% 11 : 0.7%
ERR_COUNT	011	Error detective count decision. 000 : 0 001 : 1 010 : 2 011 : 3 100 : 4 101 : 5 110 : 6 111 : 7

8.2.8 Output Register

Type: R

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
20h	**Output1**	Reserved	CH7	CH6	CH5	CH4	CH3	CH2	CH1
21h	**Output2**	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
22h	**Output3**	-	-	ND	CH20	CH19	CH18	CH17	CH16

Description

The each channel output of TS20 is provided with 1 bit. It represents to detect result as below table.
The reserved bit, output of Bit7 of register address 20h, is don't care.

Bit name	Reset	Function
CH1 ~ CH20	Read only	Output of CH1 ~ CH20 0: No touch detected 1: Touch detected
ND	Read only	Noise Detect Indication 0: No noisy state 1: Noisy state

8.2.9 Write Reference Count Register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
23h	**Ref_wr_H**	-	-	REF_COUNT[13:8]					
24h	**Ref_wr_L**	REF_COUNT[7:0]							
25h	**Ref_wr_CH1**	CH6	CH5	CH4	CH3	CH2	CH1	DUMMY	-
26h	**Ref_wr_CH2**	CH13	CH12	CH11	CH10	CH9	CH8	Reserved	CH7
27h	**Ref_wr_CH3**	CTRL	CH20	CH19	CH18	CH17	CH16	CH15	CH14

Description

User can write the reference data directly with using these registers. If bits of the register "Ref_wr_CH1~3" are set by '1' and the CTRL bit is set by '1', the reference data of selected channel will be updated with the value of the "REF_COUNT" register. The reserved bit, [Bit1] of the register address 26h, is recommended to be set '0'.

Bit name	Reset	Function
REF_COUNT[13:8]	--000000	Reference Count high Byte[13 : 8]
REF_COUNT[7:0]	00000000	Reference Count low Byte[7 : 0]
DUMMY, CHX[22]	0	Channel selection to write the reference data directly - 0 : No selected - 1 : Selected
CTRL	0	The Command bit to write reference data - 1 : Write the reference data (If this bit is set by '1', user can not change the value of the "REF_COUNT" and "Ref_wr_CH1~3" registers.) - 0 : wait until next command

[22] X = 1 to 20

8.2.10 Sensitivity Reading Channel Select Register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
29h	Sen_RD_CTRL	-	-	-	SEN_RD_CHANNEL				

Description

It is possible to read the sensitivity of selected channel directly by I2C interface. And it is possible to select channel that user want to read the sensitivity by controlling the "SEN_RD_CHANNEL" register. The detail information is in following table.

Bit name	Reset	Function
SEN_RD_CHANNEL	00000	The setting value of each channels 00001 : Channel 1 00010 : Channel 2 00011 : Channel 3 00100 : Channel 4 00101 : Channel 5 00110 : Channel 6 00111 : Channel 7 01000 : - 01001 : Channel 8 01010 : Channel 9 . . . . . 10100 : Channel 19 10101 : Channel 20

8.2.11 Sensitivity Read Register

Type: R

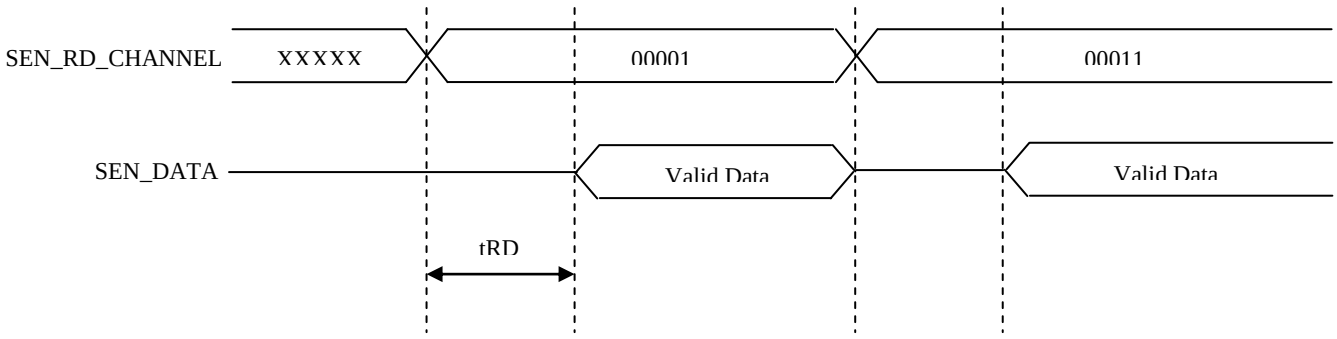
Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
29h	Sensitivity_RD	SEN_DATA							

Description

It is possible to read the sensitivity of selected channel directly by I2C interface.

Bit name	Reset	Function
SEN_DATA	Read only	The sensitivity data of selected channel Sensitivity(%) = SEN_DATA[7:0] / 2048

Sensitivity Read Operation Timing Diagram



Symbol	Parameter	Min.	Typ.	Max.	Unit
tRD	Valid Data Setup Time[23]	25(BF)/ 130(BS)	-	-	ms

[23] Condition : 3.0V, Normal bias(Refer to the “RB_SEL” register of Chapter 8.2.3)

8.2.12 Sense, Reference Count Read Register

Type: R

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
30H	**Rd_CH1**	CH6	CH5	CH4	CH3	CH2	CH1	DUMMY	CTRL
31H	**Rd_CH2**	CH13	CH12	CH11	CH10	CH9	CH8	Reserved	CH7
32H	**Rd_CH3**	-	CH20	CH19	CH18	CH17	CH16	CH15	CH14
33H	**Sen_H**	-	-	SENSE_COUNT[13:8]					
34H	**Sen_L**	SENSE_COUNT[7:0]							
35H	**Ref_H**	-	-	REFERENCE_COUNT[13:8]					
36H	**Ref_L**	REFERENCE_COUNT[7:0]							
37H	**Rd_CH4**	CH6	CH5	CH4	CH3	CH2	CH1	DUMMY	-
38H	**Rd_CH5**	CH13	CH12	CH11	CH10	CH9	CH8	Reserved	CH7
39H	**Rd_CH6**	-	CH20	CH19	CH18	CH17	CH16	CH15	CH14

Description

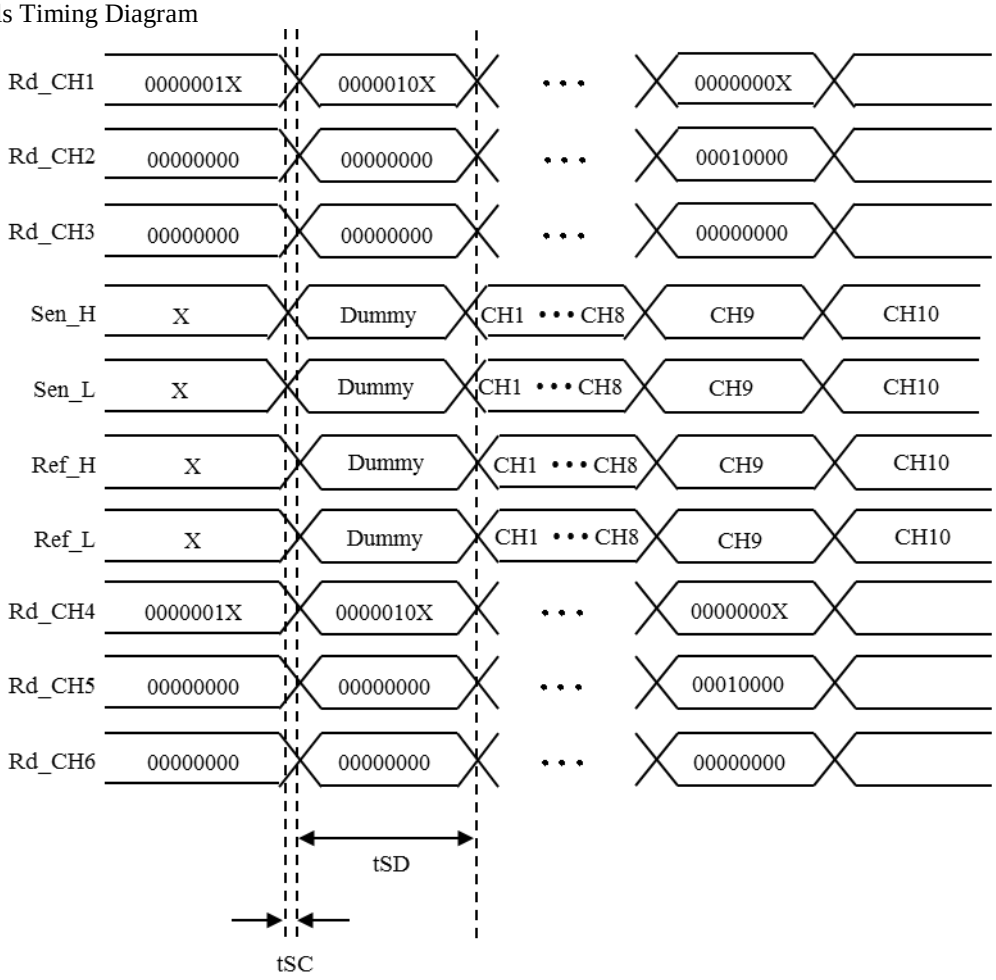
TS20 provides the special function to read sense count and reference count of each channels.
The reserved bits, [Bit1] of the register address 31h and 38h, is don't care.

Bit name	Reset	Function
CTRL	0	INT port control bit. This bit is not allowed to change by a user. 0 : Interrupt output 1 : Sensing duty output
DUMMY	Read only	If the two "DUMMY" bits of the address 30H and 37H are '1', it is indicates that the data of the address 33H ~ 36H is the sense/reference count of Dummy channel. And when one of "Dummy" bits isn't '1', the data of the address 33H~36H is invalid data for Dummy channel.
CHX[24]	Read only	If the two "CHX" bits of the address 30H and 37H are '1', it is indicates that the data of the address 33H ~ 36H is the sense/reference count of Xth channel. And when one of "CHX" bits isn't '1', the data of the address 33H~36H is invalid data for Xth channel.
SENSE_COUNT[13:0]	Read only	Sense count
REFERENCE_COUNT[13:0]	Read only	Reference count

[24] X = 1 to 20.

Sense/Reference Count Read Method

Internal Signals Timing Diagram



Symbol	Parameter	Min.	Typ.	Max.	Unit
tSC	Count Setup Time	4		10	us
tSD	One Channel Sensing Duty Time[25]	450		850	us

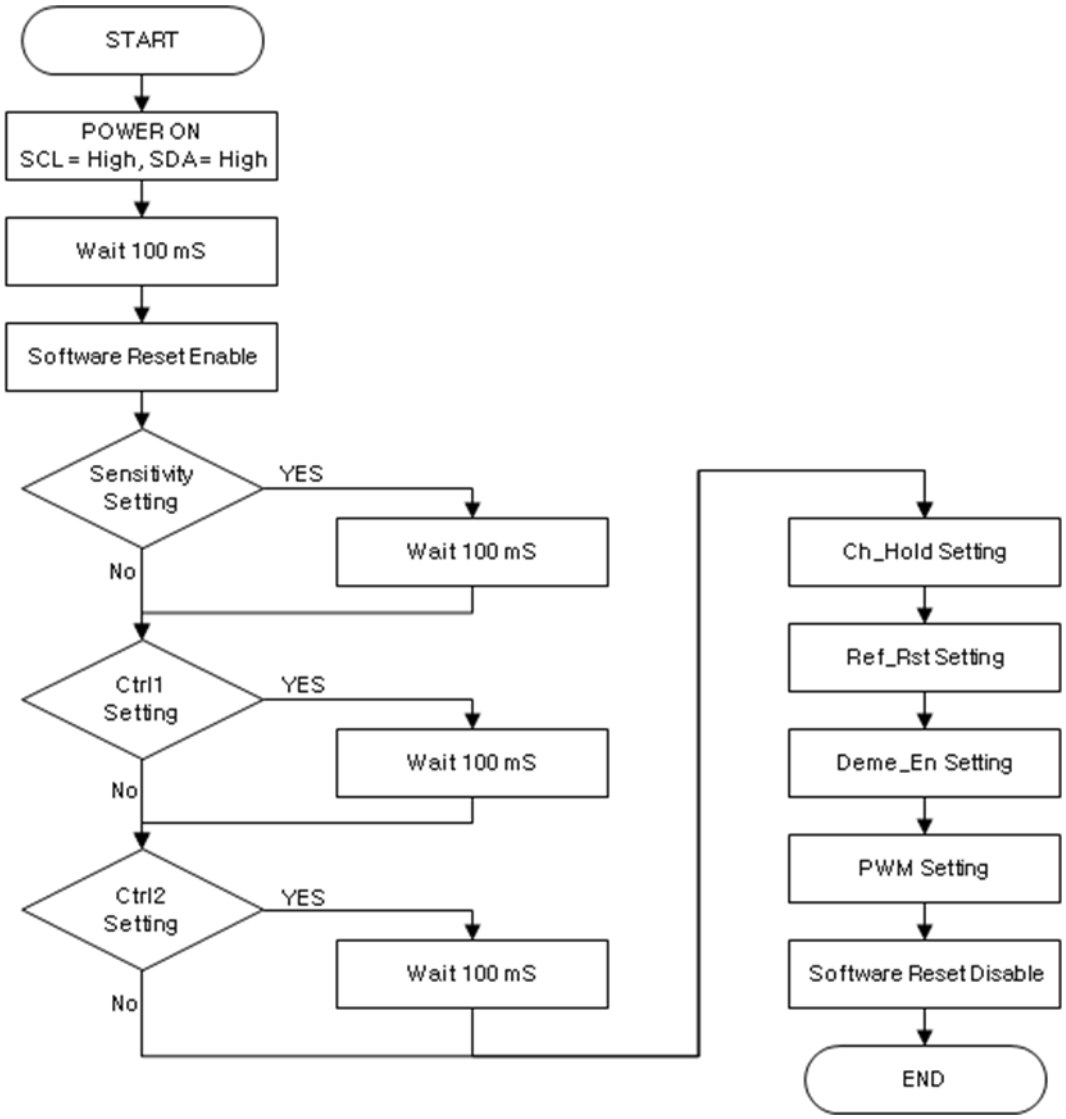
Sense/Reference Count Read Sequence

1. Read the data of the address 30H ~ 37H.
2. Compare the data of “Rd_CH1” register and the data of “Rd_CH4” register.
3. If the data of “Rd_CH1” register is not zero and equal to the data of “Rd_CH4” register, the data of “Sen_H”, “Sen_L”, “Ref_H” and “Ref_L” registers is valid for the channel that is set by “Rd_CH1” and “Rd_CH4” registers.
4. If the condition isn’t satisfied with number 3, compare “Rd_CH2” and “Rd_CH5”. And then compare “Rd_CH3” and “Rd_CH6”.

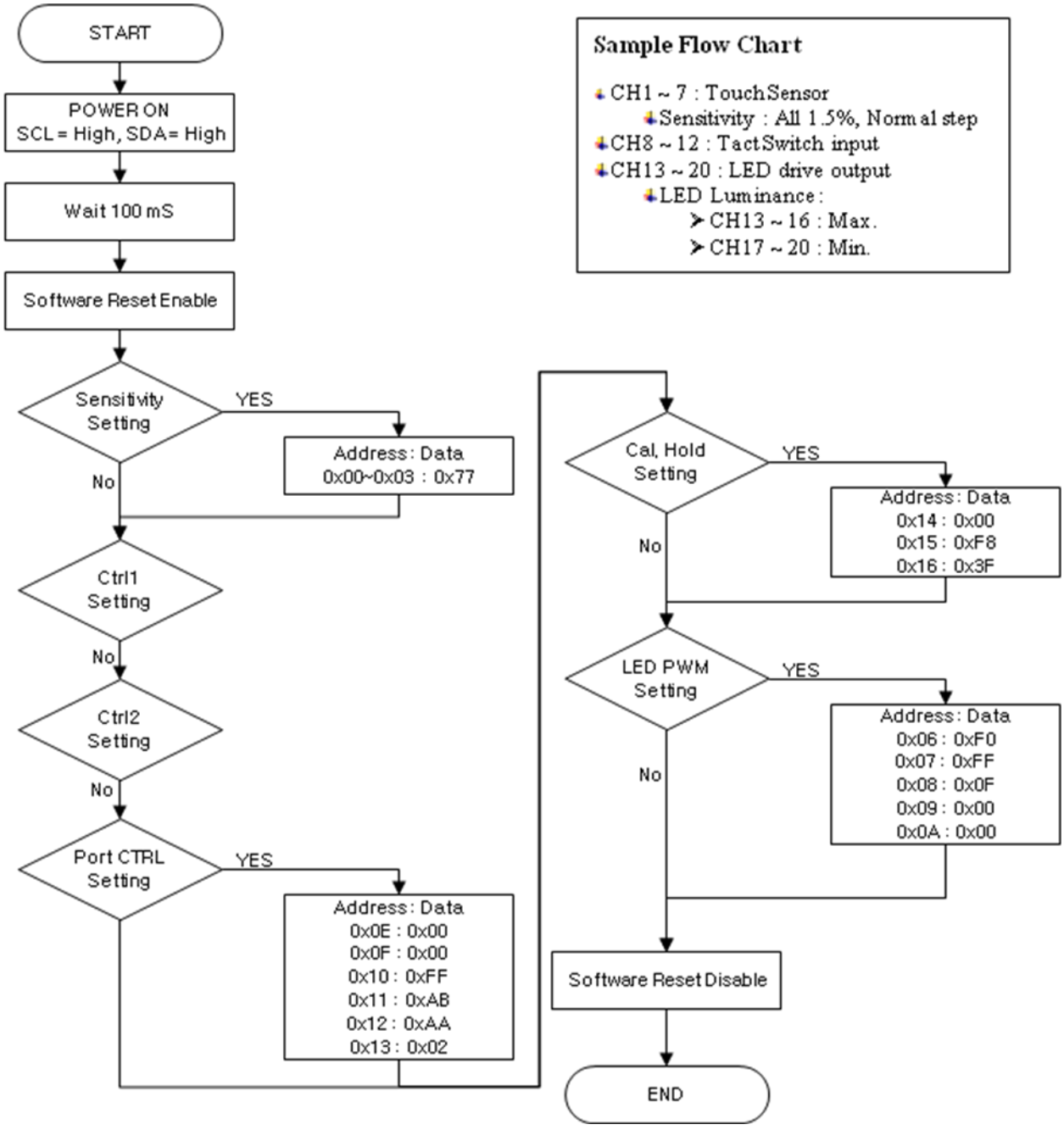
[25] Condition : 3.0V, Normal bias(Refer to the “RB_SEL” register of Chapter 8.2.3)

9 Recommended TS20 Power Up Sequence (Example)

9.1 Recommended TS20 Power Up Flow Chart

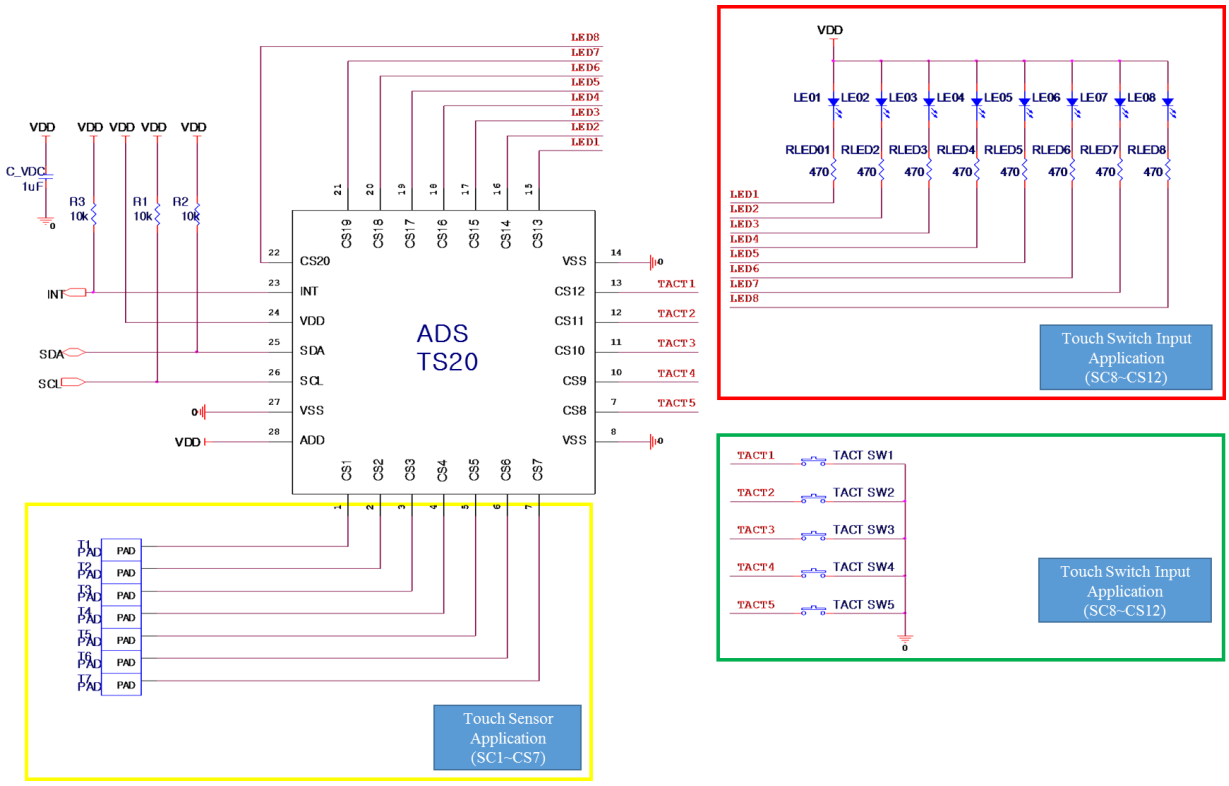


9.2 Recommended TS20 Power Up Sequence Sample



10 Recommended Circuit Diagram

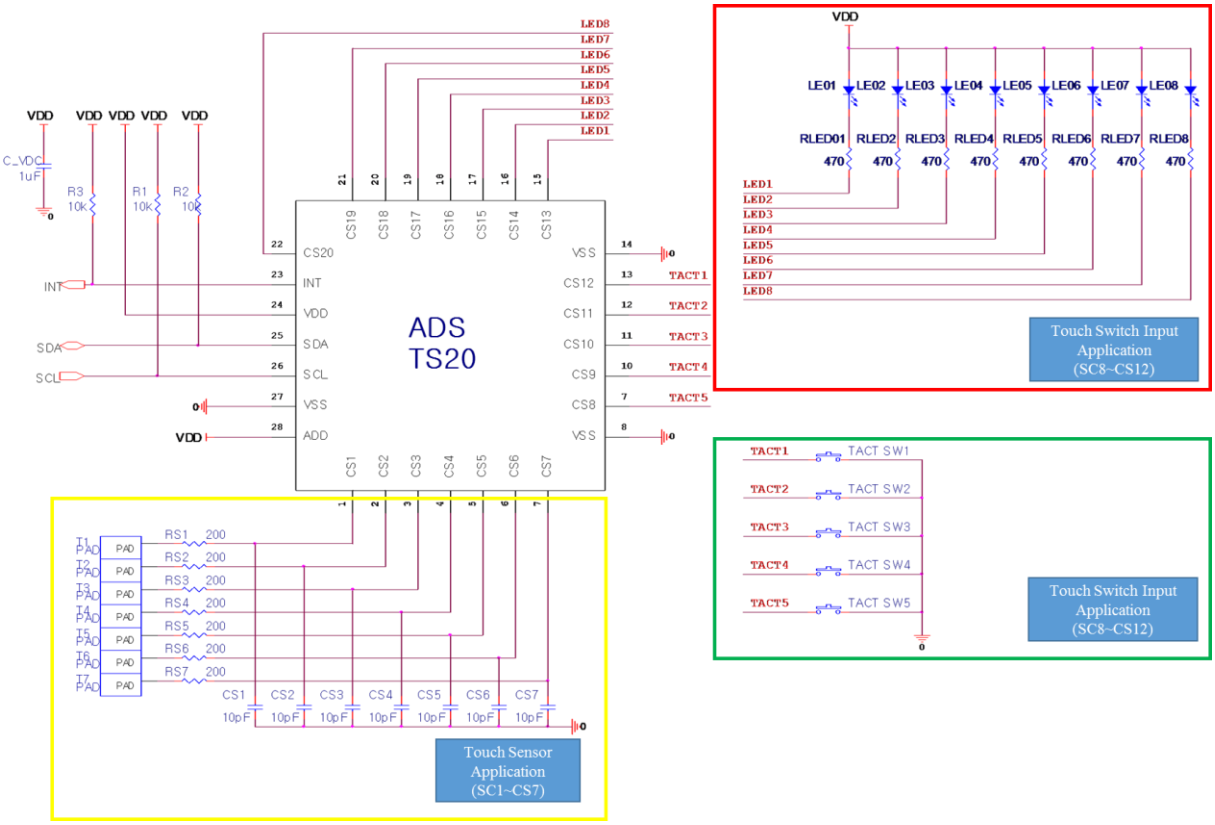
10.1 Application Example in clean power environment



TS20 Application Example Circuit (Clean power environment)

- The CS patterns also should be routed as short as possible and the width of line might be about 0.25mm (or narrower line).
- The capacitor that is between VDD and GND is an obligation. It should be located as close as possible from TS20.
- The CS pattern routing should be formed by bottom metal (opposite metal of touch PAD).
- The empty space of PCB must be filled with GND pattern to strengthen GND pattern and to prevent external noise from interfere with sensing frequency.
- The TS20 is reset when power rise from 0V to proper VDD
- The LED_GND and GND should be short in the system and the lines are recommended to be split from the most low impedance ground point to avoid ground bouncing problems.

10.2 Application Example in noisy environment

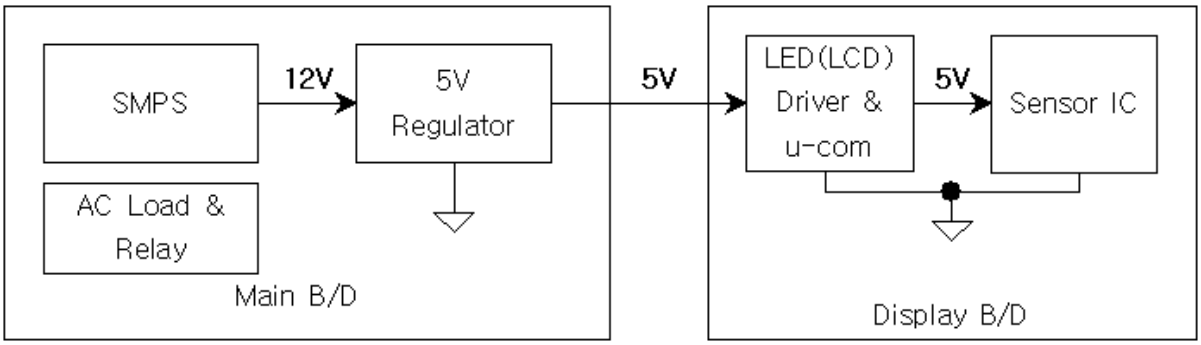


TS20 Application Example Circuit (Noisy environment)

- The VDD periodic voltage ripple over 50mV and the ripple frequency is lower than 10 kHz can cause wrong sensitivity calibration. To prevent above problem, power (VDD, GND) line of touch circuit should be separated from other circuit. Especially LED driver power line or digital switching circuit power line certainly should be treated to be separated from touch circuit.
- Thanks to the RS1 ~ RS20, CS1 ~ CS20 and CS20, the noise immunity could be improved.
- The LED_GND and GND should be short in the system and the lines are recommended to be split from the most low impedance ground point to avoid ground bouncing problems.

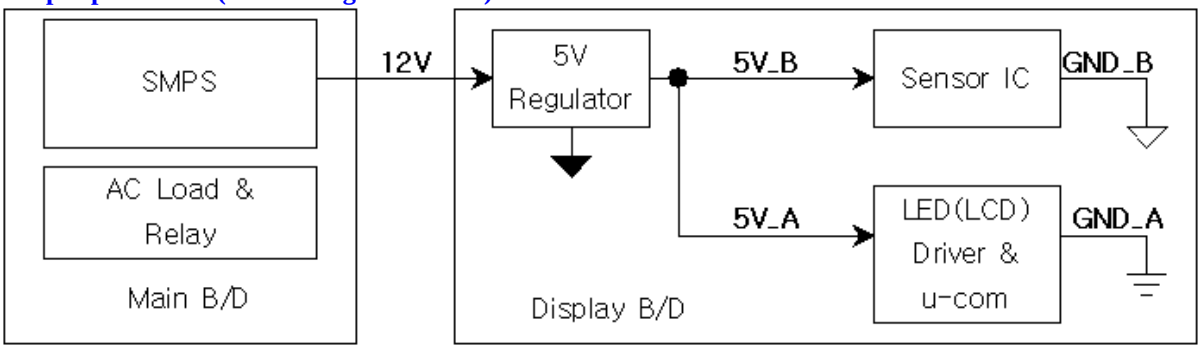
10.3 Example – Power Line Split Strategy PCB Layout

A. Not split power line (Bad power line design)

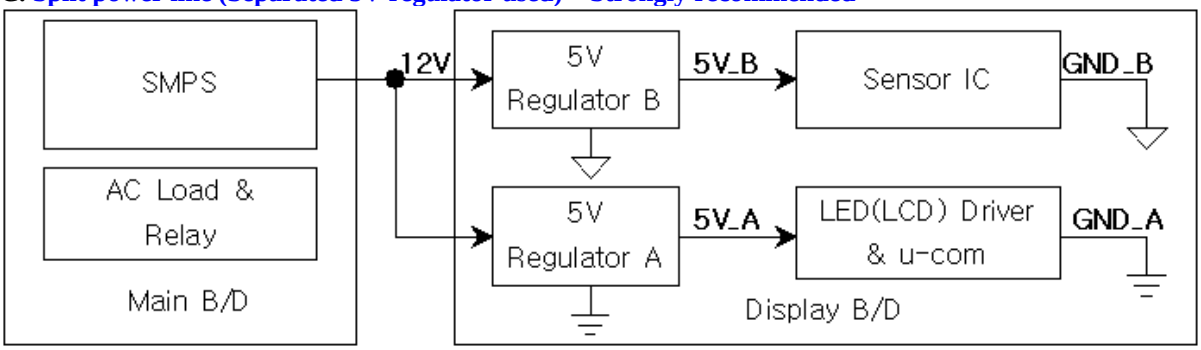


- The noise that is generated by AC load or relay can be loaded at 5V power line.
- A big inductance might be appeared in case of the connection line between main board and display board is too long, moreover the voltage ripple could be generated by LED (LCD) display driver at VDD (5V).

B. Split power line (One 5V regulator used) – Recommended

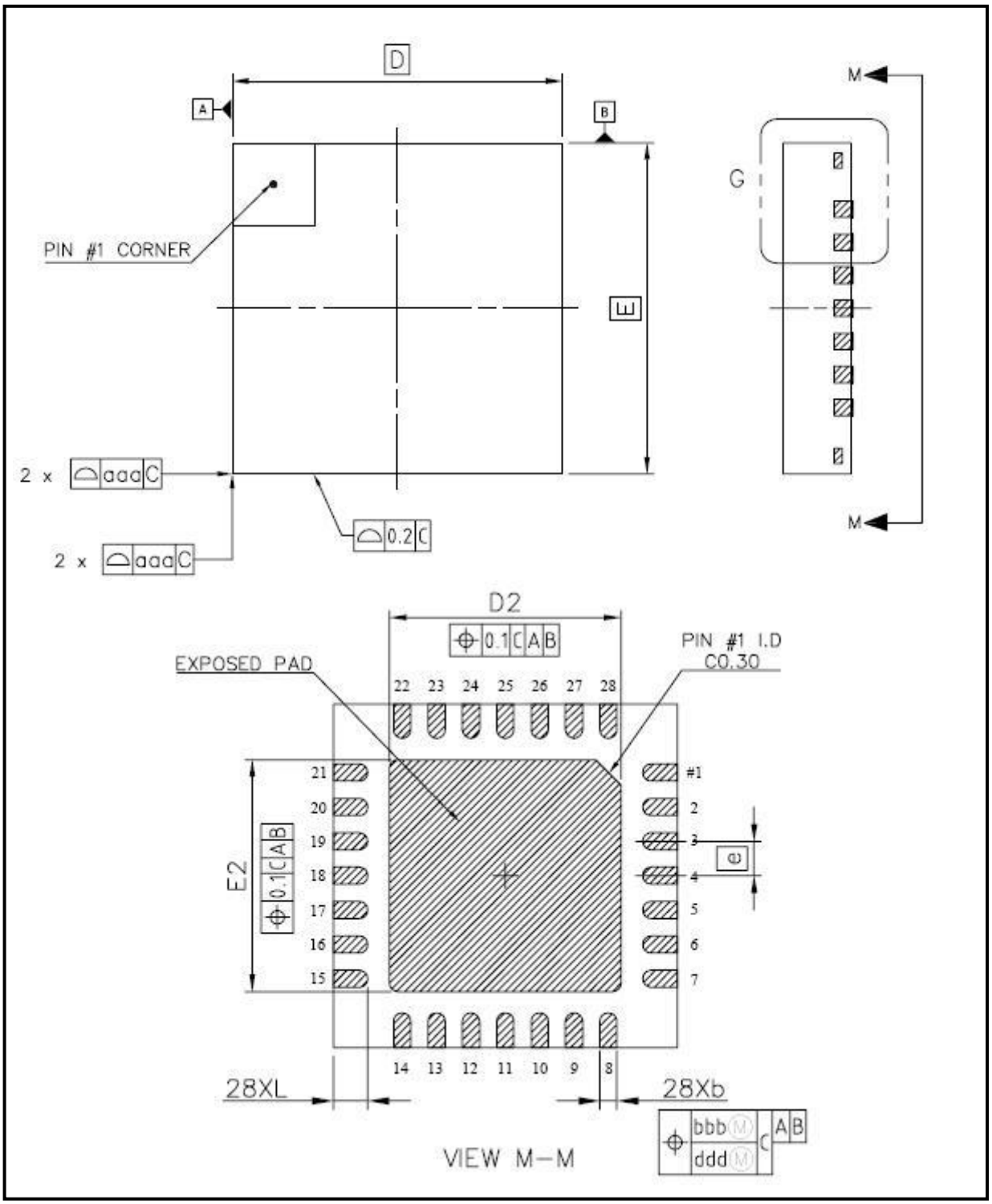


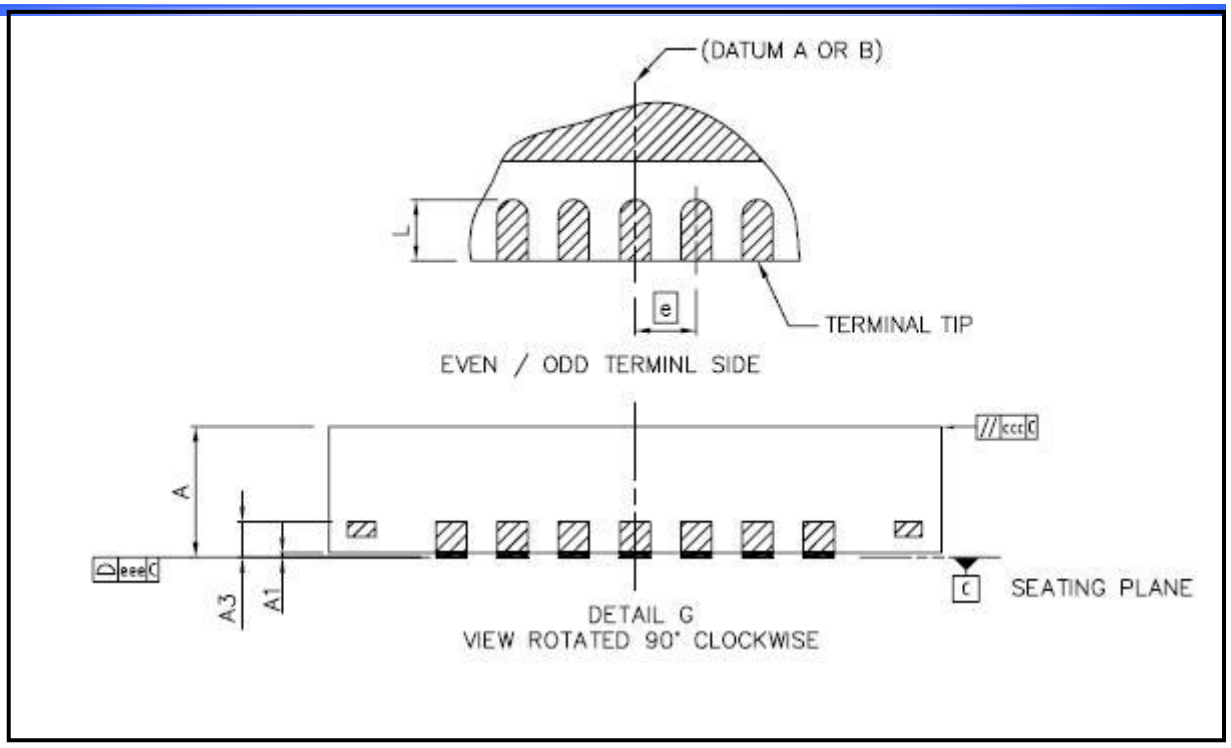
C. Split power line (Separated 5V regulator used) – Strongly recommended



11 MECHANICAL DRAWING

11.1 Mechanical Drawing of TS20-Q (28 QFN)

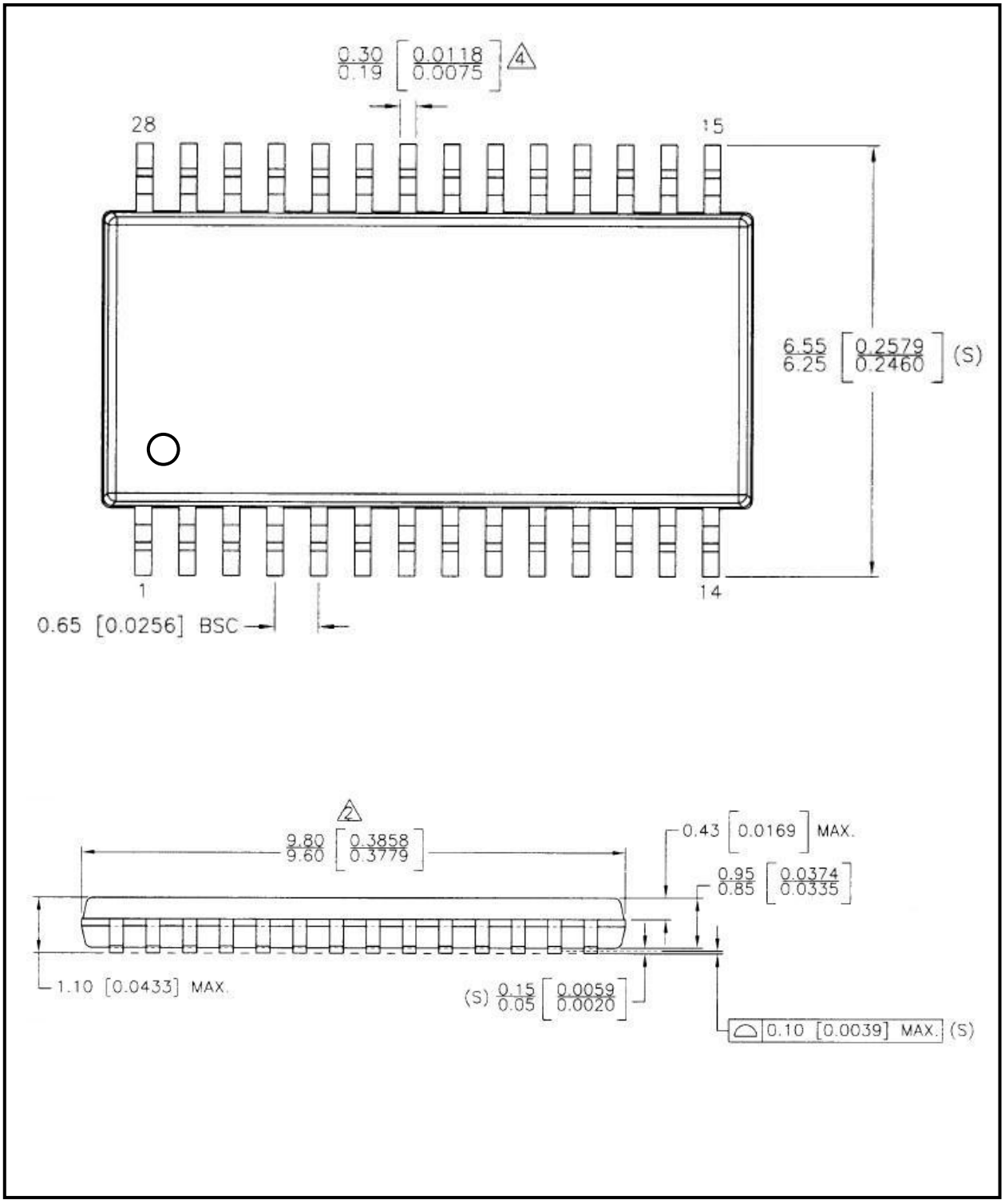


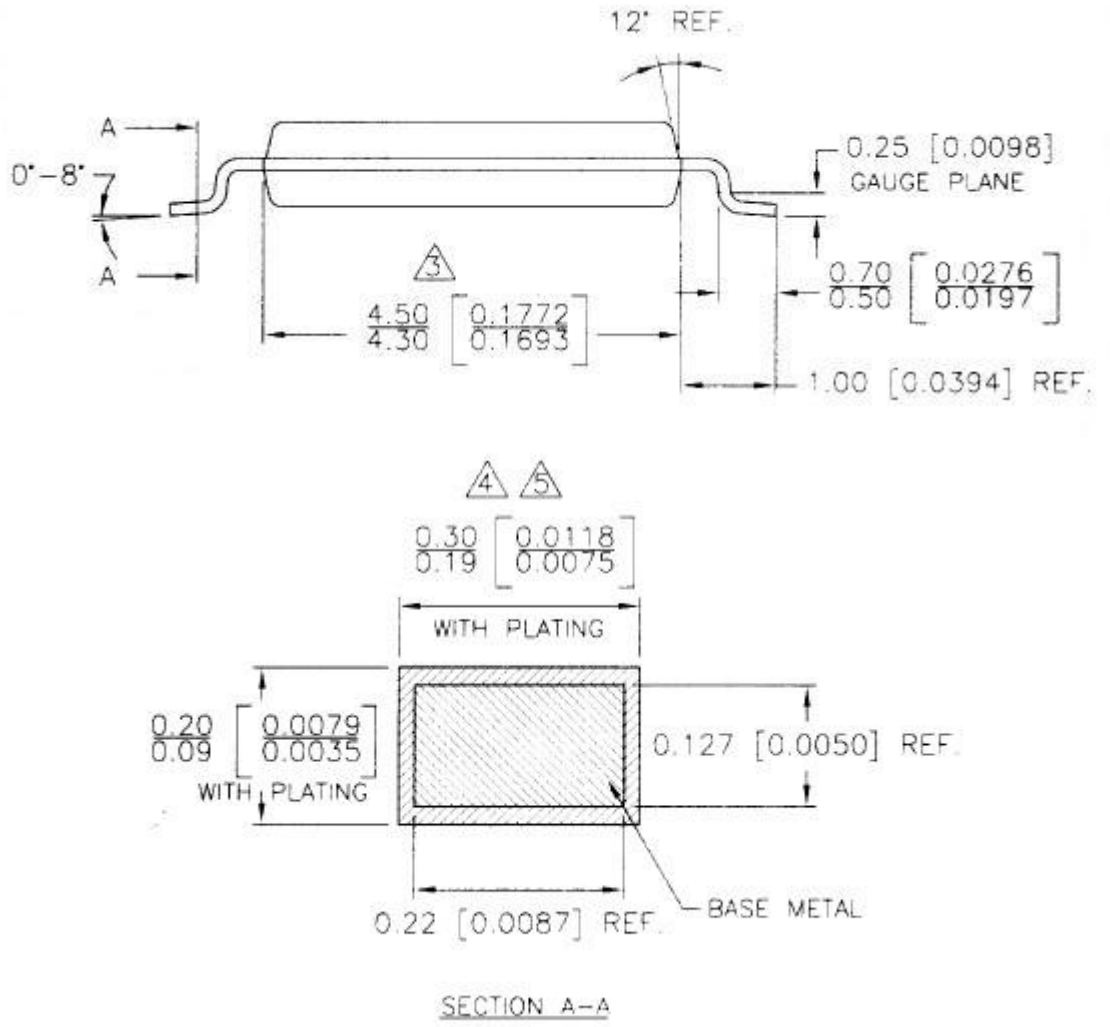


DIM	MIN	NOM	MAX	NOTES
A	0.80	0.85	0.90	1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994
A1	0.00		0.05	
A3		0.203 REF		
b	0.15	0.20	0.25	2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
D		4.00 BSC		
E		4.00 BSC		
e		0.40 BSC		3.0 DIMESION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE.
D2	2.60	2.70	2.80	
E2	2.60	2.70	2.80	
L	0.35	0.40	0.45	
aaa		0.10		4.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.
bbb		0.10		
ccc		0.10		
ddd		0.05		5.0 RADUS ON TERMINAL IS OPTIONAL.
eee		0.08		

Two channel touch key board can be designed by using only one TS02NR. The TS02NR is embedded intelligent internal power reset circuit that makes possible to save circuit cost because of reducing external components for reset.
The sensitivity calibration operation can help to prevent abnormal detection caused by external noise, temperature variation, and supply voltage drop.

11.2 Mechanical Drawing of TS20 (28 TSSOP)





SECTION A–A

NOTE :

1. CONTROLLING DIMENSIONS IN mm. [Inches.]
2. DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm. PER SIDE.
3. DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm.PER SIDE.
4. DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM.
5. CROSS SECTION A–A TO BE DETERMINED AT 0.10 TO 0.25 MM. FROM LEAD TIP.
6. LEAD SPAN / STAND OFF HEIGHT / COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTERSITIC.(S)
7. THIS PART COMPLIANT WITH JEDEC SPECFICATION MO–153 VARIATION AE.

12 MARKING DESCRIPTION

12.1 Marking Description of TS20-Q (28 QFN)

Company Code : **ADS**

→ AD Semiconductor

Device Code : **TS 20**

→ Channel Number
→ Touch Switch Group

Customer / Assembly Lot Code : **CC TTT**

→ Assembly Lot Code
→ Customer Code

Year / Week Code : **YY WW**

→ Manufacturing Week
→ Manufacturing Year

12.2 Marking Description of TS20 (28 TSSOP)

Company Code : **ADS**

→ AD Semiconductor

Device Code : **TS 20**

→ Channel Number
→ Touch Switch Group

Year / Week Code : **YY WW**

→ Manufacturing Week
→ Manufacturing Year

NOTES:

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