ADVANCED LINEAR DEVICES, INC.

DUAL N-CHANNEL AND DUAL P-CHANNEL MATCHED MOSFET PAIR

GENERAL DESCRIPTION

The ALD1103 is a monolithic dual N-channel and dual P-channel matched transistor pair intended for a broad range of analog applications. These enhancement-mode transistors are manufactured with Advanced Linear Devices' enhanced ACMOS silicon gate CMOS process. It consists of an ALD1101 N-channel MOSFET pair and an ALD1102 P-channel MOSFET pair in one package.

The ALD1103 offers high input impedance and negative current temperature coefficient. The transistor pair is matched for minimum offset voltage and differential thermal response, and it is designed for precision signal switching and amplifying applications in +2V to +10V systems where low input bias current, low input capacitance and fast switching speed are desired. Since these are MOSFET devices, they feature very large (almost infinite) current gain in a low frequency, or near DC, operating environment. When used in pairs, a dual CMOS analog switch can be constructed. In addition, the ALD1103 is intended as a building block for differential amplifier input stages, transmission gates, and multiplexer applications.

The ALD1103 is suitable for use in precision applications which require very high current gain, beta, such as current mirrors and current sources. The high input impedance and the high DC current gain of the Field Effect Transistors result in extremely low current loss through the control gate. The DC current gain is limited by the gate input leakage current, which is specified at 50pA at room temperature. For example, DC beta of the device at a drain current of 5mA at 25°C is = 5mA/50pA = 100,000,000.

FEATURES

- Thermal tracking between N-channel and P-channel pairs
- Low threshold voltage of 0.7V for both N-channel & P-channel MOSFETS
- Low input capacitance
- Low Vos -- 10mV
- High input impedance -- $10^{13}\Omega$ typical
- Low input and output leakage currents
- Negative current (I_{DS}) temperature coefficient
- Enhancement mode (normally off)
- DC current gain 10^9
- Matched N-channel and matched P-channel in one package
- RoHS compliant

### ORDERING INFORMATION ("L" suffix denotes lead-free (RoHS))

Operating Temperature Range*	
0°C to +70°C	0°C to +70°C
14-Pin SOIC Package	14-Pin Plastic Dip Package
ALD1103SBL	ALD1103PBL

* Contact factory for high temperature versions.

APPLICATIONS

- Precision current mirrors
- Complementary push-pull linear drives
- Analog switches
- Choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Analog inverter
- Precision matched current sources

PIN CONFIGURATION

DN1	1	14	DN2
GN1	2	13	GN2
SN1	3	12	SN2
V-	4	11	V+
DP1	5	10	DP2
GP1	6	9	GP2
SP1	7	8	SP2

TOP VIEW
SBL, PBL PACKAGES

BLOCK DIAGRAM

N GATE 1 (2)
N DRAIN 1 (1) — N SOURCE 1 (3)
SUBSTRATE (4)
N DRAIN 2 (14) — N SOURCE 2 (12)
N GATE 2 (13)

P GATE 1 (6)
P DRAIN 1 (5) — P SOURCE 1 (7)
SUBSTRATE (11)
P DRAIN 2 (10) — P SOURCE 2 (8)
P GATE 2 (9)
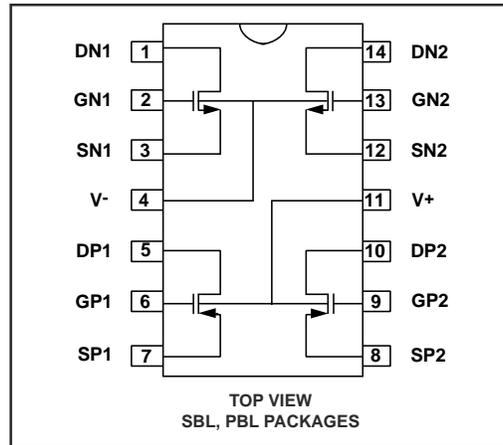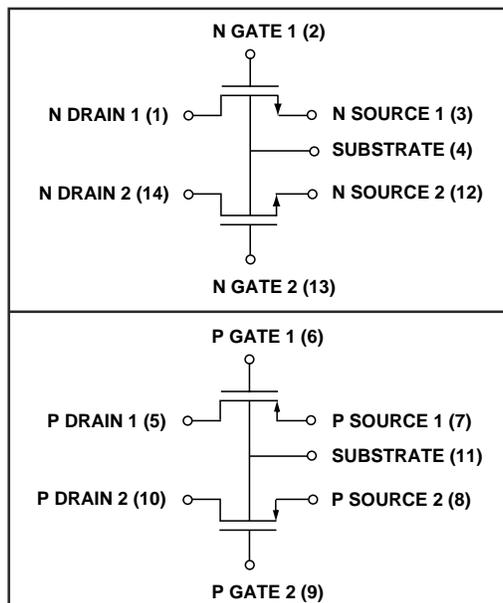
ABSOLUTE MAXIMUM RATINGS

Drain-source voltage, V_{DS} ———————————————————————— 10V
Gate-source voltage, V_{GS} ———————————————————————— 10V
Power dissipation ———————————————————————————— 500mW
Operating temperature range   SBL, PBL packages ———————————— 0°C to +70°C
Storage temperature range ——————————————————————— -65°C to +150°C
Lead temperature, 10 seconds ——————————————————————— +260°C

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

OPERATING ELECTRICAL CHARACTERISTICS
## T_A = 25°C unless otherwise specified

Parameter	Symbol	N - Channel			Unit	Test Conditions	P - Channel			Unit	Test Conditions
		Min	Typ	Max			Min	Typ	Max		
Gate Threshold Voltage	V_T	0.4	0.7	1.0	V	I_{DS} = 10µA V_{GS} = V_{DS}	-0.4	-0.7	-1.2	V	I_{DS} = -10µA V_{GS} = V_{DS}
Offset Voltage V_{GS1} - V_{GS2}	V_{OS}			10	mV	I_{DS} = 100µA V_{GS} = V_{DS}			10	mV	I_{DS} = -100µA V_{GS} = V_{DS}
Gate Threshold Temperature Drift	TC_{VT}		-1.2		mV/°C			-1.3		mV/°C	
On Drain Current	$I_{DS(ON)}$	25	40		mA	V_{GS} = V_{DS} = 5V	-8	-16		mA	V_{GS} = V_{DS} = -5V
Trans-. conductance	G_{fs}	5	10		mmho	V_{DS} = 5V I_{DS} = 10mA	2	4		mmho	V_{DS} = -5V I_{DS} = -10mA
Mismatch	ΔG_{fs}		0.5		%			0.5		%	
Output Conductance	G_{OS}		200		µmho	V_{DS} = 5V I_{DS} = 10mA		500		µmho	V_{DS} = -5V I_{DS} = -10mA
Drain Source ON Resistance	$R_{DS(ON)}$		50	75	Ω	V_{DS} = 0.1V V_{GS} = 5V		180	270	Ω	V_{DS} = -0.1V V_{GS} = -5V
Drain Source ON Resistance Mismatch	$\Delta R_{DS(ON)}$		0.5		%	V_{DS} = 0.1V V_{GS} = 5V		0.5		%	V_{DS} = -0.1V V_{GS} = -5V
Drain Source Breakdown Voltage	BV_{DSS}	10			V	I_{DS} = 10µA V_{GS} = 0V	-10			V	I_{DS} = -10µA V_{GS} = 0V
Off Drain Current	$I_{DS(OFF)}$		0.1	4 4	nA µA	V_{DS} = 10V I_{GS} = 0V T_A = 125°C		0.1	4 4	nA µA	V_{DS} = -10V V_{GS} = 0V T_A = 125°C
Gate Leakage Current	I_{GSS}		1	100 10	pA nA	V_{DS} = 0V V_{GS} = 10V T_A = 125°C		1	100 10	pA nA	V_{DS} = 0V V_{GS} = -10V T_A = 125°C
Input Capacitance	C_{ISS}		6	10	pF			6	10	pF	

TYPICAL N-CHANNEL PERFORMANCE CHARACTERISTICS
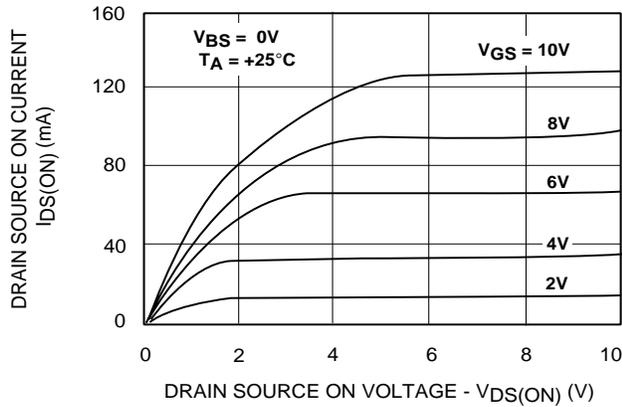
OUTPUT CHARACTERISTICS

DRAIN SOURCE ON CURRENT I_DS(ON) (mA)

$V_{BS} = 0V$
$T_A = +25°C$

$V_{GS} = 10V$
8V
6V
4V
2V

DRAIN SOURCE ON VOLTAGE - $V_{DS(ON)}$ (V)

LOW VOLTAGE OUTPUT CHARACTERISTICS

DRAIN SOURCE ON CURRENT I_DS(ON) (mA)

$V_{BS} = 0V$
$T_A = 25°C$

$V_{GS} = 10V$
8V
6V
4V
2V

DRAIN SOURCE ON VOLTAGE - $V_{DS(ON)}$ (mV)

FORWARD TRANSCONDUCTANCE vs. DRAIN-SOURCE VOLTAGE

FORWARD TRANSCONDUCTANCE (µmho)

$V_{BS} = 0V$
$f = 1KHz$

$I_{DS} = 10mA$

$T_A = +125°C$
$T_A = +25°C$

$I_{DS} = 1mA$
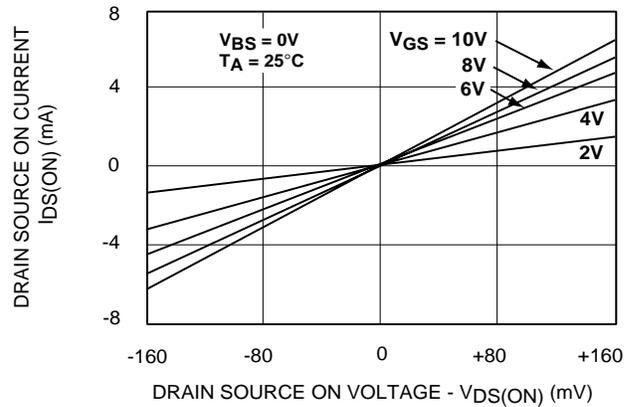
DRAIN SOURCE ON VOLTAGE - $V_{DS(ON)}$ (V)
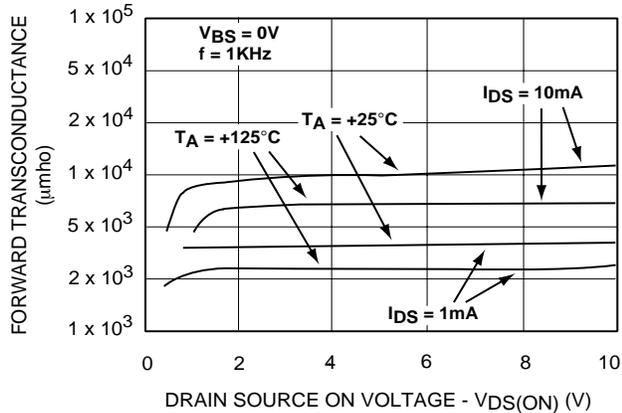
TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS

DRAIN SOURCE ON CURRENT I_DS(ON) (µA)

$V_{BS} = 0V$
-2V
-4V
-6V
-8V
-10V

$V_{GS} = V_{DS}$
$T_A = +25°C$

GATE SOURCE ON VOLTAGE - $V_{GS(ON)}$ (V)
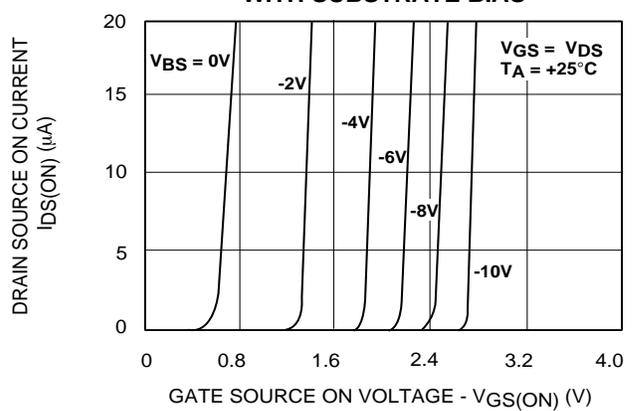
DRAIN SOURCE ON RESISTANCE vs. GATE-SOURCE VOLTAGE

DRAIN SOURCE ON RESISTANCE R_DS(ON) (Ω)

$V_{DS} = 0.2V$
$V_{BS} = 0V$

$T_A = +125°C$

$T_A = +25°C$

GATE SOURCE ON VOLTAGE - $V_{GS(ON)}$ (V)

DRAIN SOURCE OFF CURRENT vs. AMBIENT TEMPERATURE

DRAIN SOURCE OFF CURRENT R_DS(OFF) (A)

$V_{DS} = 10V$
$V_{GS} = V_{BS} = 0V$
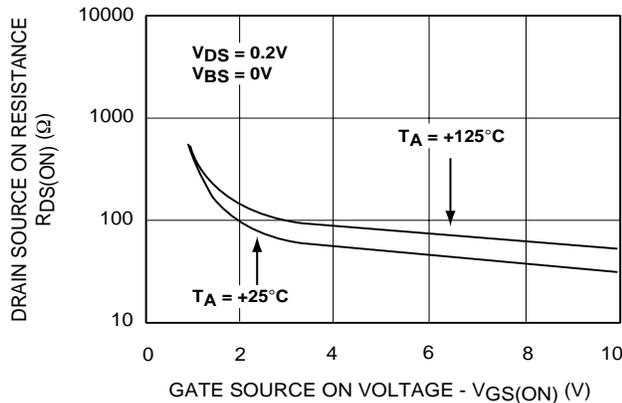
AMBIENT TEMPERATURE - T_A (°C)
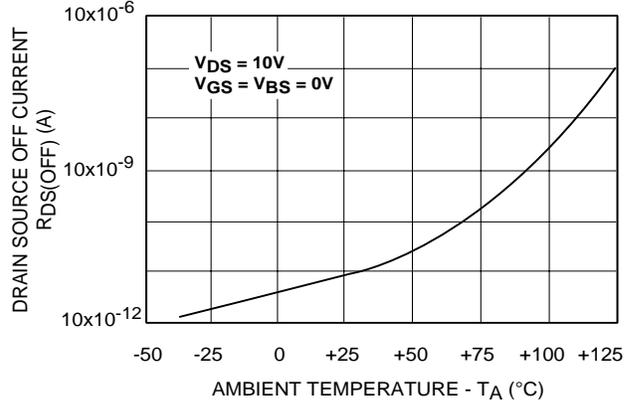
TYPICAL P-CHANNEL PERFORMANCE CHARACTERISTICS

OUTPUT CHARACTERISTICS

V_{BS} = 0V
T_A = +25°C

V_{GS} = -10V
-8V
-6V
-4V
-2V

DRAIN SOURCE ON CURRENT $I_{DS(ON)}$ (mA)

DRAIN SOURCE ON VOLTAGE - $V_{DS(ON)}$ (V)

LOW VOLTAGE OUTPUT CHARACTERISTICS

V_{BS} = 0V
T_A = 25°C

V_{GS} = -10V
-8V
-6V
-4V
-2V

DRAIN-SOURCE CURRENT $I_{DS(ON)}$ (mA)

DRAIN SOURCE ON VOLTAGE - $V_{DS(ON)}$ (mV)

FORWARD TRANSCONDUCTANCE vs. DRAIN-SOURCE VOLTAGE

T_A = +25°C

I_{DS} = -5mA

T_A = +125°C

I_{DS} = -1mA

V_{BS} = 0V
f = 1KHz

FORWARD TRANSCONDUCTANCE (µmho)

DRAIN SOURCE ON VOLTAGE - $V_{DS(ON)}$ (V)

TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS

V_{BS} = 0V
2V
4V
6V
8V
10V

V_{GS} = V_{DS}
T_A = +25°C

DRAIN SOURCE ON CURRENT $I_{DS(ON)}$ (µA)

GATE SOURCE ON VOLTAGE - $V_{GS(ON)}$ (V)

DRAIN SOURCE ON RESISTANCE vs. GATE-SOURCE VOLTAGE

V_{DS} = 0.4V
V_{BS} = 0V

T_A = +125°C

T_A = +25°C

DRAIN SOURCE ON RESISTANCE $R_{DS(ON)}$ (Ω)

GATE SOURCE ON VOLTAGE - $V_{GS(ON)}$ (V)

DRAIN SOURCE OFF CURRENT vs. AMBIENT TEMPERATURE

V_{DS} = -10V
V_{GS} = V_{BS} = 0V

DRAIN SOURCE OFF CURRENT $R_{DS(OFF)}$ (A)

AMBIENT TEMPERATURE - T_A (°C)

TYPICAL APPLICATIONS

CURRENT SOURCE MIRROR

$$I_{SOURCE} = I_{SET}$$
$$= \frac{V^+ - V_t}{R_{SET}}$$
$$\cong \frac{4}{R_{SET}}$$
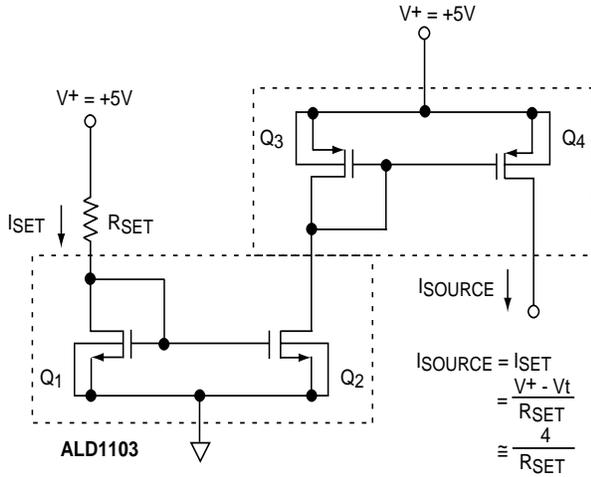
Q_1, Q_2: N-Channel MOSFET
Q_3, Q_4: P-Channel MOSFET

CURRENT SOURCE WITH GATE CONTROL
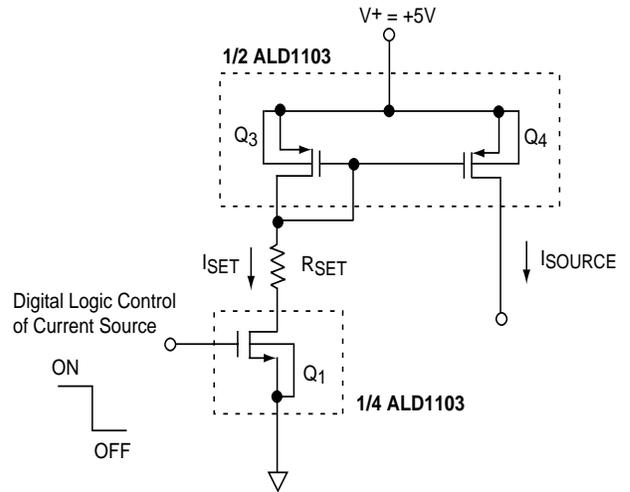
Q_1 : N-Channel MOSFET
Q_3, Q_4: P-Channel MOSFET

DIFFERENTIAL AMPLIFIER
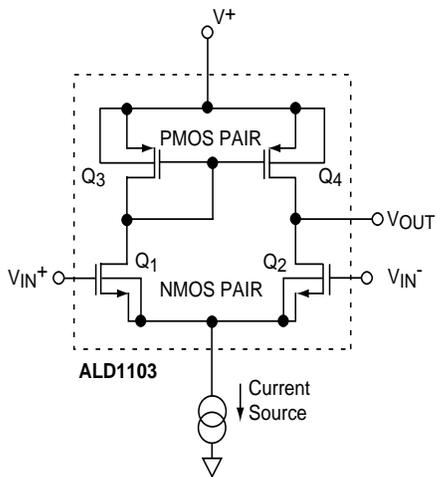
Q_1, Q_2: N-Channel MOSFET
Q_3, Q_4: P-Channel MOSFET

CURRENT SOURCE MULTIPLICATION

$$I_{SOURCE} = I_{SET} \times N$$
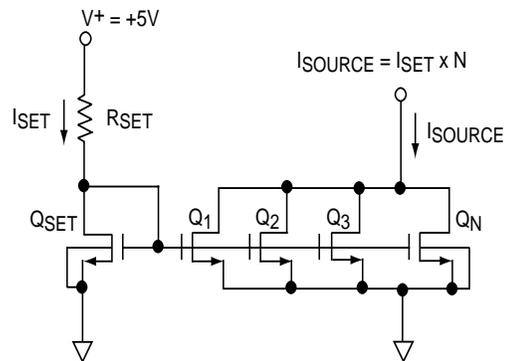
Q_{SET}, Q_1..Q_N: ALD1101 or ALD1103
N-Channel MOSFET

TYPICAL APPLICATIONS (cont.)

BASIC CURRENT SOURCES

N-CHANNEL CURRENT SOURCE

$$I_{SOURCE} = I_{SET}$$
$$= \frac{V+ - Vt}{R_{SET}}$$
$$\cong \frac{V+ - 1.0}{R_{SET}}$$
$$\cong \frac{4}{R_{SET}}$$
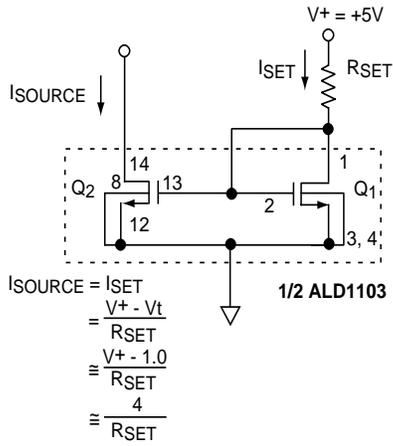
1/2 ALD1103

Q_1, Q_2: N-Channel MOSFET

P-CHANNEL CURRENT SOURCE
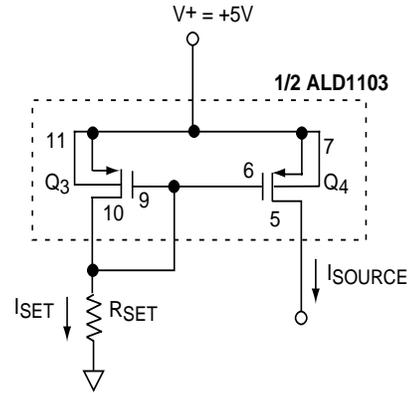
1/2 ALD1103

Q_3, Q_4: P-Channel MOSFET

CASCODE CURRENT SOURCES
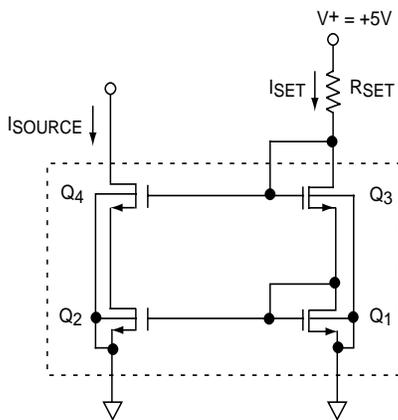
Q_1, Q_2, Q_3, Q_4: N-Channel MOSFET
(ALD1101 or ALD1103)

$$I_{SOURCE} = I_{SET} = \frac{V+ - 2Vt}{R_{SET}} \cong \frac{3}{R_{SET}}$$
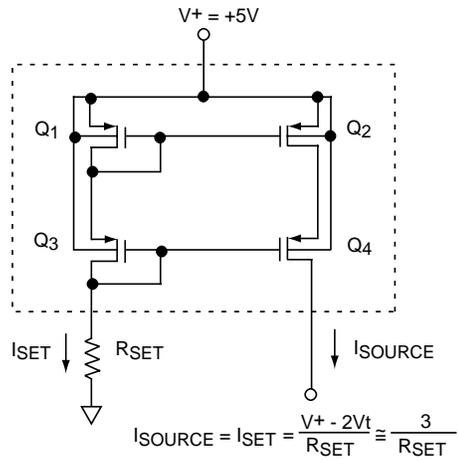
Q_1, Q_2, Q_3, Q_4: P-Channel MOSFET
(ALD1102 or ALD1103)

SOIC-14 PACKAGE DRAWING

14 Pin Plastic SOIC Package
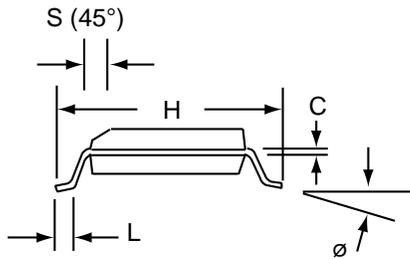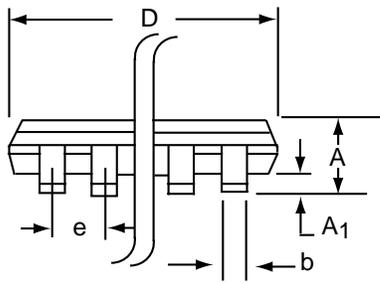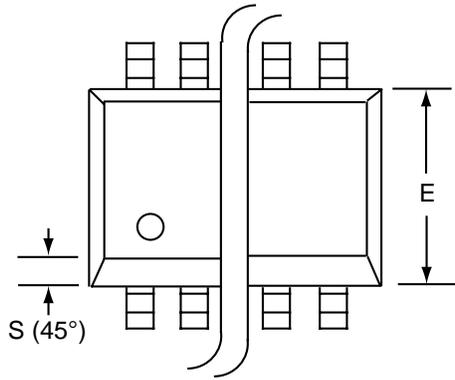
Dim	Millimeters		Inches	
	Min	**Max**	**Min**	**Max**
A	1.35	1.75	0.053	0.069
A₁	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-14	8.55	8.75	0.336	0.345
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
Ø	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020

PDIP-14 PACKAGE DRAWING

14 Pin Plastic DIP Package
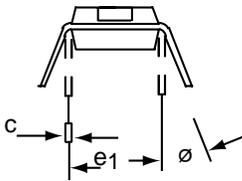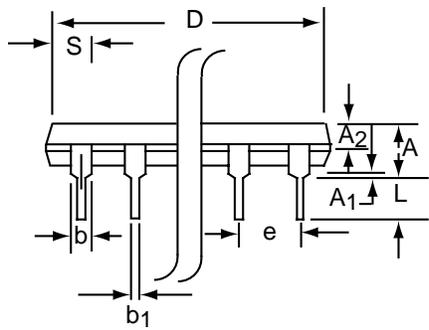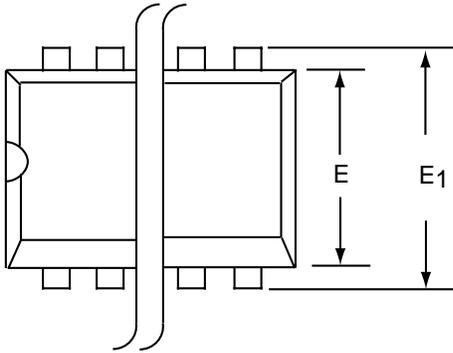
Dim	Millimeters		Inches	
	Min	**Max**	**Min**	**Max**
A	3.81	5.08	0.105	0.200
A$_1$	0.38	1.27	0.015	0.050
A$_2$	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b$_1$	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D-14	17.27	19.30	0.680	0.760
E	5.59	7.11	0.220	0.280
E$_1$	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e$_1$	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S-14	1.02	2.03	0.040	0.080
ø	0°	15°	0°	15°

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