



## COMPLEMENTARY N-CHANNEL AND P-CHANNEL MOSFET

### GENERAL DESCRIPTION

The ALD1115 is a monolithic complementary N-channel and P-channel transistor pair intended for a broad range of analog applications. These enhancement-mode transistors are manufactured with Advanced Linear Devices' enhanced ACMOS silicon gate CMOS process. It consists of a N-channel MOSFET and a P-channel MOSFET in one package. The ALD1115 is a dual version of the quad complementary ALD1105.

The ALD1115 offers high input impedance and negative current temperature coefficient. The transistor pair is designed for precision signal switching and amplifying applications in +1V to +10V systems where low input bias current, low input capacitance and fast switching speed are desired. Since these are MOSFET devices, they feature very large (almost infinite) current gain in a low frequency, or near DC, operating environment. When connected in parallel with sources, drains and gates connected together, a CMOS analog switch can be constructed. In addition, the ALD1115 is intended as a building block for CMOS inverters, differential amplifier input stages, transmission gates, and multiplexer applications.

The ALD1115 is suitable for use in precision applications which require very high current gain, beta, such as current mirrors and current sources. The high input impedance and the high DC current gain of the Field Effect Transistors result in extremely low current loss through the control gate. The DC current gain is limited by the gate input leakage current, which is specified at 100pA at room temperature. V+ is connected to the substrate, which is the most positive voltage potential of the ALD1115, usually SP (5). Similarly, V- is connected to the most negative voltage potential of the ALD1115, usually SN (1).

### FEATURES

- Thermal tracking between N-channel and P-channel
- Low threshold voltage of 0.7V for both N-channel and P-channel MOSFETs
- Low input capacitance
- High input impedance --  $10^{13}\Omega$  typical
- Low input and output leakage currents
- Negative current ( $I_{DS}$ ) temperature coefficient
- Enhancement-mode (normally off)
- DC current gain  $10^9$
- Single N-channel MOSFET and single P-channel MOSFET in one package

### ORDERING INFORMATION ("L" suffix denotes lead-free (RoHS))

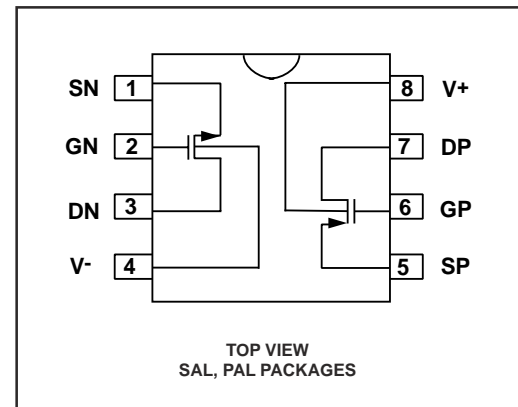
Operating Temperature Range*	
0°C to +70°C	0°C to +70°C
8-Pin SOIC Package	8-Pin Plastic Dip Package
ALD1115SAL	ALD1115PAL

\* Contact factory for high temperature versions.

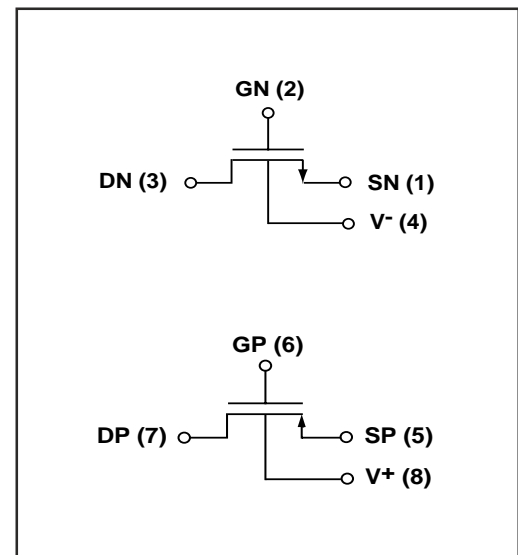
### APPLICATIONS

- Precision current mirrors
- Complementary push-pull linear drives
- Discrete analog switches
- Analog signal choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Analog current inverter
- Precision matched current sources
- CMOS inverter stage
- Diode clamps
- Source followers

### PIN CONFIGURATION



### BLOCK DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

Drain-source voltage,  $V_{DS}$  \_\_\_\_\_ 10V  
 Gate-source voltage,  $V_{GS}$  \_\_\_\_\_ 10V  
 Power dissipation \_\_\_\_\_ 500mW  
 Operating temperature range SAL, PAL packages \_\_\_\_\_ 0°C to +70°C  
 Storage temperature range \_\_\_\_\_ -65°C to +150°C  
 Lead temperature, 10 seconds \_\_\_\_\_ +260°C

**CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.**

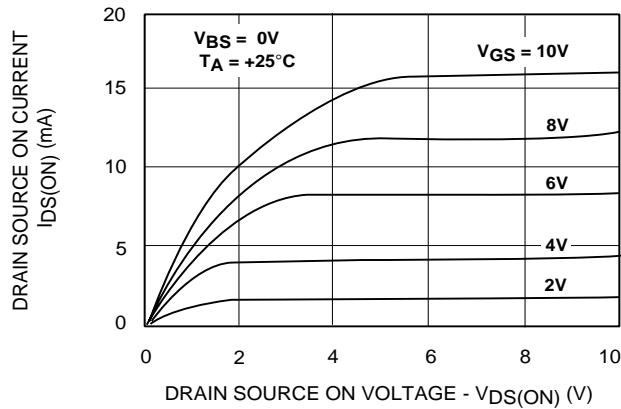
### OPERATING ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$  unless otherwise specified

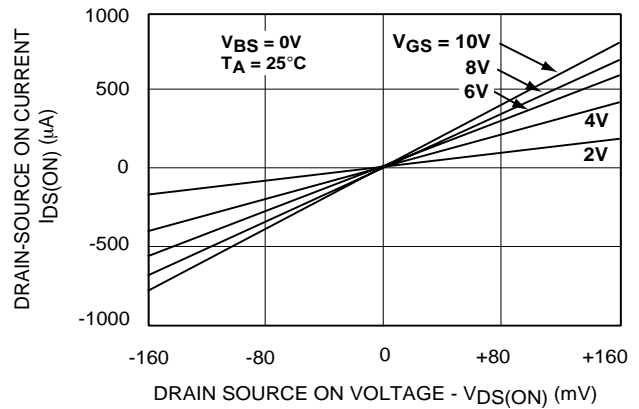
Parameter	Symbol	N - Channel			Unit	Test Conditions	P - Channel			Unit	Test Conditions
		Min	Typ	Max			Min	Typ	Max		
Gate Threshold Voltage	$V_T$	0.4	0.7	1.0	V	$I_{DS} = 1\mu\text{A}$ $V_{GS} = V_{DS}$	-0.4	-0.7	-1.2	V	$I_{DS} = -1\mu\text{A}$ $V_{GS} = V_{DS}$
Gate Threshold Temperature Drift	$TC_{VT}$		-1.2		mV/°C			-1.3		mV/°C	
On Drain Current	$I_{DS(ON)}$	3	4.8		mA	$V_{GS} = V_{DS} = 5\text{V}$	-1.3	-2		mA	$V_{GS} = V_{DS} = -5\text{V}$
Trans-conductance	$G_{fs}$	1	1.8		mmho	$V_{DS} = 5\text{V}$ $I_{DS} = 10\text{mA}$	0.25	0.67		mmho	$V_{DS} = -5\text{V}$ $I_{DS} = -10\text{mA}$
Output Conductance	$G_{OS}$		200		$\mu\text{mho}$	$V_{DS} = 5\text{V}$ $I_{DS} = 10\text{mA}$		40		$\mu\text{mho}$	$V_{DS} = -5\text{V}$ $I_{DS} = -10\text{mA}$
Drain Source ON Resistance	$R_{DS(ON)}$		350	500	$\Omega$	$V_{DS} = 0.1\text{V}$ $V_{GS} = 5\text{V}$		1200	1800	$\Omega$	$V_{DS} = -0.1\text{V}$ $V_{GS} = -5\text{V}$
Drain Source Breakdown Voltage	$BV_{DSS}$	10			V	$I_{DS} = 1\mu\text{A}$ $V_{GS} = 0\text{V}$	-10			V	$I_{DS} = -1\mu\text{A}$ $V_{GS} = 0\text{V}$
Off Drain Current	$I_{DS(OFF)}$		10	400 4	pA nA	$V_{DS} = 10\text{V}$ $I_{GS} = 0\text{V}$ $T_A = 125^\circ\text{C}$		10	400 4	pA nA	$V_{DS} = -10\text{V}$ $V_{GS} = 0\text{V}$ $T_A = 125^\circ\text{C}$
Gate Leakage Current	$I_{GSS}$		1	100 1	pA nA	$V_{DS} = 0\text{V}$ $V_{GS} = 10\text{V}$ $T_A = 125^\circ\text{C}$		1	100 1	pA nA	$V_{DS} = 0\text{V}$ $V_{GS} = -10\text{V}$ $T_A = 125^\circ\text{C}$
Input Capacitance	$C_{ISS}$		1	3	pF			1	3	pF	

# TYPICAL N-CHANNEL PERFORMANCE CHARACTERISTICS

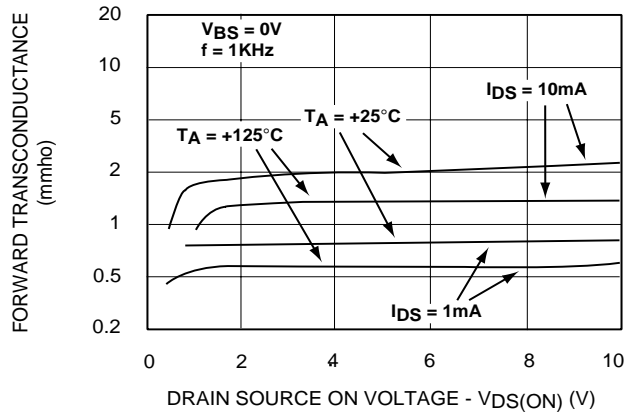
## OUTPUT CHARACTERISTICS



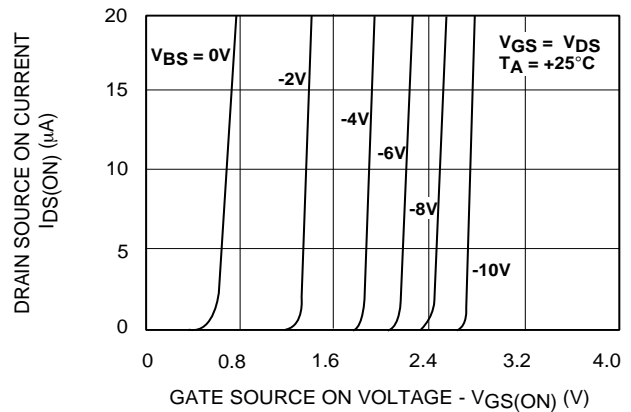
## LOW VOLTAGE OUTPUT CHARACTERISTICS



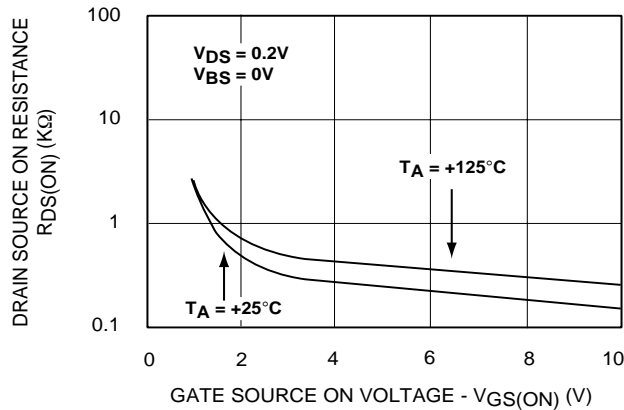
## FORWARD TRANSCONDUCTANCE vs. DRAIN-SOURCE VOLTAGE



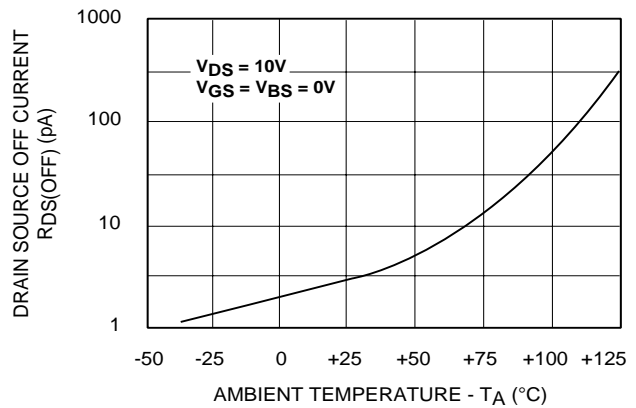
## TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS



## DRAIN SOURCE ON RESISTANCE vs. GATE-SOURCE VOLTAGE

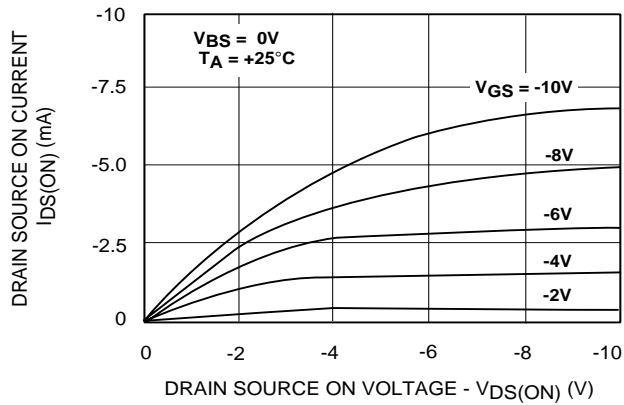


## DRAIN SOURCE OFF CURRENT vs. AMBIENT TEMPERATURE

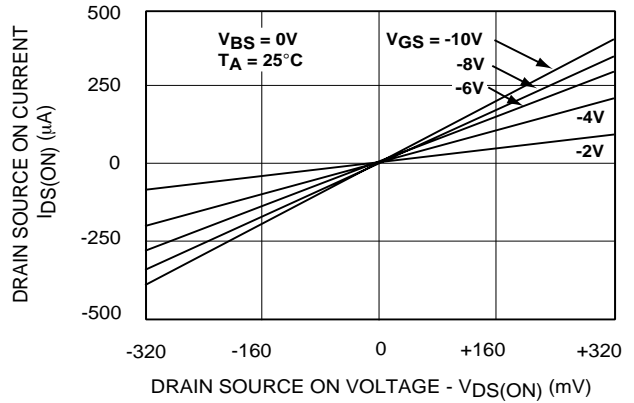


# TYPICAL P-CHANNEL PERFORMANCE CHARACTERISTICS

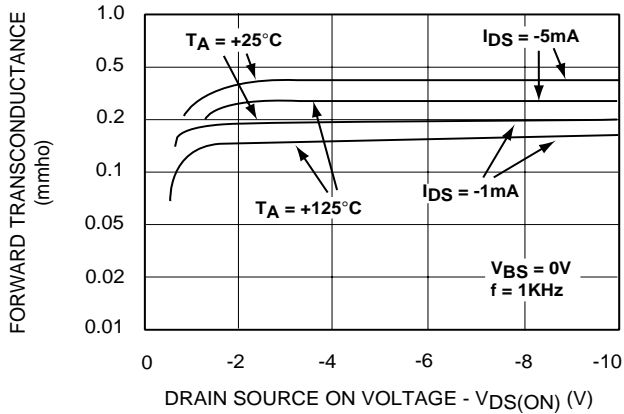
## OUTPUT CHARACTERISTICS



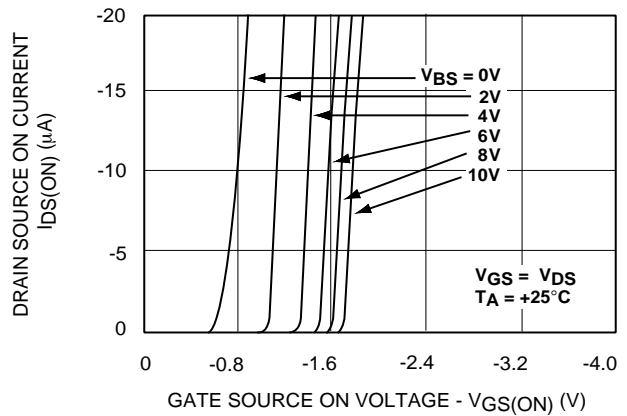
## LOW VOLTAGE OUTPUT CHARACTERISTICS



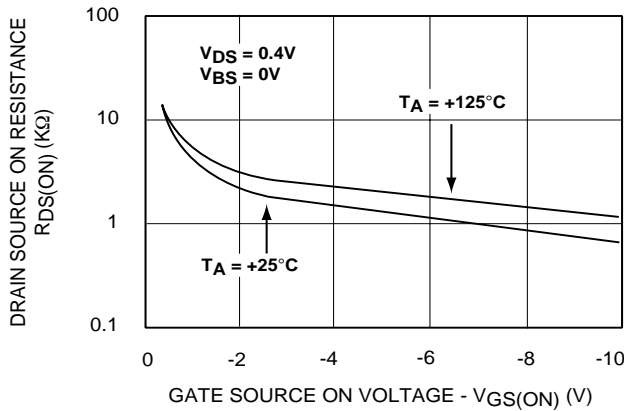
## FORWARD TRANSCONDUCTANCE vs. DRAIN-SOURCE VOLTAGE



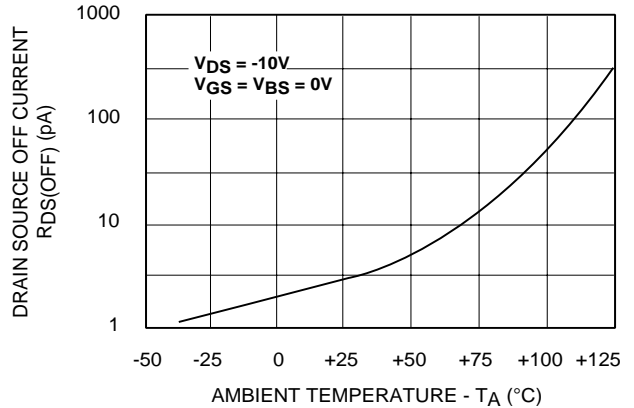
## TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS



## DRAIN SOURCE ON RESISTANCE vs. GATE-SOURCE VOLTAGE

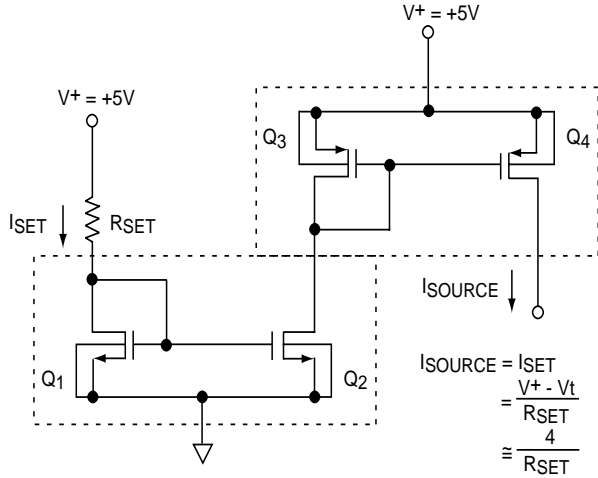


## DRAIN SOURCE OFF CURRENT vs. AMBIENT TEMPERATURE



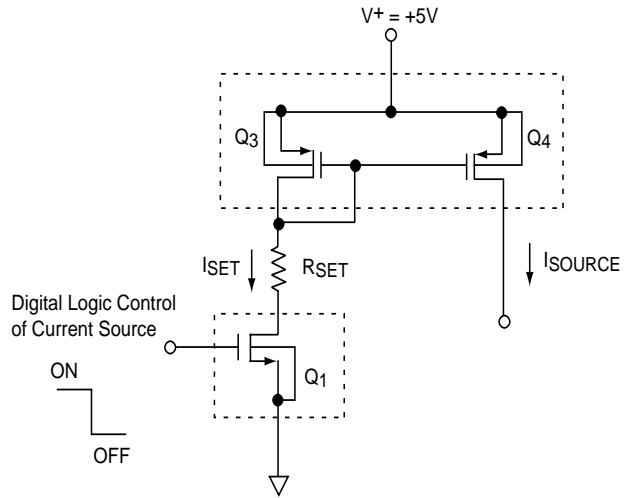
# TYPICAL APPLICATIONS

## CURRENT SOURCE MIRROR



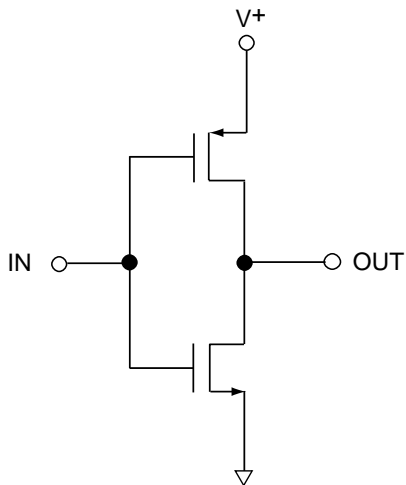
Q<sub>1</sub>, Q<sub>2</sub>: N-Channel MOSFET  
 Q<sub>3</sub>, Q<sub>4</sub>: P-Channel MOSFET

## CURRENT SOURCE WITH GATE CONTROL

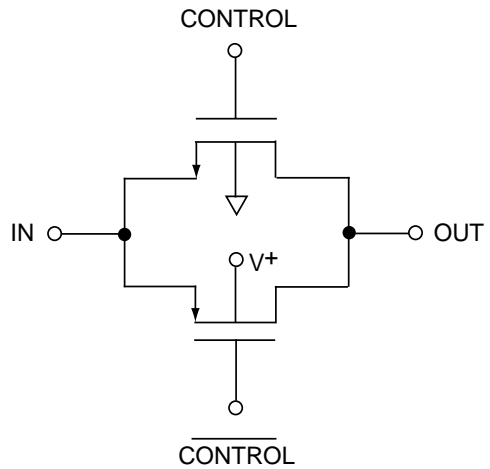


Q<sub>1</sub> : N-Channel MOSFET  
 Q<sub>3</sub>, Q<sub>4</sub>: P-Channel MOSFET

## CMOS INVERTER

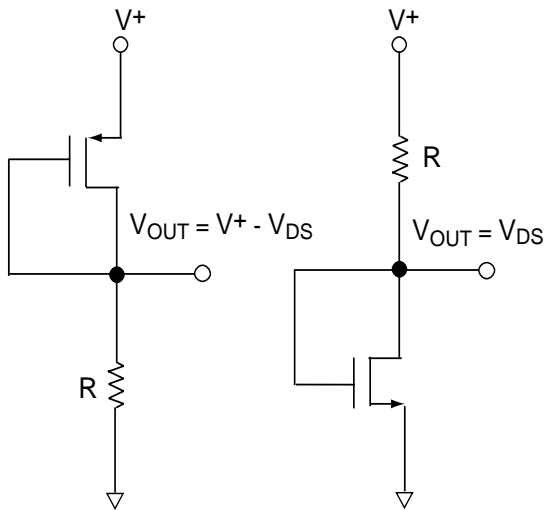


## CMOS ANALOG SWITCH

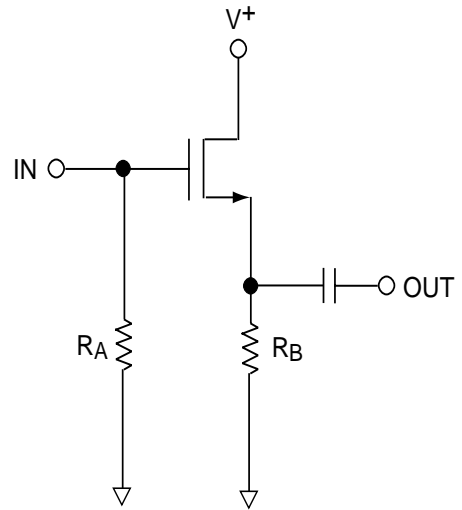


## TYPICAL APPLICATIONS (cont.)

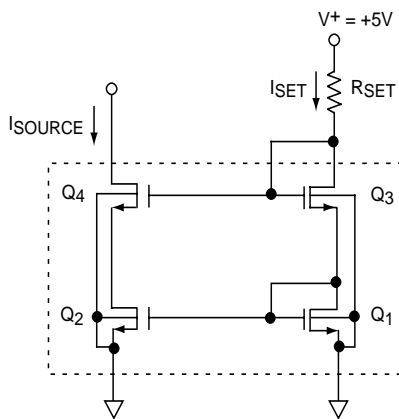
### DIODE-CONNECTED CONFIGURATION



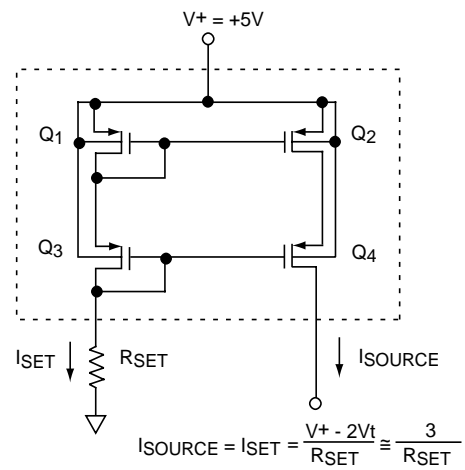
### SOURCE FOLLOWER



### CASCODE CURRENT SOURCES



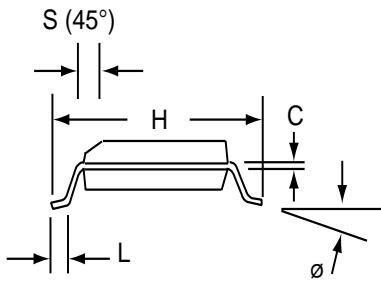
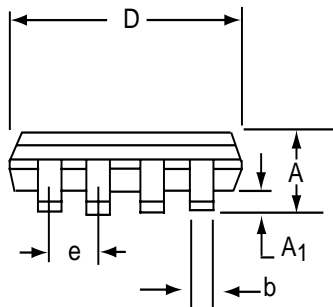
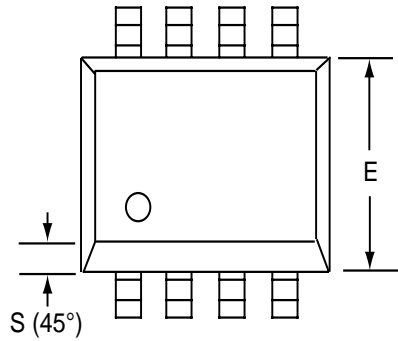
Q<sub>1</sub>, Q<sub>2</sub>, Q<sub>3</sub>, Q<sub>4</sub>: N-Channel MOSFET



Q<sub>1</sub>, Q<sub>2</sub>, Q<sub>3</sub>, Q<sub>4</sub>: P-Channel MOSFET

# SOIC-8 PACKAGE DRAWING

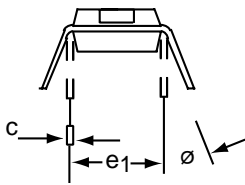
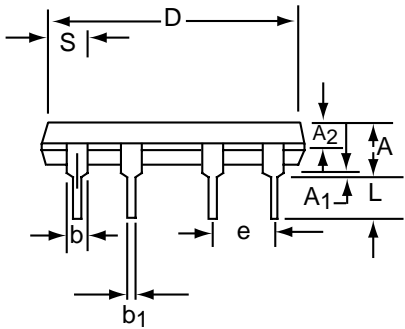
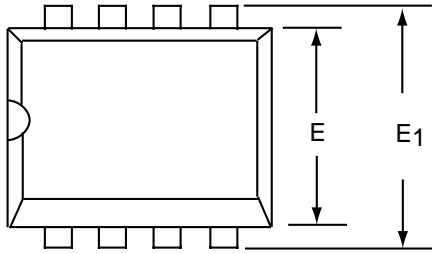
## 8 Pin Plastic SOIC Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-8	4.69	5.00	0.185	0.196
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
∅	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020

# PDIP-8 PACKAGE DRAWING

## 8 Pin Plastic DIP Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.105	0.200
A <sub>1</sub>	0.38	1.27	0.015	0.050
A <sub>2</sub>	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b <sub>1</sub>	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D-8	9.40	11.68	0.370	0.460
E	5.59	7.11	0.220	0.280
E <sub>1</sub>	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e <sub>1</sub>	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S-8	1.02	2.03	0.040	0.080
∅	0°	15°	0°	15°



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