AS7265x

Smart 18-Channel VIS to NIR Spectral_ID 3-Sensor Chipset with Electronic Shutter

General Description

The AS7265x chipset consists of three sensor devices AS72651 with master capability, AS72652 and AS72653. The multispectral sensors can be used for spectral identification in a range from visible to NIR. Every of the three sensor devices has 6 independent on-device optical filters whose spectral response is defined in a range from 410nm to 940nm with FWHM of 20nm. The AS72651, combined with the AS72652 (spectral response from 560nm to 940nm) and the AS72653 (spectral response from 410nm to 535nm) form an AS7265x 18-channel multi-spectral sensor chip-set. Using the AS7265x chipset requires the use of firmware. It must be loaded into a serial flash via a UART interface. The list of **ams** tested serial flash memories can be found in Figure 56. The components AS72651, AS72652 and AS72653 are pre-calibrated with a specific light source. The information about the conditions of the performed calibration (for example light source, gain, integration time) can be found in the table of optical characteristics of the respective component. Any operation other than these conditions might require a new calibration in the application.

Each AS7265x device has two integrated LED drivers with programmable current and can be timed for electronic shutter applications.

The device family integrates Gaussian filters into standard CMOS silicon via nano-optic deposited interference filter technology in LGA packages that also provide built-in apertures to control the light entering the sensor array.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS7265x, Smart 18-Channel VIS to NIR Spectral_ID 3-Sensor Chipset with Electronic Shutter are listed below:

Figure 1:
AS7265x Chip-Set Benefits and Features

Benefits	Features
• Compact 18-channel spectrometry chip-set solution	• 3 chip set including master device delivering 18 visible and NIR channels from 410nm to 940nm each with 20nm FWHM
	• UART or I^2C slave digital Interface
	• Visible filter set realized by silicon interference filters
• No additional signal conditioning required	• 16-bit ADC with digital access
	• Programmable LED drivers
	• 2.7V to 3.6V with I^2C interface
• Small, robust package, with built-in aperture	• 20-pin LGA package 4.5mm x 4.7mm x 2.5mm -40°C to 85°C temperature range

Applications

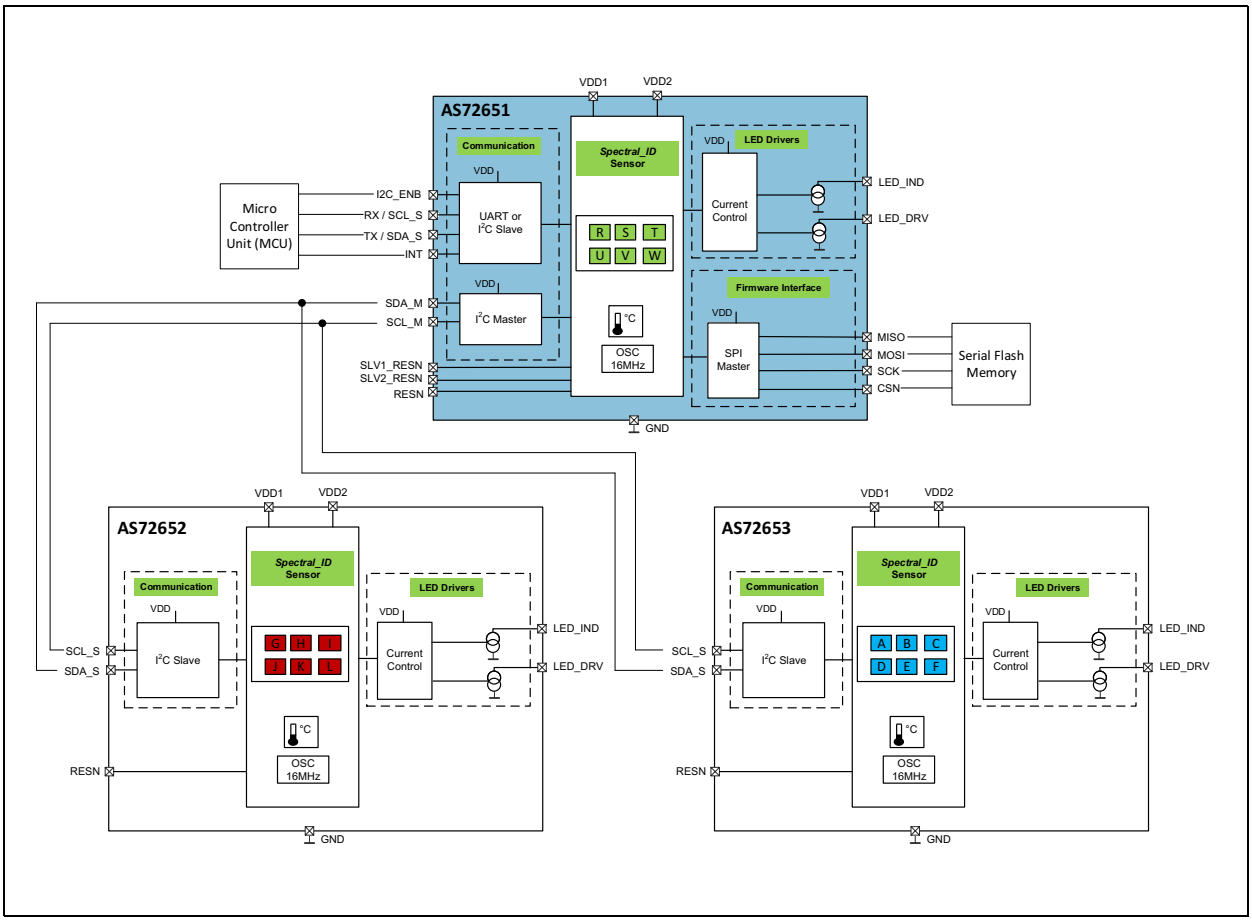
The AS7265x applications include:

- Product/Brand authentication
- Anti-counterfeiting
- Portable spectroscopy
- Product safety/adulteration detection
- Horticultural and specialty lighting
- Material analysis

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
AS7265x Chip-Set Block Diagram



Note(s):

1. Refer to the Application Diagram in Figure 60.

Pin Assignments

The device pin assignments are described below.

Figure 3:
Pin Diagram of AS7265x (Top View)

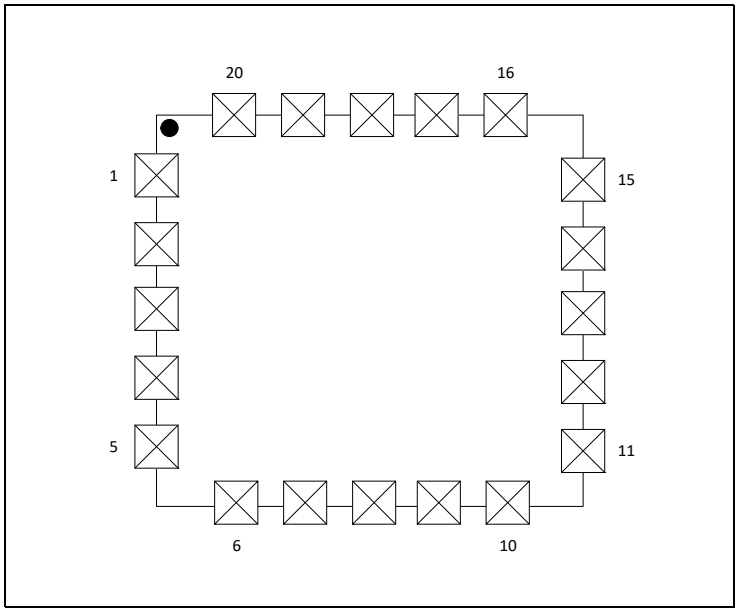


Figure 4:
AS72651 Pin Description

Pin No.	Pin Name	Pin Type	Description
1	SLV1_RESN	Digital Input and Output	Reset pin for Slave 1 e.g. AS72652, active low
2	RESN	Digital Input	Reset pin, active low (with internal pull-up to VDD)
3	SCK	Digital Output	SPI serial clock
4	MOSI	Digital Input and Output	SPI MOSI
5	MISO	Digital Input and Output	SPI MISO
6	CSN	Digital Output	Chip select for external flash
7	NC		Not functional, no connect
8	I2C_ENB	Digital Input	Selects UART (low) or I^2C (high) operation
9	SCL_M	Digital Output	I^2C master clock for communication with AS72652 and AS72653
10	SDA_M	Digital Input and Output	I^2C master data for communication with AS72652 and AS72653

Pin No.	Pin Name	Pin Type	Description
11	RX / SCL_S	Digital Input and Output	RX (UART) or SCL_S (I^2C slave) depending on I2C_ENB setting
12	TX / SDA_S	Digital Input and Output	TX (UART) or SDA_S (I^2C slave) depending on I2C_ENB setting
13	INT	Digital Output	INT is active low
14	VDD2	Voltage Supply	Voltage supply
15	LED_DRV	Analog Output	LED driver output for driver LED, current sink
16	GND	Supply	Ground
17	VDD1	Voltage Supply	Voltage supply
18	LED_IND	Analog Output	LED driver output for indicator LED, current sink
19	NC		Not functional, no connect
20	SLV2_RESN	Digital Output	Reset pin for slave 2 e.g. AS72653, active low

Note(s):

1. Pin out is valid for firmware versions from 11 and later.

Figure 5:
AS72652 and AS72653 Pin Description

Pin No.	Pin Name	Pin Type	Description
1	NC		Not functional, no connect
2	RESN	Digital Input	Reset pin, active low (with internal pull-up to VDD)
3	NC		Not functional, no connect
4	NC		Not functional, no connect
5	NC		Not functional, no connect
6	NC		Not functional, no connect
7	NC		Not functional, no connect
8	NC		Not functional, no connect
9	SCL_S	Digital Input and Output	I^2C slave clock for communication with master AS72651
10	SDA_S	Digital Input and Output	I^2C slave data for communication with master AS72651

Pin No.	Pin Name	Pin Type	Description
11	NC		Not functional, no connect
12	NC		Not functional, no connect
13	INT	Digital Output	INT is active low
14	VDD2	Voltage Supply	Voltage supply
15	LED_DRV	Analog Output	LED driver output for driver LED, current sink
16	GND	Supply	Ground
17	VDD1	Voltage Supply	Voltage supply
18	LED_IND	Analog Output	LED driver output for indicator LED, current sink
19	NC		Not functional, no connect
20	NC		Not functional, no connect

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings of AS7265x may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device is not designed for high energy UV (ultraviolet) environments, including upward looking outdoor applications, which could affect long term optical performance.

Figure 6:
Absolute Maximum Ratings of AS7265x

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
V_{DD1_MAX}	Supply Voltage VDD1	-0.3	5	V	Pin VDD1 to GND
V_{DD2_MAX}	Supply Voltage VDD2	-0.3	5	V	Pin VDD2 to GND
V_{DD_IO}	Input/Output Pin Voltage	-0.3	VDD+0.3	V	Input/Output Pin to GND
I_{SCR}	Input Current (latch-up immunity)	± 100		mA	JESD78D
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	±1000		V	JS-001-2014
ESD_{CDM}	Electrostatic Discharge CDM	±500		V	JESD22-C101F
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage Temperature Range	-40	85	°C	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices”
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	3			Represents a 168 hour max. floor lifetime

Electrical Characteristics

All limits are guaranteed with VDD = VDD1 = VDD2 = 3.3V, T_{AMB} = 25°C. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

VDD1 and VDD2 should be sourced from the same power supply output.

Figure 7:
Electrical Characteristics of AS7265x

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General Operating Conditions						
VDD1 /VDD2	Voltage Operating Supply	UART Interface	2.97	3.3	3.6	V
VDD1 /VDD2	Voltage Operating Supply	I^2C Interface	2.7	3.3	3.6	V
T_{AMB}	Operating Temperature		-40	25	85	°C
I_{VDD}	Operating Current				5	mA
Internal RC Oscillator						
F_{OSC}	Internal RC Oscillator Frequency		15.7	16	16.3	MHz
t_{JITTER} (1)	Internal Clock Jitter	@25°C			1.2	ns
Temperature Sensor						
D_{TEMP}	Absolute Accuracy of the Internal Temperature Measurement		-8.5		8.5	°C
Indicator LED						
I_{IND}	LED Current		1		8	mA
I_{ACC}	Accuracy of Current		-30		30	%
V_{LED}	Voltage Range of Connected LED	Vds of current sink	0.3		VDD	V
LED_DRV						
I_{LED1}	LED Current		12.5		100	mA
I_{ACC}	Accuracy of Current		-10		10	%
V_{LED}	Voltage Range of Connected LED	Vds of current sink	0.3		VDD	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital Inputs and Outputs						
I_{IH}, I_{IL}	Logic Input Current	Vin=0V or VDD	-1		1	µA
V_{IH}	CMOS Logic High Input		0.7* VDD		VDD	V
V_{IL}	CMOS Logic Low Input		0		0.3* VDD	V
V_{OH}	CMOS Logic High Output	I=1mA			VDD-0.4	V
V_{OL}	CMOS Logic Low Output	I=1mA			0.4	V
t_{RISE} (1)	Current Rise Time	C(Pad)=30pF			5	ns
t_{FALL} (1)	Current Fall Time	C(Pad)=30pF			5	ns

Note(s):

1. Guaranteed by design, not tested in production.

Timing Characteristics

Figure 8:
AS7265x I²C Slave Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I²C Interface						
f_{SCLK}	SCL Clock Frequency		0		400	kHz
t_{BUF}	Bus Free Time Between a STOP and START		1.3			µs
$t_{HS:STA}$	Hold Time (Repeated) START		0.6			µs
t_{LOW}	LOW Period of SCL Clock		1.3			µs
t_{HIGH}	HIGH Period of SCL Clock		0.6			µs
$t_{SU:STA}$	Setup Time for a Repeated START		0.6			µs
$t_{HS:DAT}$	Data Hold Time		0		0.9	µs
$t_{SU:DAT}$	Data Setup Time		100			ns
t_R	Rise Time of Both SDA and SCL		20		300	ns
t_F	Fall Time of Both SDA and SCL		20		300	ns
$t_{SU:STO}$	Setup Time for STOP Condition		0.6			µs
C_B	Capacitive Load for Each Bus Line	CB - total capacitance of one bus line in pF			400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL)				10	pF

Figure 9:
I²C Slave Timing Diagram

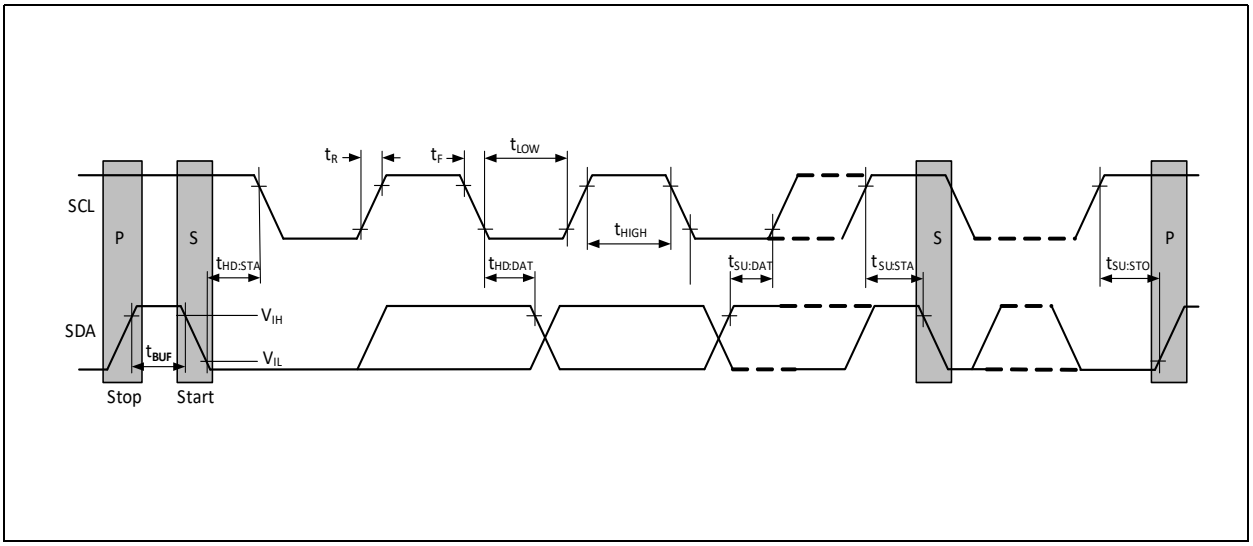


Figure 10:
AS72651 SPI Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPI Interface						
f_{SCK}	Clock Frequency		0		16	MHz
t_{SCK_H}	Clock High Time		40			ns
t_{SCK_L}	Clock Low Time		40			ns
t_{SCK_RISE}	SCK Rise Time		5			ns
t_{SCK_FALL}	SCK Fall Time		5			ns
t_{CSN_S}	CSN Setup Time	Time between CSN high-low transition to first SCK high transition	50			ns
t_{CSN_H}	CSN Hold Time	Time between last SCK falling edge and CSN low-high transition	100			ns
t_{CSN_DIS}	CSN Disable Time		100			ns
t_{DO_S}	Data-Out Setup Time		5			ns
t_{DO_H}	Data-Out Hold Time		5			ns
t_{DI_V}	Data-In Valid		10			ns

Figure 11:
SPI Master Write Timing Diagram

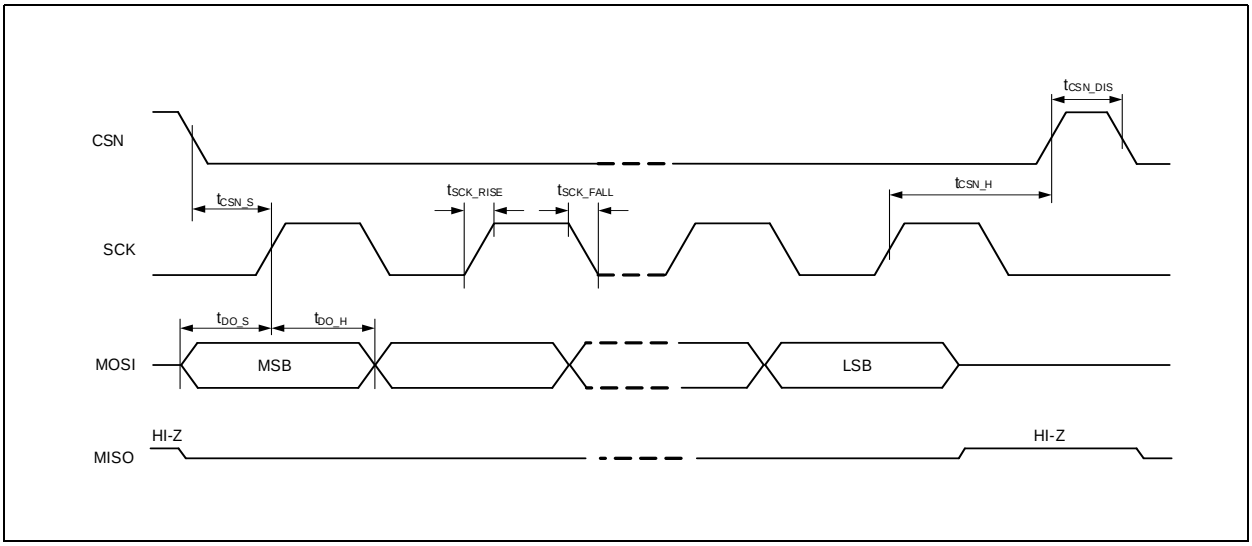
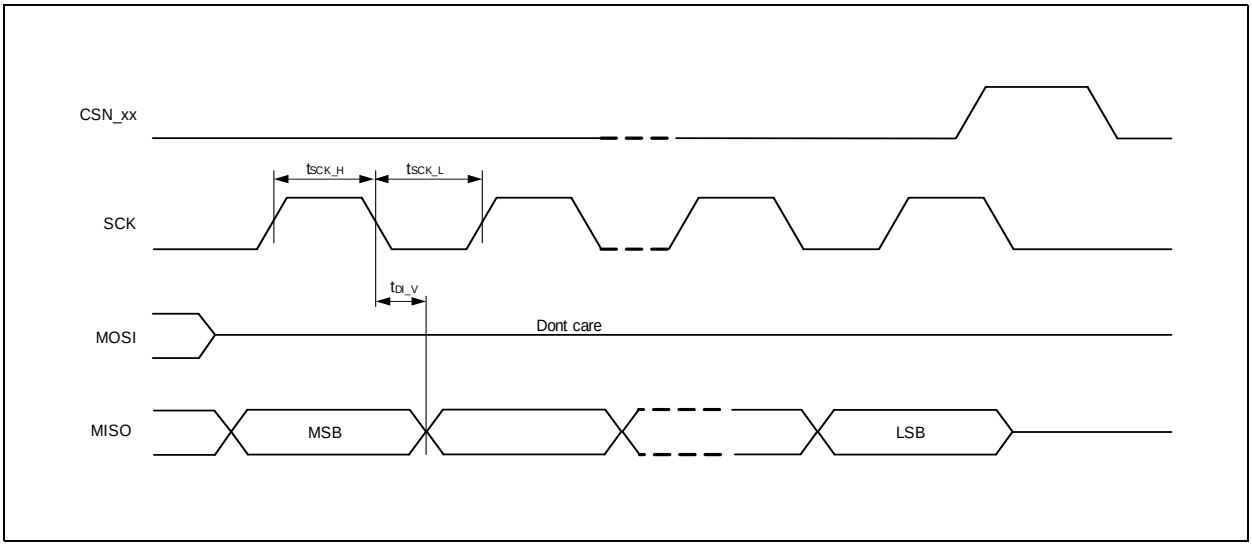


Figure 12:
SPI Master Read Timing Diagram



Typical Operating Characteristics

Optical Characteristics

All optical characteristics are optimized for diffused light. When using a point light source or collimated light on the sensor, the sensor opening must be covered by a lambertian diffuser with achromatic characteristics. Diffusor of Tsujiden like D121UP have been successfully tested at **ams**. If in the application diffused light, e.g. used by a reflective surface, no additional diffuser is required.

Figure 13:
AS7265x LGA Average Field of View

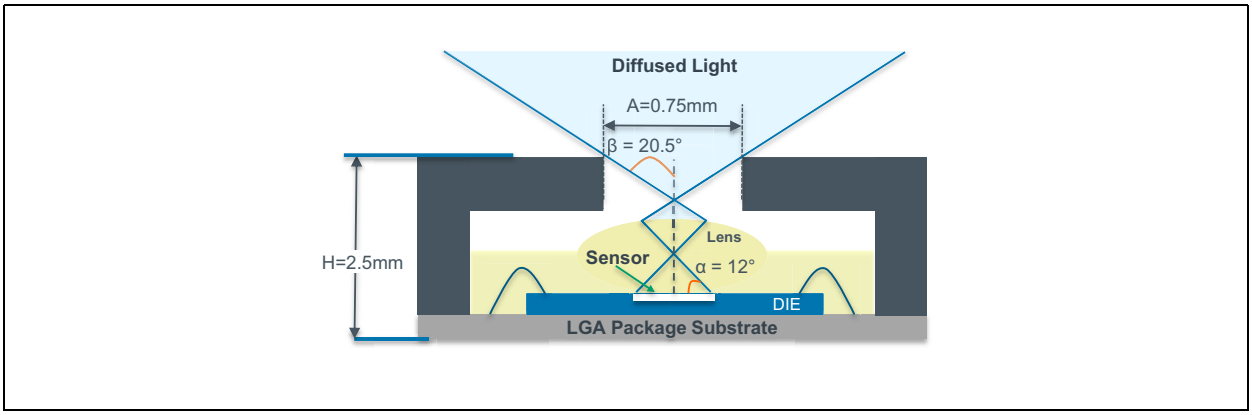


Figure 14:
AS7265x 18-Channel Spectral Responsivity

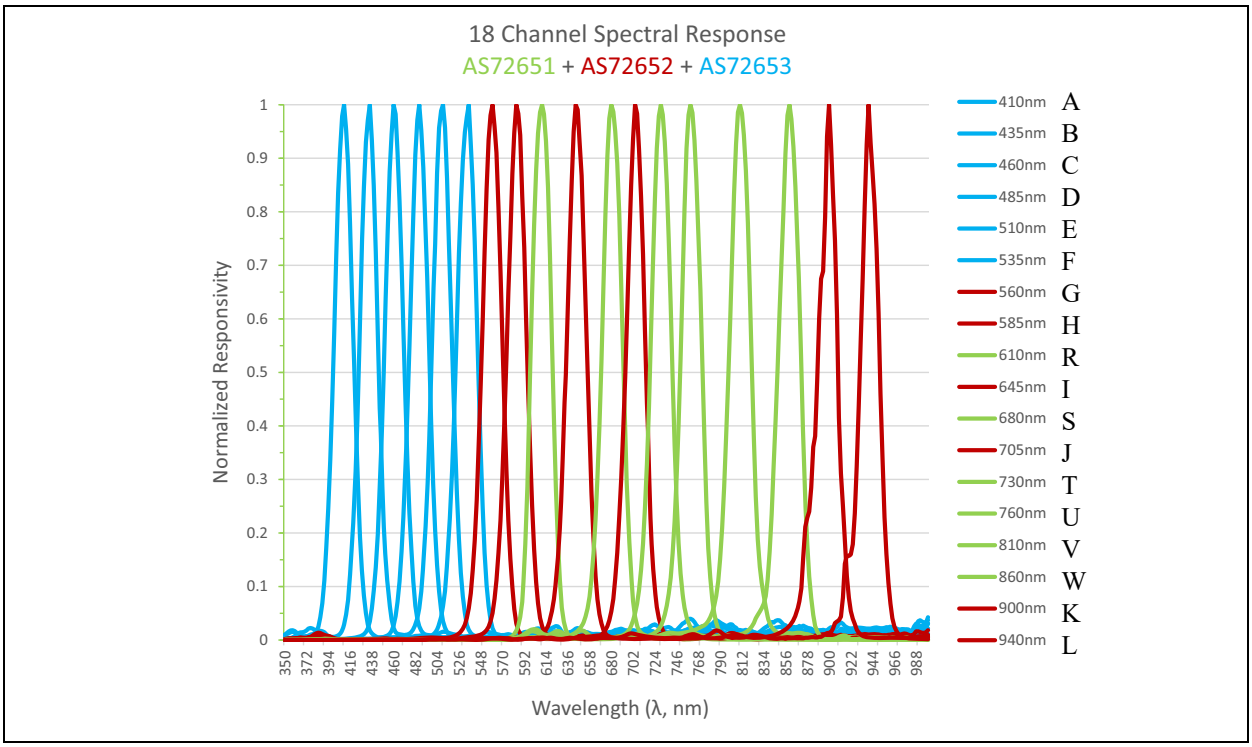


Figure 15:
AS72651 Spectral Responsivity

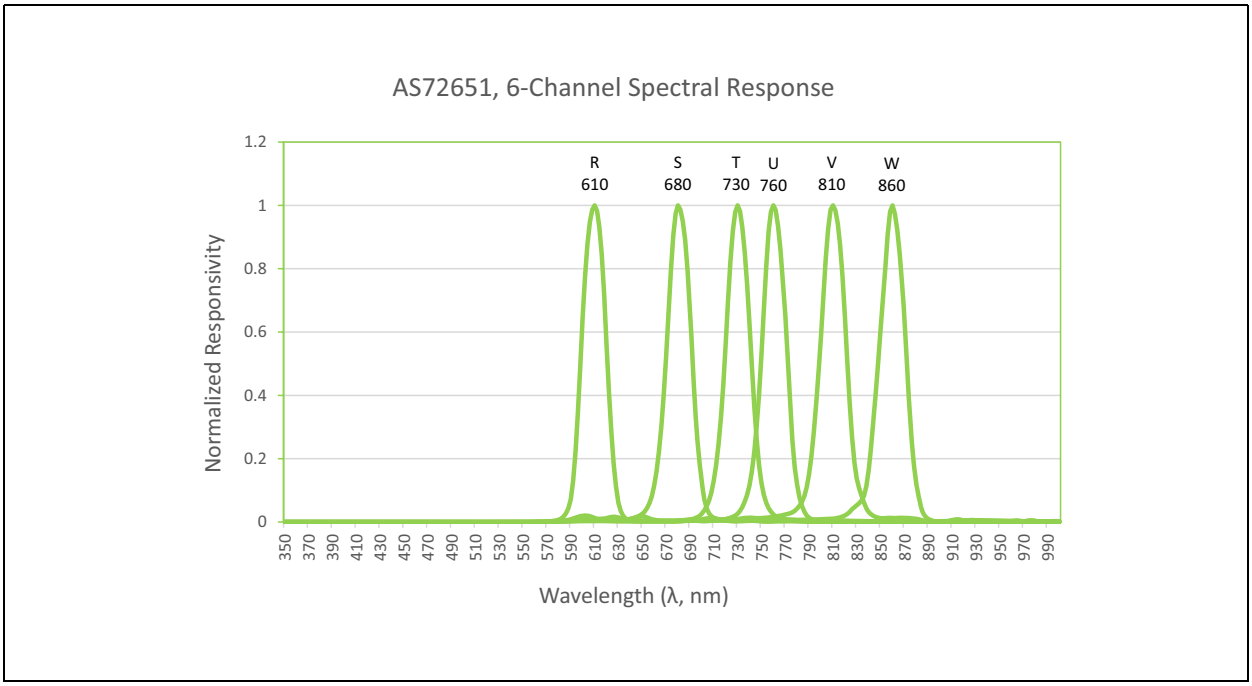


Figure 16:
Optical Characteristics of AS72651 (Pass Band) (1)

Symbol	Parameter	Test Conditions	Channel (nm)	Min	Typ	Max	Unit
R	Channel R	Incandescent(2),(4)	610		35(3),(4)		counts/ (µW/cm^2)
S	Channel S	Incandescent(2),(4)	680		35(3),(4)		counts/ (µW/cm^2)
T	Channel T	Incandescent(2),(4)	730		35(3),(4)		counts/ (µW/cm^2)
U	Channel U	Incandescent(2),(4)	760		35(3),(4)		counts/ (µW/cm^2)
V	Channel V	Incandescent(2),(4)	810		35(3),(4)		counts/ (µW/cm^2)
W	Channel W	Incandescent(2),(4)	860		35(3),(4)		counts/ (µW/cm^2)
FWHM	Full Width Half Max				20		nm
Wacc	Wavelength Accuracy			+10		-10	nm

Symbol	Parameter	Test Conditions	Channel (nm)	Min	Typ	Max	Unit
dark	Dark Channel Counts	GAIN=64, T_{AMB}=25°C t_{int}=165ms				5	counts
AFOV	Average Field of View				±20.5		deg

Note(s):

1. Calibration and measurements are made using diffused light.
2. Each channel is tested with GAIN = 16x, Integration Time (INT_T) = 166ms and VDD = VDD1 = VDD2 = 3.3V, T_{AMB}=25°C.
3. The accuracy of the channel counts/µW/cm^2 is ±12%.
4. The light source is an incandescent light with an irradiance of ~1500µW/cm^2 (300-1000nm).

Figure 17:
AS72652 Spectral Responsivity

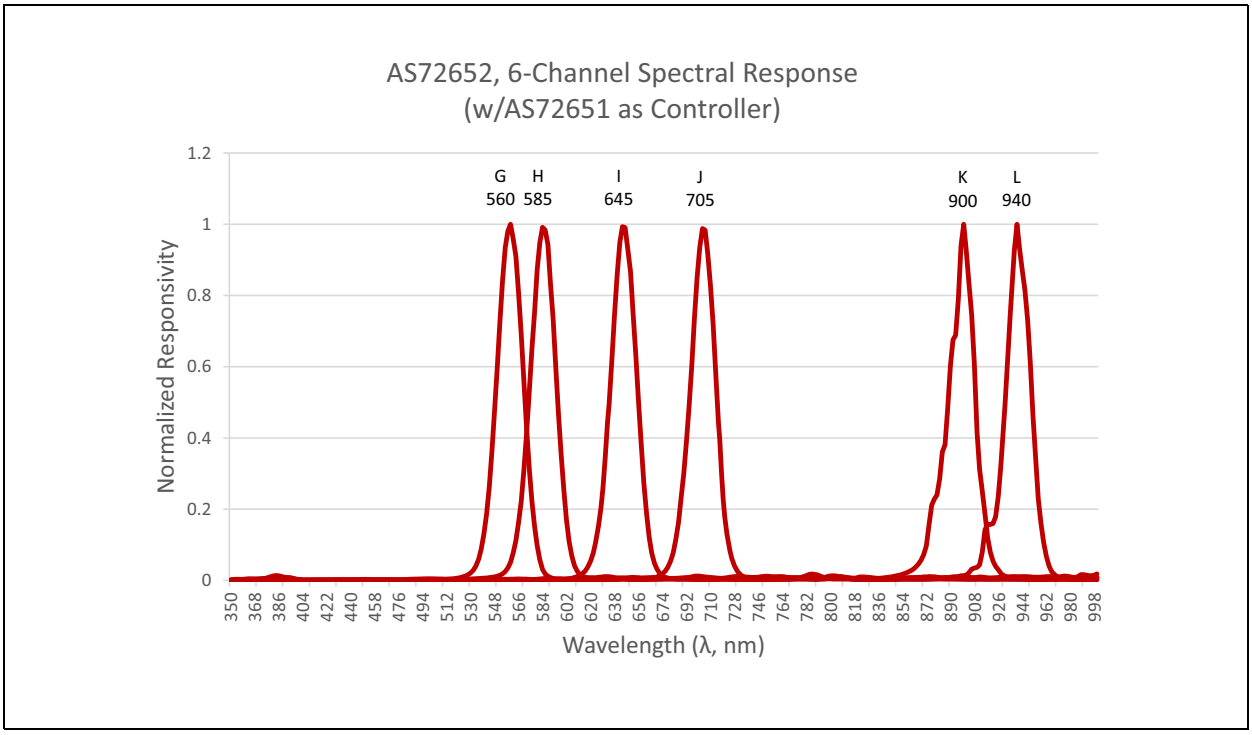


Figure 18:
Optical Characteristics of AS72652 (Pass Band) (1)

Symbol	Parameter	Conditions	Channel (nm)	Min	Typ	Max	Unit
G	Channel G	3300K White LED(2)	560		35(3)		counts/ ($\mu W/cm^2$)
H	Channel H	3300K White LED(2)	585		35(3)		counts/ ($\mu W/cm^2$)
I	Channel I	3300K White LED(2)	645		35(3)		counts/ ($\mu W/cm^2$)
J	Channel J	3300K White LED(2)	705		35(3)		counts/ ($\mu W/cm^2$)
K	Channel K	Incandescent(2)	900		35(3)		counts/ ($\mu W/cm^2$)
L	Channel L	940nm LED(2)	940		35(3)		counts/ ($\mu W/cm^2$)
FWHM	Full Width Half Max				20		nm
Wacc	Wavelength Accuracy			-10		+10	nm
dark	Dark Channel Counts	GAIN=64, T_{AMB}=25°C t_{int} = 165ms				5	counts
AFOV	Average Field of View				±20.5		deg

Note(s):

1. Calibration and measurements are made using diffused light.
2. Each channel is tested with GAIN = 16x, Integration Time (INT_T) = 166ms and VDD = VDD1 = VDD2 = 3.3V, T_{AMB}=25°C.
3. The accuracy of the channel counts/$\mu W/cm^2$ is ±12%.

Figure 19:
AS72653 Spectral Responsivity

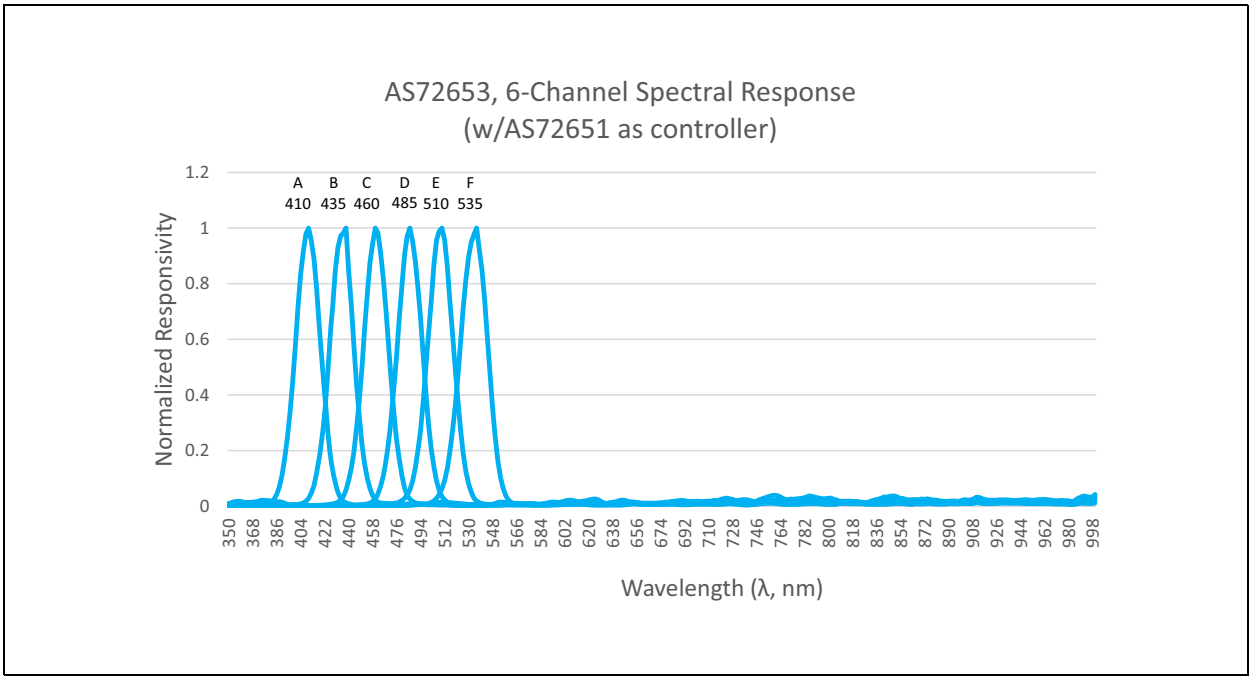


Figure 20:
Optical Characteristics of AS72653 (Pass Band)[1]

Symbol	Parameter	Conditions	Channel (nm)	Min	Typ	Max	Unit
A	Channel A	LED:[2] 395nm 415nm 428nm 5600K white	410		35[3]		counts/ ($\mu W/cm^2$)
B	Channel B		435		35[3]		counts/ ($\mu W/cm^2$)
C	Channel C		460		35[3]		counts/ ($\mu W/cm^2$)
D	Channel D		485		35[3]		counts/ ($\mu W/cm^2$)
E	Channel E		510		35[3]		counts/ ($\mu W/cm^2$)
F	Channel F		535		35[3]		counts/ ($\mu W/cm^2$)
FWHM	Full Width Half Max				20		nm
Wacc	Wavelength Accuracy			-10		+10	nm
dark	Dark Channel Counts	GAIN=64, T_{AMB}=25°C t_{int} = 165ms				5	counts
AFOV	Average Field of View				±20.5		deg

Note(s):

1. Calibration and measurements are made using diffused light.
2. Each channel is tested with GAIN = 16x, Integration Time (INT_T) = 166ms and VDD = VDD1 = VDD2 = 3.3V, T_{AMB}=25°C.
3. The accuracy of the channel counts/$\mu W/cm^2$ is ±12%.

Detailed Description

AS7265x 18-Channel *Spectral_ID* Detector Overview

Each of the three AS7265x *Spectral_ID* devices are next-generation digital 6-channel spectral sensor devices. Each of the 6 channels has a Gaussian filter characteristic with a full width half maximum (FWHM) bandwidth of 20nm. The filters use an interference topology design providing high stability in terms of drift in time and temperature. The drifts are so small that it is undetectable in the measurement. The temperature drift of the device is largely determined by the drift of the sensor and the electronics. To compensate for the temperature drift in the application, every device of the AS7265x chipset includes an integrated temperature sensor.

Filter accuracy will be affected by the angle of incidence which itself is limited by integrated aperture and internal micro-lens structure. The aperture-limited average field of view is ±20.5° to deliver specified accuracy. All optical characteristics are optimized for using diffused light.

Each device contains an analog-to-digital converter (16-bit resolution ADC) which integrates the current from each channel's photodiode. Upon completion of the conversion cycle, the integrated result is transferred to the corresponding data registers. The transfers are double-buffered to ensure data integrity is maintained.

The external MCU interface control via I^2C registers or AT commands, transparently controls the AS72652 and/or AS72653.

A serial flash is a required operating companion for this device and enables factory calibration/normalization of the filters. Supported device types are noted in Ordering & Contact Information at the end of this document. Required operating code can be downloaded at download.ams.com.

Channel Data Conversion of the AS7265x Devices

All three of these 6 channel devices use conversion implemented via two photodiode banks in each device. Refer to Figure 21and Figure 22. Bank 1 consists of register data from 4 of the 6 photodiodes, with 2 registers zeroed and Bank 2 consists of data from a different set of 4 of the 6 photodiodes, with 2 different registers zeroed. Spectral conversion requires the integration time (IT in ms) set to complete. If both photodiode banks are required to complete the conversion, the 2^{nd} bank requires an additional IT ms. Minimum IT for a single bank conversion is 2.8 ms. If data is required from all 6 photodiodes then the device must perform 2 full conversions (2 x Integration Time).

This spectral data conversion process operates continuously, new data is available after each IT ms period.

The conversion process is controlled with BANK Mode settings in the AS72651 as follows:

BANK Mode 0 Registers:

AS72651 data will be in S, T, U & V registers (R & W will be zero)

AS72652 data will be in G, H, K & I registers (J & L will be zero)

AS72653 data will be in A, B, E & C registers (D & F will be zero)

BANK Mode 1 Registers:

AS72651 data will be in R, T, U & W registers (S & V will be zero)

AS72652 data will be in G, H, J & L registers (I & K will be zero)

AS72653 data will be in F, A, B & D registers (C & E will be zero)

BANK Mode 2 Registers:

AS72651 data will be in S, T, U, V, R & W registers

AS72652 data will be in G, H, K, I, J & L registers

AS72653 data will be in A, B, C, D, E & F registers

For BANK Mode 2, care should be taken to assure prompt interrupt servicing so integration values from both banks are all derived from the same spectral conversion cycle.

Figure 21:
AS7265x Photo Diode Arrays

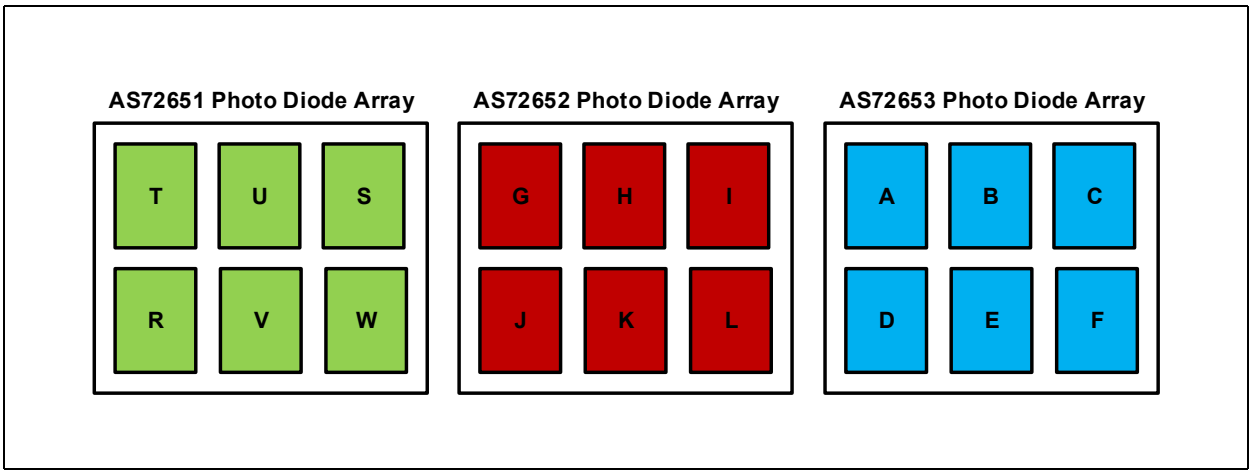
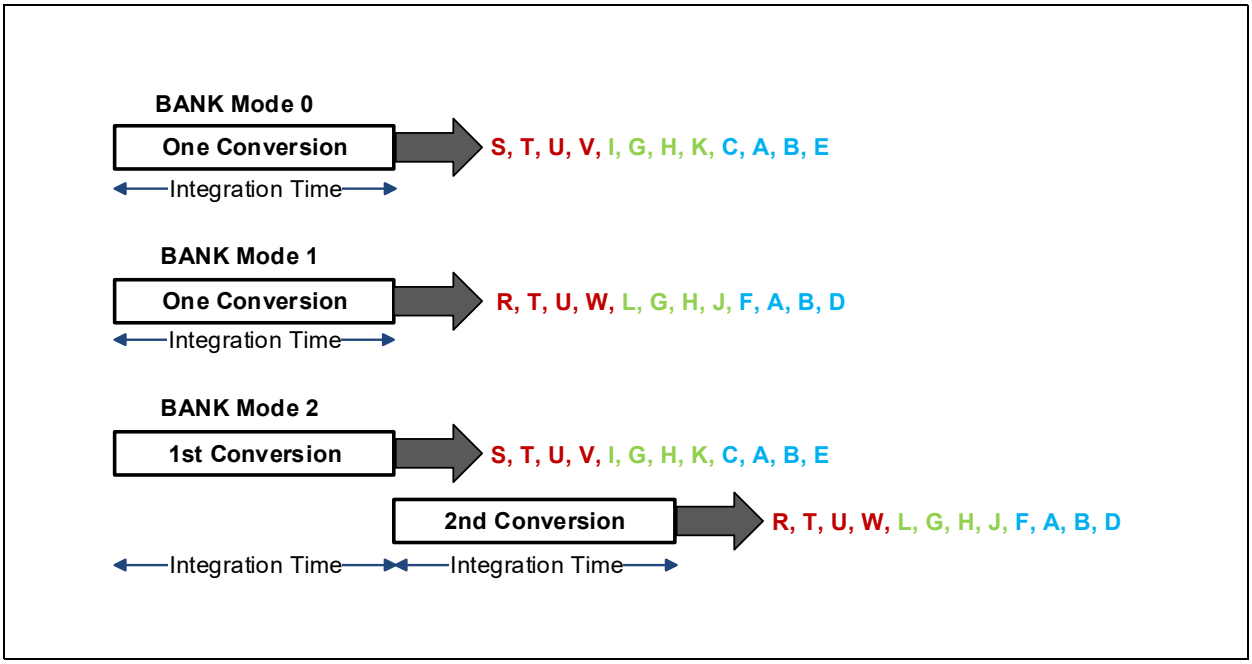


Figure 22:
Bank Mode and Data Conversion



RC Oscillator

The timing generation circuit consists of on-chip 16MHz, temperature compensated oscillators, which provide the individual master clocks of the AS7625x devices

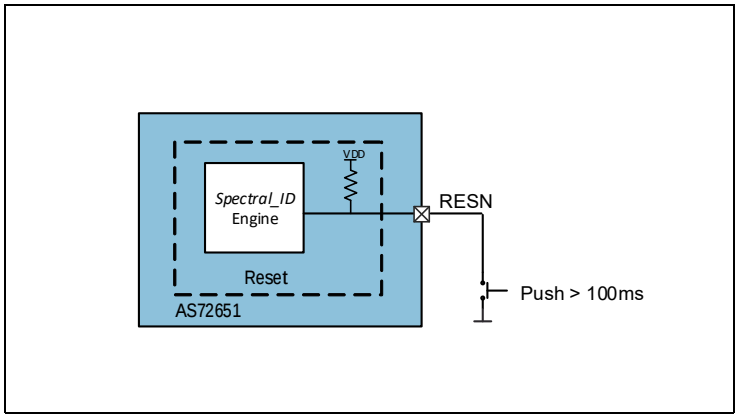
Temperature Sensor

The AS7265x internal temperature sensors are constantly measuring on-chip temperature to enable temperature compensation procedures, and can be read via I^2C registers or AT commands in the AS72651.

Reset

Pulling down the RESN pin for longer than 100ms resets the AS72651 which proceed to reset the AS72562 and the same RESN signal shown below can be used directly to reset the AS72653.

Figure 23:
Reset Circuit



AS7265x LED_IND Controls

There are LED_IND pins on all AS7265x devices. An LED connected to LED_IND can be used as a general power indicator and will automatically be used to indicate a Flash firmware update is occurring.

The LED_IND can then be setup as needed. Each AS7265x LED_IND source can be turned on/off via AT commands or I^2C register control, and LED_IND sink current is programmable to 1mA, 2mA, 4mA or 8mA. This LED_IND control can also be used in applications just like the LED_DRV control (described below), if the lower current sink of the LED_IND control is appropriate.

Electronic Shutter with AS7265x LED_DRV Driver Control

There are LED_DRV pins on all AS7265x devices. The LED_DRV pin can be used to control external LED sources as needed for sensor applications. LED_DRV can sink a programmable current of 12.5mA, 25mA, 50mA or 100mA. The control can be turned on/off via I^2C registers or AT commands, and as such it provides the AS7265x device with an electronic shutter.

Interrupt Operation

Interrupt operation is only needed for AS72651 as it transparently controls data collection from the AS72652 (if used) or AS72653 (if used).

If BANK is set in the AS72651 to Mode 0 or Mode 1, data is ready after the 1st integration time. If BANK is set to Mode 2, data is ready after two integration times.

For interrupt operation using I²C registers, if interrupts are enabled and data is ready, the INT pin is set low and DATA_RDY is set to 1. Reading the raw or calibration data releases (returns high) the interrupt. For multi-byte sensor data (2 or 4 bytes), after the 1st byte is read the remaining bytes are shadow protected in case an integration cycle completes just after the 1st byte is read. The sensors continue to gather information at the rate of the integration time, hence if the sensor registers are not read when the interrupt line goes low, it will stay low and the next cycle's sensor data will be available in the registers at the end of the next integration cycle.

For interrupt operation using AT Commands, if interrupts are enabled and data is ready the INT pin is set low and is released (returns high) after any sensor data is read.

Required Flash Memory

Serial flash is a required operating companion for this device, and enables the I²C and UART interfaces, as well as enabling calibrated data results. Supported device types are noted in Ordering & Contact Information at the end of this document. Required operating code can be downloaded at download.ams.com.

I²C Slave Interface

If selected by the I2C_ENB pin setting, interface and control can be accomplished through an I²C compatible slave interface to a set of registers that provide access to device control functions and output data. These registers on the AS72651 are, in reality, implemented as *virtual* registers in software. The actual I²C slave hardware registers number only three and are described in the table below. The steps necessary to access the virtual registers defined in the following are explained in pseudocode for external I²C master writes and reads below.

I²C Feature List

- Fast mode (400kHz).
- 7+1-bit addressing mode.
- Write format: Byte.
- Read format: Byte.
- SDA input delay and SCL spike filtering by integrated RC-components.

Figure 24:
I²C Slave Device Address and Physical Registers

Entity	Description	Note
Device Slave Address	8-bit slave address	Byte = 1001001x (device address = 49 hex) • x= 1 for Master Read (byte = 93 hex) • x= 0 for Master Write (byte = 92 hex)
STATUS Register	I²C slave interface STATUS register. Read-only.	Register Address = 0x00 Bit 1: TX_VALID • 0 - New data may be written to WRITE register • 1 -WRITE register occupied. Do NOT write. Bit 0: RX_VALID • 0 -No data is ready to be read in READ register. • 1 -Data byte available in READ register.
WRITE Register	I²C slave interface WRITE register. Write-only.	Register Address = 0x01 • 8-Bits of data written by the I²C Master intended for receipt by the I²C slave. Used for both *virtual* register addresses and write data.
READ Register	I²C slave interface READ register. Read-only.	Register Address = 0x02 • 8-Bits of data to be read by the I²C Master.

I²C Virtual Register Write Access

I²C Virtual Resister Byte Write, detailed below, shows the pseudocode necessary to write virtual registers on the AS72651. Note that, because the actual registers of interest are realized as virtual registers, a means of indicating whether there is a pending read or write operation of a given virtual register is needed. To convey this information, the most significant bit of the virtual register address is used as a marker. If it is 1, then a write is pending, otherwise the slave is expecting a virtual read operation. The pseudocode illustrates the proper technique for polling of the I²C slave status register to ensure the slave is ready for each transaction.

I²C Virtual Register Byte Write

Pseudocode

Poll I²C slave STATUS register;

If TX_VALID bit is 0, a write can be performed on the interface;

Send a virtual register address and set the MSB of the register address to 1 to indicate the pending write;

Poll I²C slave STATUS register;

If TX_VALID bit is 0, the virtual register address for the write has been received and the data may now be written;

Write the data.

Sample Code:

```
#define I2C_AS72XX_SLAVE_STATUS_REG     0x00
#define I2C_AS72XX_SLAVE_WRITE_REG      0x01
#define I2C_AS72XX_SLAVE_READ_REG       0x02
#define I2C_AS72XX_SLAVE_TX_VALID       0x02
#define I2C_AS72XX_SLAVE_RX_VALID       0x01

void i2cm_AS72xx_write(uint8_t virtualReg, uint8_t d)
{
        volatile uint8_tstatus;

        while (1)
        {
                // Read slave I2C status to see if the write buffer is ready.
                status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG);

                if ((status & I2C_AS72XX_SLAVE_TX_VALID) == 0)
                        // No inbound TX pending at slave.  Okay to write now.
                        break ;
        }
        // Send the virtual register address (enabling bit 7 to indicate a write).
        i2cm_write(I2C_AS72XX_SLAVE_WRITE_REG, (virtualReg | 0x80)) ;

        while (1)
        {
                // Read the slave I2C status to see if the write buffer is ready.
                status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG) ;

                if ((status & I2C_AS72XX_SLAVE_TX_VALID) == 0)
                        // No inbound TX pending at slave.  Okay to write data now.
                        break ;
        }
        // Send the data to complete the operation.
        i2cm_write(I2C_AS72XX_SLAVE_WRITE_REG, d) ;
}
```

I²C Virtual Register Read access

I²C Virtual Register Byte Read, detailed below, shows the pseudocode necessary to read virtual registers on the AS72651. Note that in this case, reading a virtual register, the register address is not modified.

I²C Virtual Register Byte Read

Pseudocode

```
Poll I²C slave STATUS register;
If TX_VALID bit is 0, the virtual register address for the read may be written;
Send a virtual register address;
Poll I²C slave STATUS register;
If RX_VALID bit is 1, the read data is ready;
Read the data.
```

Sample Code

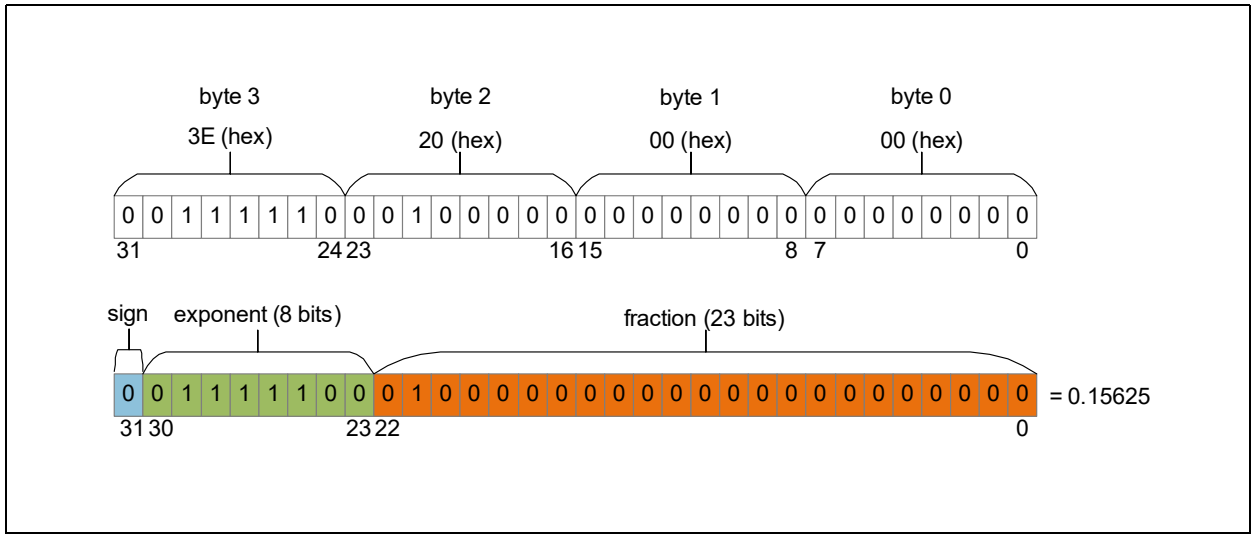
```
uint8_t i2cm_AS72xx_read(uint8_t virtualReg)
{
	volatile uint8_t status, d;

	while (1)
	{
		// Read slave I²C status to see if the read buffer is ready.
		status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG) ;

		if ((status & I2C_AS72XX_SLAVE_TX_VALID) == 0)
			// No inbound TX pending at slave. Okay to write now.
			break;
	}
	// Send the virtual register address (disabling bit 7 to indicate a read).
	i2cm_write(I2C_AS72XX_SLAVE_WRITE_REG, virtualReg);

	while (1)
	{
		// Read the slave I²C status to see if our read data is available.
		status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG);

		if ((status & I2C_AS72XX_SLAVE_RX_VALID)!= 0)
			// Read data is ready.
			break;
	}
	// Read the data to complete the operation.
	d = i2cm_read(I2C_AS72XX_SLAVE_READ_REG) ;
	return d;s
}
```

The details of the i2cm_read() and i2cm_write() functions in previous figures are dependent upon the nature and implementation of the external I²C master device.

4-Byte Floating-Point (FP) Registers

Several 4 byte registers (hex) are used by the AS72651. Here is an example of how these registers are used to represent floating point data (based on the IEEE 754 standard).

Figure 25:
Example of the IEEE 754 Standard



The floating point (FP) value assumed by 32 bit **binary32 data** with a biased exponent **e** (the 8 bit unsigned integer) and a **23 bit fraction** is (for the above example):

(EQ1)

$$FPvalue = (-1)^{sign} \cdot \left(1 + \sum_{i-1}^{23} b_{23-i} \cdot 2^{-i}\right) \cdot 2^{(e-127)}$$

$$FPvalue = (-1)^{0} \cdot \left(1 + \sum_{i-1}^{23} b_{23-i} \cdot 2^{-i}\right) \cdot 2^{(124-127)}$$

$$FPvalue = 1 \cdot (1 + 2^{-2}) \cdot 2^{-3} = 0.15625$$

I²C Virtual Register Set

The figure below provides a summary of the AS72651 I²C register set for the AS72651 which serves as the master interface of the 3 device AS7265x set. Figures after that provide additional register details. All register data is hex, and all multi-byte entities are Big Endian (most significant byte is situated at the lowest register address).

Multiple byte registers (2 byte integer, or, 4 byte floating point) must be read in the order of ascending register addresses (low to high) and if capable of being written to, must also be written in the order ascending register addresses.

Figure 26:
AS72651 I²C Master Device Virtual Register Set Overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x00	HW Version	HW Version H							
0x01		HW Version L							
0x02	FW Version	FW Version H							
0x03		FW Version L							
0x04	Configuration	SRST	INT		GAIN	BANK	DATA_RDY		FRST
0x05	Integration Time	Integration Time							
0x06	Temperature	Temperature							
0x07	LED Configuration	READ_ERR		LED_DRV		ENA-BLELED_DRV	LED_INT		ENABLE LED_INT
0x08	RAW value R, G, A	RAW value H							
0x09	RAW value R, G, A	RAW value L							
0x0A	RAW value S, H, B	RAW value H							
0x0B	RAW value S, H, B	RAW value L							
0x0C	RAW value T, I, C	RAW value H							
0x0D	RAW value T, I, C	RAW value L							
0x0E	RAW value U, J, D	RAW value H							
0x0F	RAW value U, J, D	RAW value L							
0x10	RAW value V, K, E	RAW value H							
0x11	RAW value V, K, E	RAW value L							
0x12	RAW value W, L, F	RAW value H							
0x13	RAW value W, L, F	RAW value L							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x14	Calibrated value channel R, G, A	CAL CHAN0_0							
0x15	Calibrated value channel R, G, A	CAL CHAN0_1							
0x16	Calibrated value channel R, G, A	CAL CHAN0_2							
0x17	Calibrated value channel R, G, A	CAL CHAN0_3							
0x18	Calibrated value channel S, H, B	CAL CHAN0_0							
0x19	Calibrated value channel S, H, B	CAL CHAN0_1							
0x1A	Calibrated value channel S, H, B	CAL CHAN0_2							
0x1B	Calibrated value channel S, H, B	CAL CHAN0_3							
0x1C	Calibrated value channel T, I, C	CAL CHAN0_0							
0x1D	Calibrated value channel T, I, C	CAL CHAN0_1							
0x1E	Calibrated value channel T, I, C	CAL CHAN0_2							
0x1F	Calibrated value channel T, I, C	CAL CHAN0_3							
0x20	Calibrated value channel U, J, D	CAL CHAN0_0							
0x21	Calibrated value channel U, J, D	CAL CHAN0_1							
0x22	Calibrated value channel U, J, D	CAL CHAN0_2							
0x23	Calibrated value channel U, J, D	CAL CHAN0_3							
0x24	Calibrated value channel V, K, E	CAL CHAN0_0							
0x25	Calibrated value channel V, K, E	CAL CHAN0_1							
0x26	Calibrated value channel V, K, E	CAL CHAN0_2							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x27	Calibrated value channel V, K, E	CAL CHAN0_3							
0x28	Calibrated value channel W, L, F	CAL CHAN0_0							
0x29	Calibrated value channel W, L, F	CAL CHAN0_1							
0x2A	Calibrated value channel W, L, F	CAL CHAN0_2							
0x2B	Calibrated value channel W, L, F	CAL CHAN0_3							
0x48	FW control	START	STOP	BYTES_ TRANSF ERRED	LOCK	SWITC H	BANK1	ERROR	CHKSU M
0x49	FW byte count	FW_BYTE_COUNT_H							
0x4A	FW byte count	FW_BYTE_COUNT_L							
0x4B	FW payload	HW version H							
0x4F	DEV SEL			Second Slave	First Slave			SELECT DATA	
0x50	COEF DATA	COEF_DATA_0							
0x51	COEF DATA	COEF_DATA_1							
0x52	COEF DATA	COEF_DATA_2							
0x53	COEF DATA	COEF_DATA_3							
0x54	COEF READ	COEF_READ							
0x55	COEF WRITE	COEF_WRITE							

Detailed Register Descriptions

Figure 27:
HW Version Registers

Addr: 0x00,0x01		HW Version		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
15:8	HW version H	0x40	R	Device type
7:0	HW version L	0x41	R	HW version

Figure 28:
FW Version Registers

Addr: 0x02,0x03		FW Version		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
15:8	FW version H	0	R/W	Set register 0x02, 0x03 to 0x01 to 0x03 to get each firmware positions high byte 0x01: MAJOR version [15..8] 0x02: PATCH version [15..8] 0x03: BUILD version [15..8]
7:0	FW version L	0	R/W	

Figure 29:
Configuration Register

Addr: 0x04		Configuration		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	SRST	0	W	[W] software reset [R] gain error
6	INT	0	R/W	Enable interrupt pin
5:4	GAIN	01	R/W	Gain configuration: b00=1x; b01=3.7x; b10=16x; b11=64x
3:2	BANK	10	R/W	Measurement mode: b00=Mode 0: 4 channels b01=Mode 1: 4 channels b10=Mode 2: All 6 channels b11=Mode 3: One-Shot operation of mode 2
1	DATA_RDY	0	R	Data ready to read
0	FRST	0	W	Factory reset

The maximum sensitivity value depends on the integration time. For every 2.78ms of integration time, the maximum sensitivity value increases by 1024 counts. This means that to be able to reach the full sensitivity scale, the sensitivity has to be at least 64*2.78ms.

Figure 30:
Integration Time Register

<table>
<tr><th colspan="2">Addr: 0x05</th><th colspan="6">Integration Time</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="4">Bit Description</th></tr>
<tr><td rowspan="9">7:0</td><td rowspan="9">INTEGRATION_ TIME</td><td rowspan="9">20</td><td rowspan="9">R/W</td><td colspan="4">Integration time = <value> * 2.8ms (applies to all channels); value: 1-255;Return 0 - read error</td></tr>
<tr><td>Value</td><td>Integration Cycles</td><td>Integration Time</td><td>Maximum ADC Value</td></tr>
<tr><td>0x00</td><td>1</td><td>2.78ms</td><td>1023</td></tr>
<tr><td>0x01</td><td>2</td><td>5.56ms</td><td>2047</td></tr>
<tr><td>...</td><td>...</td><td>...</td><td>...</td></tr>
<tr><td>0x11</td><td>18</td><td>50ms</td><td>18431</td></tr>
<tr><td>0x40</td><td>65</td><td>181ms</td><td>65535</td></tr>
<tr><td>...</td><td>...</td><td>...</td><td>...</td></tr>
<tr><td>0xFF</td><td>256</td><td>711ms</td><td>65535</td></tr>
</table>

Figure 31:
Temperature Register

Addr: 0x06		Temperature		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Temperature	-	R	Temperature of the device in °C Read value from every device in dependency of register DEV_SEL From -127 to 127 Return -128: Means error

Figure 32:
LED Configuration Register

Addr: 0x07		LED Configuration		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	READ_ERR	0	R	Error while reading status
5:4	LED_DRV	00	R/W	LED_DRV current limit: b00=12.5mA; b01=25mA; b10=50mA; b11=100mA Device depends on register DEV_SEL
3	ENABLE LED_ DRV	0	R/W	Enable LED DRV Device depends on register DEV_SEL
2:1	LED_INT	01	R/W	Current limit: b00=1mA; b01=2mA; b10=4mA; b11=8mA Device depends on register DEV_SEL
0	ENABLE LED_ INT	0	R/W	Enable LED IND Device depends on register DEV_SEL

Figure 33:
RAW Value Channel R,G,A Register

Addr: 0x08,0x09		RAW Value Channel R,G,A		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
15:8	RAW value H	-	R	Channel R or J or D depends on register DEV_SEL
7:0	Raw value L	-	R	

Figure 34:
RAW Value Channel S,H,B Register

Addr: 0x0A,0x0B		RAW Value Channel S,H,B		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
15:8	RAW value H	-	R	Channel S or I or C depends on register DEV_SEL
7:0	Raw value L	-	R	

Figure 35:
RAW Value Channel T,I,C Register

Addr: 0x0C/0x0D		RAW Value Channel T,I,C		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
15:8	RAW value H	-	R	Channel T or G or A depends on register DEV_SEL
7:0	Raw value L	-	R	

Figure 36:
RAW Value Channel U,J,D Register

Addr: 0x0E,0x0F		RAW Value Channel U,J,D		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
15:8	RAW value H	-	R	Channel U or H or B depends on register DEV_SEL
7:0	Raw value L	-	R	

Figure 37:
RAW Value Channel V,K,E Register

Addr: 0x10,0x011		RAW Value Channel V,K,E		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
15:8	RAW value H	-	R	Channel V or K or E depends on register DEV_SEL
7:0	Raw value L	-	R	

Figure 38:
RAW Value Channel W,L,F Register

Addr: 0x12,0x013		RAW Value Channel W,L,F		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
15:8	RAW value H	-	R	Channel W or L or F depends on register DEV_SEL
7:0	Raw value L	-	R	

Figure 39:
Calibrated Value Channel R,G,A Register

Addr: 0x17,0x016,0x15,0x014		Calibrated Value Channel R,G,A		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:24	CAL CHAN0_3	FF	R	Channel R or J or D depends on register DEV_SEL
23:16	CAL CHAN0_2	FF	R	
15:8	CAL CHAN0_1	FF	R	
7:0	CAL CHAN0_0	FF	R	

Figure 40:
Calibrated Value Channel S, H, B Register

Addr: 0x1B,0x01A,0x19,0x018		Calibrated Value Channel S,H,B		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:24	CAL CHAN1_3	FF	R	Channel S or I or C depends on register DEV_SEL
23:16	CAL CHAN1_2	FF	R	
15:8	CAL CHAN1_1	FF	R	
7:0	CAL CHAN1_0	FF	R	

Figure 41:
Calibrated Value Channel T, I, C Register

Addr: 0x1F,0x01E,0x1D,0x01C		Calibrated Value Channel T,I,C		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:24	CAL CHAN2_3	FF	R	Channel T or G or A depends on register DEV_SEL
23:16	CAL CHAN2_2	FF	R	
15:8	CAL CHAN2_1	FF	R	
7:0	CAL CHAN2_0	FF	R	

Figure 42:
Calibrated Value Channel U, J, D Register

Addr: 0x23,0x022,0x21,0x20		Calibrated Value Channel U,J,D		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:24	CAL CHAN3_3	FF	R	Channel U or H or B depends on register DEV_SEL
23:16	CAL CHAN3_2	FF	R	
15:8	CAL CHAN3_1	FF	R	
7:0	CAL CHAN3_0	FF	R	

Figure 43:
Calibrated Value Channel V, K, E Register

Addr: 0x27,0x026,0x25,0x24		Calibrated Value Channel V,K,E		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:24	CAL CHAN4_3	FF	R	Channel V or K or E depends on register DEV_SEL
23:16	CAL CHAN4_2	FF	R	
15:8	CAL CHAN4_1	FF	R	
7:0	CAL CHAN4_0	FF	R	

Figure 44:
Calibrated Value Channel W, L, F Register

Addr: 0x2B,0x02A,0x29,0x28		Calibrated Value Channel W,L,F		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:24	CAL CHAN5_3	FF	R	Channel W or L or F depends on register DEV_SEL
23:16	CAL CHAN5_2	FF	R	
15:8	CAL CHAN5_1	FF	R	
7:0	CAL CHAN5_0	FF	R	

Figure 45:
FW Control Register

Addr: 0x48		FW Control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	START		R/W	Set bit once to configure the device update
6	STOP		W	Reset firmware update state machine
5	BYTES_ TRANSFERRED		R	All 56kbytes are transferred
4	LOCK		R/W	Lock this firmware for the next start
3	SWITCH		W	Switch between both firmware
2	BANK1		R	Set if bank 1 is active, else bank 2
1	ERROR		R	Error occurred while firmware update
0	CHKSUM		R	Checksum of other bank is valid

Figure 46:
FW Byte Count Register

Addr: 0x49,0x4A		FW Byte Count		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
15:8	FW_BYTE_ COUNT_H	0	R	Byte counter of transferred image
7:0	FW_BYTE_ COUNT_L		R	

Figure 47:
FW Payload Register

Addr:0x4B		FW Payload		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	HW version H	0	R/W	Transfer of firmware byte

Figure 48:
DEV SEL Register

Addr: 0x4F		DEV SEL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
5	SECOND SLAVE	0	R	Second slave Available
5	FIRST SLAVE	0	R	First slave available
1:0	SELECT DATA	00	R/W	0x00: Select master data 0x01: Select first slave data 0x02: Select second slave data

Figure 49:
COEF DATA Register

Addr: 0x53,0x52,0x51,0x50		COEF DATA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:24	COEF_DATA_3		R/W	Data heap to read and write calibration data
23:16	COEF_DATA_2		R/W	
15:8	COEF_DATA_1		R/W	
7:0	COEF_DATA_0		R/W	

Figure 50:
COEF READ Register

Addr:0x54		COEF READ		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	COEF_READ		R/W	Set sub addresses to read different calibration data from COEF_DATA register

Figure 51:
COEF WRITE Register

Addr:0x55		COEF WRITE		
Bit	Bit Name	Default	Access	Bit Description
7:0	COEF_WRITE		R/W	Set sub addresses to write different calibration data from COEF_DATA register to persistent memory

AS72651 I²C Firmware (FW) Update Procedure

- In the FW Update Control register set the Start_XFR bit to 1.
- Write 56k of data to the FW Download register starting with the first byte in the ams file, then proceed the end of the ams 56k file with consecutive writes.
- If desired read the FW Byte Count registers to see which byte is expected to be written next into the FW Download register.
- When the download file is completely written, confirm the action by using the FW Update Control register bit XFR_56k (should =1 if 56k has been downloaded).
- In the FW Update Control register, set the Toggle bit to 1 which will reboot the AS72651 with the new FW after checking the new FW for correct CRC. If the CRC is incorrect the toggle bit will not change and the new FW will not be used.

Figure 52:
Firmware Byte Count High Byte

Addr: 0x60/0xE0		Control_Setup		
Bit	Bit Name	Default	Access	Bit Description
7	Start_XFR	0	R/W	Set to 1 to start firmware update
6	Kill_XFR	0	R/W	Set to 1 to stop firmware update.
5	XFR_56K	0	R	Set to 1 when 56k bytes have been downloaded.
4	Reserved			Reserved, do not use.
3	Toggle	0	R/W	Set to 1 to toggle firmware image partition.
2:0	Reserved			Reserved, do not use.

Figure 53:
Firmware Byte Count, High Byte Register

Addr: 0x61/0xE1		Firmware Byte Count, High Byte		
Bit	Bit Name	Default	Access	Bit Description
7:0	FWBC_HIGH		R	Firmware byte address to be downloaded next, High Byte

Figure 54:
Firmware Byte Count, Low Byte Register

Addr: 0x62/0xE2		Firmware Byte Count, Low Byte		
Bit	Bit Name	Default	Access	Bit Description
7:0	FWBC_LOW		R	Firmware byte address to be downloaded next, Low Byte

Figure 55:
Firmware Download Register

Addr: 0x63/0xE3		Firmware Download		
Bit	Bit Name	Default	Access	Bit Description
7:0	FWLOAD		R/W	Firmware byte to be downloaded

UART Command Interface

If selected by the I2C_ENB pin setting, the UART module implements the TX and RX signals as defined in the RS-232 / V.24 standard communication protocol. Serial flash EPROM is a required operating companion device to enable the UART command interface.

Figure 56:
Flash Memory Overview

Serial Flash	Manufacturer
AT25SF041xx	Adesto Technologies
AT25DF041xx	Adesto Technologies
MX25L4006ExxI-12G	Macronix
SST25PF040C	Microchip Technology
W25X40CLSNIG	Winbond Electronics
LE25U40CMD	ON Semiconductor

Note(s):

1. Where xx= alternative packages.

UART Feature List

- Full duplex operation (independent serial receive and transmit registers).
- Factory set to 115.2k Baud
- Supports serial frames with 8 Data Bits, no Parity and 1 Stop Bit.

Operation

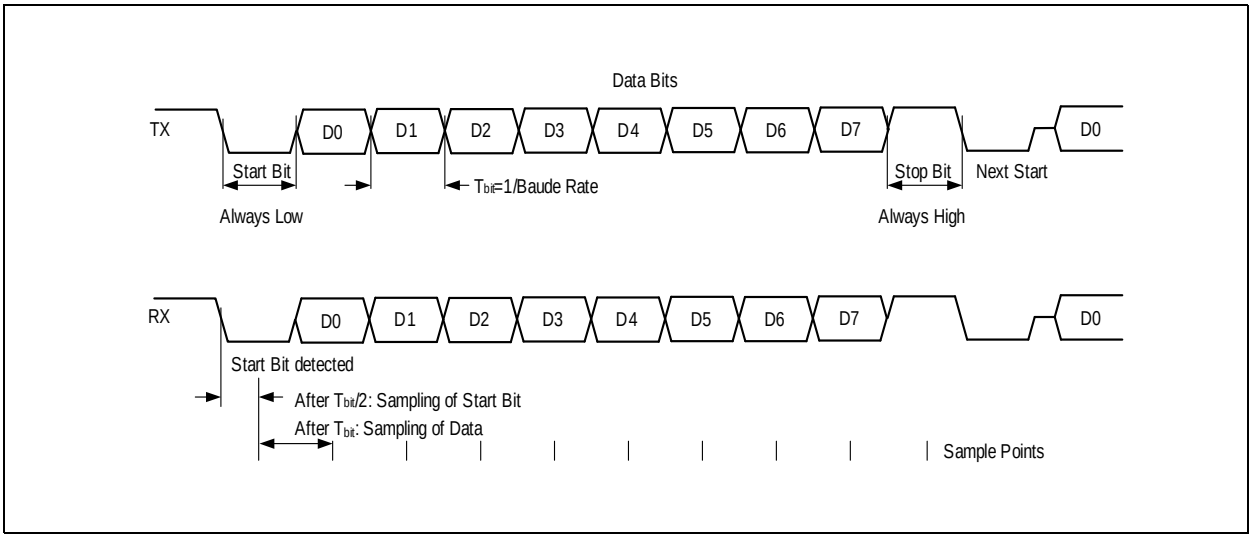
Transmission

If data is available in the transmit FIFO, it will be moved into the output shift register and the data will be transmitted at the configured Baud Rate, starting with a Start Bit (logic zero) and followed by a Stop Bit (logic one).

Reception

At any time, with the receiver being idle, if a falling edge of a start bit is detected on the input, a byte will be received and stored in the receive FIFO. The following Stop Bit will be checked to be logic one.

Figure 57:
UART Protocol



AT Command Interface

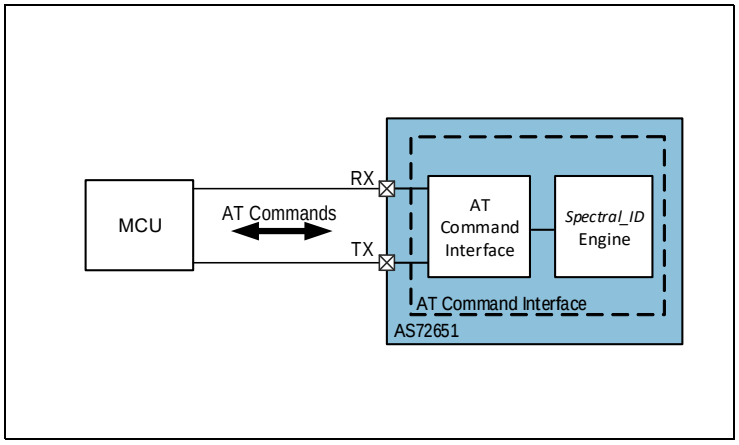
The microprocessor interface to control the AS72651 *Spectral_ID* sensor(s) is via AT Commands across the UART interface. The AS72651 provides a text-based serial command interface borrowed from the "AT Command" model used in early Hayes modems.

For example:

Read DATA value:	ATDATA →	<data>OK
Set the gain of the sensor to 1x:	ATGAIN=0→	OK

The AT Command Interface, shown below provides access to the *Spectral_ID* engine's control and configuration functions.

Figure 58:
AT Command Interface Block Diagram



In the AT Commands figure below, numeric values may be specified with no leading prefix, in which case they will be interpreted as decimals, or with a leading "0x" to indicate that they are hexadecimal numbers. The commands are loosely grouped into functional areas. Texts appearing between angle brackets ('<'and '>') are commands or response arguments. A carriage return character, a linefeed character, or both may terminate commands and responses. Note that any command that encounters an error will generate the "ERROR" response shown, for example, in the NOP command at the top of the first table, but has been omitted elsewhere in the interest of readability and clarity.

Note(s): The Figure 59 shows the complete list of all AS7265x AT commands.

Figure 59:
AS7265x AT Commands

Commands	Direction	Description	Format	Value Range	Default
Status					
AT	R	NOP	-	-	-
ATVERSW	R	Return the current software version number	DEC	<MAJOR.PATCH. BUILD>	-
ATVERHW	R	Returns the system hardware as a HEX value of the form PRDTx where P=PartID and R=ChipRevision and DT= DeviceType	HEX	<0xPRDT> PR = 40 DT = 15	0x4041
ATTEMP	R	Read the current device temperature in degrees Celsius	DEC	Send three temperature values (Format: A, B, C)	-
ATDATA	R	Read all six raw vales per device(<65535)	DEC	< R, S, T, U, V, W, G, H, I, J, K, L, A, B, C, D, E, F>	-
ATCDATA	R	Read all six calibrated values per device. Returns comma-separated 32-bit floating point values.	DEC	< R, S, T, U, V, W, G, H, I, J, K, L, A, B, C, D, E, F>	-

Commands	Direction	Description	Format	Value Range	Default
Control					
ATINTTIME	R/W	Set sensor integration time. Integration time = <value> * ~2.8ms.	DEC	1-255	20
ATGAIN	R/W	Set sensor gain: 0=1x gain, 1=3.7x, 2=16x, 3=64x	DEC	0-3	1
ATINTRP	R/W	Enable/Disable interrupt pin	DEC	0 - Disable 1 - Enable Interrupt pin functionality	0
ATTCSMD	R/W	Set measurement mode	DEC	0: Captures bank0 (1 integration period) 1: Captures bank1 (1 integration period) 2: Captures bank0+ bank1(2 integration period) 3:Captures bank0+ bank1 in one shot mode (2 integration period)	2
ATINTRVL	R/W	Set the sampling interval as an integer multiple of the integration time. The <value> is an integer between [1...255]. A sampling interval=1 implies a sampling rate of 1x the current integration time. A sampling interval=255 implies a slow sampling rate of 255 times the current integration time	DEC	1…255	1

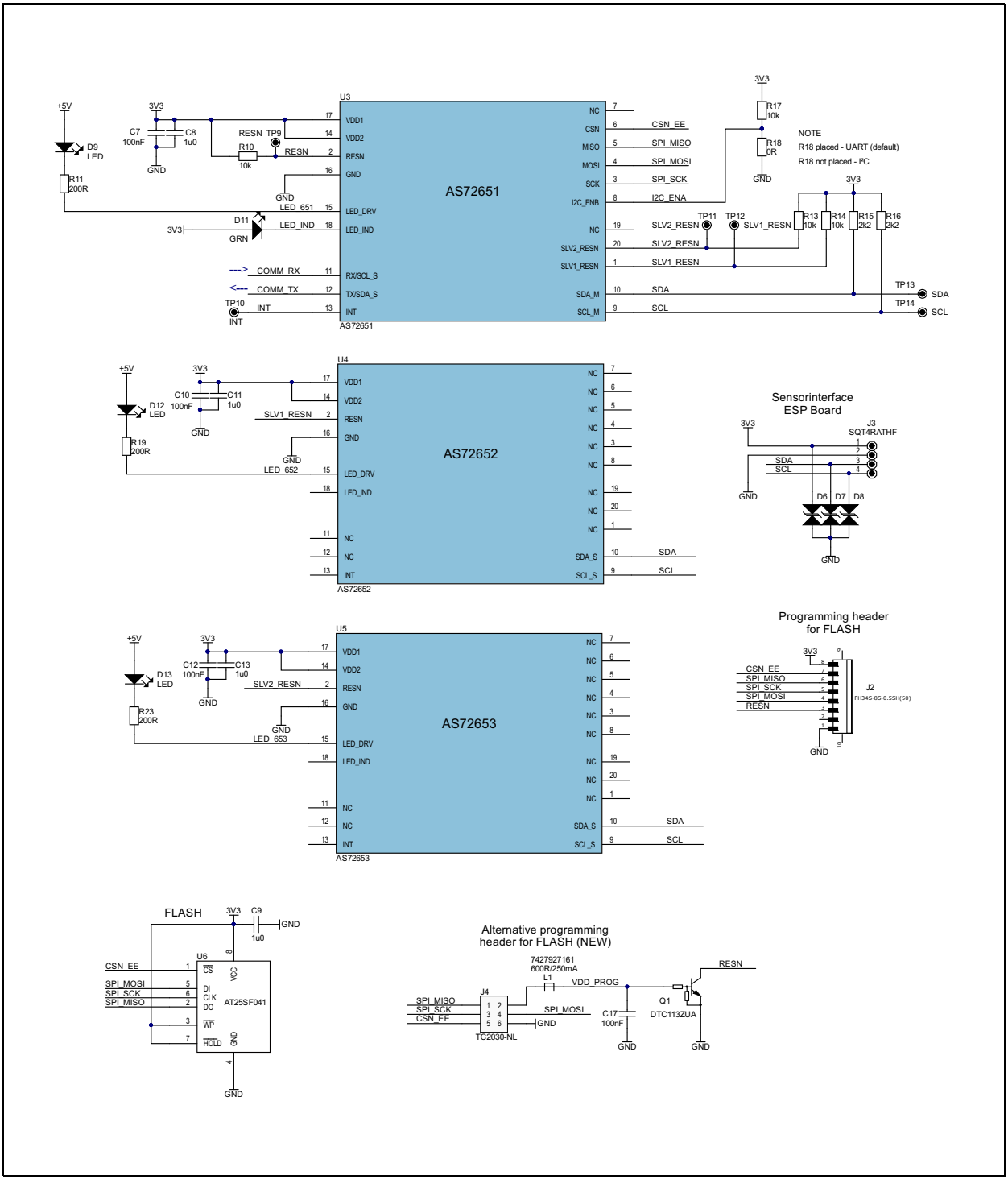
Commands	Direction	Description	Format	Value Range	Default
ATBURST	R/W	Sends a number of calibrated data without separate requests second parameter for the burst mode is optionally format: Send: ATBURST=10,0 or ATBURST=10 Read: ATBURST ≥ 10,0 OK	DEC	BURST NUMBER: 0 - Burst mode is deactivated 1-254 - Number of burst transfers 255 - Send unlimited bursts (stops with ATBURST=0) BURST MODE: 0 - Raw values (default, like ATDATA) 1 - Calibrated values (like ATCDATA)	0
ATLED0	R/W	Enables or disables the indication LED	DEC	0 - LED off 1 - LED on	1
ATLED1	R/W	Enables or disables the driver LED	DEC	0 - LED off 1 - LED on	0
ATLED2	R/W	Enables or disables the indication LED for first I^2C slave	DEC	0 - LED off 1 - LED on	1
ATLED3	R/W	Enables or disables the driver LED for first I^2C slave	DEC	0 - LED off 1 - LED on	0
ATLED4	R/W	Enables or disables the indication LED for second I^2C slave	DEC	0 - LED off 1 - LED on	1
ATLED5	R/W	Enables or disables the driver LED for second I^2C slave	DEC	0 - LED off 1 - LED on	0
ATLEDC	R/W	Sets LED_IND and LED_DRV current (for master only)	HEX	[1...0] LED_IND: b00=1mA; b01=2mA; b10=4mA; b11=8mA [5...4] LED_DRV: b00=12.5mA; b01=25mA; b10=50mA; b11=100mA	0x00

Commands	Direction	Description	Format	Value Range	Default
ATLEDD	R/W	Sets LED_IND and LED_DRV current for first I^2C slave	HEX	[1...0] LED_IND: b00=1mA; b01=2mA; b10=4mA; b11=8mA [5...4] LED_DRV: b00=12.5mA; b01=25mA; b10=50mA; b11=100mA	0x00
ATLEDE	R/W	Sets LED_IND and LED_DRV current for second I^2C slave	HEX	[1...0] LED_IND: b00=1mA; b01=2mA; b10=4mA; b11=8mA [5...4] LED_DRV: b00=12.5mA; b01=25mA; b10=50mA; b11=100mA	0x00
ATFRST	W	Factory Reset. Stored values are reset to 'Factory' defaults. Afterwards a software reset is started.	-	-	-
ATSRST	W	Software reset	-	-	-
Calibration Values					
ATSCLx	R/W	Read/Write scalar for the raw values (x=0...17)	DEC		p2ram value
Firmware Update					
ATFWU	W	Starts firmware update process and transfer the bin file checksum	-	-	-
ATFW	W	Download new firmware. Up to 7 bytes of FW image at a time (14 hex bytes with no leading or trailing 0x). Repeat command till all 56kBytes of firmware are downloaded	-	HEX STRING (without 0x), max. 7 bytes	-

Commands	Direction	Description	Format	Value Range	Default
ATFWS	W	Tests the checksum on the non-active FW partition and, if correct, switches active partition. This is a toggle and used to toggle between the 2 FW partitions. Note: The first 5 bytes in page 0 are not touched. It is only a temporary switch and must be used to check the new firmware whether the communication works!	-	-	-
ATFWL	W	This command locks the current firmware to starts on power cycles. It rewrites the first five bytes in page0!	-	-	-
ATFWC	R	This command gives information about the current firmware state	-	Bit0 - Checksum of non-active firmware OK Bit1 - Error occurred Bit2 - Bank 1 active Bit3 - Not used Bit4 - Current firmware is locked Bit5 - 56kBytes transferred Bit6 - Not used Bit7 - Firmware update active	-
ATFWA	W	Only for backward compatibility to support old firmware, update mechanism. Always returns with OK. Because of flash devices, it is not possible to increment the address separately (page erase necessary!)	-	-	-

Application Information

Figure 60:
Typical AS7265x 18-Channel Application Circuit

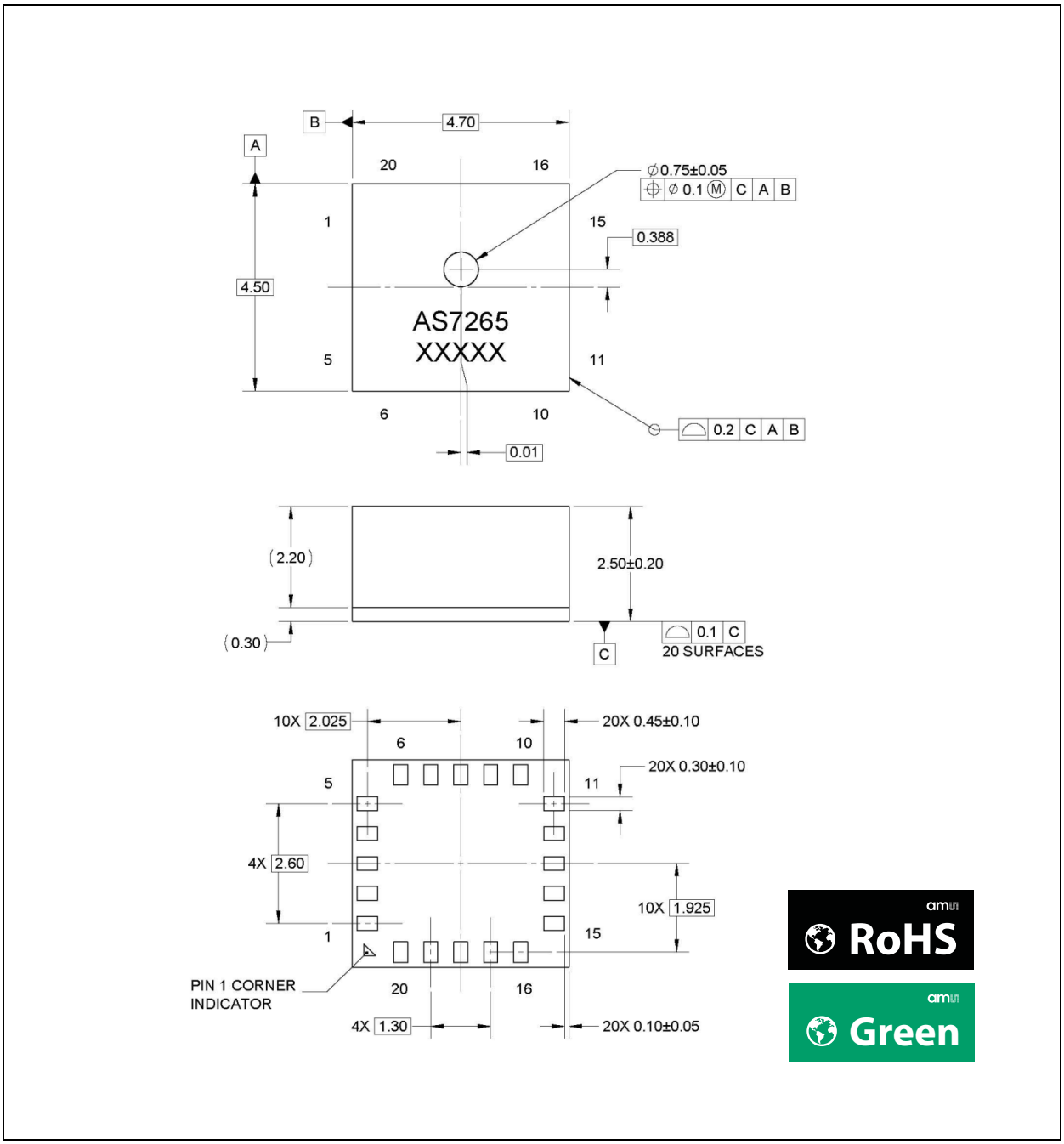


Note(s):

1. For each AS7265x device, orientation of the device aperture to any light source(s) will determine spectral content to be measured. For example with the proper orientation, sensors on the AS72651 can be used to measure light from the LEDs on the AS72652 and/or AS76253.
2. The AS72651 is required while the AS72652 and AS72653 are both optional for a total solution of 6, 12 or 18 channels.

Package Drawings & Markings

Figure 61:
Package Drawing



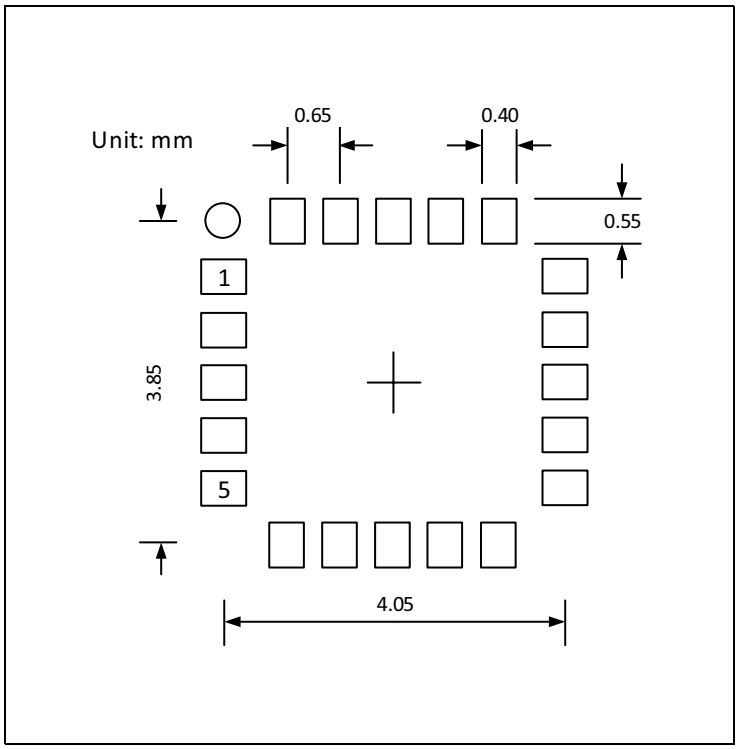
Note(s):

1. All dimensions are in millimeters.
2. XXXXX = tracecode.
3. Unless otherwise specified tolerances are: Angular (±.5°), Two Place Decimal (±.1), Three Place Decimal (±.05).
4. Contact finish is Au.
5. This package contains no lead (Pb).
6. This drawing is subject to change without notice.

PCB Pad Layout

Suggested PCB pad layout guidelines for the LGA device are shown. Flash Gold is recommended as a surface finish for the landing pads.

Figure 62:
Recommended PCB Pad Layout (Top View)

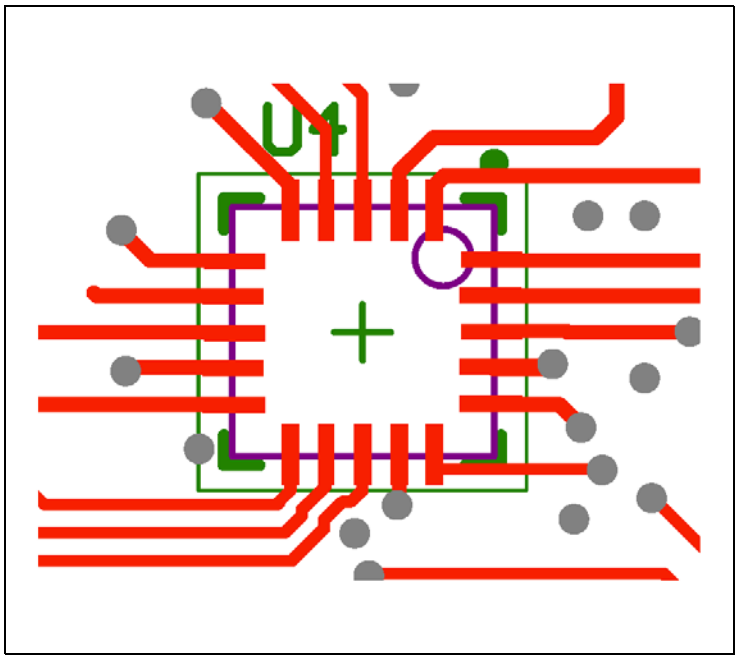


Note(s):

1. Unless otherwise specified, all dimensions are in millimeters.
2. Add 0.05mm all around the nominal lead width and length for the PCB pad land pattern.
3. This drawing is subject to change without notice.

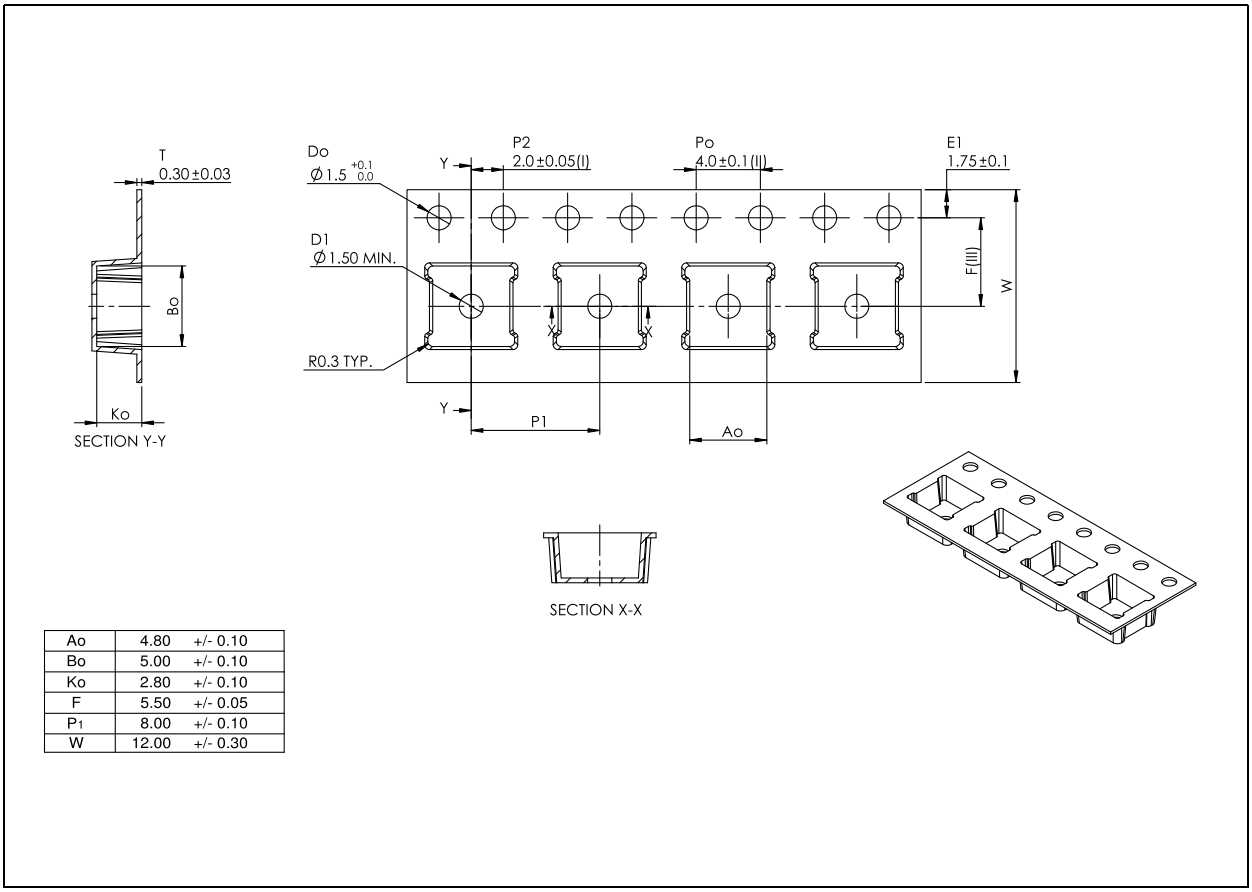
In order to prevent interference, avoid trace routing feedthroughs with exposure directly under the AS7265x devices. An example routing is illustrated in the Figure 63.

Figure 63:
Typical Layout Routing



Mechanical Data

Figure 64:
Tape & Reel Information



Ao	4.80	+/- 0.10
Bo	5.00	+/- 0.10
Ko	2.80	+/- 0.10
F	5.50	+/- 0.05
P_1	8.00	+/- 0.10
W	12.00	+/- 0.30

Note(s):

1. All dimensions in millimeters unless of otherwise stated.
2. Measured from centreline of sprocket hole to centreline of pocket.
3. Cumulative tolerance of 10 sprocket holes is ±0.20.
4. Measured from centreline of sprocket hole to centreline of pocket.
5. Other material available.

Soldering & Storage Information

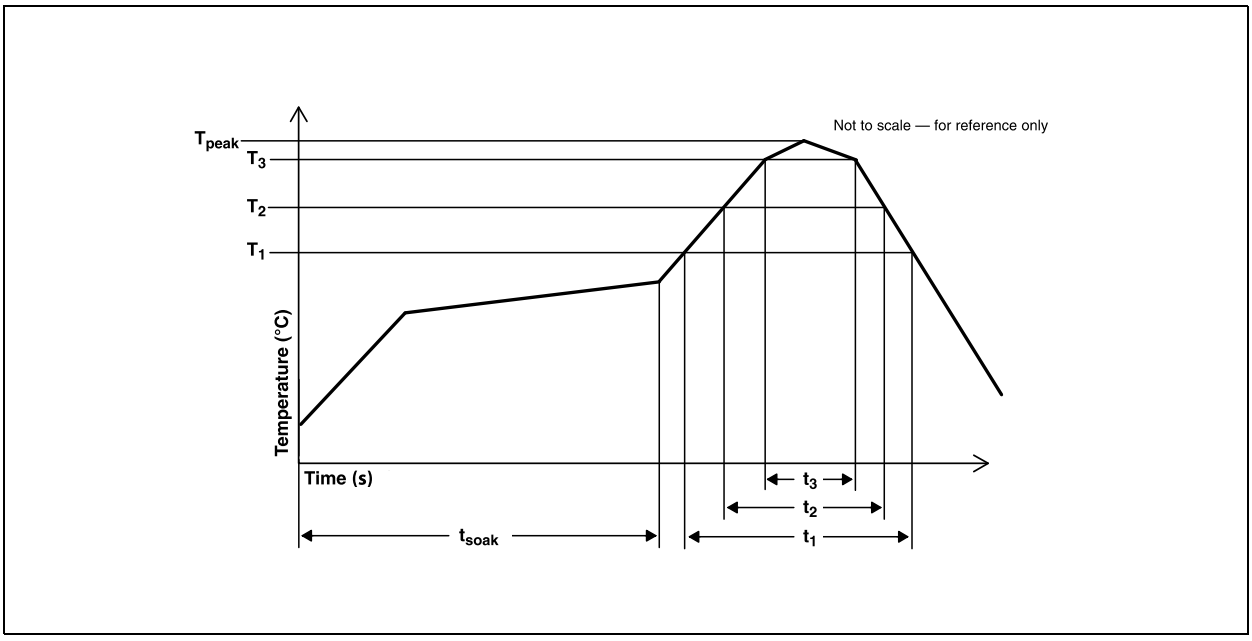
Soldering Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 65:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5°C/s
Soak time	t_{SOAK}	2 to 3 minutes
Time above 217°C(T_1)	t_1	Max 60s
Time above 230°C(T_2)	t_2	Max 50s
Time above T_{peak} - 10°C(T_3)	t_3	Max 10s
Peak temperature in reflow	T_{peak}	260°C
Temperature gradient in cooling		Max -5°C/s

Figure 66:
Solder Reflow Profile Graph



Manufacturing Process Considerations

The AS72651,AS72652 and AS72653 packages are compatible with standard reflow no-clean and cleaning processes including aqueous, solvent or ultrasonic techniques. However, as an open-aperture device, precautions must be taken to avoid particulate or solvent contamination as a result of any manufacturing processes, including pick and place, reflow, cleaning, integration assembly and/or testing. Temporary covering of the aperture is allowed. To avoid degradation of accuracy or performance in the end product, care should be taken that any temporary covering and associated sealants/debris are thoroughly removed prior to any optical testing or final packaging.

Storage Information

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping.

Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: <40°C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

Floor Life: 168 hours

Ambient Temperature: <30°C

Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

Ordering & Contact Information

Figure 67:
Ordering Information

Ordering Code	Package	Marking	Description	Delivery Form	Delivery Quantity
AS72651-BLGT	20-pin LGA	AS7265	Smart 6-Channel NIR Spectral_ID Sensor with Electronic Shutter and 18-Channel AS7265x Master Capability	Tape & Reel	2000 pcs/reel
AS72652-BLGT	20-pin LGA	AS7266	Smart 6-Channel NIR Spectral_ID Sensor with Electronic Shutter	Tape & Reel	2000 pcs/reel
AS72653-BLGT	20-pin LGA	AS7267	Smart 6-Channel Spectral_ID Sensor with Electronic Shutter	Tape & Reel	2000 pcs/reel

Note(s):

1. The AS72651 is required for operation of either the AS72652 or AS72653.
2. A companion flash memory is required for functionality and should be ordered from the flash memory supplier or their authorized channels. See approved flash memory manufacturers in Figure 56. For latest update of the flash memory list contact regional FAE support.
3. AS72651 flash memory software is available from **ams**.

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Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Updated text under Key Benefits & Features	1
Updated Figure 2 (AS7265x Chip- Set Block Diagram)	3
Renamed Figure 3 to “Pin Diagram of AS72651,AS72652 and AS72653 (Top View)”	4
Updated Figure 4 (AS72651 pin description)	4
Added Figure 5 (AS72652 and AS72653 pin description)	5
Updated text under “Absolute Maximum Ratings” (replaced AS72651 with AS7265x)	7
Updated titles names in Figure 6,8 to AS7265x	7,10
Updated title name in Figure 7 and notes under it	8
Updated text under Optical Characteristics	13
Moved Figure “AS7265x LGA Average Field of View” under “Optical Characteristics”	13
Updated Figure 14	13
Updated Figure 16	14
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Updated title name in figure 20 and notes under it	18
Updated text under AS7265x 18-Channel Spectral_ID Detector Overview	19
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Updated text under Interrupt Operation	22
Updated text under Required Flash Memory	23
Updated text under I^2C Feature List	23
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Updated text under Detailed Register Descriptions including Figure 27 to 51	31
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Updated text under Figure 58	43

Changes from 1-03 (2017-Oct-17) to current revision 1-04 (2018-Jul-09)	Page
Updated Figure 59 (AS7265x AT Commands) and text above it	43
Updated Figure 60 (Typical AS7265x 18-Channel Application Circuit)	48
Updated text under Manufacturing Process Considerations (replaced AS72651 with AS72651, AS72652,AS72653)	54
Updated note under Figure 67	56

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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