General Description

The AGM609S combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

This device is ideal for load switch and battery protection applications.

Features

- Advance high cell density Trench technology
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

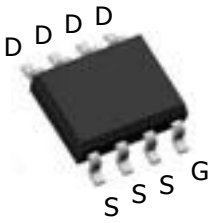
Application

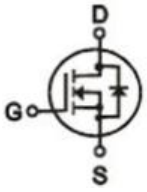
- MB/VGA Vcore
- SMPS 2nd Synchronous Rectifier
- POL application
- BLDC Motor driver

Product Summary

BVDSS	RDSON	ID
60V	7.2mΩ	14A

SOP8 Pin Configuration





Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
AGM609S	AGM609S	SOP8	330mm	12mm	3000

Table 1. Absolute Maximum Ratings (TA=25℃)

Symbol	Parameter	Value	Unit
VDS	Drain-Source Voltage (VGS=0V)	60	V
VGS	Gate-Source Voltage (VDS=0V)	±20	V
ID	Drain Current-Continuous(TA=25℃) **(Note 1)**	14	A
	Drain Current-Continuous(TA=100℃)	12	A
IDM (pluse)	Drain Current-Continuous@ Current-Pulsed **(Note 2)**	56	A
PD	Maximum Power Dissipation(TA=25℃)	2.5	w
	Maximum Power Dissipation(TA=100℃)	1.0	w
TJ,TSTG	Operating Junction and Storage Temperature Range	-55 To 150	℃

Table 2. Thermal Characteristic

Symbol	Parameter	Typ	Max	Unit
RθJA	Thermal Resistance Junction-ambient (Steady State)[1]	--	50	℃/W

Table 3. Electrical Characteristics (TA=25℃unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV_{DSS}	Drain-Source Breakdown Voltage	VGS=0V ID=250μA	60	--	--	V
IDSS	Zero Gate Voltage Drain Current	VDS=60V,VGS=0V	--	--	1	μA
IGSS	Gate-Body Leakage Current	VGS=±20V,VDS=0V	--	--	±100	nA
VGS(th)	Gate Threshold Voltage	VDS=VGS,ID=250μA	1.2	1.6	2.5	V
gFS	Forward Transconductance	VDS=25V,ID=8A	--	14	--	S
RDS(on)	Drain-Source On-State Resistance	VGS=10V, ID=12A	--	7.2	10	mΩ
		VGS=4.5V, ID=10A	--	9.5	15	mΩ
Dynamic Characteristics						
Ciss	Input Capacitance	VDS=20V,VGS=0V, F=1MHZ	--	1450	--	pF
Coss	Output Capacitance		--	280	--	pF
Crss	Reverse Transfer Capacitance		--	4.1	--	pF
Rg	Gate resistance	VGS=0V, VDS=0V,f=1.0MHz	--	1.7	--	Ω
Switching Times						
td(on)	Turn-on Delay Time	VGS=15V,VDS=30V, RL=0.75Ω,RGEN=3.3Ω	--	11	--	nS
tr	Turn-on Rise Time		--	50	--	nS
td(off)	Turn-Off Delay Time		--	56	--	nS
tf	Turn-Off Fall Time		--	12	--	nS
Qg	Total Gate Charge	VGS=10V, VDS=30V, ID=12A	--	23	--	nC
Qgs	Gate-Source Charge		--	48	--	nC
Qgd	Gate-Drain Charge		--	2.1	--	nC
Source-Drain Diode Characteristics						
ISD	Source-Drain Current(Body Diode)		--	--	14	A
VSD	Forward on Voltage	VGS=0V,IS=15A	--	--	1.2	V
trr	Reverse Recovery Time	IF=15A , dI/dt=100A/μs , TJ=25℃	--	--	32	ns
Qrr	Reverse Recovery Charge		--	--	46	nc

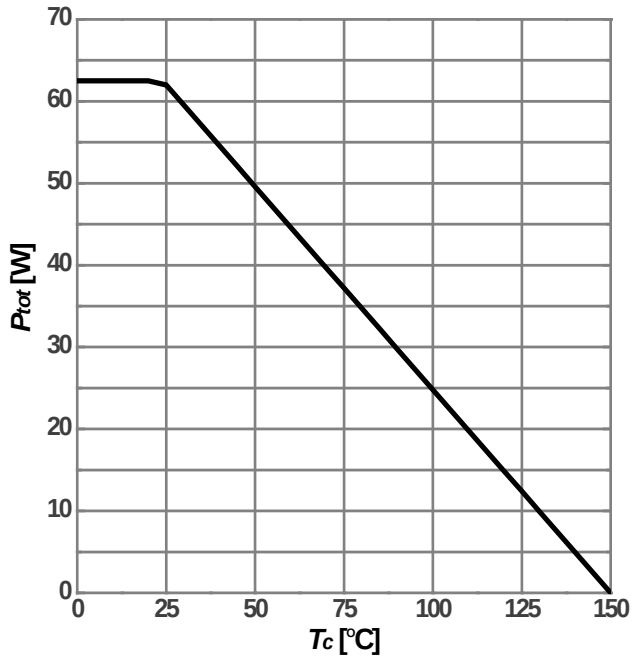
Notes 1.The maximum current rating is package limited.

Notes 2.Repetitive Rating: Pulse width limited by maximum junction temperature

Notes 3.EAS condition: TJ=25℃

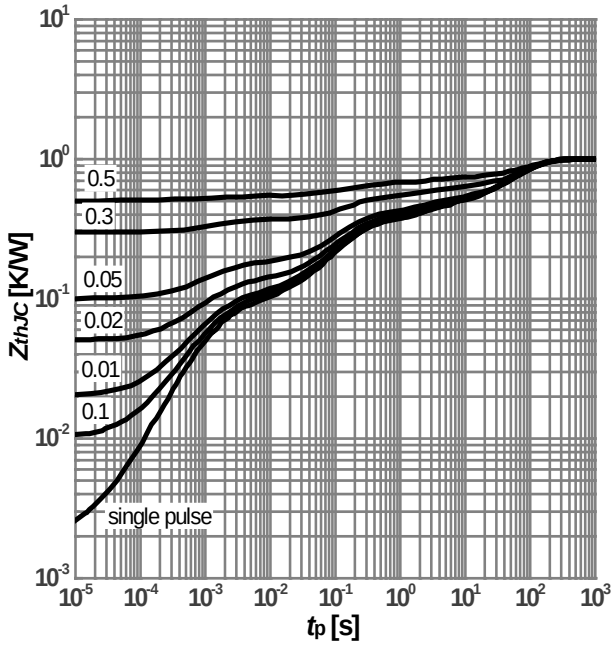
Electrical characteristics diagrams

Diagram 1: Power dissipation (SOP-8)



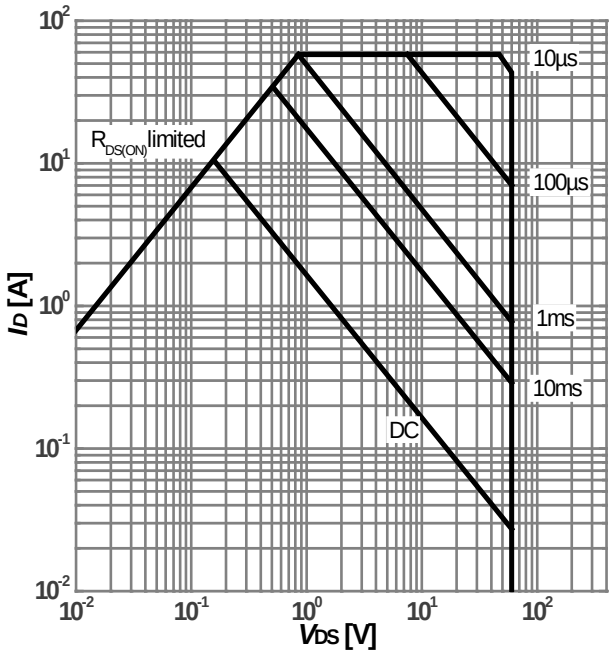
P_{tot}=f(T_C)

Diagram 2: Max. transient thermal impedance (SOP-8)



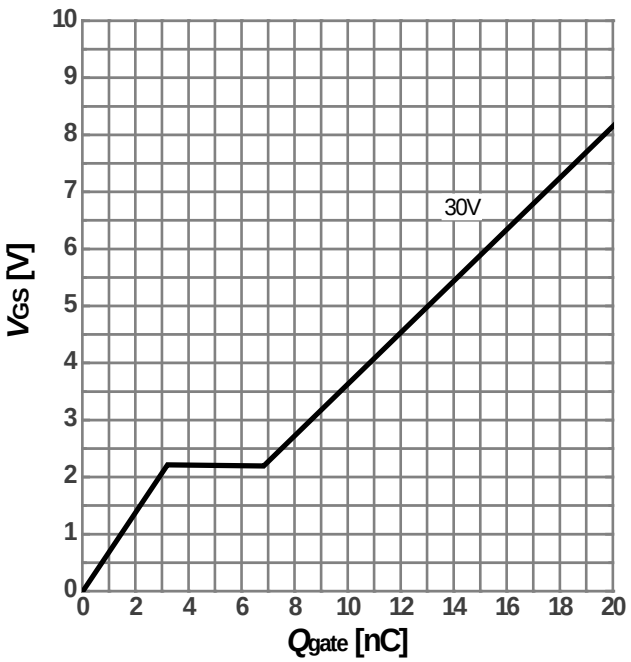
Z_{thJC}=f(t_p); parameter: D= t_p/T

Diagram 3: Safe operating area (SOP-8)



I_D=f(V_{DS}); Tj=25°C; D=0; parameter: t_p

Diagram 4: Typ. gate charge



V_{GS}=f(Q_{gate}); I_D=14.5A pulsed; V_{DS}=30V

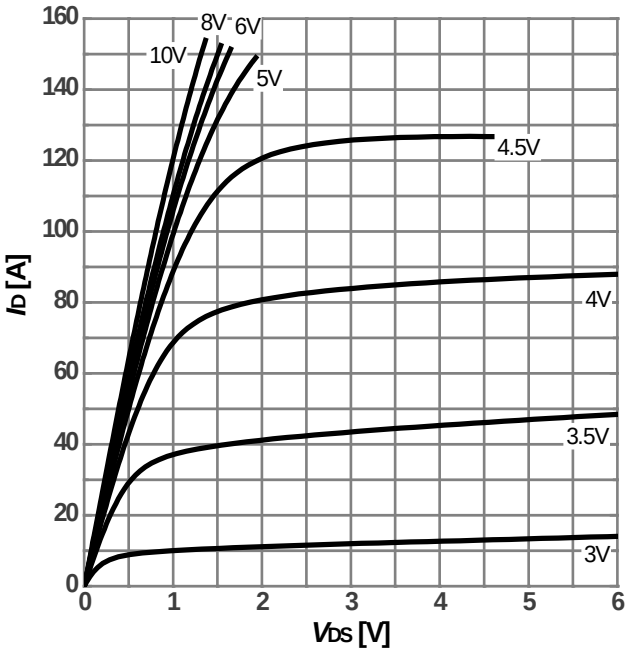
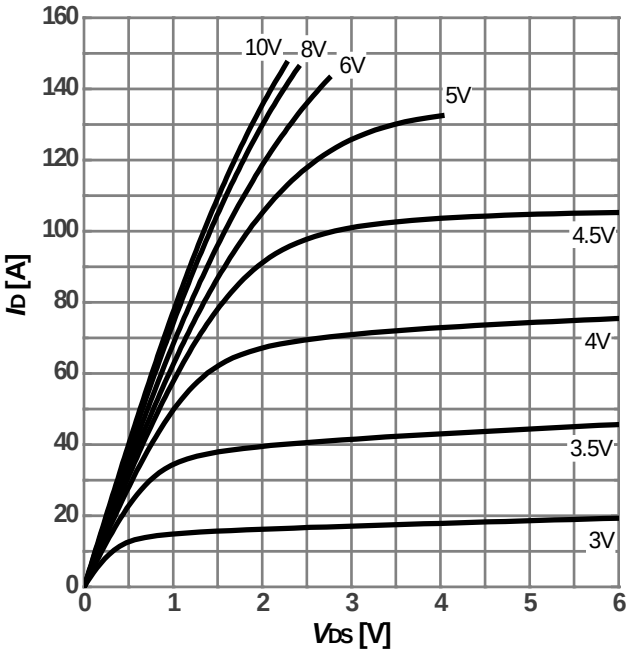
Diagram 5: Typ. output characteristics	Diagram 6: Typ. output characteristics
	
I_D=f(V_{DS}); Tj=25°C; parameter: V_{GS}	I_D=f(V_{DS}); Tj=125°C; parameter: V_{GS}

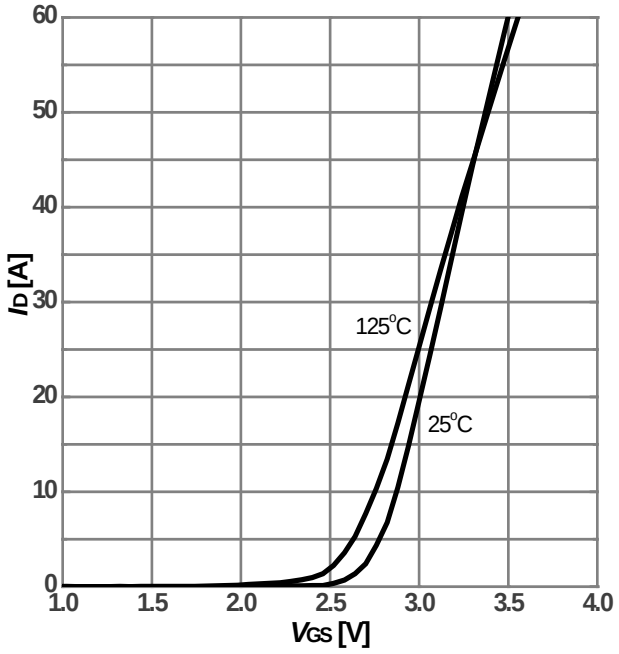
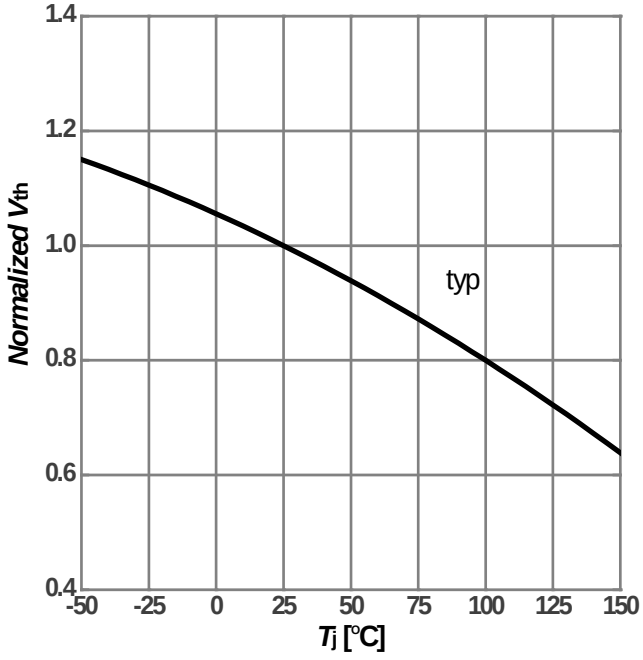
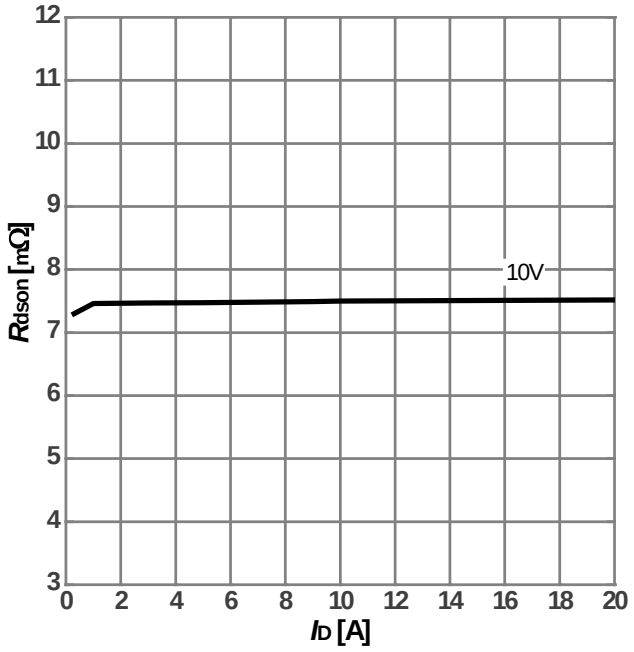
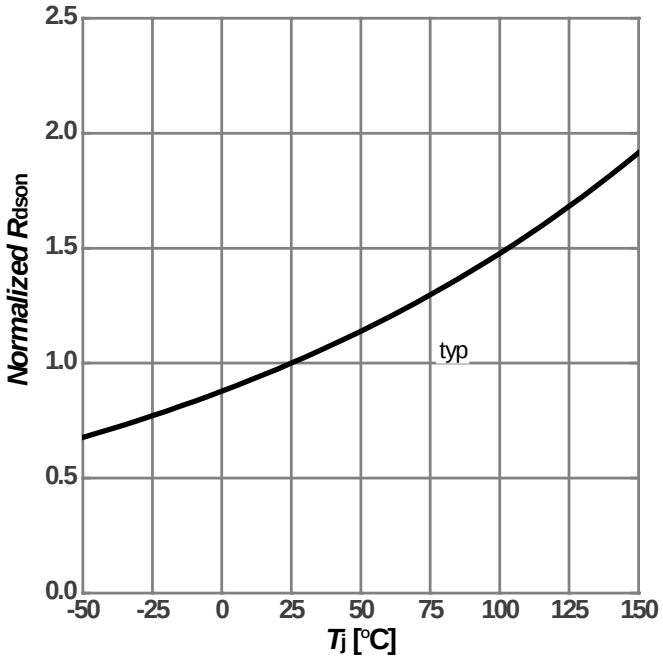
Diagram 7: Typ. transfer characteristics	Diagram 8: Gate threshold voltage vs. Junction temperature
	
I_D=f(V_{GS}); V_{DS}=15V; parameter: T_j	V_{th}=f(T_j); I_D=250μA

Diagram 9: On-state resistance vs. Drain current



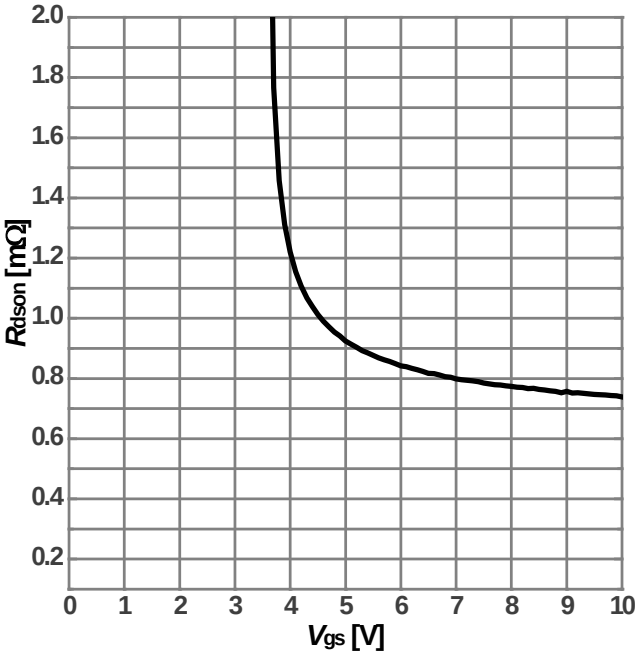
R_{DS}(on)=f(I_D); Tj=25°C; parameter: V_{GS}

Diagram 10: On-state resistance vs. Junction temperature



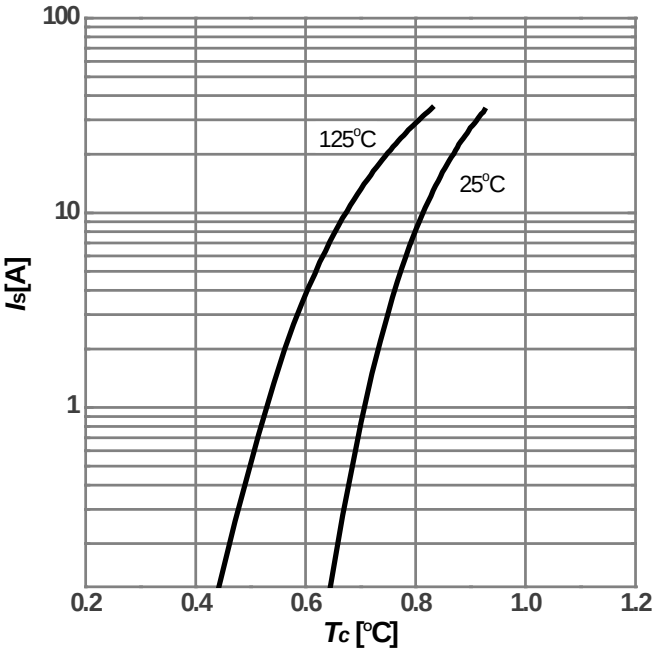
R_{DS}(on)=f(T_j); I_D=14A; V_{GS}=10V

Diagram 11: On-state resistance vs. Vgs characteristics



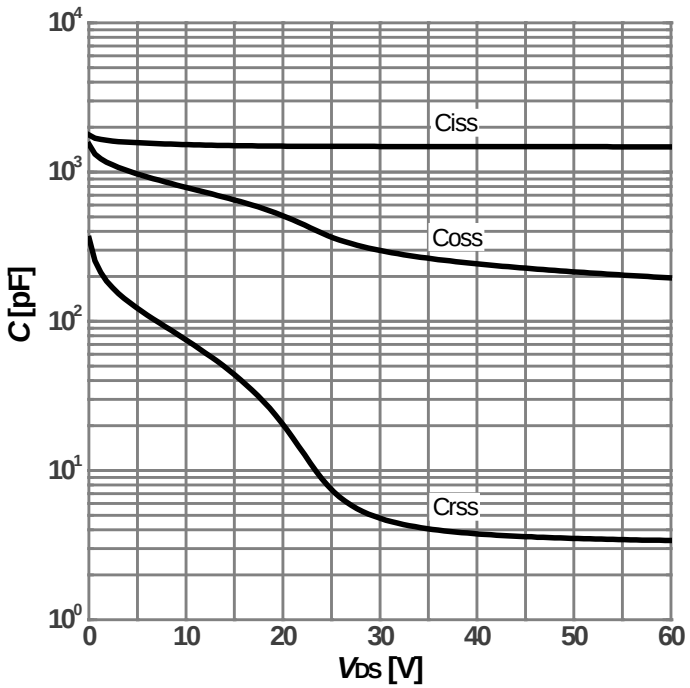
R_{DS}(on)=f(V_{gs}); Tj=25°C; I_D=14A

Diagram 12: Forward characteristics of reverse diode



I_F=f(V_{SD}); parameter: T_j

Diagram 13: Typ. capacitances



C=f(V_{DS}); V_{GS}=0V; f=1MHz

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