

● General Description

The AGMH12N10I combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

This device is ideal for load switch and battery protection applications.

● Features

- Advance high cell density Trench technology
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance
- 100% Avalanche test
- 100% DVDS tested

● Application

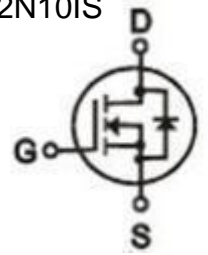
- MB/VGA Vcore
- SMPS 2nd Synchronous Rectifier
- POL application
- BLDC Motor driver

Product Summary

BVDSS	RDS(ON)	ID
100V	9.6mΩ	65A

TO-251 Pin Configuration

AGMH12N10IS



AGMH12N10I

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
AGMH12N10I	AGMH12N10I	TO-251	---	---	4500
AGMH12N10IS	AGMH12N10IS	TO-251	---	---	4500

Table 1. Absolute Maximum Ratings (TC=25°C)

Symbol	Parameter	Value	Unit
VDS	Drain-Source Voltage (VGS=0V)	100	V
VGS	Gate-Source Voltage (VDS=0V)	±20	V
ID	Drain Current-Continuous(Tc=25°C) (Note 1)	65	A
	Drain Current-Continuous(Tc=100°C)	39	A
IDM (pulse)	Drain Current-Continuous@ Current-Pulsed (Note 2)	260	A
PD	Maximum Power Dissipation(Tc=25°C)	96	w
	Maximum Power Dissipation(Tc=100°C)	38	w
EAS	Avalanche energy (Note 3)	81	mJ
TJ,TSTG	Operating Junction and Storage Temperature Range	-55 To 150	°C

Table 2. Thermal Characteristic

Symbol	Parameter	Typ	Max	Unit
RθJA	Thermal Resistance Junction-ambient (Steady State) ¹	---	94	°C/W
RθJC	Thermal Resistance Junction-Case ¹	---	1.3	°C/W

Table 3. Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BVDSS	Drain-Source Breakdown Voltage	VGS=0V ID=250μA	100	--	--	V
IDSS	Zero Gate Voltage Drain Current	VDS=100V,VGS=0V	--	--	1.0	μA
IGSS	Gate-Body Leakage Current	VGS=±20V,VDS=0V	--	--	±100	nA
VGS(th)	Gate Threshold Voltage	VDS=VGS,ID=250μA	2.5	3.0	4.0	V
gFS	Forward Transconductance	VDS=5V,ID=15A	--	18	--	S
RDS(on)	Drain-Source On-State Resistance	VGS=10V, ID=20A	--	9.6	13	mΩ
Dynamic Characteristics						
Ciss	Input Capacitance	VDS=50V,VGS=0V, F=1MHZ	--	1200	--	pF
Coss	Output Capacitance		--	460	--	pF
Crss	Reverse Transfer Capacitance		--	9.0	--	pF
Rg	Gate resistance	VGS=0V, VDS=0V,f=1.0MHz	--	11.5	--	Ω
Switching Times						
td(on)	Turn-on Delay Time	VGS=10V,VDS=50V, ID=10A, RGEN=5Ω	--	16	--	nS
tr	Turn-on Rise Time		--	18	--	nS
td(off)	Turn-Off Delay Time		--	32	--	nS
tf	Turn-Off Fall Time		--	10	--	nS
Qg	Total Gate Charge	VGS=10V, VDS=50V, ID=10A	--	21.8	--	nC
Qgs	Gate-Source Charge		--	3.7	--	nC
Qgd	Gate-Drain Charge		--	5.0	--	nC
Source-Drain Diode Characteristics						
ISD	Source-Drain Current(Body Diode)		--	--	65	A
VSD	Forward on Voltage	VGS=0V,IS=10A	--	--	1.2	V
trr	Reverse Recovery Time	Is=10A , VDD=50V,dl/dt=100A/μs	--	43	--	ns
Qrr	Reverse Recovery Charge		--	90	--	nc

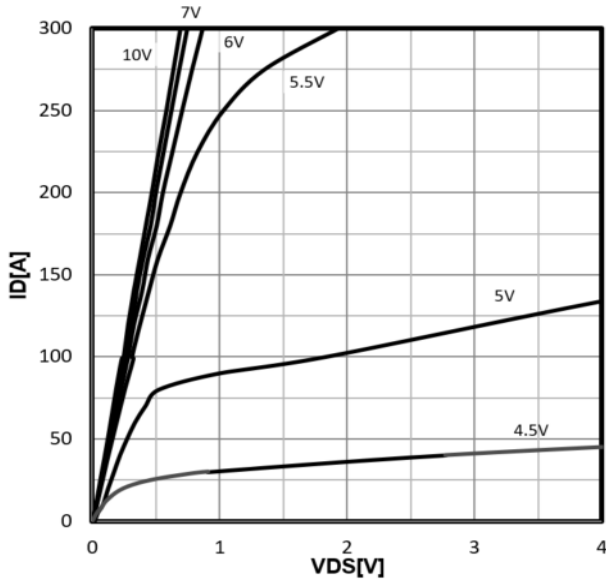
Notes 1.The maximum current rating is package limited.

Notes 2.Repetitive Rating: Pulse width limited by maximum junction temperature

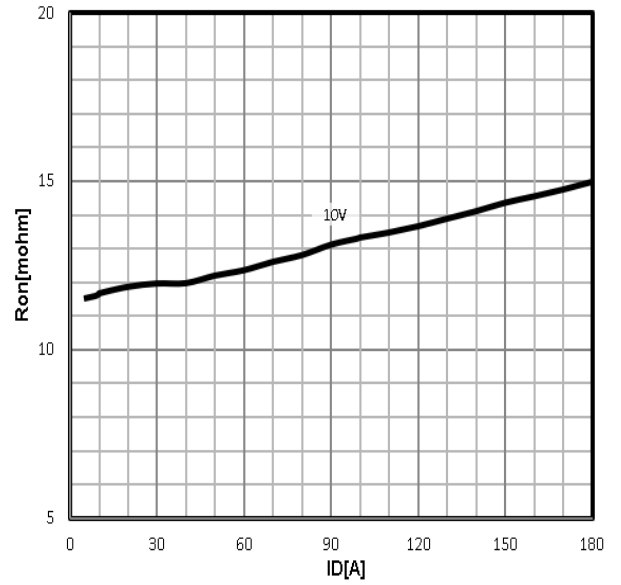
Notes 3.EAS condition: T_J=25°C

Characteristics Curve:

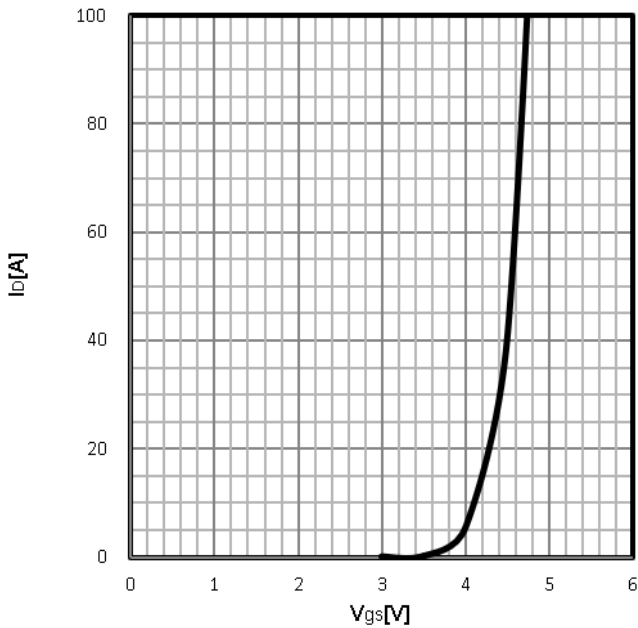
Typ. output characteristics
 $I_D = f(V_{DS})$



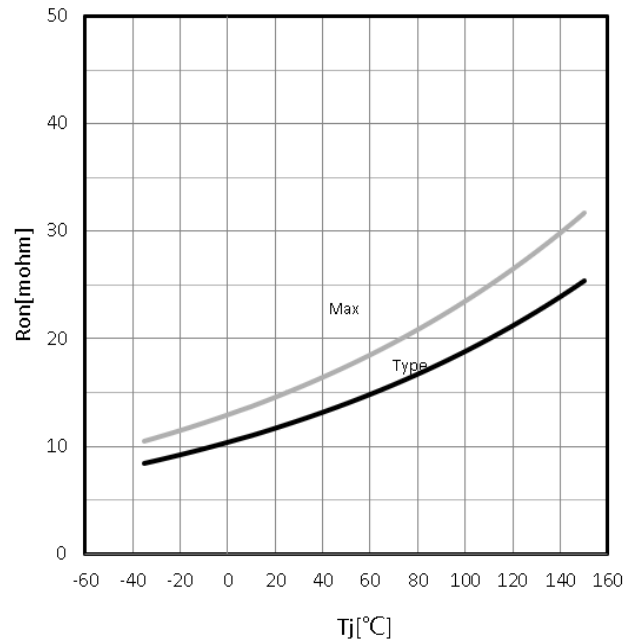
Typ. drain-source on resistance
 $R_{DS(on)} = f(I_D)$



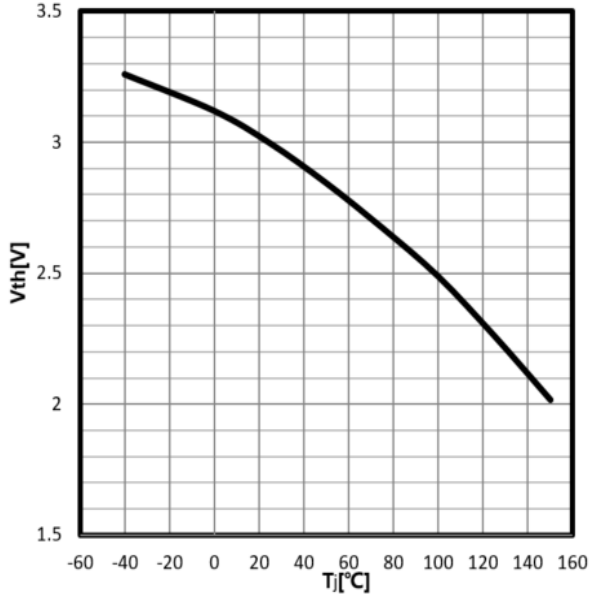
Typ. transfer characteristics
 $I_D = f(V_{GS})$



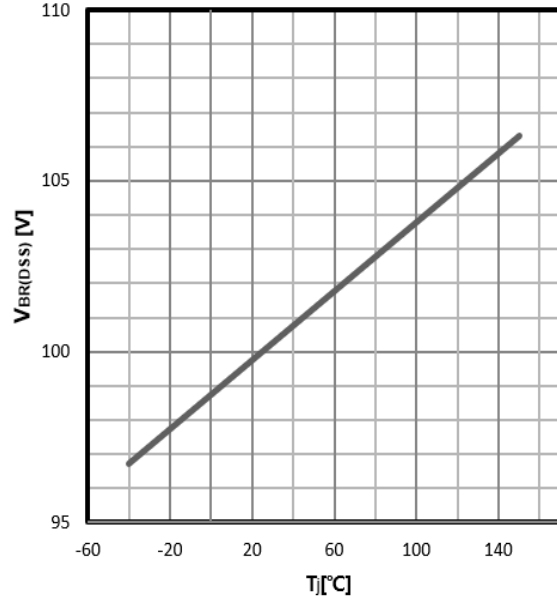
Drain-source on-state resistance
 $R_{DS(on)} = f(T_j); I_D = 20A; V_{GS} = 10V$



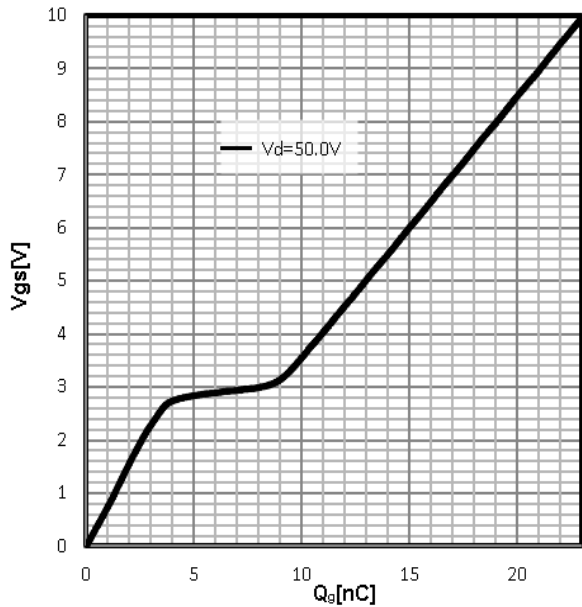
Gate Threshold Voltage
 $V_{TH}=f(T_j)$; $I_D=250\mu A$



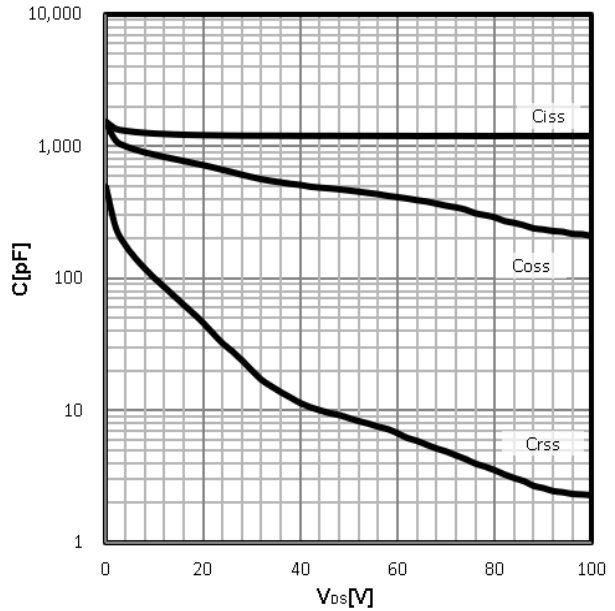
Drain-source breakdown voltage
 $V_{BR(DSS)}=f(T_j)$; $I_D=250\mu A$



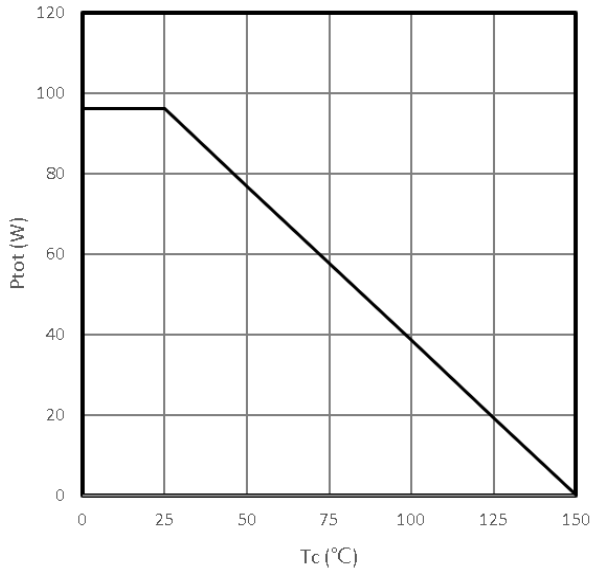
Typ. gate charge
 $V_{GS}=f(Q_g)$; $I_D=10A$



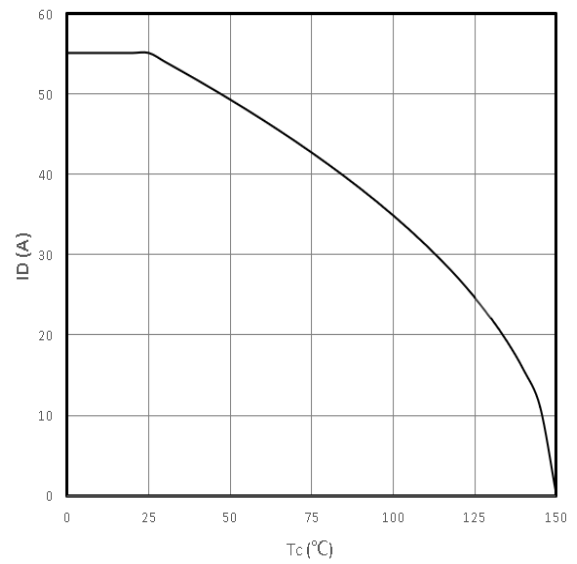
Typ. capacitances
 $C=f(V_{DS})$; $V_{GS}=0V$; $f=1MHz$



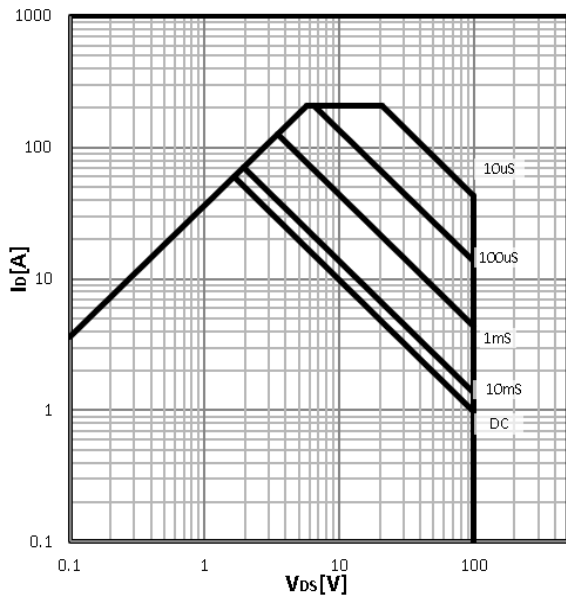
Power Dissipation
 $P_{tot}=f(T_c)$



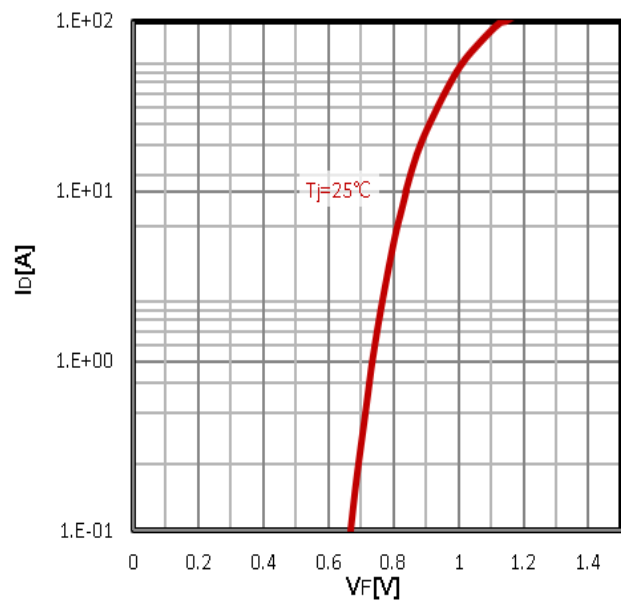
Maximum Drain Current
 $I_D=f(T_c)$



Safe operating area
 $I_D=f(V_{DS})$

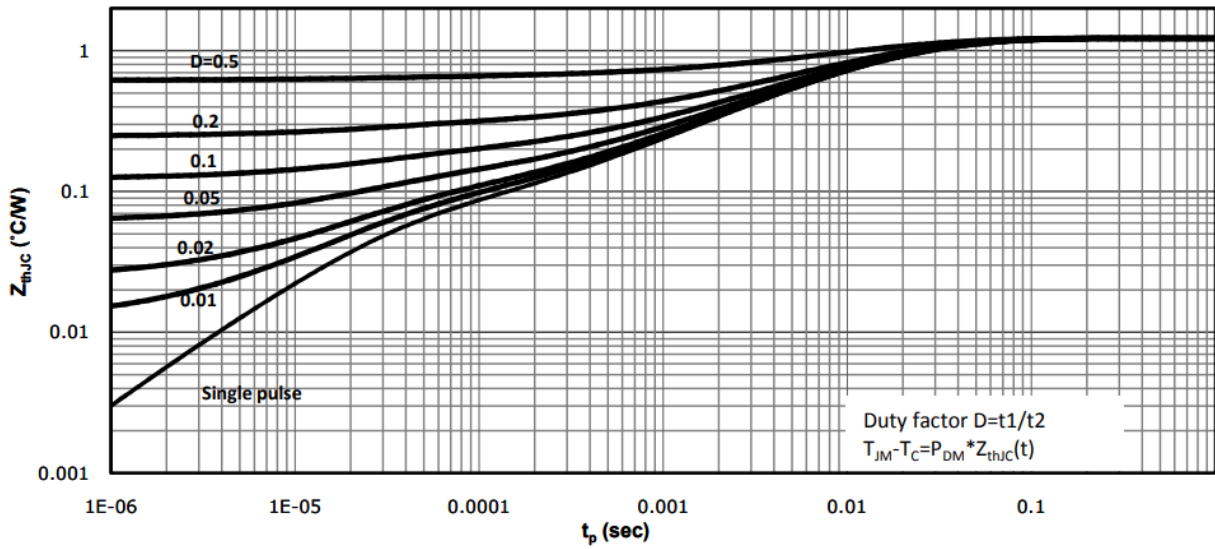


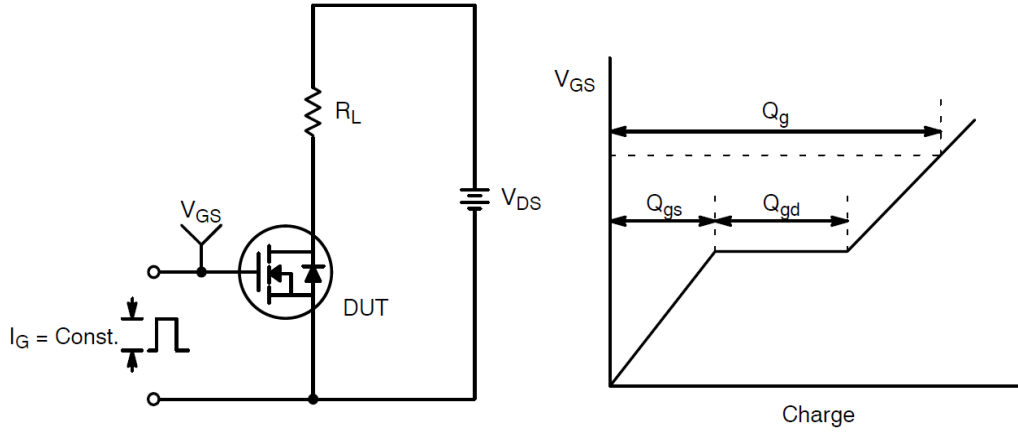
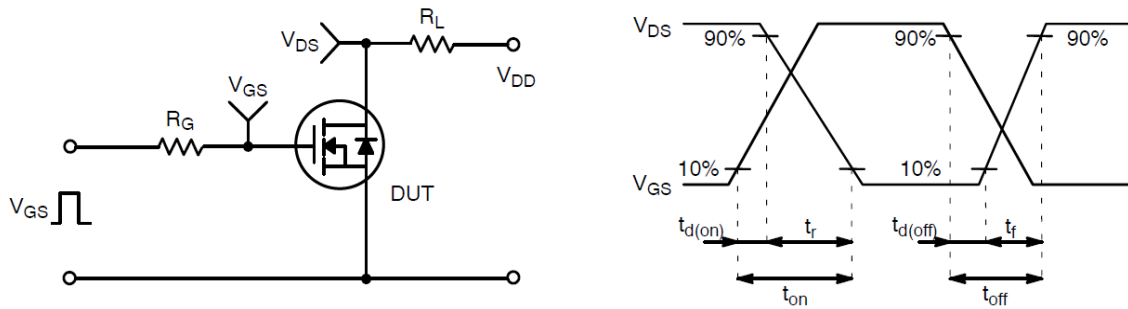
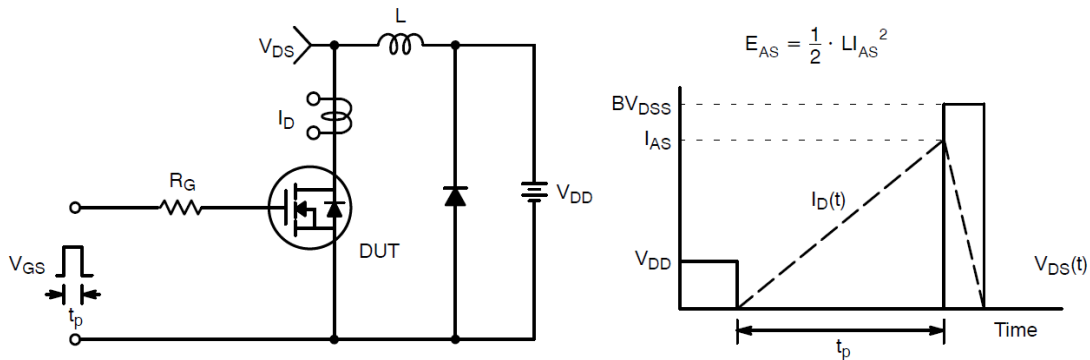
Body Diode Forward Voltage Variation
 $I_F=f(V_{GS})$

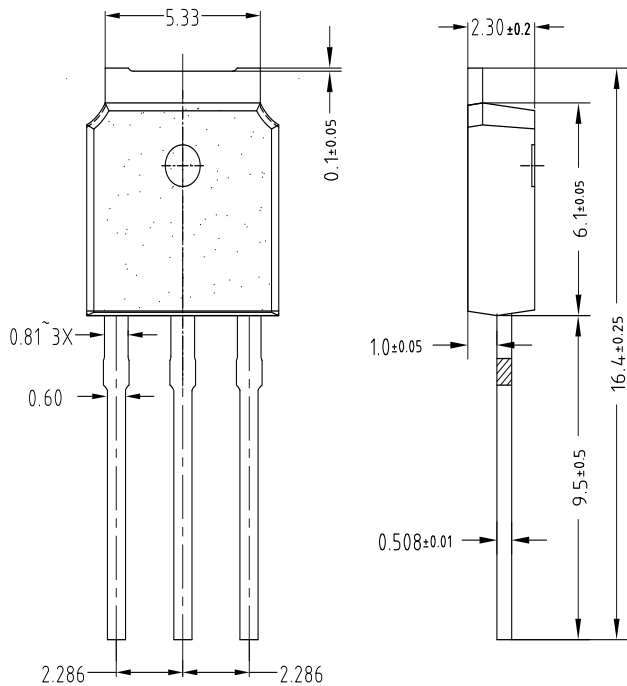
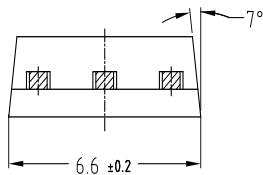
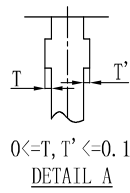
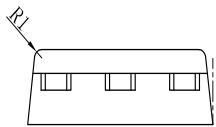
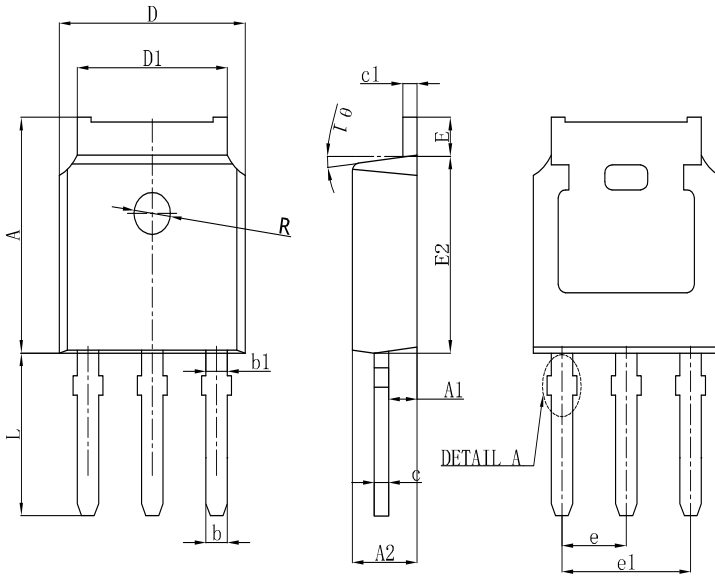


Max. transient thermal impedance

$$Z_{thJC} = f(t_p)$$



Test Circuit and Waveform:

Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms

Unclamped Inductive Switching Test Circuit & Waveforms

TO-251 Package Outline Data


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	7.050	7.100	7.150
A1	0.960	1.010	1.060
A2	2.250	2.300	2.350
b	0.760REF.		
b1	1.000REF.		
c	0.508REF.		
c1	0.508REF.		
D	6.550	6.600	6.650
D1	5.220	5.320	5.420
E	0.950	1.000	1.050
E2	6.050	6.100	6.150
e	2.286BSC		
e1	4.572REF.		
L	4.800	5.000	5.200
θ 1	7° REF.		
R	1.300REF.		
R1	0.250REF.		

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