AK4356
192kHz 24Bit Six-Channel DAC for DVD-Audio

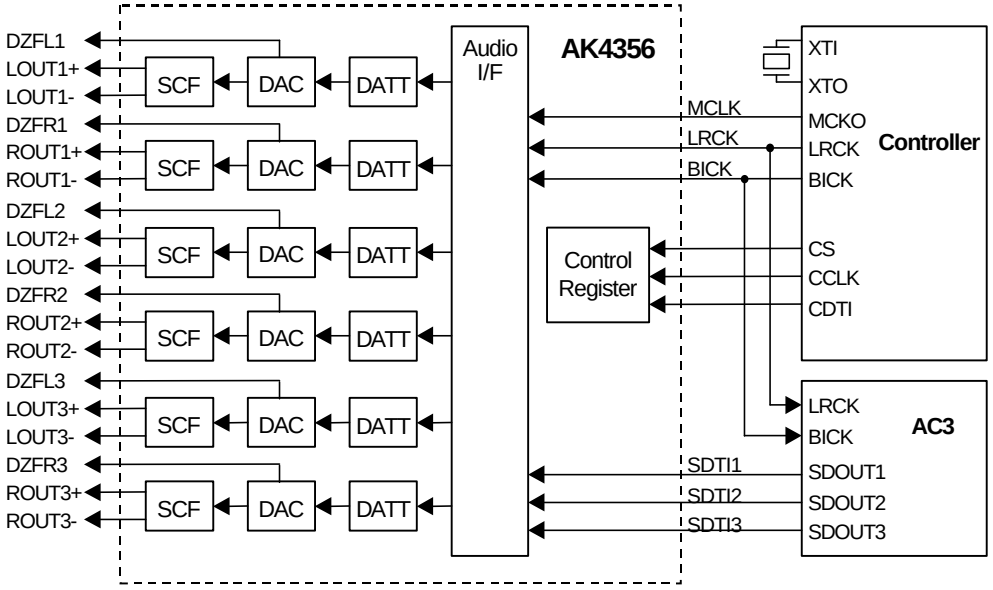
GENERAL DESCRIPTION

The AK4356 is a high performance six channels DAC corresponding to 96kHz sampling mode of DVD. Two channels of them can operate up to 192kHz sampling fully correspond to DVD-Audio standards. The AK4356 introduces the advanced multi-bit architecture for ΔΣ modulator. This new architecture achieves the wider dynamic range, while keeping much the same superior distortion characteristics as conventional Single Bit way. In the AK4356, the analog outputs are filtered in the analog domain by switched-capacitor filter (SCF) with high tolerance to clock jitter. The analog outputs are full differential output, so the device is suitable for hi-end applications.

FEATURES

- **128x Oversampling**
- **Sampling Rate up to 192kHz for 2 channels mode,**
  96kHz for 6 channels mode
- **24Bit 8 times Digital Filter with Slow roll-off option**
  Ripple: ±0.005dB, Attenuation: 75dB
- **THD+N: -94dB**
- **DR, S/N: 112dB**
- **High Tolerance to Clock Jitter**
- **Low Distortion Differential Output**
- **Channel Independent Digital De-emphasis for 32, 44.1 & 48kHz sampling**
- **Channel Independent Zero Detect Pin**
- **Channel Independent Digital Attenuator with soft-transition**
- **Soft Mute**
- **3-wire Serial Interface for Volume Control**
- **I/F format: MSB justified, LSB justified, I2S**
- **TTL Level Digital I/F**
- **Master Clock**
  Normal Speed: 256fs, 384fs, 512fs or 768fs
  Double Speed: 128fs, 192fs, 256fs or 384fs
- **Power Supply: 4.75 to 5.25V**
- **44pin LQFP Package**
- **Ta: -40 to 85°C**

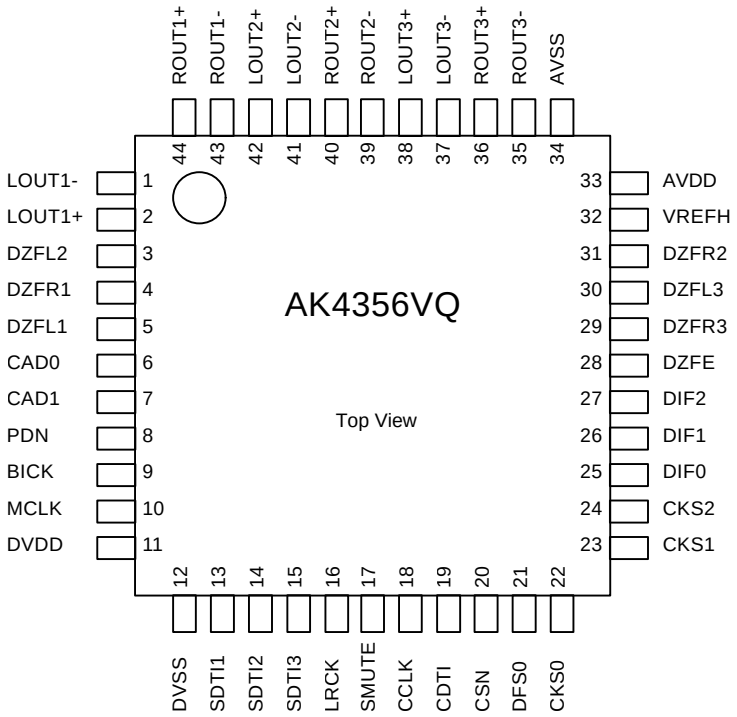
■ Block Diagram



■ Ordering Guide

AK4356VQ	-40~+85°C	44pin LQFP(0.8mm pitch)
AKD4356	Evaluation Board	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	LOUT1-	O	DAC1 Lch Negative Analog Output Pin
2	LOUT1+	O	DAC1 Lch Positive Analog Output Pin
3	DZFL2	O	DAC2 Lch Zero Input Detect Pin
4	DZFR1	O	DAC1 Rch Zero Input Detect Pin
5	DZFL1	O	DAC1 Lch Zero Input Detect Pin
6	CAD0	I	Chip Address 0 Pin
7	CAD1	I	Chip Address 1 Pin
8	PDN	I	Power-Down & Reset Pin When "L", the AK4356 is powered-down and the control registers are reset to default state. If the state of CAD0-1 changes, then the AK4356 must be reset by PDN.
9	BICK	I	Audio Serial Data Clock Pin
10	MCLK	I	Master Clock Input Pin
11	DVDD	-	Digital Power Supply Pin, +4.75~+5.25V
12	DVSS	-	Digital Ground Pin
13	SDTI1	I	DAC1 Audio Serial Data Input Pin
14	SDTI2	I	DAC2 Audio Serial Data Input Pin
15	SDTI3	I	DAC3 Audio Serial Data Input Pin
16	LRCK	I	Audio Input Channel Clock Pin
17	SMUTE	I	Soft Mute Pin (Note) When this pin goes to "H", soft mute cycle is initialized. When returning to "L", the output mute releases.
18	CCLK	I	Control Data Clock Pin
19	CDTI	I	Control Data Input Pin
20	CSN	I	Chip Select Pin This pin should be held to "H" except for access.

No.	Pin Name	I/O	Function
21	DFS0	I	Double Speed Sampling Mode 0 Pin (Note) "L": Normal Speed, "H": Double Speed at DFS1 bit = "0".
22	CKS0	I	Input Clock Select 0 Pin (Note)
23	CKS1	I	Input Clock Select 1 Pin (Note)
24	CKS2	I	Input Clock Select 2 Pin (Note)
25	DIF0	I	Audio Data Interface Format 0 Pin (Note)
26	DIF1	I	Audio Data Interface Format 1 Pin (Note)
27	DIF2	I	Audio Data Interface Format 2 Pin (Note)
28	DZFE	I	Zero Input Detect Enable Pin (Note)
29	DZFR3	O	DAC3 Rch Zero Input Detect Pin
30	DZFL3	O	DAC3 Lch Zero Input Detect Pin
31	DZFR2	O	DAC2 Rch Zero Input Detect Pin
32	VREFH	I	Positive Voltage Reference Input Pin, AVDD
33	AVDD	-	Analog Power Supply Pin
34	AVSS	-	Analog Ground Pin, +4.75~+5.25V
35	ROUT3-	O	DAC3 Rch Negative Analog Output Pin
36	ROUT3+	O	DAC3 Rch Positive Analog Output Pin
37	LOUT3-	O	DAC3 Lch Negative Analog Output Pin
38	LOUT3+	O	DAC3 Lch Positive Analog Output Pin
39	ROUT2-	O	DAC2 Rch Negative Analog Output Pin
40	ROUT2+	O	DAC2 Rch Positive Analog Output Pin
41	LOUT2-	O	DAC2 Lch Negative Analog Output Pin
42	LOUT2+	O	DAC2 Lch Positive Analog Output Pin
43	ROUT1-	O	DAC1 Rch Negative Analog Output Pin
44	ROUT1+	O	DAC1 Rch Positive Analog Output Pin

Note: SMUTE, DFS0, CKS0, CKS1, CKS2, DIF0, DIF1, DIF2, DZFE pins are ORed with serial control register.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies	Analog	AVDD	-0.3	6.0	V
	Digital	DVDD	-0.3	6.0	V
	|AVSS-DVSS| (Note 2)	ΔGND	-	0.3	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage		VINA	-0.3	AVDD+0.3	V
Digital Input Voltage		VIND	-0.3	DVDD+0.3	V
Ambient Temperature		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Note:1. All voltages with respect to ground.
2. AVSS and DVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog	AVDD	4.75	5.0	5.25	V
(Note 3)	Digital	DVDD	4.75	5.0	5.25	V

Note:1. All voltages with respect to ground.
3. The power up sequence between AVDD and DVDD is not critical.

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=5V; AVSS, DVSS=0V; VREFH=AVDD; fs=44.1kHz; BICK=64fs;
Signal Frequency =1kHz; 24bit Data; $R_L \geq 2k\Omega$; Measurement Frequency=20Hz~20kHz at 44.1kHz,
20Hz~40kHz at fs=96kHz, 20Hz~80kHz at fs=192kHz; unless otherwise specified)

Parameter		min	typ	max	Units
Dynamic Characteristics (Note 4)					
Resolution				24	Bits
S/(N+D)	fs=44.1kHz	88	94		dB
	fs=96kHz	86	92		dB
DR (-60dBFS)	fs=44.1kHz, A-weighted	106	112		dB
	fs=96kHz	-	105		dB
S/N (Note 5,6)	fs=44.1kHz, A-weighted	106	112		dB
	fs=96kHz	-	105		dB
Interchannel Isolation		90	110		dB
DC Accuracy					
Interchannel Gain Mismatch			0.2	0.5	dB
Gain Drift	(Note 7)		20	-	ppm/°C
Output Voltage	(AOUT+) - (AOUT-) (Note 8)	±2.55	±2.75	±2.95	Vpp
Load Resistance	(Note 9)	2			kΩ
Load Capacitance				25	pF
Power Supply Rejection	(Note 10)		50		dB
Power Supplies					
Power Supply Current					
Normal Operation (PDN = "H")					
AVDD			60	90	mA
DVDD	(fs=44.1kHz)		15	30	mA
	(fs=96kHz)		20	40	mA
	(fs=192kHz)		15	30	mA
Power-Down-Mode (PDN = "L")					
AVDD+DVDD	(Note 11)		10	100	μA

Note: 4. Measured by UPD(ROHDE & SCHWARZ). Refer to the evaluation board manual.
5. 107dB at CCIR-ARM weighted
6. S/N is independent of input bit length.
7. VREFH is constantly +5.0V.
8. Full scale voltage (0dB). Output voltage scales with the voltage of VREFH pin.
AOUT(typ.@0dB)=(AOUT+)-(AOUT-)=±2.75Vpp*VREFH/5.0
9. AC load
10. PSR is applied to AVDD, DVDD with 1kHz, 100mVpp. VREFH pin is held a constant voltage.
11. All digital input pins including clock pins (MCLK, BICK and LRCK) are connected to DVSS.

FILTER CHARACTERISTICS (fs=44.1kHz)

(Ta=25°C; AVDD, DVDD=4.75~5.25V; fs=44.1kHz; DFS1 = DFS0 = "0"; DEM=OFF)

Parameter			Symbol	min	typ	max	Units
Digital Filter							
Passband	(Note 12)	±0.01dB -6.0dB	PB	0 -	 22.05	20.0 -	kHz kHz
Stopband	(Note 12)		SB	24.1			kHz
Passband Ripple			PR			±0.005	dB
Stopband Attenuation			SA	75			dB
Group Delay	(Note 13)		GD	-	27.2	-	1/fs
Digital Filter + SCF							
Frequency Response:	0~20.0kHz		FR	-	±0.2	-	dB

Note:12. The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs(@±0.01dB), SB=0.546*fs.

13. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24bit data of both channels on the input register to the output of analog signal.

FILTER CHARACTERISTICS (fs=96kHz)

(Ta=25°C; AVDD, DVDD=4.75~5.25V; fs=96kHz; DFS1 = "0"; DFS0 = "1"; DEM=OFF)

Parameter			Symbol	min	typ	max	Units
Digital Filter							
Passband	(Note 14)	±0.01dB -6.0dB	PB	0 -	 48.0	43.5 -	kHz kHz
Stopband	(Note 14)		SB	52.5			kHz
Passband Ripple			PR			±0.005	dB
Stopband Attenuation			SA	75			dB
Group Delay	(Note 13)		GD	-	27.2	-	1/fs
Digital Filter + SCF							
Frequency Response:	0~40.0kHz		FR	-	±0.3	-	dB

Note:14. The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs(@±0.01dB), SB=0.546*fs.

FILTER CHARACTERISTICS (fs=192kHz)

(Ta=25°C; AVDD, DVDD=4.75~5.25V; fs=192kHz; DFS1 = "1"; DFS0 = "0"; DEM=OFF)

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 15)	±0.01dB	PB	0		87.0	kHz
	-6.0dB		-	96.0	-	kHz
Stopband (Note 15)		SB	105			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	75			dB
Group Delay (Note 13)		GD	-	27.2	-	1/fs
Digital Filter + SCF						
Frequency Response: 0~80.0kHz		FR	-	±0.5	-	dB

Note:15. The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs(@±0.01dB), SB=0.546*fs.

DIGITAL CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=4.75~5.25V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage		VIH	2.2	-	-	V
Low-Level Input Voltage		VIL	-	-	0.8	V
Hight-Level Output Voltage	(Iout= -100μA)	VOH	DVDD-0.5	-	-	V
Low-Level Output Voltage	(Iout= 100μA)	VOL	-	-	0.5	V
Input Leakage Current		Iin	-	-	±10	μA

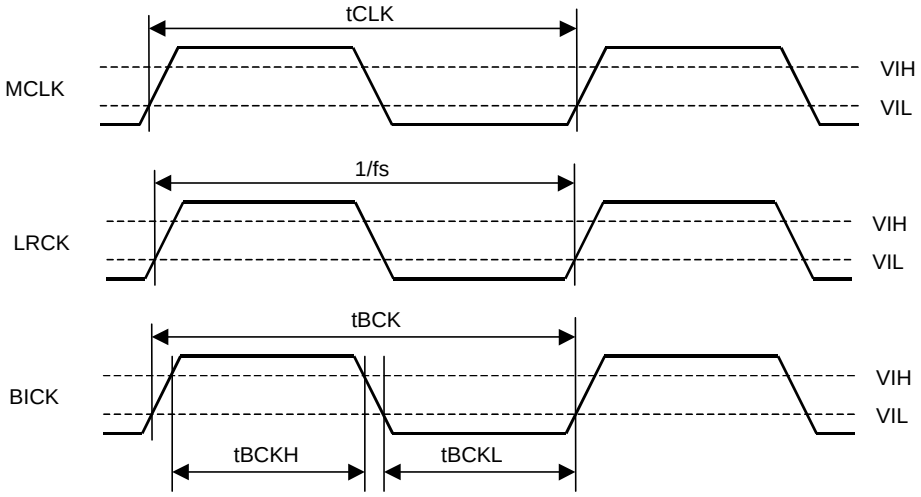
SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=4.75~5.25V; C_L=20pF)

Parameter		Symbol	min	typ	max	Units
Master Clock Timing	(Note 16)					
Frequency		fCLK	8.192		36.864	MHz
Duty		Duty	40		60	%
LRCK frequency	(Note 17)					
Normal Speed Mode (DFS1-0 = "00")		fsn	32		48	kHz
Double Speed Mode (DFS1-0 = "01")		fsd	64		96	kHz
4 times Speed Mode (DFS1-0 = "10")		fsq	128		192	kHz
Duty Cycle		Duty	45		55	%
Serial Interface Timing						
BICK Period						
Normal Speed Mode		tBCK	1/128fs			ns
Double Speed Mode		tBCK	1/64fs			ns
4 times Speed Mode		tBCK	1/64fs			ns
BICK Pulse Width Low		tBCKL	33			ns
Pulse Width High		tBCKH	33			ns
BICK "↑" to LRCK Edge	(Note 18)	tBLR	20			ns
LRCK Edge to BICK "↑"	(Note 18)	tLRB	20			ns
SDTI Hold Time		tSDH	20			ns
SDTI Setup Time		tSDS	20			ns
Control Interface Timing						
CCLK Period		tCCK	200			ns
CCLK Pulse Width Low		tCCKL	80			ns
Pulse Width High		tCCKH	80			ns
CDTI Setup Time		tCDS	40			ns
CDTI Hold Time		tCDH	40			ns
CSN "H" Time		tCSW	150			ns
CSN "↓" to CCLK "↑"		tCSS	50			ns
CCLK "↑" to CSN "↑"		tCSH	50			ns
Rise Time of CSN		tR1			20	ns
Fall Time of CSN		tF1			20	ns
Rise Time of CCLK		tR2			20	ns
Fall Time of CCLK		tF2			20	ns
Power-down/Reset Timing						
PDN Pulse Width	(Note 19)	tPDW	150			ns

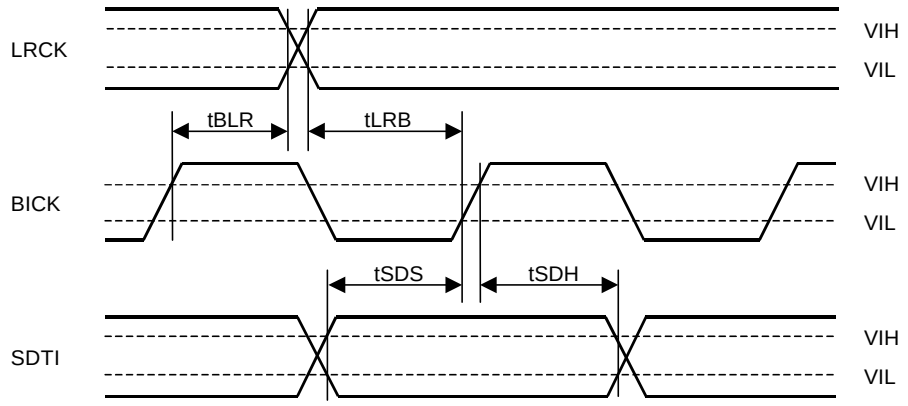
Note:16. **For Double and 4 times Speed modes please see Appendix A for relationship of MCLK and BCLK/LRCK.**
17. If sampling speed mode (DFS0-1) changes, please reset by PDN pin or RSTN bit.
18. BICK rising edge must not occur at the same time as LRCK edge.
19. The AK4356 can be reset by PDN pin "L" upon power up.
If CKS0-2 or DFS0-1 changes, the AK4356 should be reset by PDN pin or RSTN bit.

■ Timing Diagram

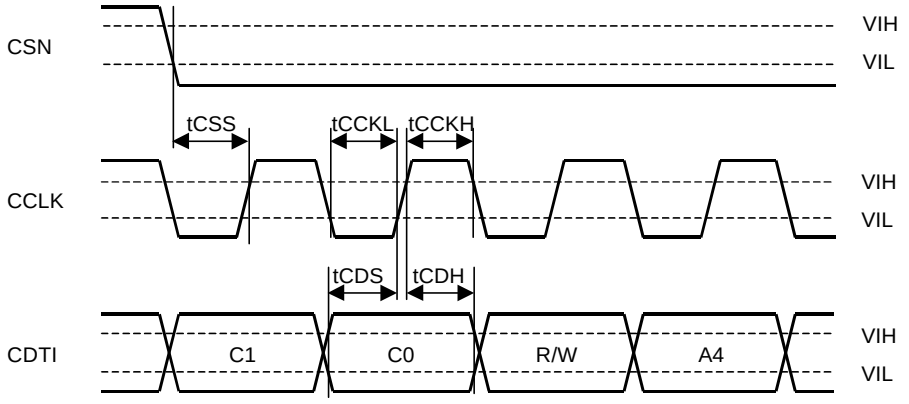


Clock Timing

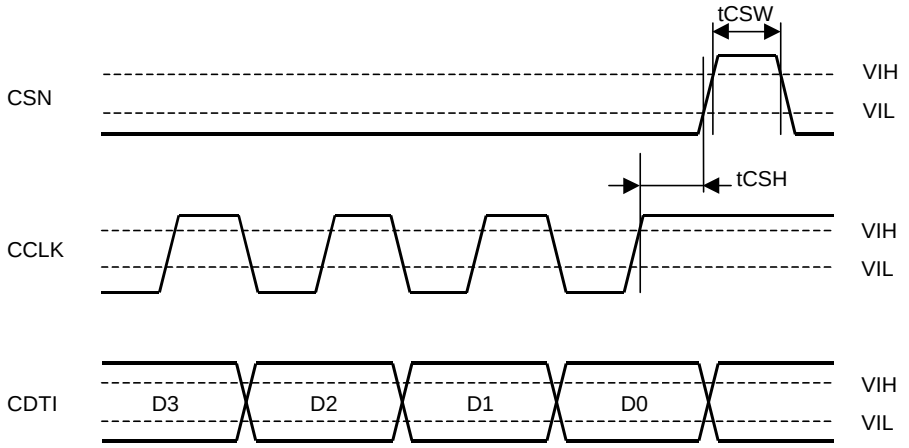
For Double and 4 times Speed modes timing please see Appendix A for relationship of MCLK and BCLK/LRCK.



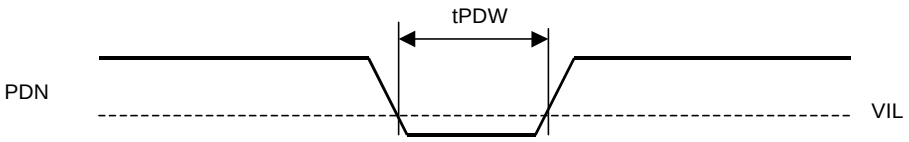
Audio Interface Timing



WRITE Command Input Timing



WRITE Data Input Timing



Power-down & Reset Timing

OPERATION OVERVIEW

■ System Clock Input

The external clocks which are required to operate the AK4356 are MCLK, LRCK and BICK. The master clock (MCLK) should be synchronized with sampling clock (LRCK) but the phase is not critical. **However, in Double and 4 times Speed Modes, the phase relationship between MCLK and LRCK/BICK is limited. (Refer to Appendix A).** MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. The frequency of MCLK can be set by CKS0-2, and can be selected to normal, double or 4 times speed mode by DFS0-1 (See Table 1). 4 times speed mode can be used for only DAC1. If DAC1 is in 4 times speed mode, DAC2 and DAC3 are automatically powered down. When the states of SLOW, DIF2-0, DFS1-0 or CKS2-0 changes, the AK4356 should be reset by PDN pin or RSTN bit.

All external clocks (MCLK, BICK and LRCK) should always be present whenever the AK4356 is in normal operation mode (PDN = "H"). If these clocks are not provided, the AK4356 may draw excess current and may not possibly operate properly because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4356 should be in the power-down mode (PDN = "L" or all DACs are set in the power-down mode by PW1-3 bits) or in the reset mode (RSTN = "0"). After exiting reset at power-up etc., the AK4356 is in the power-down mode until MCLK and LRCK are input.

Mode	CKS2	CKS1	CKS0	DFS1-0		
				"00" (Normal Speed)	"01" (Double Speed)	"10" (4 times Speed)
0	0	0	0	**256fs**	128fs	N/A
1	0	0	1	256fs	256fs	N/A
2	0	1	0	384fs	192fs	N/A
3	0	1	1	384fs	384fs	N/A
4	1	0	0	512fs	256fs	128fs
5	1	0	1	512fs	N/A	N/A
6	1	1	0	768fs	384fs	192fs
7	1	1	1	768fs	N/A	N/A

default (DFS1-0 = "00")

Table 1. System Clock (DFS1-0 = "11": reserved)

fs [kHz]	Mode	128fs	192fs	256fs	384fs	512fs	768fs
32	Normal	-	-	8.1920	12.2880	16.3840	24.5760
64	Double	8.1920	12.2880	16.3840	24.5760	-	-
128	4 times	16.3840	24.5760	-	-	-	-
44.1	Normal	-	-	11.2896	16.9344	22.5792	33.8688
88.2	Double	11.2896	16.9344	22.5792	33.8688	-	-
176.4	4 times	22.5792	33.8688	-	-	-	-
48	Normal	-	-	12.2880	18.4320	24.5760	36.8640
96	Double	12.2880	18.4320	24.5760	36.8640	-	-
192	4 times	24.5760	36.8640	-	-	-	-

Table 2. Example of System Clock [MHz]

■ Audio Serial Interface Format

Audio data is input to the AK4356 via the SDTI1-3 pins using BICK and LRCK inputs. 5 serial data formats are supported and selected by DIF2-0 pins or DIF2-0 bits (See Table 3, compatible with the AK4324/4393). In all modes the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 2 can be used for 20 and 16 MSB justified formats by zeroing the unused LSBs.

Mode	DIF2	DIF1	DIF0	SDTI	L/R	BICK	Figure	
0	0	0	0	16bit, LSB justified	H/L	≥32fs	Figure 1	default
1	0	0	1	20bit, LSB justified	H/L	≥40fs	Figure 2	
2	0	1	0	24bit, MSB justified	H/L	≥48fs	Figure 3	
3	0	1	1	I2S	L/H	32fs or ≥48fs	Figure 4	
4	1	0	0	24bit, LSB justified	H/L	≥48fs	Figure 2	

Table 3. Audio data format

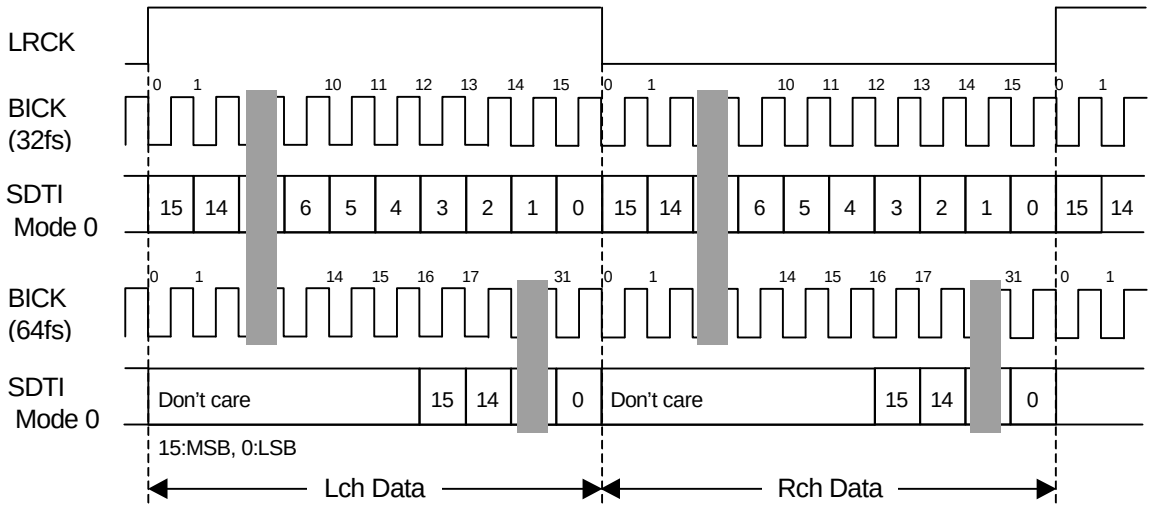


Figure 1. Mode 0 Timing

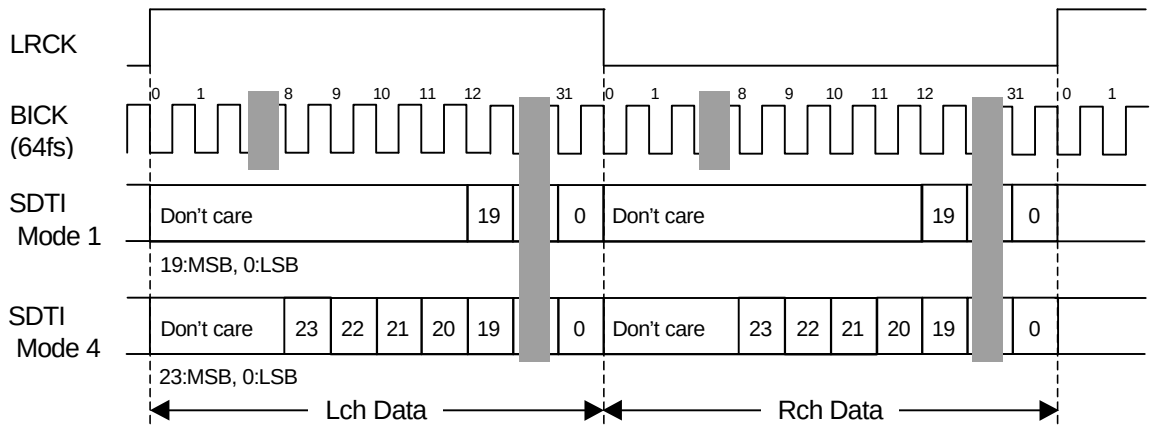


Figure 2. Mode 1,4 Timing

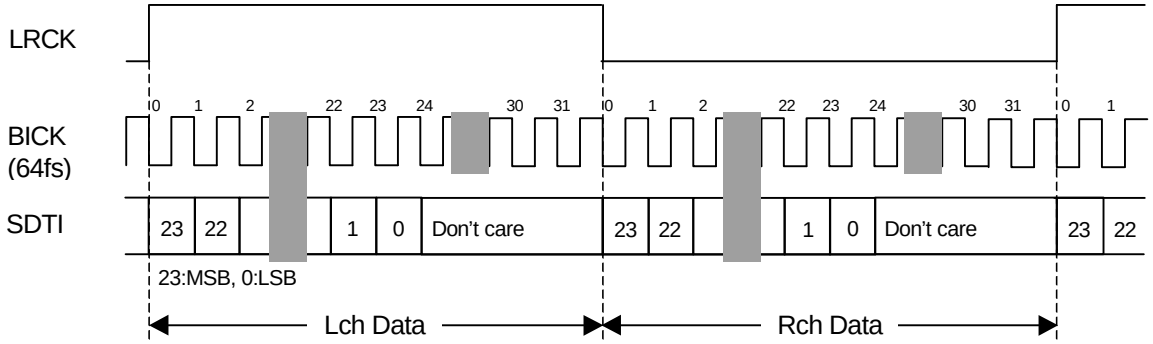


Figure 3. Mode 2 Timing

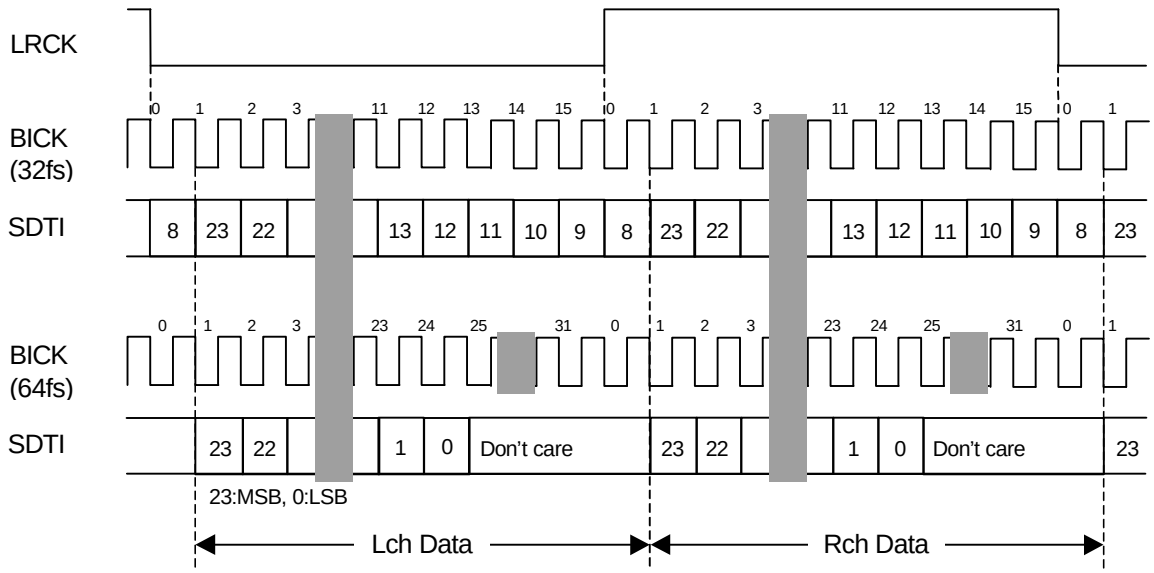


Figure 4. Mode 3 Timing

■ Output Volume

The AK4356 includes channel independent digital output volumes (ATT) with 256 levels at 0.5dB steps including MUTE. These volumes are in front of the DAC and can attenuate the input data from 0dB to –127dB and mute. When changing levels, transitions are executed via soft changes; thus no switching noise occurs during these transitions.

■ De-emphasis filter

A digital de-emphasis filter is available for 32, 44.1 or 48kHz sampling rates (tc=50/15μs). It can be set for DAC1 (SDTI1), DAC2 (SDTI2) and DAC3 (SDTI3) independently. It is enabled or disabled with the control register data of DEM1-0 and DFS1-0. The de-emphasis filter is disabled at double or 4 times sampling mode (except for DFS0 = DFS1 = "0").

DEM1	DEM0	De-emphasis	
0	0	44.1kHz	
0	1	OFF	default
1	0	48kHz	
1	1	32kHz	

Table 4. De-emphasis filter control with DEM1-0 (DFS1-0 = "00")

DFS1	DFS0	De-emphasis	
0	0	See Table 4.	default
0	1	OFF	
1	0	OFF	
1	1	OFF	

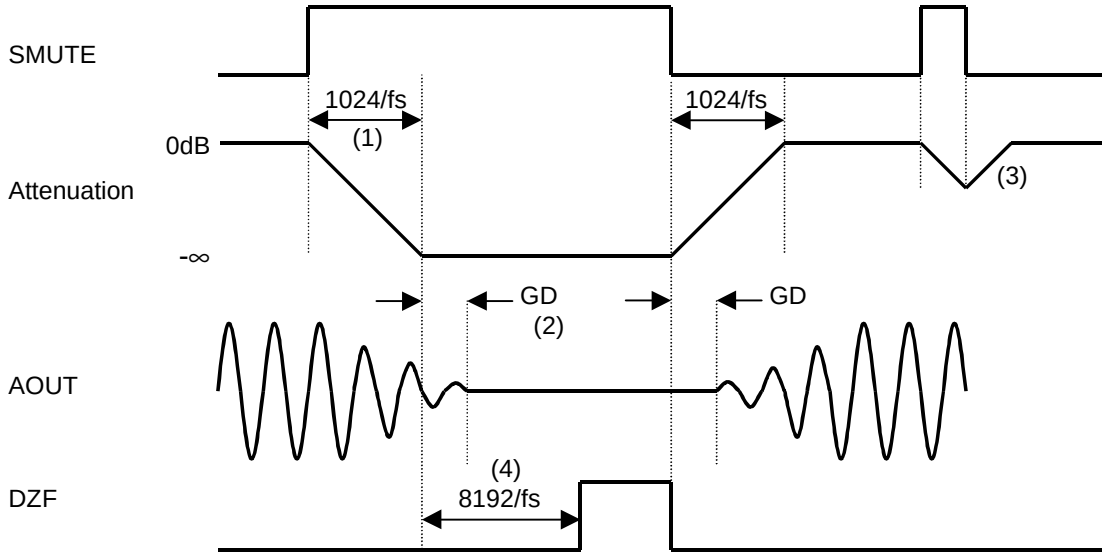
Table 5. De-emphasis filter control with DFS1-0

■ Zero detection

The AK4356 has channel-independent zeros detect function. When the input data at each channel is continuously zero for 8192 LRCK cycles, DZF pin of each channel goes to "H". DZF pin of each channel immediately goes to "L" if input data of each channel is not zero after going DZF "H". If RSTN bit is "0", DZF pins of all channels go to "H". DZF pins of all channels go to "L" 4/fs after RSTN bit returns to "1". If DZFM bit is set to "1", DZF pins of all channels go to "H" only when the input data at all channels are continuously zeros for 8192 LRCK cycles. Zero detect function can be disabled by DZFE bit. In this case, DZF pins of all channels are always "L" (except for the case of RSTN = "0").

■ Soft mute operation

Soft mute operation is performed at digital domain. When the SMUTE pin goes to "H", the output signal is attenuated by -∞ during 1024 LRCK cycles. When the SMUTE pin is returned to "L", the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled within 1024 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:
(1) The output signal is attenuated by -∞ during 1024 LRCK cycles (1024/fs).
(2) Analog output corresponding to digital input have the group delay (GD).
(3) If the soft mute is cancelled within 1024 LRCK cycles, the attenuation is discontinued and returned to 0dB.
(4) When the input data at each channel is continuously zeros for 8192 LRCK cycles, DZF pin of each channel goes to "H". DZF pin immediately goes to "L" if input data are not zero after going DZF "H".

Figure 5. Soft mute and zero detection

■ System Reset

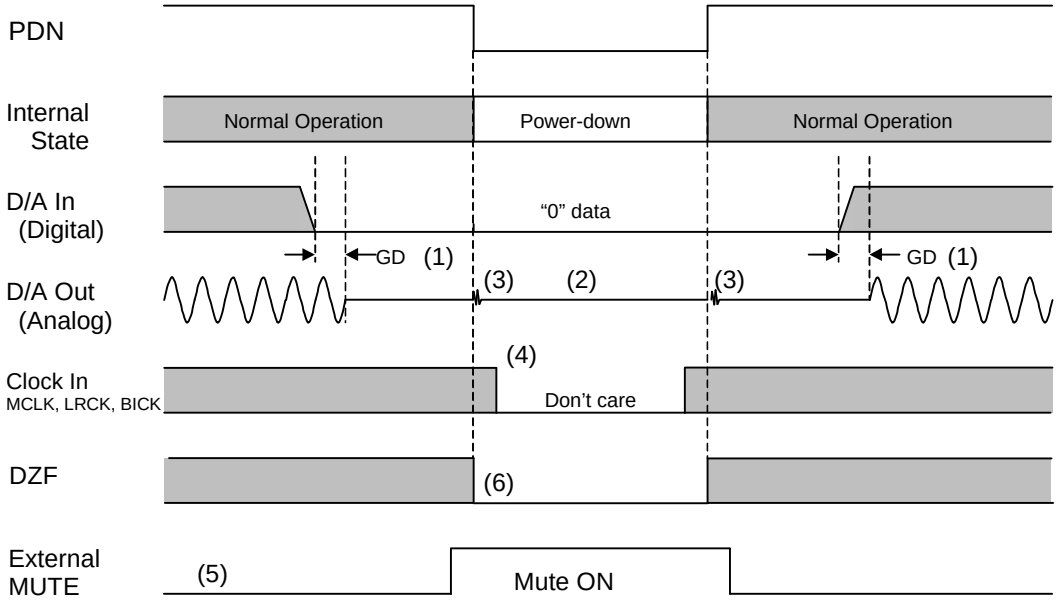
The AK4356 should be reset once by bringing PDN = "L" upon power-up. The AK4356 is powered up and the internal timing starts clocking by LRCK "↑" after exiting reset and power down state by MCLK. The AK4356 is in the power-down mode until MCLK and LRCK are input.

■ Power-down

All DACs are placed in the power-down mode by bringing PDN pin "L" and each digital filter is also reset at the same time. The internal register values are initialized by PDN "L". This reset should always be done after power-up. Because some click noise occurs at the edge of PDN, the analog output should be muted externally if the click noise influences system application. Figure 6 shows the power-down/up sequence.

Each DAC can be powered down by each power-down bit (PW1-3) "0". In this case, the internal register values are not initialized and the analog output is Hi-Z. Because some click noise occurs, the analog output should be muted externally if the click noise influences system application.

If DAC1 is in 4 times speed mode (DFS1=1, DFS0=0), DAC2 and DAC3 are automatically powered down. Both analog outputs go to analog common voltage (AVDD/2).



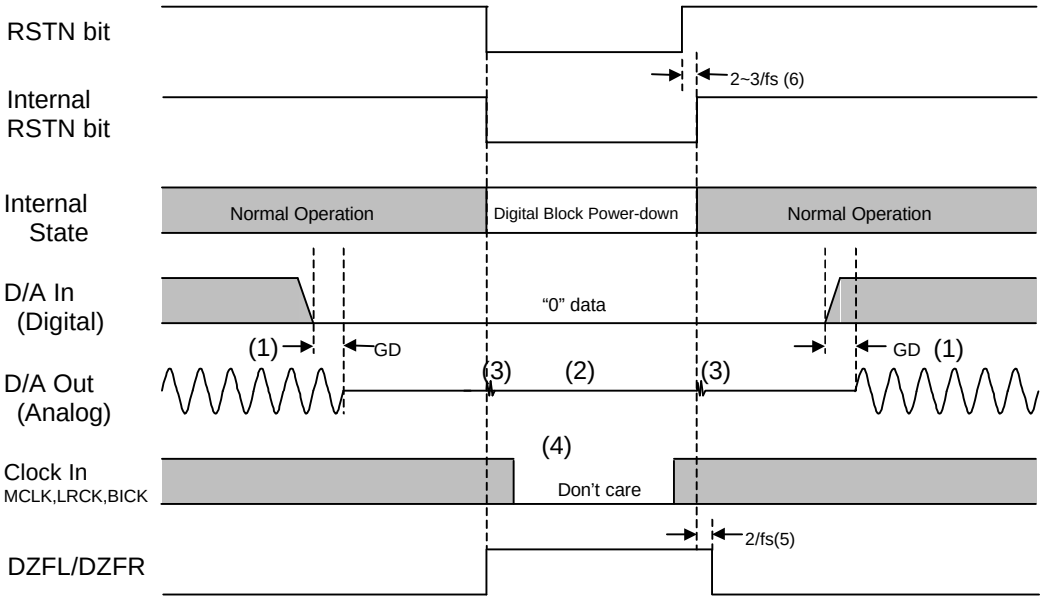
Notes:

(1) The analog output corresponding to digital input has the group delay (GD).
(2) Analog outputs are floating (Hi -Z) at the power-down mode.
(3) Click noise occurs at the edge of PDN signal. This noise is output even if "0" data is input.
(4) The external clocks (MCLK, BICK and LRCK) can be stopped in the power-down mode (PDN = "L").
(5) Please mute the analog output externally if the click noise (3) influences system application. The timing example is shown in this figure.
(6) DZF pins of all channels are "L" in the power-down mode (PDN = "L").

Figure 6. Power-down/up sequence example

■ Reset Function

When RSTN=0, all DACs are powered down but the internal register values are not initialized. The analog outputs go to VCOM voltage and DZF pins of all channels go to "H". Figure 7 shows the sequence of reset by RSTN bit.



Notes:

(1) The analog output corresponding to digital input has the group delay (GD).
(2) Analog outputs go to VCOM voltage.
(3) Click noise occurs at the edges("↑ ↓") of the internal timing of RSTN bit. This noise is output even if "0" data is input.
(4) The external clocks (MCLK, BICK and LRCK) can be stopped in the reset mode (RSTN = "L").
(5) DZF pins go to "H" when the RSTN bit becomes "0", and go to "L" at 4~5/fs after RSTN bit becomes "1".
(6) There is a delay, 2~3/fs from RSTN bit "1" to the internal RSTN "1".

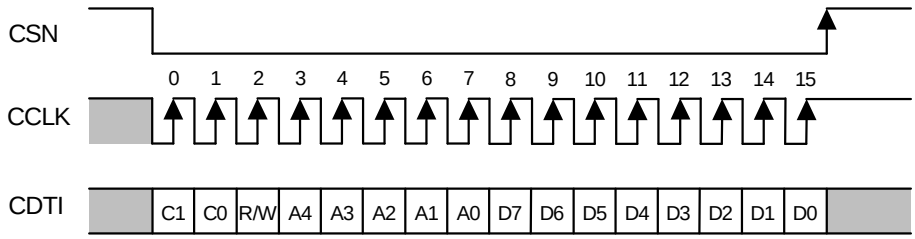
Figure 7. Reset sequence example

■ Serial Control Interface

The AK4356 can control its functions via both pins and registers. CKS2-0, DIF2-0, DFS0, DZFE and SMUTE pins are ORed with their registers.

Internal registers may be written to the 3 wire uP interface pins: CSN, CCLK & CDTI. The data on this interface consists of Chip address (2bits, CAD0/1), Read/Write (1bit), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data is clocked in on the rising edge of CCLK. Data is latched after a low-to-high transition of CSN. The clock speed of CCLK is 5MHz(max). The CSN pin should be held to "H" except for access.

The chip address is determined by the state of the CAD0 and CAD1 inputs. PDN = "L" initializes the registers to their default values. Writing "0" to the RSTN bit can initialize the internal timing circuit. But in this case, the register data is not be initialized.



C1-C0: Chip Address (C1=CAD1, C0=CAD0)
R/W: Read/Write (Fixed to "1" : Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 7. Control I/F Timing

Function	Pin set-up	Register set-up
Double Speed	O	O
4 times Speed	X	O
De-emphasis	X	O
DZFE	O	O
DZFM	X	O
SMUTE	O	O
Attenuator	X	O
Slow roll-off response	X	O

Table 6. Function Table (O: Supported, X: Not supported)

Note: Writing to control register is inhibited when PDN = "L" or the MCLK is not fed.

■ Mapping of Program Registers

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	0	SLOW	DZFM	DZFE	DIF2	DIF1	DIF0	RSTN
01H	Control 2	0	0	0	CKS2	CKS1	CKS0	SMUTE	RSTN
02H	Speed & Power Down Control	0	0	DFS1	DFS0	PW3	PW2	PW1	RSTN
03H	De-emphasis Control	0	0	DEMC1	DEMC0	DEMB1	DEMB0	DEMA1	DEMA0
04H	LOUT1 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
05H	ROUT1 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
06H	LOUT2 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
07H	ROUT2 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
08H	LOUT3 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
09H	ROUT3 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0AH	Test Mode	0	0	0	TEST4	TEST3	TEST2	TEST1	TEST0

Note: For addresses from 0BH to 1FH, data is not written.

When PDN goes to “L”, the registers are initialized to their default values.

When RSTN bit goes to “0”, the internal timing is reset, DZF pins of all channels go to “H” but registers are not initialized to their default values.

DZFE, DIF2-0, CKS2-0, SMUTE and DFS0 are ORed with pins.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	0	SLOW	DZFM	DZFE	DIF2	DIF1	DIF0	RSTN
Default		0	0	0	0	0	0	0	1

RSTN: Internal timing reset
0: Reset. DZF pins of all channels go to "H" and registers are not initialized.
1: Normal operation
When the states of SLOW, DIF2-0, CKS2-0 or DFS0-1 changes, the AK4356 should be reset by PDN pin or RSTN bit. Some click noise occurs at that timing.

DIF2-0: Audio data interface modes (See Table 3.)
Initial: "000", Mode 0
Register bits of DIF2-0 are ORed with the DFS2-0 pins.

DZFE: Data Zero Detect Enable
0: Disable
1: Enable
Zero detect function can be disabled by DZFE bit. In this case, the DZF pins of all channels are always "L". Register bit of DZFE is ORed with the DZFE pin.

DZFM: Data Zero Detect Mode
0: Channel Separated Mode
1: Channel ANDed Mode
If the DZFM bit is set to "1", the DZF pins of all channels go to "H" only when the input data at all channels are continuously zeros for 8192 LRCK cycles.

SLOW: Slow roll-off response enable
0: Disable
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	0	0	0	CKS2	CKS1	CKS0	SMUTE	RSTN
Default		0	0	0	0	0	0	0	1

RSTN: Internal timing reset
0: Reset. DZF pins of all channels go to "H" and registers are not initialized.
1: Normal operation
When the states of SLOW, DIF2-0, CKS2-0 or DFS0-1 changes, the AK4356 should be reset by PDN pin or RSTN bit. Some click noise occurs at that timing.

SMUTE: Soft Mute Enable
0: Normal operation
1: All DAC outputs soft-muted
Register bit of SMUTE is ORed with the SMUTE pin.

CKS2-0: Master Clock Frequency Select (See Table 2.)
Initial: "000", Mode 0
Register bits of CKS2-0 are ORed with the CKS2-0 pins.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Speed & Power Down Control	0	0	DFS1	DFS0	PW3	PW2	PW1	RSTN
Default		0	0	0	0	1	1	1	1

RSTN: Internal timing reset

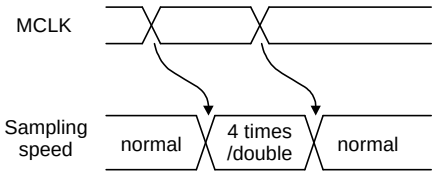
0: Reset. DZF pins of all channels go to "H" and registers are not initialized.
1: Normal operation
When the states of SLOW, DIF2-0, CKS2-0 or DFS0-1 changes, the AK4356 should be reset by PDN pin or RSTN bit. Some click noise occurs at that timing.

PW3-1: Power-down control (0: Power-down, 1: Power-up)

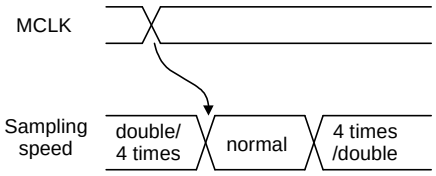
PW1: Power down control of DAC1
PW2: Power down control of DAC2
PW3: Power down control of DAC3
All sections are powered-down by PW1=PW2=PW3=0.

DFS1-0: Sampling speed control (See Table 1.)

00: Normal speed
01: Double speed
10: 4 times speed (DAC2 and DAC3 are automatically powered down.)
Register bit of DFS0 is ORed with the DFS0 pin.
When sampling speed mode is changed between normal and double/4 times speed mode, DFS1-0 bit should be changed after changing MCLK frequency (figure below). Some click noise occurs at this timing.



When sampling speed mode is changed between double and 4 times speed mode, sampling mode should be changed to normal speed mode after changing MCLK frequency, and then it should be changed to double/4 times speed mode (figure below). Some click noise occurs at those changing timing.



Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	De-emphasis Control	0	0	DEMC1	DEMC0	DEMB1	DEMB0	DEMA1	DEMA0
Default		0	0	0	1	0	1	0	1

DEMA1-0: De-emphasis response control for DAC1 data on SDTI1 (See Table 4,5.)
Initial: "01", OFF

DEMB1-0: De-emphasis response control for DAC2 data on SDTI2 (See Table 4,5.)
Initial: "01", OFF

DEMC1-0: De-emphasis response control for DAC3 data on SDTI3 (See Table 4,5.)
Initial: "01", OFF

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	LOUT1 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
05H	ROUT1 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
06H	LOUT2 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
07H	ROUT2 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
08H	LOUT3 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
09H	ROUT3 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
Default		1	1	1	1	1	1	1	1

ATT7-0: Attenuation Level
256 levels, 0.5dB step

ATT7-0	Attenuation
FFH	0dB
FEH	-0.5dB
FDH	-1.0dB
:	:
:	:
02H	-126.5dB
01H	-127.0dB
00H	MUTE (-∞)

The transition between set values is soft transition of 7425 levels. It takes 7424/fs (168ms@fs=44.1kHz) from FFH(0dB) to 00H(MUTE).
If PDN pin goes to "L", the ATTs are initialized to FFH.
The ATTs are FFH when RSTN = "0". When RSTN return to "1", the ATTs fade to their current value.
Digital attenuator is independent of soft mute function.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Test Mode	0	0	0	TEST4	TEST3	TEST2	TEST1	TEST0
Default		0	0	0	0	0	0	0	0

TEST4-0: Test mode

SYSTEM DESIGN

Figure 8 shows the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

Condition: Chip Address="00"

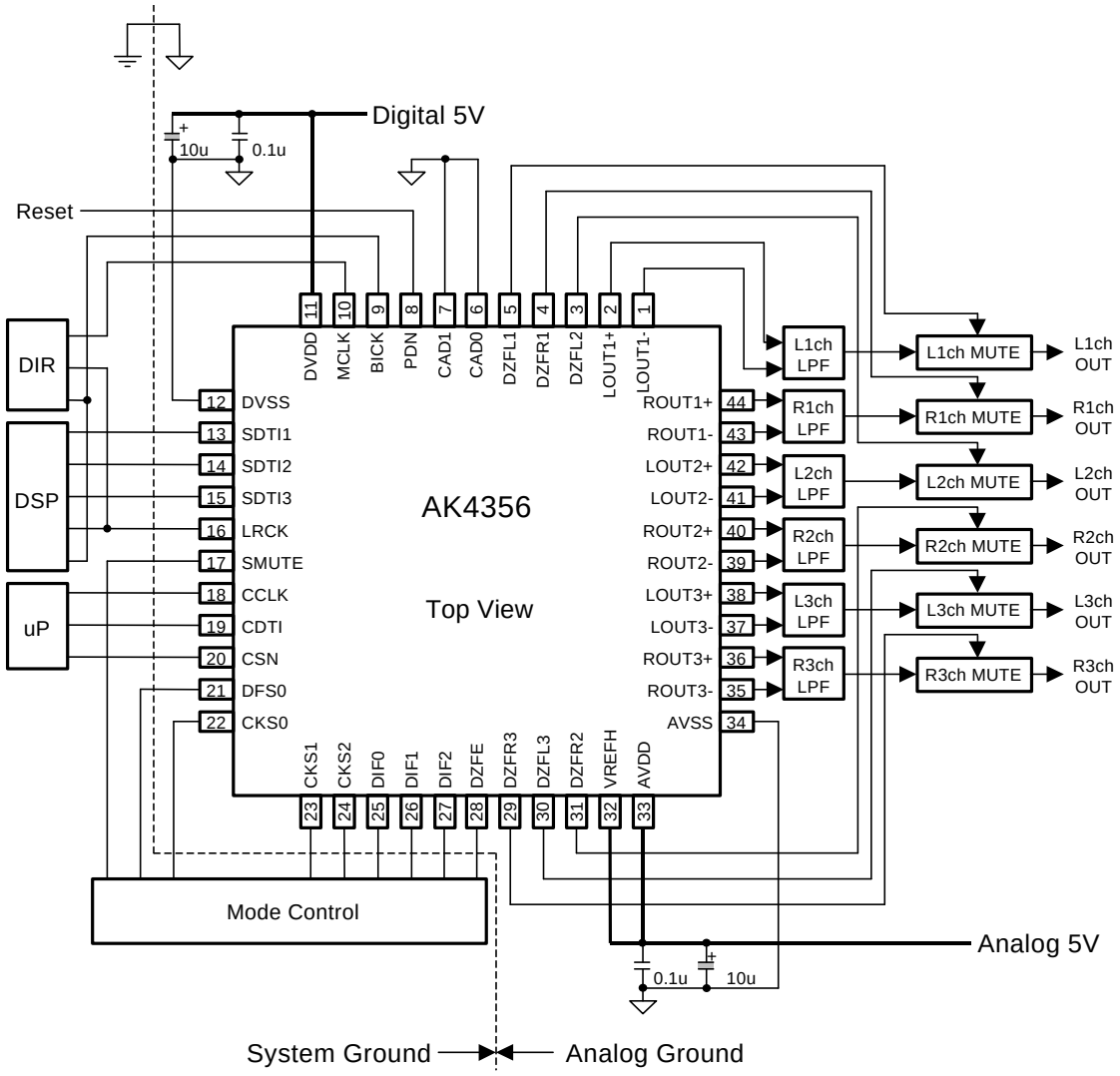


Figure 8. Typical Connection Diagram

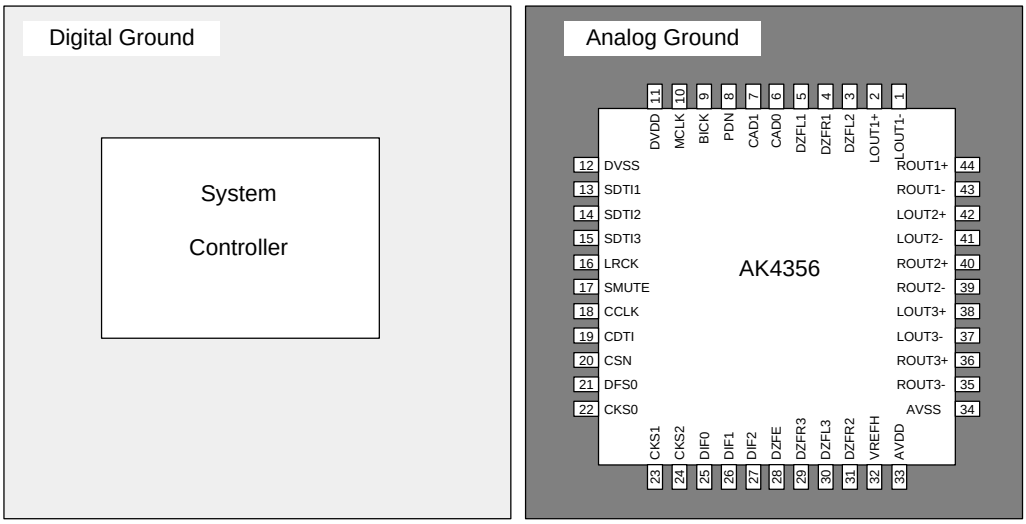


Figure 9. Ground Layout

Note: AVSS and DVSS must be connected to the same analog ground plane.

1. Grounding and Power Supply Decoupling

The AK4356 requires careful attention to power supply and grounding arrangements. AVDD and DVDD are usually supplied from analog supply in system. Alternatively if AVDD and DVDD are supplied separately, the power up sequence is not critical. **AVSS and DVSS of the AK4356 must be connected to analog ground plane**. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be near to the AK4356 as possible, with the small value ceramic capacitors being the nearest.

2. Voltage Reference Inputs

VREFH sets the analog output range. VREFH pin is normally connected to AVDD with a 0.1μF ceramic capacitor. All signals, especially clocks, should be kept away from the VREFH pin in order to avoid unwanted coupling into the AK4356.

3. Analog Outputs

The analog outputs are full-differential outputs and 0.55 x VREFH Vpp (typ) centered around the internal common voltage (about AVDD/2). The differential outputs are summed externally, V_{AOUT}=(AOUT+)-(AOUT-) between AOUT+ and AOUT-. If the summing gain is 1, the output range is 5.5Vpp (typ @VREFH=5V). The bias voltage of the external summing circuit is supplied externally. The input data format is 2's complement. The output voltage(V_{AOUT}) is a positive full scale for 7FFFFF(@24bit) and a negative full scale for 800000H(@24bit). The ideal V_{AOUT} is 0V for 000000H(@24bit).

The internal switched-capacitor filter and external low pass filter attenuate the noise generated by the delta-sigma modulator beyond the audio passband.

DC offset on AOUT+/- is eliminated without AC coupling since the analog outputs are differential. Figure 10 and 11 show the example of external op-amp circuit summing the differential outputs.

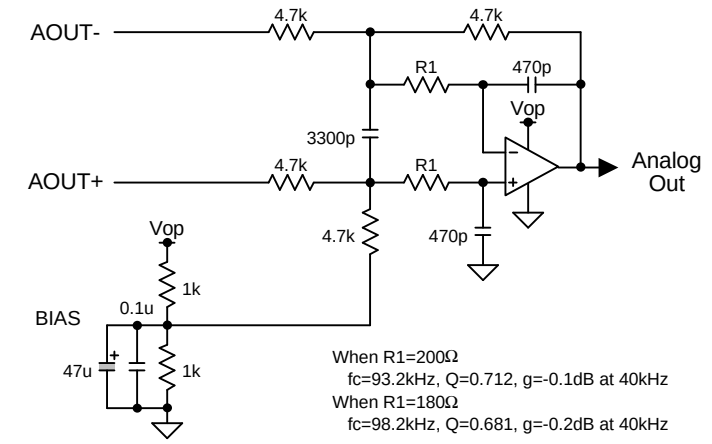


Figure 10. External 2nd order LPF Circuit Example (using op-amp with single power supply)

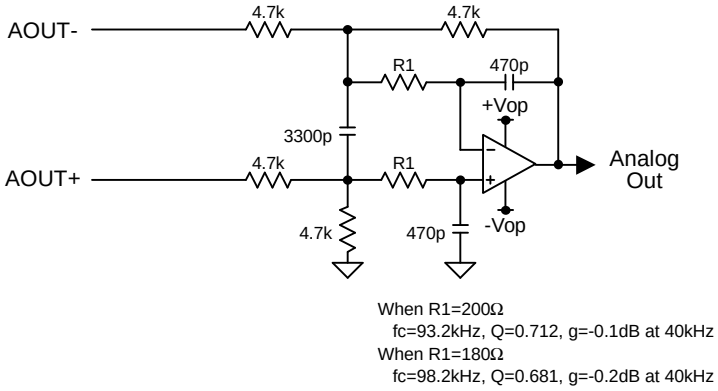
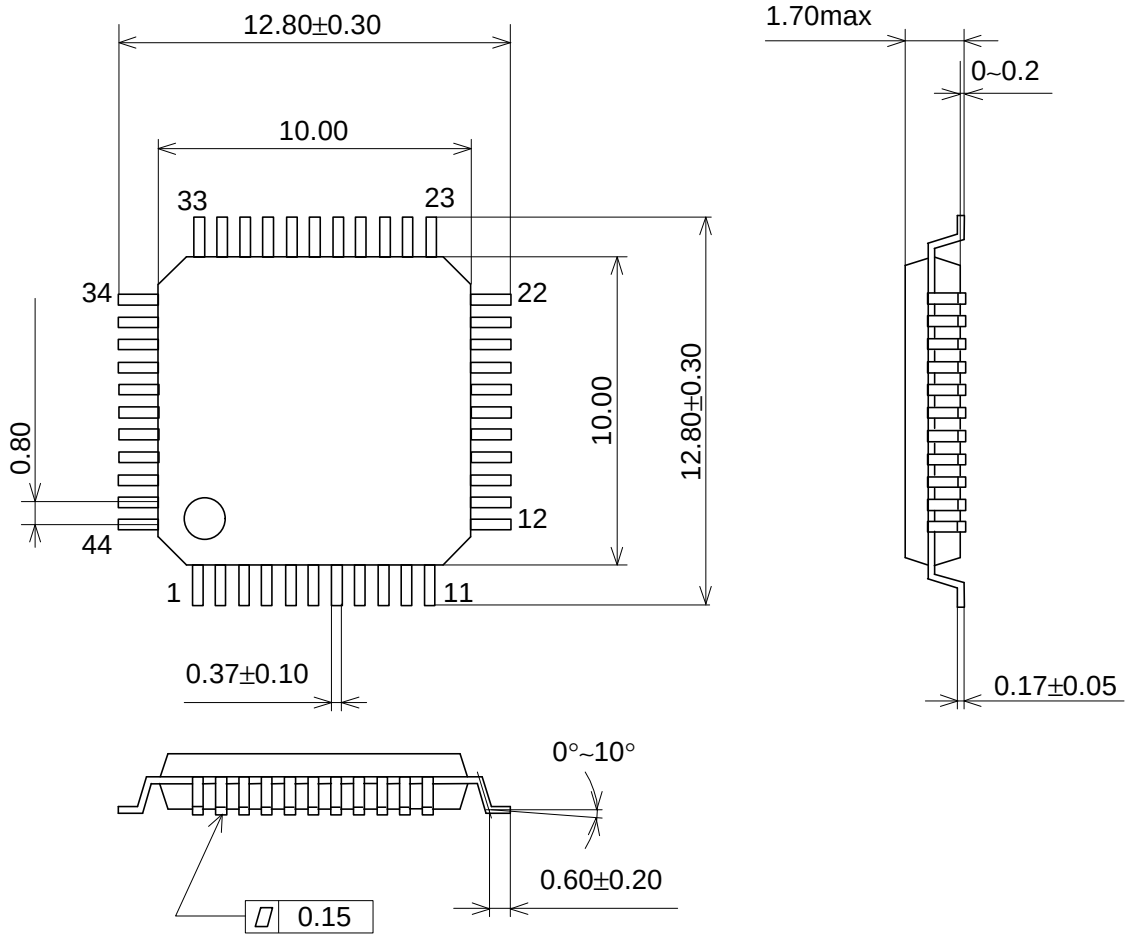


Figure 11. External 2nd order LPF Circuit Example (using op-amp with dual power supplies)

PACKAGE

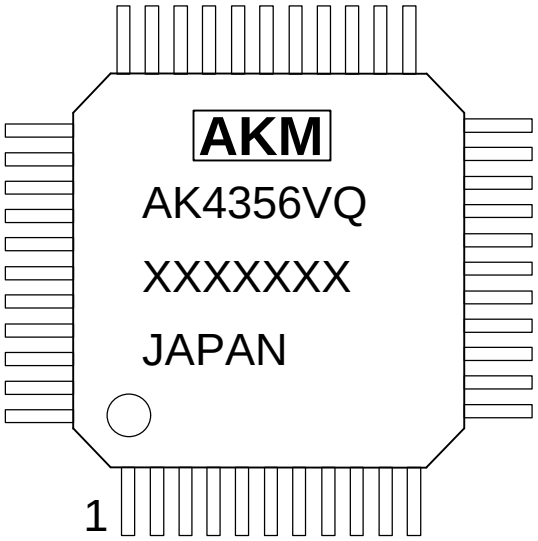
44pin LQFP (Unit: mm)



■ **Package & Lead frame material**

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate

MARKING



1) Pin #1 indication
2) Date Code: XXXXXXX(7 digits)
3) Marking Code: AK4356VQ
4) Country of Origin
5) Asahi Kasei Logo

Appendix A

In Double and 4 times Speed Modes, the phase relationship between MCLK and LRCK/BICK is limited (Table 7). If the phase relationship happens during this prohibited period, it is possible to occur the inverse of output channel. The phase relationship must be set to avoid the prohibited period when the AK4356 operates at Double Speed Mode or 4 times Speed Mode. The prohibited period is specified by the combination of digital power supply voltage (DVDD), MCLK frequency and audio data format (Table 3). When the audio data formats are 16/20/24bit LSB Justified (Mode 0,1,4) and 24bit MSB Justified (Mode 2), the phase relationship (tLRM: Figure 12) between the rising edge of LRCK and the rising edge of MCLK has the prohibited period of min to max in Table 7. In case of I^2S Compatible (Mode 3), the relationship between the falling edge of BICK and the rising edge of MCLK has the prohibited period (tBCM: Figure 13)

Sampling Mode	Digital Power Supply, DVDD	MCLK Frequency	Mode Setting					Prohibited Period		Units
			CKS2	CKS1	CKS0	DFS1	DFS0	min	max	
Double Speed	4.75 to 5.25V	128fs	0	0	0	0	1	0.1	0.6	ns
Double Speed	4.75 to 5.25V	192fs	0	1	0	0	1	-0.6	-0.1	ns
Double Speed	4.75 to 5.25V	256fs	0	0	1	0	1	-0.7	-0.2	ns
Double Speed	4.75 to 5.25V	256fs	1	0	0	0	1	-0.7	-0.2	ns
Double Speed	4.75 to 5.25V	384fs	0	1	1	0	1	-1.4	-0.9	ns
Double Speed	4.75 to 5.25V	384fs	1	1	0	0	1	-1.4	-0.9	ns
4 times Speed	4.75 to 5.25V	128fs	1	0	0	1	0	-0.7	-0.2	ns
4 times Speed	4.75 to 5.25V	192fs	1	1	0	1	0	-1.4	-0.9	ns

Table **7**. Prohibited Period

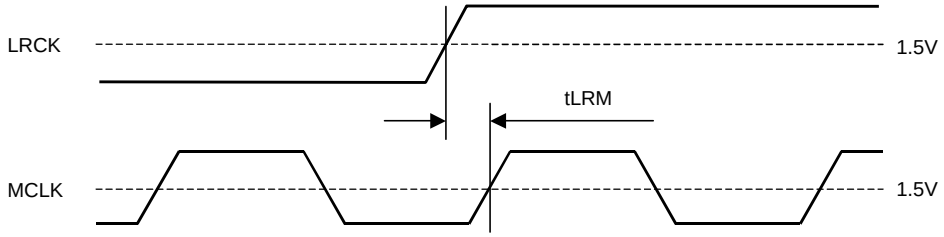


Figure 12. 16/20/24bit LSB Justified, 24bit MSB Justified

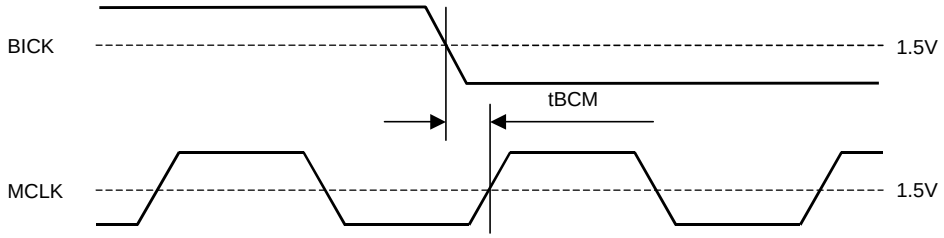


Figure 13. I^2S Compatible

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