A1324, A1325, and A1326

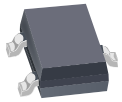
Low Noise, Linear Hall Effect Sensor ICs with Analog Output

Features and Benefits

- Temperature-stable quiescent output voltage and sensitivity
- Output voltage proportional to magnetic flux density
- Low-noise output increases accuracy
- Precise recoverability after temperature cycling
- Ratiometric rail-to-rail output
- Wide ambient temperature range: –40°C to 150°C
- Immune to mechanical stress
- Solid-state reliability
- Enhanced EMC performance for stringent automotive applications

Packages

3-pin ultramini SIP 1.5 mm × 4 mm × 3 mm (suffix UA)	3-pin SOT23-W 2 mm × 3 mm × 1 mm (suffix LH)



Approximate footprint

Description

New applications for linear output Hall-effect devices, such as displacement, angular position, and current measurement, require high accuracy in conjunction with small package size. The Allegro™ A1324, A1325, and A1326 linear Hall-effect sensor ICs are designed specifically to achieve both goals. This temperature-stable device is available in a miniature surface mount package (SOT23W) and an ultra-mini through-hole single in-line package.

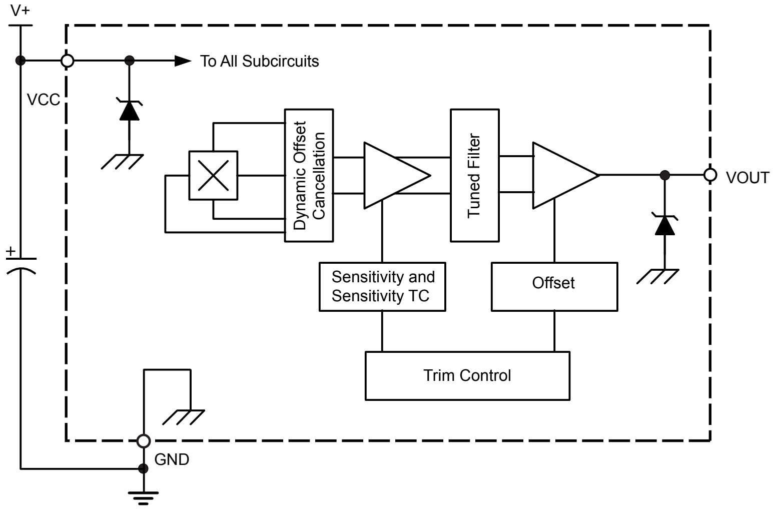
These ratiometric Hall effect sensor ICs provide a voltage output that is proportional to the applied magnetic field. They feature a quiescent voltage output of 50% of the supply voltage. The A1324/25/26 feature factory programmed sensitivities of 5.0 mV/G, 3.125 mV/G, and 2.5 mV/G, respectively.

The features of these linear devices make them ideal for use in automotive and industrial applications requiring high accuracy, and operate through an extended temperature range, –40°C to 150°C.

Each BiCMOS monolithic circuit integrates a Hall element, temperature-compensating circuitry to reduce the intrinsic sensitivity drift of the Hall element, a small-signal high-gain amplifier, a clamped low-impedance output stage, and a proprietary dynamic offset cancellation technique.

These devices are available in a 3-pin ultra-mini SIP package (UA), and a 3-pin surface mount SOT-23 style package (LH). Both are lead (Pb) free, with 100% matte tin leadframe plating.

Functional Block Diagram



Selection Guide

Part Number	Packing[1]	Package	Sensitivity (Typ.) (mV/G)
A1324LLHLT-T	3 000 pieces per reel	3-pin SOT-23W surface mount	5.000
A1324LLHLX-T	10 000 pieces per reel	3-pin SOT-23W surface mount	
A1324LUA-T[2]	500 pieces per bag	3-pin ultramini SIP through hole mount	
A1325LLHLT-T	3 000 pieces per reel	3-pin SOT-23W surface mount	3.125
A1325LLHLX-T	10 000 pieces per reel	3-pin SOT-23W surface mount	
A1325LUA-T[2]	500 pieces per bag	3-pin ultramini SIP through hole mount	
A1326LLHLT-T	3 000 pieces per reel	3-pin SOT-23W surface mount	2.500
A1326LLHLX-T	10 000 pieces per reel	3-pin SOT-23W surface mount	
A1326LUA-T[2]	500 pieces per bag	3-pin ultramini SIP through hole mount	

[1] Contact Allegro™ for additional packing options.
[2] Contact factory for availability.

Absolute Maximum Ratings

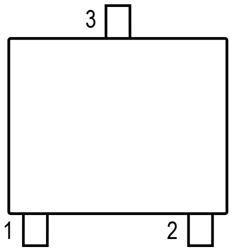
Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		8	V
Reverse Supply Voltage	V_{RCC}		–0.1	V
Forward Output Voltage	V_{OUT}		15	V
Reverse Output Voltage	V_{ROUT}		–0.1	V
Output Source Current	$I_{OUT(SOURCE)}$	VOUT to GND	2	mA
Output Sink Current	$I_{OUT(SINK)}$	VCC to VOUT	10	mA
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

Thermal Characteristics may require derating at maximum conditions, see application information

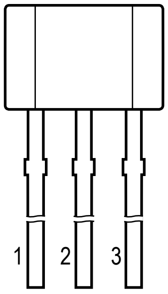
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Package LH, on 4-layer PCB with copper limited to solder pads	228	ºC/W
		Package LH, on 2-layer PCB with 0.463 in.^{2} of copper area each side, connected by thermal vias	110	ºC/W
		Package UA, on 1-layer PCB with copper limited to solder pads	165	ºC/W

*Additional thermal information available on the Allegro website

Pin-out Diagrams



LH Package



UA Package

Terminal List Table

Name	Number		Function
	LH	UA	
VCC	1	1	Input power supply; tie to GND with bypass capacitor
VOUT	2	3	Output signal; also used for programming
GND	3	2	Ground

OPERATING CHARACTERISTICS Valid throughout T_A range, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
Electrical Characteristics						
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Supply Current	I_{CC}	No load on VOUT	–	6.9	9	mA
Power-On Time[2]	t_{PO}	T_A = 25°C, C_L (PROBE) = 10 pF	–	32	–	µs
Supply Zener Clamp Voltage	V_Z	T_A = 25°C, I_{CC} = 12 mA	6	8.3	–	V
Internal Bandwidth	BW_i	Small signal, –3 dB	–	17	–	kHz
Chopping Frequency[3]	f_C	T_A = 25°C	–	400	–	kHz
Output Characteristics						
Quiescent Voltage Output	$V_{OUT(Q)}$	B = 0 G, T_A = 25°C	2.425	2.500	2.575	V
Output Referred Noise	V_N	A1324, T_A = 25°C, C_{BYPASS} = 0.1 µF	–	7.0	–	$mV_{(p-p)}$
		A1325, T_A = 25°C, C_{BYPASS} = 0.1 µF	–	4.4	–	$mV_{(p-p)}$
		A1326, T_A = 25°C, C_{BYPASS} = 0.1 µF	–	3.5	–	$mV_{(p-p)}$
Input Referred RMS Noise Density	V_{NRMS}	T_A = 25°C, C_{BYPASS} = open, no load on VOUT, f << BW_i	–	1.3	–	mG/√Hz
DC Output Resistance	R_{OUT}		–	< 1	–	Ω
Output Load Resistance	R_L	VOUT to VCC	4.7	–	–	kΩ
		VOUT to GND	4.7	–	–	kΩ
Output Load Capacitance	C_L	VOUT to GND	–	–	10	nF
Output Saturation Voltage	$V_{OUT(sat)HIGH}$	$R_{PULLDOWN}$ = 4.7 kΩ, V_{CC} = 5 V	4.7	–	–	V
	$V_{OUT(sat)LOW}$	R_{PULLUP} = 4.7 kΩ, V_{CC} = 5 V	–	–	0.30	V
Magnetic Characteristics						
Sensitivity	Sens	A1324, T_A = 25°C	4.750	5.000	5.250	mV/G
		A1325, T_A = 25°C	2.969	3.125	3.281	mV/G
		A1326, T_A = 25°C	2.375	2.500	2.625	mV/G
Sensitivity Temperature Coefficient	TC_{Sens}	LH package; programmed at T_A = 150°C, calculated relative to Sens at 25°C	–	0	–	%/°C
		UA package; programmed at T_A = 150°C, calculated relative to Sens at 25°C	–	0.03	–	%/°C
Error Components						
Sensitivity Drift at Maximum Ambient Operating Temperature	$\Delta Sens_{(TAmax)}$	LH package; from hot to room temperature	–5	–	5	%
		UA package; from hot to room temperature	–2.5	–	7.5	%
Sensitivity Drift at Minimum Ambient Operating Temperature	$\Delta Sens_{(TAmin)}$	LH package; from cold to room temperature	–3.5	–	8.5	%
		UA package; from cold to room temperature	–6	–	4	%

Continued on the next page…

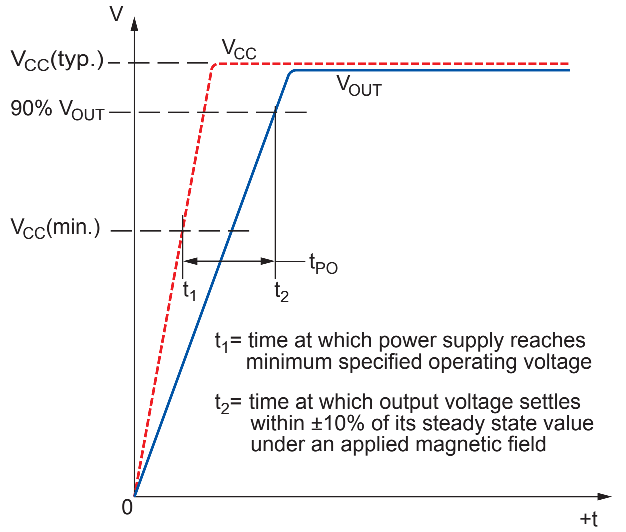
OPERATING CHARACTERISTICS (continued) Valid throughout T_A range, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
Error Components (continued)						
Quiescent Voltage Output Drift Through Temperature Range	$\Delta V_{OUT(Q)}$	Defined in terms of magnetic flux density, B	–10	–	10	G
Linearity Sensitivity Error	Lin_{ERR}		–1.5	–	1.5	%
Symmetry Sensitivity Error	Sym_{ERR}		–1.5	–	1.5	%
Ratiometry Quiescent Voltage Output Error[4]	$Rat_{VOUT(Q)}$	Throughout supply voltage range (relative to V_{CC} = 5 V)	–1.3	–	1.3	%
Ratiometry Sensitivity Error[4]	Rat_{Sens}	Throughout supply voltage range (relative to V_{CC} = 5 V), T_A = 25°C and 150°C	–1.5	–	1.5	%
		Throughout supply voltage range (relative to V_{CC} = 5 V), T_A = –40°C	–2	–	2	%
Sensitivity Drift Due to Package Hysteresis	$\Delta Sens_{PKG}$	T_A = 25°C, after temperature cycling	–	±2	–	%

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] See Characteristic Definitions section.
[3] f_C varies up to approximately ±20% over the full operating ambient temperature range and process.
[4] Percent change from actual value at V_{CC} = 5 V, for a given temperature.

Characteristic Definitions

Power-On Time When the supply is ramped to its operating voltage, the device output requires a finite time to react to an input magnetic field. Power-On Time is defined as the time it takes for the output voltage to begin responding to an applied magnetic field after the power supply has reached its minimum specified operating voltage, V_{CC}(min).



Quiescent Voltage Output In the quiescent state (that is, with no significant magnetic field: B = 0), the output, $V_{OUT(Q)}$, equals a ratio of the supply voltage, V_{CC}, throughout the entire operating range of V_{CC} and the ambient temperature, T_A.

Quiescent Voltage Output Drift Through Temperature Range Due to internal component tolerances and thermal considerations, the quiescent voltage output, $V_{OUT(Q)}$, may drift from its nominal value through the operating ambient temperature range, T_A. For purposes of specification, the Quiescent Voltage Output Drift Through Temperature Range, $\Delta V_{OUT(Q)}$ (mV), is defined as:

$$\Delta V_{OUT(Q)} = V_{OUT(Q)TA} - V_{OUT(Q)25°C} \qquad (1)$$

Sensitivity The presence of a south-polarity magnetic field perpendicular to the branded surface of the package increases the output voltage from its quiescent value toward the supply voltage rail. The amount of the output voltage increase is proportional to the magnitude of the magnetic field applied. Conversely, the application of a north polarity field will decrease the output voltage from its quiescent value. This proportionality is specified as the magnetic sensitivity, Sens (mV/G), of the device and is defined as:

$$\text{Sens} = \frac{V_{OUT(B+)} - V_{OUT(B-)}}{B(+) - B(-)} \qquad (2)$$

where B(+) and B(–) are two magnetic fields with opposite polarities.

Sensitivity Temperature Coefficient The device sensitivity changes with temperature, with respect to its sensitivity temperature coefficient, TC_{SENS}. TC_{SENS} is programmed at 150°C, and calculated relative to the nominal sensitivity programming temperature of 25°C. TC_{SENS} (%/°C) is defined as:

$$TC_{Sens} = \left(\frac{\text{Sens}_{T2} - \text{Sens}_{T1}}{\text{Sens}_{T1}} \times 100\%\right)\left(\frac{1}{T2-T1}\right) \qquad (3)$$

where T1 is the nominal Sens programming temperature of 25°C, and T2 is the TC_{SENS} programming temperature of 150°C.

The ideal value of sensitivity through the temperature range, $\text{Sens}_{IDEAL(TA)}$, is defined as:

$$\text{Sens}_{IDEAL(TA)} = \text{Sens}_{T1} \times (100\% + TC_{SENS(TA-T1)}) \qquad (4)$$

Sensitivity Drift Through Temperature Range Second order sensitivity temperature coefficient effects cause the magnetic sensitivity to drift from its ideal value through the operating ambient temperature, T_A. For purposes of specification, the sensitivity drift through temperature range, ΔSens_{TC}, is defined as:

$$\Delta\text{Sens}_{TC} = \frac{\text{Sens}_{TA} - \text{Sens}_{IDEAL(TA)}}{\text{Sens}_{IDEAL(TA)}} \times 100\% \qquad (5)$$

Sensitivity Drift Due to Package Hysteresis Package stress and relaxation can cause the device sensitivity at T_A = 25°C to change during or after temperature cycling. This change in sensitivity follows a hysteresis curve.

For purposes of specification, the Sensitivity Drift Due to Package Hysteresis, ΔSens_{PKG}, is defined as:

$$\Delta\text{Sens}_{PKG} = \frac{\text{Sens}_{(25°C)2} - \text{Sens}_{(25°C)1}}{\text{Sens}_{(25°C)1}} \times 100\% \qquad (6)$$

where $\text{Sens}_{(25°C)1}$ is the programmed value of sensitivity at

T_A = 25°C, and $\mathrm{Sens}_{(25°C)1}$ is the value of sensitivity at T_A = 25°C after temperature cycling T_A up to 150°C, down to –40°C, and back to up 25°C.

Linearity Sensitivity Error The 132x is designed to provide linear output in response to a ramping applied magnetic field. Consider two magnetic fields, B1 and B2. Ideally the sensitivity of a device is the same for both fields for a given supply voltage and temperature. Linearity sensitivity error is present when there is a difference between the sensitivities measured at B1 and B2.

Linearity Sensitivity Error is calculated separately for the positive ($\mathrm{LIN}_{\mathrm{ERR+}}$) and negative ($\mathrm{LIN}_{\mathrm{ERR-}}$) applied magnetic fields. Linearity Sensitivity Error (%) is measured and defined as:

$$\mathrm{Lin}_{\mathrm{ERR+}} = \left(1-\frac{\mathrm{Sens}_{\mathrm{B}(++)}}{\mathrm{Sens}_{\mathrm{B}(+)}}\right)\times 100\%$$

$$\mathrm{Lin}_{\mathrm{ERR-}} = \left(1-\frac{\mathrm{Sens}_{\mathrm{B}(--)}}{\mathrm{Sens}_{\mathrm{B}(-)}}\right)\times 100\% \qquad (7)$$

and

$$\mathrm{Lin}_{\mathrm{ERR}} = \max(|\mathrm{Lin}_{\mathrm{ERR+}}|\,,\ |\mathrm{Lin}_{\mathrm{ERR-}}|\,) \qquad (8)$$

where:

$$\mathrm{Sens}_{\mathrm{Bx}} = \left(\frac{|V_{\mathrm{OUT(Bx)}} - V_{\mathrm{OUT(Q)}}|}{B_{\mathrm{X}}}\right) \qquad (9)$$

and B(++), B(+), B(––), and B(–) are positive and negative magnetic fields with respect to the quiescent voltage output such that |B(++)| > |B(+)| and |B(––)| > |B(–)| .

Symmetry Sensitivity Error The magnetic sensitivity of a device is constant for any two applied magnetic fields of equal magnitude and opposite polarities.

Symmetry Error (%), is measured and defined as:

$$\mathrm{Sym}_{\mathrm{ERR}} = \left(1-\frac{\mathrm{Sens}_{\mathrm{B}(+)}}{\mathrm{Sens}_{\mathrm{B}(-)}}\right)\times 100\% \qquad (11)$$

where $\mathrm{Sens}_{\mathrm{Bx}}$ is defined as in equation 9, and B(+), B(–) are positive and negative magnetic fields such that |B(+)| = |B(–)|.

Ratiometry Error The A132x features a ratiometric output. This means that the quiescent voltage output, $V_{\mathrm{OUT(Q)}}$, magnetic sensitivity, Sens, and clamp voltages, V_{CLPHIGH} and V_{CLPLOW}, are proportional to the supply voltage, V_{CC}. In other words, when the supply voltage increases or decreases by a certain percentage, each characteristic also increases or decreases by the same percentage. Error is the difference between the measured change in the supply voltage, relative to 5 V, and the measured change in each characteristic.

The ratiometric error in quiescent voltage output, $\mathrm{Rat}_{\mathrm{VOUT(Q)}}$ (%), for a given supply voltage, V_{CC}, is defined as:

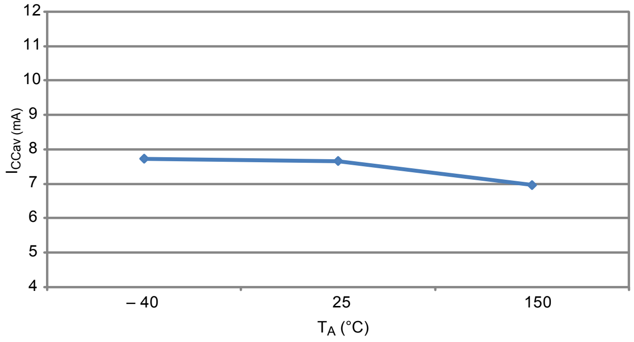
$$\mathrm{Rat}_{\mathrm{VOUT(Q)}} = \left(1-\frac{V_{\mathrm{OUT(Q)VCC}} \,/\, V_{\mathrm{OUT(Q)5V}}}{V_{\mathrm{CC}} \,/\, 5\ \mathrm{V}}\right)\times 100\% \qquad (12)$$

The ratiometric error in magnetic sensitivity, $\mathrm{Rat}_{\mathrm{SENS}}$ (%), for a given supply voltage, V_{CC}, is defined as:

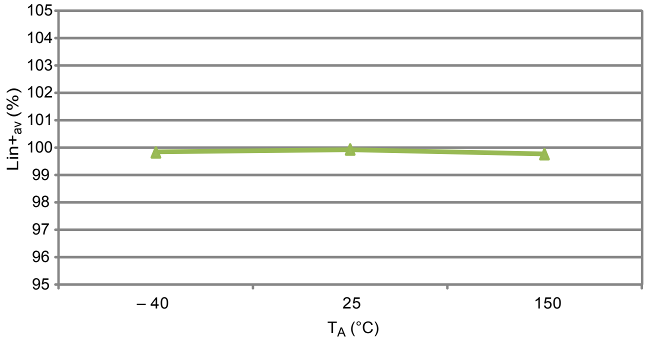
$$\mathrm{Rat}_{\mathrm{VOUT(Q)}} = \left(1-\frac{\mathrm{Sens}_{\mathrm{VCC}} \,/\, \mathrm{Sens}_{\mathrm{5V}}}{V_{\mathrm{CC}} \,/\, 5\ \mathrm{V}}\right)\times 100\% \qquad (13)$$

Typical Characteristics
(30 pieces, 3 fabrication lots)

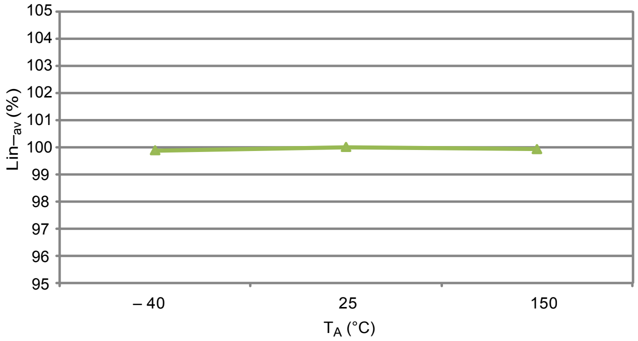
Average Supply Current versus Ambient Temperature
V_{CC} = 5 V



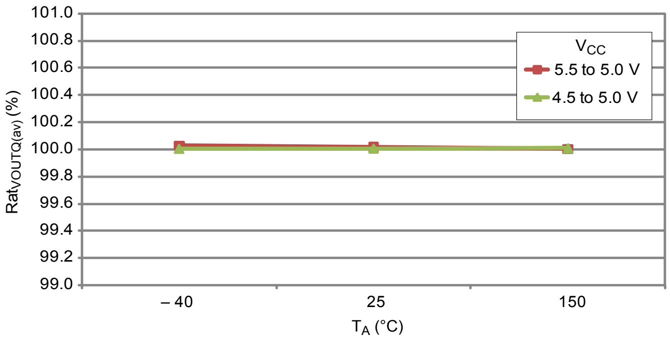
Average Postive Linearity versus Ambient Temperature
V_{CC} = 5 V



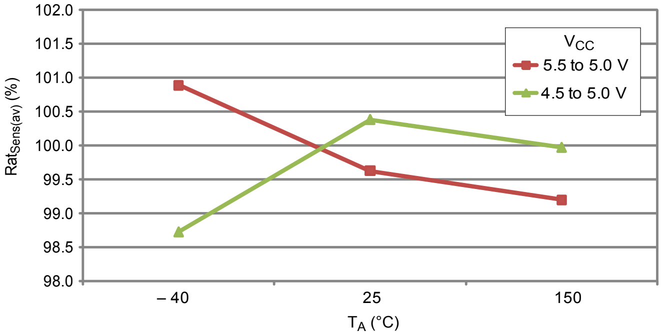
Average Negative Linearity versus Ambient Temperature
V_{CC} = 5 V



Average Quiescent Voltage Output Ratiometry versus Ambient Temperature

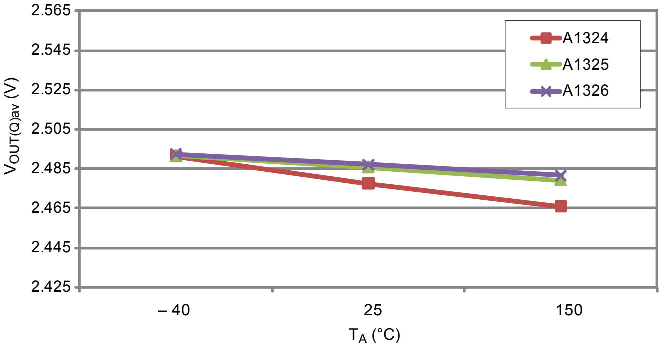


Average Sensitivity Ratiometry versus Ambient Temperature

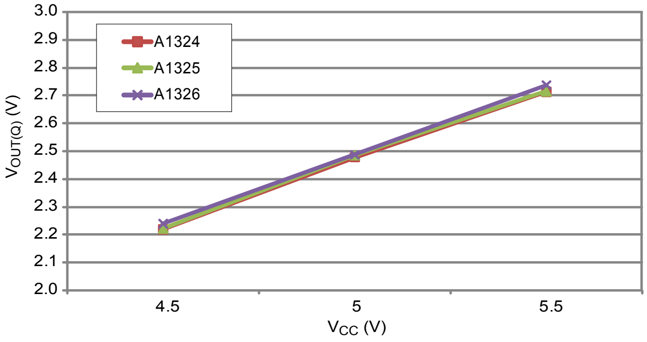


Typical Characteristics, continued
(30 pieces, 3 fabrication lots)

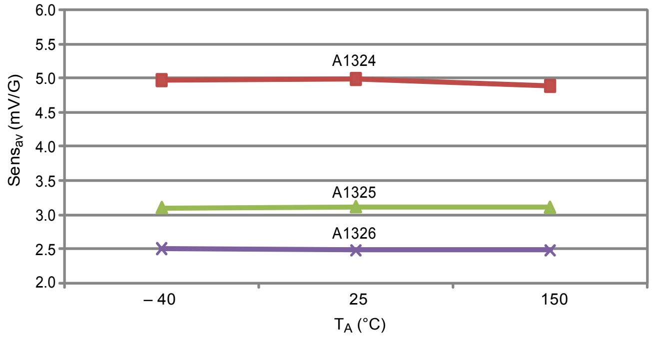
Average Absolute Quiescent Voltage Output versus Ambient Temperature
V_{CC} = 5 V



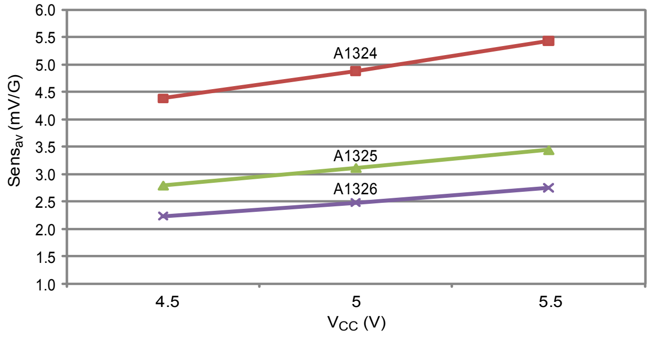
Quiescent Voltage Output versus Supply Voltage
T_A = 25°C



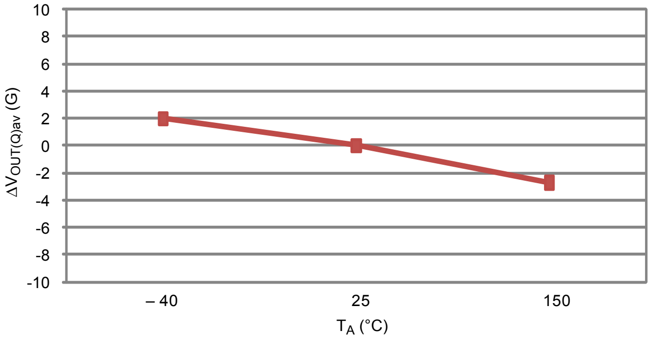
Average Absolute Sensitivity versus Ambient Temperature
V_{CC} = 5 V



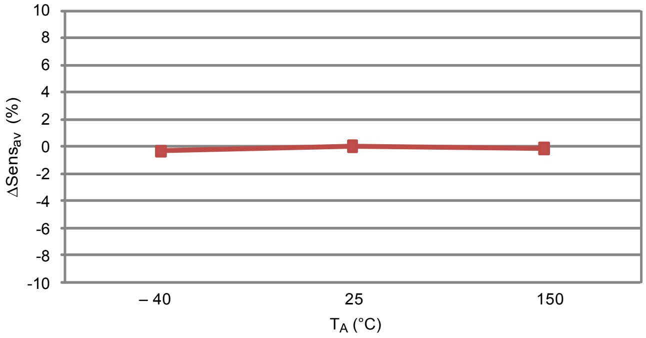
Average Sensitivity versus Supply Voltage
T_A = 25°C

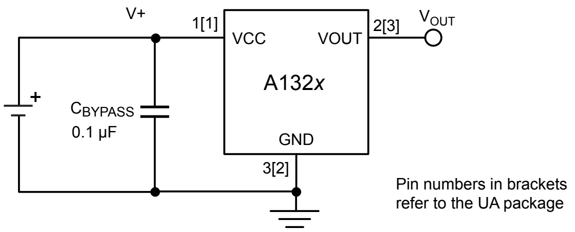


Average Quiescent Voltage Output Drift versus Ambient Temperature
$\Delta V_{OUT(Q)av}$ values relative to 25°C, V_{CC} = 5 V



Average Sensitivity Drift versus Ambient Temperature
$\Delta Sens_{av}$ values relative to 25°C, V_{CC} = 5 V

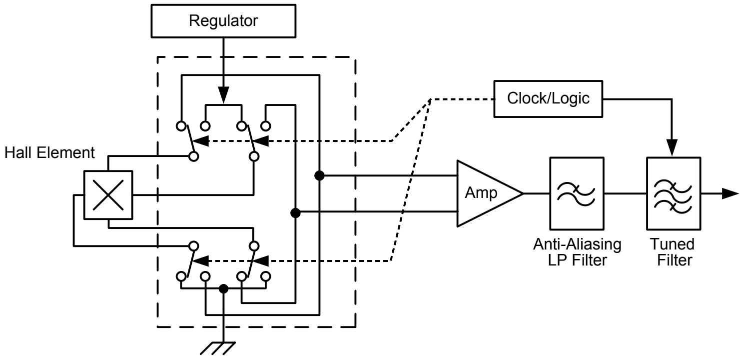




Typical Application Circuit

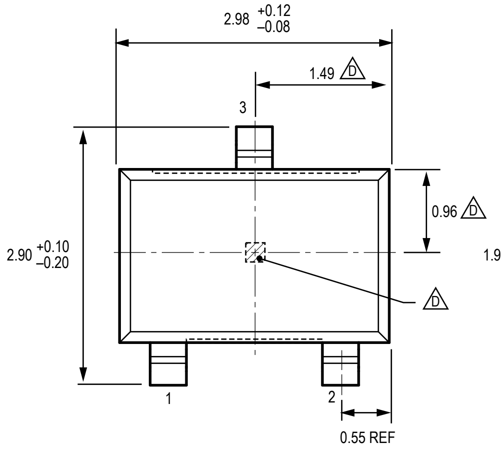
Chopper Stabilization Technique

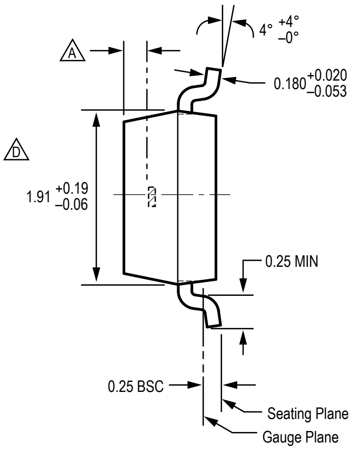
When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall IC. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip. Allegro employs a technique to remove key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at baseband, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. In addition to the removal of the thermal and stress related offset, this novel technique also reduces the amount of thermal noise in the Hall IC while completely removing the modulated residue resulting from the chopper operation. The chopper stabilization technique uses a high frequency sampling clock. For demodulation process, a sample-and-hold technique is used. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

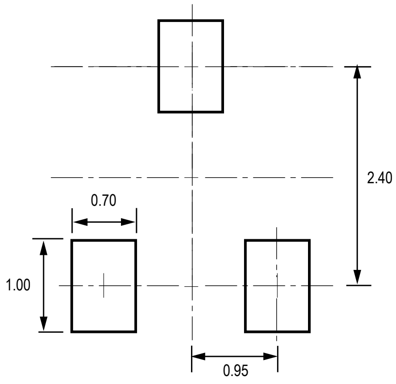


Concept of Chopper Stabilization Technique

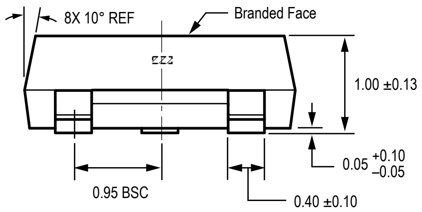
Package LH, 3-Pin SOT23W

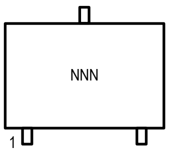






B PCB Layout Reference View





C Standard Branding Reference View

N = Last three digits of device part number

For Reference Only; not for tooling use (reference DWG-2840)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

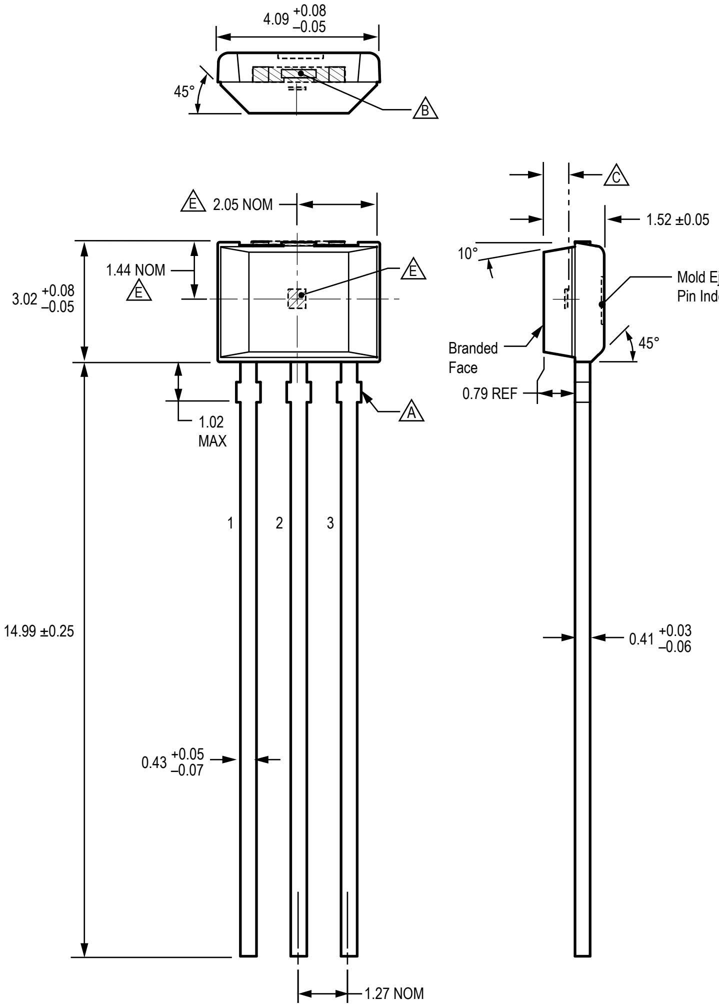
A Active Area Depth, 0.28 mm REF

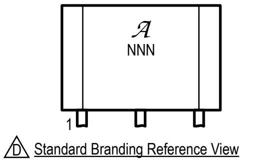
B Reference land pattern layout
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

D Hall element, not to scale

Package UA, 3-Pin SIP





D Standard Branding Reference View

= Supplier emblem
N = Last three digits of device part number

For Reference Only; not for tooling use (reference DWG-9065)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusi
Exact case and lead configuration at supplier discretion within limits

A Dambar removal protrusion (6X)
B Gate and tie bar burr area
C Active Area Depth, 0.50 mm REF
D Branding scale and appearance at supplier discretion
E Hall element (not to scale)

Revision History

Revision	Revision Date	Description of Revision
Rev. 3	September 16, 2013	Update product selection
Rev. 4	September 26, 2013	Fixed UA package drawing
Rev. 5	February 14, 2019	Minor editorial updates

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