A1335

Precision Hall-Effect Angle Sensor IC with I²C, SPI, and SENT Interfaces

FEATURES AND BENEFITS

- 360° contactless high-resolution angle position sensor
- Circular vertical Hall (CVH) technology
- Available with either a single die or dual independent die housed within a single package
- Digital output format selectable among serial port interface (SPI), inter-integrated circuit (I²C), and single-edge nibble transmission (SENT)
- SENT output is SAEJ2716 JAN2010-compliant, with Allegro-proprietary, enhanced, programmable features
- Customer-programmable SENT tick times, ranging from 0.5 to 7.9 µs
- SPI interface allows use of multiple independent sensor ICs for applications requiring redundancy
- Refresh rate: 32 µs, 12-bit resolution
- Programmable via Manchester encoding on the VCC line, reducing external wiring
- Automotive temperature range: –40°C to 150°C
- AEC-Q100 automotive qualified

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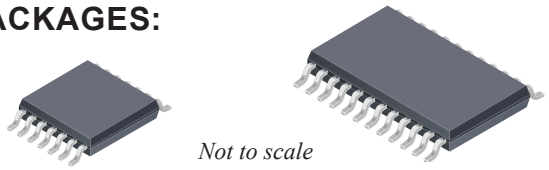
PACKAGES:



Not to scale

Single SoC, 14-pin TSSOP (suffix LE) **Dual Independent SoCs, 24-pin TSSOP (suffix LE)**

DESCRIPTION

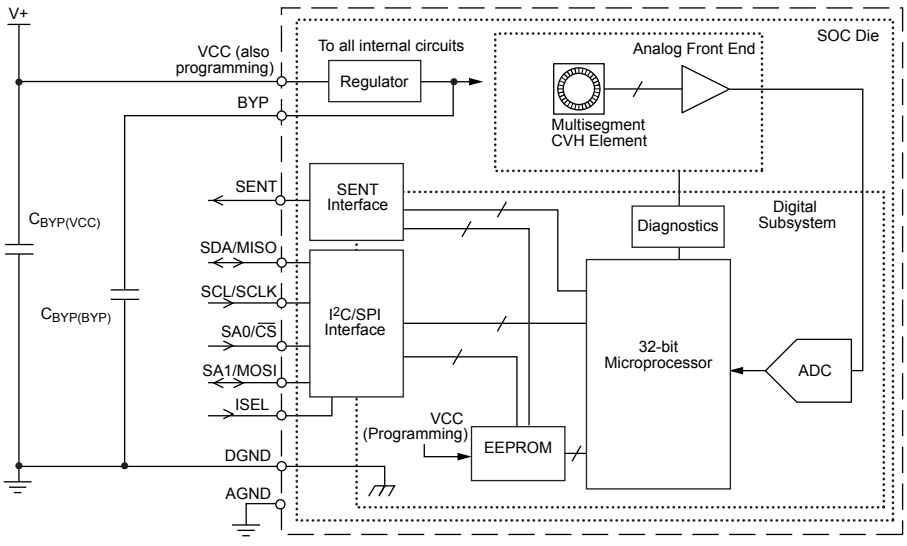
The A1335 is a 360° contactless high-resolution programmable magnetic angle position sensor IC. It is designed for digital systems and is capable of communicating via an I²C, SPI, or SENT interface.

This system-on-chip (SoC) architecture includes a front end based on circular vertical Hall (CVH) technology, programmable microprocessor-based signal processing, and an interface capable of supporting I²C, SPI, and SENT. In addition to providing full-turn angular measurement, the A1335 also provides scaling for angle measurement applications of less than 360°. It includes on-chip EEPROM technology, capable of supporting up to 100 read/write cycles, for flexible programming of calibration parameters.

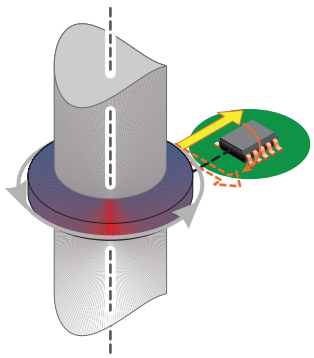
Digital signal processing functions, including temperature compensation and gain/offset trim, as well as advanced output linearization algorithms, provide an extremely accurate and linear output for both end-of-shaft applications and off-axis applications.

The A1335 is ideal for automotive applications requiring high-speed 360° angle measurements, such as: electronic power steering (EPS), transmission, torsion bar, and other systems that require accurate measurement of angles. The A1335 linearization schemes were designed with challenging off-axis applications in mind.

The A1335 is available as a single die in a 14-pin TSSOP, or dual die in a 24-pin TSSOP. Both packages are lead (Pb) free with 100% matte tin leadframe plating.



Functional Block Diagram



Industry-leading linearization enables off-axis (side-shaft) operation

FEATURES AND BENEFITS (continued)

- Two types of linearization algorithms offered: harmonic linearization and segmented linearization
  - □ Enables off-axis operation
- Programmable range—can scale 22.5° to full-scale digital output
- Microprocessor-based output linearization
- EEPROM with error correction control (ECC) for trimming calibration
- 1 mm-thin (TSSOP) package
- Improved air gap performance, based on continuous background calibration

SELECTION GUIDE

Part Number	System Die	Package	Packing [1]
A1335LLETR-T	Single	14-pin TSSOP	4000 pieces per 13-in. reel
A1335LLETR-DD-T	Dual	24-pin TSSOP	4000 pieces per 13-in. reel

[1] Contact Allegro for additional packing options

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		24	V
Reverse Supply Voltage	V_{RCC}		–18	V
All Other Pins	V_{IN}		–0.5 to 5.5	V
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LE-14 package	82	ºC/W
		LE-24 package	117	ºC/W

[1] Additional thermal information available on the Allegro website.

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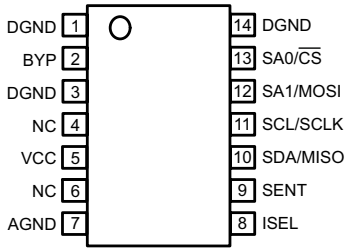
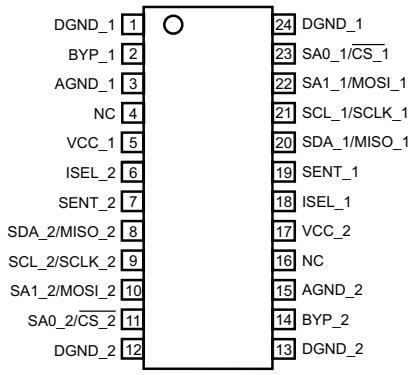
PINOUT DIAGRAMS AND TERMINAL LIST



LE-14 Package
(Single SoC)



LE-24 Package
(Dual SoC)

Terminal List Table

Pin Name [1]	Pin Number		Function
	LE-14	LE-24	
VCC_1	5	5	Device power supply and input for EEPROM writing pulses. Used to enter/exit Manchester serial communication mode; serves as programming data input once mode has been entered.
VCC_2	–	17	
AGND_1	7	3	Device analog ground terminal.
AGND_2	–	15	
BYP_1	2	2	Internal bypass node, connect with bypass capacitor to DGND (die 1).
BYP_2	–	14	Internal bypass node, connect with bypass capacitor to DGND (die 2).
DGND_1	1, 3, 14	1, 24	Device digital ground terminal.
DGND_2	–	12,13	
ISEL_1	8	18	Selects between I²C operation (set to logic low) or SPI operation (set to logic high) (for SENT/Manchester operation set low) (die 1).
ISEL_2	–	6	Selects between I²C operation (set to logic low) or SPI operation (set to logic high) (for SENT/Manchester operation set low) (die 2).
NC	4, 6	4, 16	Not Connected; connect to GND for optimal ESD performance.
SA0_1/CS_1	13	23	I²C: SA0 digital input. Sets peripheral address bit 0 (LSB) [2]; tie to BYP for 1, tie to DGND for 0. SPI: Chip-select input, active low (die 1). Manchester: LSB of the ID value for die 1. tie to BYP for 1, to DGND for 0. Must be in I²C operation (ISEL set to a logic low).
SA0_2/CS_2	–	11	I²C: SA0 digital input. Sets peripheral address bit 0 (LSB) [2]; tie to BYP for 1, tie to DGND for 0. SPI: Chip-select input, active low (die 2). Manchester: LSB of the ID value for die 2. tie to BYP for 1, to DGND for 0. Must be in I²C operation (ISEL set to a logic low).
SA1_1/ MOSI_1	12	22	I²C: SA1 digital input: Sets peripheral address bit 1 (LSB) [2]; tie to BYP for 1, tie to DGND for 0. SPI: Controller output/slave input terminal (die 1). Manchester: MSB of the ID value for Die 1. tie to BYP for 1, to DGND for 0. Must be in I²C operation (ISEL set to a logic low).
SA1_2/ MOSI_2	–	10	I²C: SA1 digital input: Sets peripheral address bit 1 (LSB) [2]; tie to BYP for 1, tie to DGND for 0. SPI: Controller output/slave input terminal (die 2). Manchester: MSB of the ID value for Die 2. tie to BYP for 1, to DGND for 0. Must be in I²C operation (ISEL set to a logic low).
SCL_1/ SCLK_1	11	21	Digital input: Serial clock (I²C: SCL, SPI: SCLK); open drain, pull up externally to 3.3 V (die 1).
SCL_2/ SCLK_2	–	9	Digital input: Serial clock (I²C: SCL, SPI: SCLK); open drain, pull up externally to 3.3 V (die 2).
SDA_1/ MISO_1	10	20	I²C: Digital data terminal: digital output of evaluated target angle, also programming data input; open drain, pull up externally to 3.3 V (die 1). SPI: Master Input/Slave Output terminal (die 1).
SDA_2/ MISO_2	–	8	I²C: Digital data terminal: digital output of evaluated target angle, also programming data input; open drain, pull up externally to 3.3 V (die 2). SPI: Master Input/Slave Output terminal (die 2).
SENT_1	9	19	SENT transmission output terminal (die 1); Manchester output in Manchester mode; open drain, pull-up to external supply.
SENT_2	–	7	SENT transmission output terminal (die 2); Manchester output in Manchester mode; open drain, pull-up to external supply.

[1] The number following the underscore refers to the die number in a dual SOC variant
[2] For additional information regarding the INTF register, I2CM field, refer to the Programming Reference addendum, EEPROM Description and Programming section.

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OPERATING CHARACTERISTICS: Valid throughout full operating voltage and ambient temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit [2]
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		4.5	5	5.5	V
Supply Current	I_{CC}		–	15	20	mA
VCC Low Flag Threshold	$V_{CCLOW(TH)}$		4.4	4.55	4.75	V
Supply Zener Clamp Voltage	V_{ZSUP}	$I_{ZCC} = I_{CC} + 3$ mA, $T_A = 25°C$	26.5	–	–	V
Reverse Battery Voltage	V_{RCC}	$I_{RCC} = –3$ mA, $T_A = 25°C$	–	–	–18	V
Power-On Time [3][4]	t_{PO}	$T_A = 25°C$	2	–	40	ms
SPI INTERFACE SPECIFICATIONS [5]						
Digital Input High Voltage [3]	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	2.8	–	3.63	V
Digital Input Low Voltage [3]	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
SPI Output High Voltage	V_{OH}	MISO pins, $T_A = 25°C$	2.93	3.3	3.69	V
SPI Output Low Voltage	V_{OL}	MISO pins	–	0.3	–	V
SPI Clock Frequency [3]	f_{SCLK}	MISO pins, $C_L = 50$ pF	0.1	–	10	MHz
SPI Clock Duty Cycle [3]	D_{fSCLK}		40	–	60	%
Chip Select to First SCLK Edge [3]	t_{CS}	Time from $\overline{CS}$ going low to SCLK falling edge	50	–	–	ns
Chip Select Idle Time [3]	t_{CS_IDLE}	Time $\overline{CS}$ must be high between SPI message frames	200	–	–	ns
Data Output Valid Time [3]	t_{DAV}	Data output valid after SCLK falling edge	–	45	–	ns
MOSI Setup Time [3]	t_{SU}	Input setup time before SCLK rising edge	10	–	–	ns
MOSI Hold Time [3]	t_{HD}	Input hold time after SCLK rising edge	50	–	–	ns
SCLK to $\overline{CS}$ Hold Time [3]	t_{CHD}	Hold SCLK high time before $\overline{CS}$ rising edge	5	–	–	ns
Load Capacitance [3]	C_L	Loading on digital output (MISO) pin	–	–	50	pF
I²C INTERFACE SPECIFICATIONS (V_{PU} = 3.3 V on SDA and SCL pins)						
Bus Free Time Between Stop and Start [3]	t_{BUF}		1.3	–	–	µs
Hold Time Start Condition [3]	$t_{HD(STA)}$		0.6	–	–	µs
Setup Time for Repeated Start Condition [3]	$t_{SU(STA)}$		0.6	–	–	µs
SCL Low Time [3]	t_{LOW}		1.3	–	–	µs
SCL High Time [3]	t_{HIGH}		0.6	–	–	µs
Data Setup Time [3]	$t_{SU(DAT)}$		100	–	–	ns
Data Hold Time [3]	$t_{HD(DAT)}$		0	–	900	ns
Setup Time for Stop Condition [3]	$t_{SU(STO)}$		0.6	–	–	µs
Logic Input Low Level (SDA and SCL pins) [6]	$V_{IL(I2C)}$		–	–	0.9	V
Logic Input High Level (SDA and SCL pins) [6]	$V_{IH(I2C)}$		2.1	–	3.63	V

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OPERATING CHARACTERISTICS (continued): Valid throughout full operating voltage and ambient temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit [2]
I²C INTERFACE SPECIFICATIONS (V_{PU} = 3.3 V on SDA and SCL pins) (continued)						
Logic Input Current [3]	I_{IN}	V_{IN} = 0 V to V_{CC}	–1	–	1	µA
Output Voltage (SDA pin)	$V_{OL(I2C)}$	R_{PU} = 1 kΩ, C_B = 100 pF, T_A = 25°C	–	–	0.6	V
Logic Input Rise Time (SDA and SCL pins) [3]	$t_{r(IN)}$		–	–	300	ns
Logic Input Fall Time (SDA and SCL pins) [3]	$t_{f(IN)}$		–	–	300	ns
SDA Output Rise Time [3]	$t_{r(OUT)}$	R_{PU} = 1 kΩ, C_B = 100 pF	–	–	300	ns
SDA Output Fall Time [3]	$t_{F(OUT)}$	R_{PU} = 1 kΩ, C_B = 100 pF	–	–	300	ns
SCL Clock Frequency [6]	f_{CLK}		–	–	400	kHz
SDA and SCL Bus Pull-Up Resistor	R_{PU}		–	1	–	kΩ
Total Capacitive Load on SDA Line [3]	C_B		–	–	100	pF
Pull-Up Voltage [3]	V_{PU}	R_{PU} = 1 kΩ, C_B = 100 pF	2.97	3.3	3.63	V
SENT Interface Specifications [3]						
SENT Message Duration	t_{SENT}	Tick time = 3 µs	–	–	1	ms
Minimum Programmable SENT Message Duration	$t_{SENTMIN}$	Tick time = 0.5 µs, 3 data nibbles, SCN, and CRC, nibble length = 27 ticks	–	96	–	µs
SENT Output Signal	$V_{SENT(L)}$	5 kΩ ≤ R_{pullup} ≤ 50 kΩ	–	–	0.10	V
	$V_{SENT(H)}$	Minimum R_{pullup} = 5 kΩ	0.9 × V_S	–	–	V
		Maximum R_{pullup} = 50 kΩ	0.7 × V_S	–	–	V
SENT Trigger Signal	$V_{SENTtrig(L)}$		–	–	1.4	V
	$V_{SENTtrig(H)}$		2.8	–	–	V
Minimum Time Frame for SENT Trigger Signal	$T_{trig(MIN)}$		2	–	–	µs
Triggered Delay Time	t_{dSENT}	From end of trigger pulse to beginning of SENT message frame. TSENT (SENT_MODE 3 and SENT_MODE 4)	–	7	–	tick
Maximum Sink Current	I_{LIMIT}	Output FET on, T_A = 25°C	–	30	–	mA
Magnetic Characteristics						
Magnetic Field [7]	B	Range of input field	–	–	1500	G

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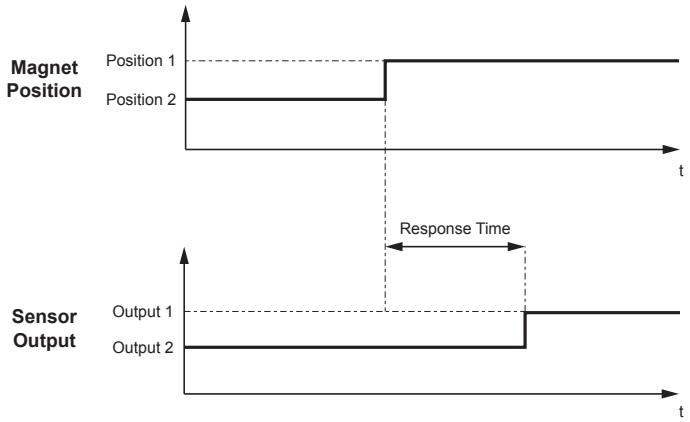
OPERATING CHARACTERISTICS (continued): Valid throughout full operating voltage and ambient temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit [2]
ANGLE CHARACTERISTICS						
Output [8]	RES_{ANGLE}		–	12	–	bit
Effective resolution [9]		B = 300 G, T_A = 25ºC, ORATE = 0	–	10.8	–	bits
		B ≥ 700 G, T_A = 25ºC, ORATE = 0	–	12	–	bits
Angle Refresh Rate [10]	t_{ANG}	ORATE = 0	–	32	–	µs
Response Time [11]	$t_{RESPONSE}$	All linearization and computations disabled, see Figure 1	–	60	–	µs
Angle Error [12]	ERR_{ANG}	T_A = 25°C, ideal magnet alignment, B = 300 G, target rpm = 0, no linearization	–	±0.5	–	degrees
		T_A = 25°C, ideal magnet alignment, B = 900 G, target rpm = 0, no linearization	–	±0.2	–	degrees
		T_A = 150°C, ideal magnet alignment, B = 300 G, target rpm = 0, no linearization	–1.3	–	+1.3	degrees
		T_A = 150°C, ideal magnet alignment, B = 900 G, target rpm = 0, no linearization	–	±0.3	–	degrees
Angle Noise [12][13]	N_{ANG}	T_A = 25°C, B = 300 G, no internal filtering, 3 sigma value	–	0.6	–	degrees
		T_A = 150°C, B = 300 G, no internal filtering, 3 sigma value	–	0.8	–	degrees
Temperature Drift	$ANGLE_{DRIFT}$	T_A = 150°C, B = 300 G	–1.4		1.4	degrees
		T_A = –40°C, B = 300 G	–	±1.2	–	degrees
Angle Drift Over Lifetime [14]	$ANGLE_{DRIFT-LIFE}$	B = 300 G, typical maximum drift observed of peak angle error following AEC-Q100 Grade 0 qualification testing	–	±0.7	–	degrees

[1] Typical data is at T_A = 25°C and V_{CC} = 5 V and it is for design information only.
[2] 1 G (gauss) = 0.1 mT (millitesla).
[3] Parameters for this characteristic are determined by design. They are not measured at final test.
[4] Power-on time may be reduced by disabling CVH self-test at power-on.
[5] During the power-on phase, the A1335 SPI transactions are not guaranteed.
[6] Parameter is tested at wafer probe only.
[7] The A1335 operates in Magnetic fields lower than 300 G, but with reduced accuracy and resolution. CVH self-test operation is not guaranteed at field levels above 300 G.
[8] RES_{ANGLE} represents the number of bits of data available for reading from the die registers.
[9] Effective Resolution is calculated using the formula below:

$$log_2(360) - log_2\left(\frac{1}{n}\sum_{i=1}^{n}\sigma_i\right)$$

where σ is the Standard Deviation based on thirty measurements taken at each of the 32 angular positions, I = 11.25, 22.5, … 360.
[10] The rate at which a new angle reading is ready. This value varies with the ORATE selection.
[11] This value assumes no post-processing and is the response time to read the magnetic position with no further computations. Actual response time is dependent on EEPROM settings. Settings related to filter design, signal path computations, and linearization will increase the response time.
[12] Error and noise values are with no further signal processing. Angle Error can be corrected with linearization algorithm, and Angle Noise can be reduced with internal filtering and slower Angle Refresh Rate value.
[13] 3 sigma value at 300 G. Operation with a larger magnetic field results in improved noise performance. For 600 G operation, noise reduced by 40-50% vs. 300 G.
[14] Maximum observed drift in angle error parameter following AEC-Q100 Grade 0 stress was 1.7 degrees following temperature cycle stress.



Definition of Response Time

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FUNCTIONAL DESCRIPTION

Overview

The A1335 incorporates a Hall sensor IC that measures the direction of the magnetic field vector through 360° in the X-Y plane (parallel to the branded face of the device). The A1335 computes the angle based on the actual physical reading, as well as any internal parameters that have been set by the user. The end user can configure the output dynamic range, output scaling, and filtering.

This device is an advanced, programmable internal microprocessor-driven system-on-chip (SoC). It includes a Circular vertical Hall (CVH) analog front end, a high-speed sampling analog-to-digital converter, digital filtering, a 32-bit custom microprocessor, a digital control interface capable of supporting I²C, SPI and SENT, and digital output of processed angle data.

Advanced linearization, offset, and gain adjustment options are available in the A1335. These options can be configured in onboard EEPROM providing a wide range of sensing solutions in the same device. Device performance can be optimized by enabling individual functions or disabling them in EEPROM to minimize latency.

Operation

The device is designed to acquire angular position data by sampling a rotating bipolar magnetic target using a multisegmented circular vertical Hall-effect (CVH) detector. The analog output is processed, then digitized and compensated before being loaded into the output register. For a depiction of the signal process flow described here, refer to Figure 1.

• ***Analog Front End.*** In this stage, the applied magnetic signal is detected and digitized for more-advanced processing.

A1 CVH Element. The CVH is the actual magnetic-sensing element that measures the direction of the applied magnetic vector.

A2 Analog Signal Conditioning. The signal acquired by the CVH is sampled.

A3 Analog-to-Digital Converter. The analog signal is digitized and handed off to the digital-front-end stage.

• ***Digital Front End.*** In this preprocessing stage, the digitized signal is conditioned for analysis.

D1 Digital Signal Conditioning. The digitized signal is decimated and bandpass filtered.

D2 Raw Angle Computation. For each sample, the raw angle value is calculated.

• ***Microprocessor.*** The preprocess signal is subjected to various user-selected computations. The type and selection of computations used involves a trade-off between precision and increased response time in producing the final output.

P1 Angle Averaging. The raw angle data is received in a periodic stream, and several samples are accumulated and averaged based on the user-selected output rate. This feature increases the effective resolution of the system. The amount of averaging is determined by the user-programmable output rate (ORATE) field. The user can configure the quantity of averaged samples by powers of two to determine the *refresh rate*, the rate at which successive averaged angle values are fed into the post-processing stages. The available rates are set as shown in Table 1.

Table 1: Refresh Rates of Averaged Samples

ORATE [2:0]	Quantity of Samples Averaged	Refresh Rate (µs)
000	1	32
001	2	64
010	4	128
011	8	256
100	16	512
101	32	1024
110	64	2048
111	128	4096

P1a IIR Filter (Optional). The optional infinite impulse response (IIR) filter can provide more-advanced multiorder filtering of the input signal. Filter coefficients can be user-programmed, and the filter (FI) bit can be programmed by the user to enable or disable this feature.

P2 Angle Compensation. The A1335 is capable of compensating for drift in angle readings that result from changes in the device temperature through the operating ambient temperature range. The device comes from the factory preprogrammed with coefficient settings to allow compensation of linear shifts of angle with temperature.

P2a Prelinearization Rotation (Optional, but required if linearization is used). The linearization algorithms require input functions that are both continuous and monotonically increasing. The LR bit sets which relative direction of target rotation results in an increasing angle value. The bit must be set such that the input to the linearization algorithm is increasing.

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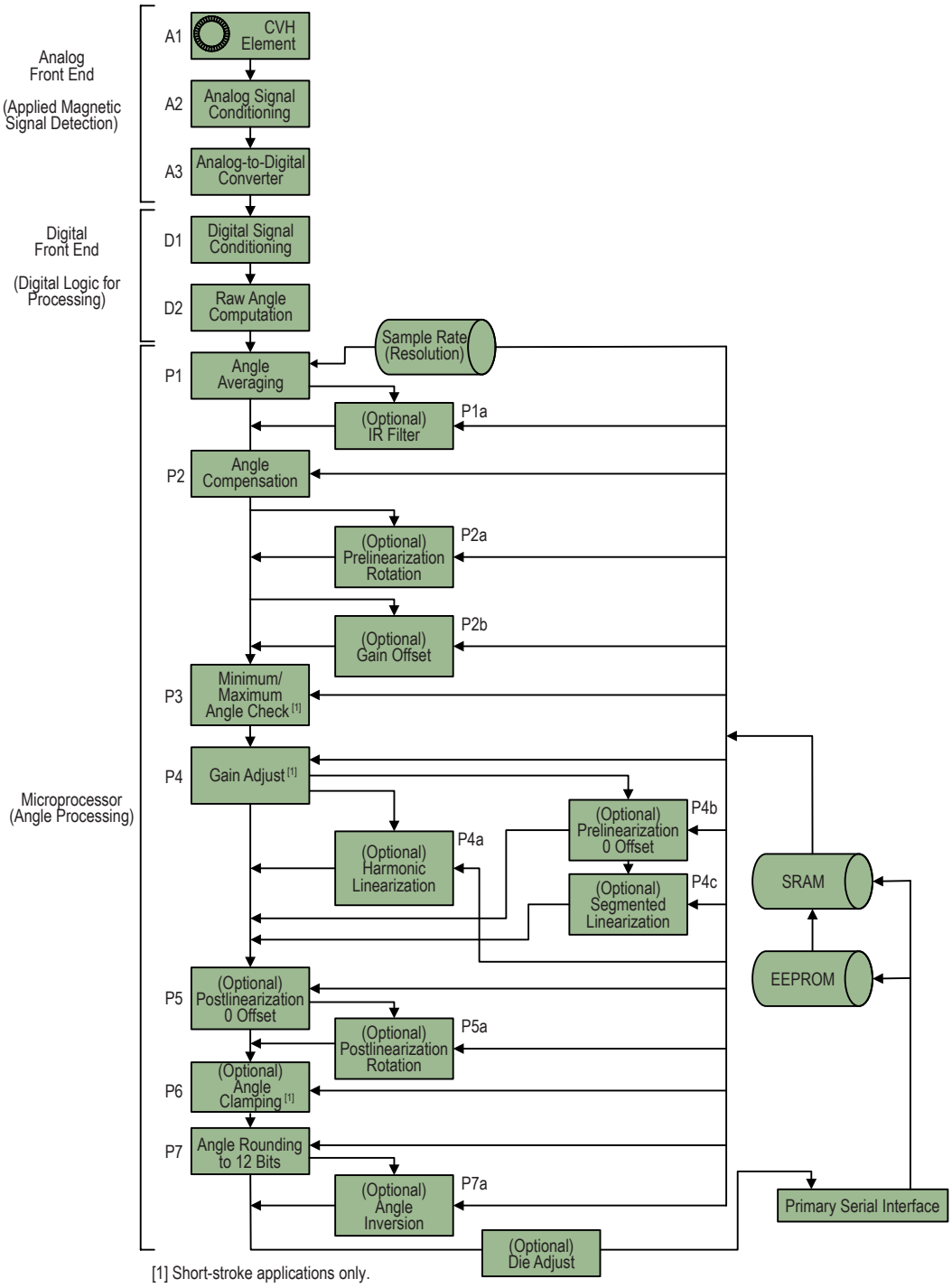

Figure 1: Signal Processing Flow (refer by index number to text descriptions)

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P2b Gain Offset (Optional). Allows zeroing out of the angle prior to applying gain. Set via the GAIN_OFFSET field.

$$\text{Angle} = \text{Angle} - \text{GAIN\_OFFSET}.$$

P3 Minimum/Maximum Angle Check (Short-Stroke Applications Only). The device compares the raw angle value to the angle-value boundaries set by user-programming of the MIN_ANGLE_S or MAX_ANGLE_S fields. If the angle is excessive, an error flag is set at ERR[AH] (high boundary violation) or ERR[AL] (low boundary violation). This feature is useful for applications that use angle strokes less than 360 degrees (short stroke). (Note: This feature is only active if the short-stroke bit has been set.)

P4 Gain Adjust (Short-Stroke Applications Only). This bit adjusts the output dynamic range of the device. For example, if the application only requires 45 degrees of stroke, the user can set this field such that a 45-degree angular change would be distributed across the entire 4095 → 0 code range. Set using the GAIN field. (Note: This feature is only active if the short-stroke bit has been set.)

P4a Harmonic Linearization (Optional). Applies user-programmed error correction coefficients (set in the LINC registers) to the raw angle measurements. Use the HL bit to enable harmonic linearization.

P4b Prelinearization 0 Offset (optional but required if segmented linearization is used). The expected angle values should be distributed throughout the input dynamic range to optimize angle post-processing. This is mostly needed for applications that use full 360-degree rotations. This value establishes the position that corresponds to zero error. This value should be set such that the 360 ≥ degree range corresponds to the 4095 ≥ 0 code range. Setting this point is critical if segmented linearization is used. This is required prior to going through linearization, as the compensation requires a continuous input function to operate correctly. Set using the LIN_OFFSET field.

P4c Segmented Linearization (Optional). Applies user-programmed error correction coefficients (set in the LINC registers) to the raw angle measurements. Use the SL bit to enable segmented linearization.

P5 Postlinearization 0 Offset (Optional). This computation assigns the final angle offset value, to set the low expected angle value to code 0 in the output dynamic range, after all linearization and processing has been completed. Set using the ZERO_OFFSET field.

P5a Postlinearization Rotation (Optional). This feature allows the user to chose the polarity of the final angle output, relative to the result of the prelinearization rotation direction setting (LR bit, previously described). Set using the RO bit.

P6 Angle Clamping (Short-Stroke Applications Only). The A1335 has the ability to apply digital clamps to the output signal. This feature is most useful for applications that use angle strokes less than 360 degrees. If the output signal exceeds the upper clamp, the output stays at the clamped value. If the output signal is lower than the lower clamp, the output stays at the low clamp value. Set using the CLAMP_HI and CLAMP_LO fields. (Note: This feature is only active if the short-stroke bit has been set.)

P7 Angle Rounding to 12 Bits. All internal calculations for angle processing in the A1335 are performed with 16-bit precision. This step rounds the data into a 12-bit word for output through the primary serial interface.

P7a Angle Inversion (Short-Stroke Applications Only). Rotation within the high and low clamp values:

$$\text{CLAMP\_HI} - (\text{Angle} - \text{CLAMP\_LO})$$

(Note: This feature is only active if the short-stroke bit has been set.)

P8 Die Adjust (Optional). Rotates final angle 180 degrees. Used to compensate for the 180-degree offset between die in dual SoC packages.

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Diagnostic Features

The A1335 was designed with diagnostic requirements in mind and supports many on-chip diagnostics as well as error/status flags, enabling the host microcontroller to assess the operational status of each die.

In addition, the A1335 supports three different on-chip user-initiated diagnostics.

USER-INITIATED DIAGNOSTICS

The following three internal self-tests may be configured to run at power-on, and may also be initiated at any time by the system microcontroller via extended access commands through the SPI/I²C interface. A failure of any one of the three self-tests asserts the self-test (ST) failure flag within the extended error register. The specific failing test can be identified by performing an extended address read (address 0xFFFC).

- **CVH Self-Test**
  The CVH self-test is a signal-path diagnostic used to verify both analog and digital system integrity. Test execution requires approximately 36 ms, during which time no new angle measurements are generated by the sensor. The test is implemented by changing the transducer switch configuration from typical mode into a test configuration, allowing a test current to drive the CVHD in place of the magnetic field. By changing the direction of the test current and sequencing different elements within the CVH, the self-test emulates a changing magnetic-field angle. The measured angle is monitored to determine a passing or failing device. A failure of the CVH self-test asserts the ST flag. If the self-test was initiated via the extended access command, test results for the individual Hall elements are stored in the SRAM CMDSTATUS field (0x00) and the primary serial interface ERD register (0x0E through 0x11).
  Due to the sensitivity of the self-test, test results are only valid at field levels equal to or less than 300 G and temperatures at or above 25°C.
- **SRAM BIST**
  The SRAM built-in self-test (BIST) verifies proper functionality of the SRAM. The test may be run in either long or short mode, and can be configured to halt on error. A failure of the SRAM BIST asserts the ST flag. When enabled to run on power-up, the short-test mode is used, requiring approximately 100 µs to complete. For more information on SRAM BIST options, consult the A1335 programming guide.

Table 2: Status and Error Flags

Fault Condition	Description	Sensor Response
$V_{CC} < V_{CCLOW(TH)(min)}$	Indicates potential for reduced angle accuracy	UV error flag is set
$V_{CC} > 8.8$ V	Indicates possible system-level power supply failure	OV error flag is set [1]
Field > MAG_HIGH	MAG_HIGH programmable from 0 to1240 G in 40 G steps. Monitors level of MAG field in case of mechanical failure	MH flag is set
Field < MAG_LOW	MAG_LOW programmable from 0-620 G in 20 G steps. Monitors level of MAG field in case of mechanical failure	ML flag is set
–60°C > T_A > 180°C	Ambient temperature beyond maximum rating detected	TR flag is set
Processor Halt	Monitors digital logic for proper functionality	WT and WC flags are set
Single-Bit EEPROM Error (correctable)	Detects and corrects a single-bit EEPROM Error	ES error flag is set
Multi-Bit EEPROM Error (uncorrectable)	Detects a multi-bit uncorrectable EEPROM ERROR	EU error flag is set
Single-Bit SRAM Error (correctable)	Detects and corrects a single-bit SRAM Error	SS error flag is set
Multi-Bit SRAM Error (uncorrectable)	Detects a multi-bit uncorrectable SRAM ERROR	SU error flag is set
Angle-Processing Errors	New angle measurement did not occur within the maximum time allotted.	AT flag is set
Angle Out of Range	Angle value (prior to scaling by gain) is outside the range set by MIN_ANGLE and MAX_ANGLE. Short-stroke only.	AL or AH flag is set
Loss of V_{CC}	Determines if system power was lost. Also detects a reset of the internal microprocessor	POR and RC flags are set
Self-Test Failure	Indicates a failure of one of the three internal self-tests: SRAM BIST, ROM checksum verification, and CVH self-test. Tests can be individually configured to run at power-up and may also be user initiated.	ST flag is set

[1] EEPROM programming pulses result in OV flag assertion.

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- **ROM Checksum**
  Verification of the ROM checksum may be configured to occur at power-on. In addition, the checksum is continuously recalculated in the background during typical operation (independent of power-on configuration). This test may be initiated at any time by the system microcontroller via an extended access command (0xFFE0). If the self-test was initiated via the extended access command, the failing checksum is stored in the CMDSTATUS SRAM register (0x00). A bad ROM checksum asserts the self-test (ST) failure flag.

LOW VOLTAGE DETECTION

In addition to setting the undervoltage (UV) flag, a V_{CC} ramp also changes the state of the output pins (SDA/MISO and SENT) as the part enters and exits the reset condition. This is shown in Figure 2.

For more information about diagnostic features and flags, refer to the more-complete description of the available flags and settings in the A1335 Programming Manual. [1]

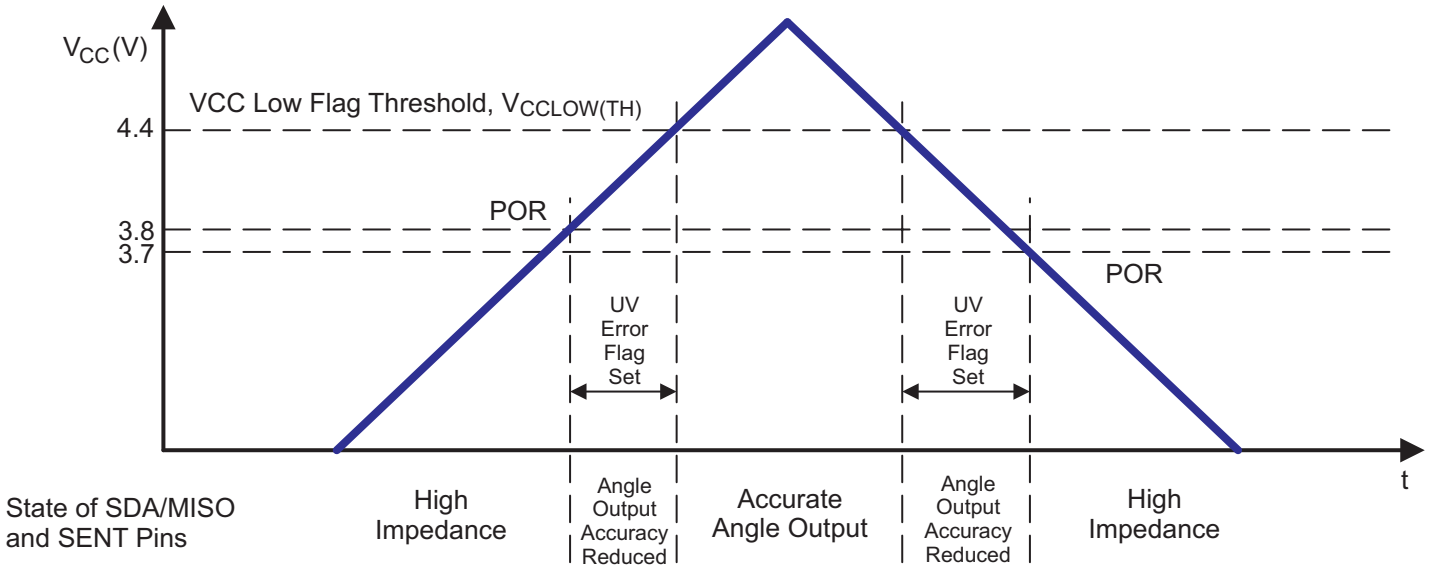

Figure 2: Relationship of V_{CC} and Output

Programming Modes

The EEPROM can be written through the dedicated I²C or SPI interface pins or via Manchester encoding on the VCC pin, allowing process coefficients to be entered and options selected. (Note: programming EEPROM also requires the VCC line to be pulsed, which could adversely affect other devices if powered from the same line). Certain operating commands also are available by writing directly to SRAM. The EEPROM and SRAM provide parallel data structures for operating parameters. The SRAM provides a rapid test and measurement environment for application development and bench-testing. The EEPROM provides persistent storage at the end of line for final parameters. At power-on initialization, the EEPROM contents are read into the corresponding SRAM. Provided the lock microprocessor (LM) bit within EEPROM is not set, SRAM can be overwritten during operation (use caution). The EEPROM is permanently locked by setting the lock EEPROM (LE) bit in the EEPROM.

The A1335 EEPROM is programmed via either the I²C, the SPI, or the VCC pin serial interface, with additional power provided by pulses on the VCC pin to set the EEPROM bit fields.

[1] https://www.allegromicro.com/-/media/files/application-notes/an296127-a1335-advanced-on-chip-linearization.pdf?sc_lang=en

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MANCHESTER SERIAL INTERFACE

To facilitate addressable device programming when using the unidirectional SENT output mode with no need for additional wiring, the A1335 incorporates a serial interface on the VCC line. (Note: The A1335 may be programmed via the SPI or I²C interfaces, with additional wiring connections. For detailed information about part programming, refer to the A1335 Programming Manual). This interface allows an external controller to read and write registers in the A1335 EEPROM and volatile memory. The device uses a point-to-point communication protocol, based on Manchester encoding per G.E. Thomas (a rising edge indicates a 0, and a falling edge indicates a 1), with address and data transmitted MSB first. The addressable Manchester code implementation uses the logic states of the SA0/SA1 pins to set address values for each die. In this way, individual communication with up to four A1335 die is possible.

To prevent any undesired programming of the A1335, the serial interface can be disabled by setting the disable Manchester bit. With this bit set, the A1335 ignores any Manchester input on VCC.

Entering Manchester Communication Mode

Provided the disable Manchester bit is not set in EEPROM, the A1335 continuously monitors the VCC line for valid Manchester commands. The part takes no action until a valid Manchester access code is received.

There are two special Manchester code commands used to activate or deactivate the serial interface and specify the output format used during read operations:

1. **Manchester Access Code:** Enters Manchester communication mode; Manchester code is output on the SENT pin.
2. **Manchester Exit Code;** returns the SENT pin to typical (angle data) output format.

Once the Manchester communication mode is entered, the SENT output pin ceases to provide angle data, interrupting any data transmission in progress.

Transaction Types

The A1335 receives all commands via the VCC pin, and responds to read commands via the SENT pin, as shown in Figure 3.This implementation of Manchester encoding requires the communication pulses to be within a high ($V_{MAN(H)}$) and low ($V_{MAN(L)}$) range of voltages on the VCC line. Writing to EEPROM is supported by two high-voltage pulses on the VCC line.

Each transaction is initiated by a command from the controller; the A1335 does not initiate any transactions. Two commands are recognized by the A1335: write and read.

Writing to EEPROM

When a write command requires writing to nonvolatile EEPROM, after the write command, the controller must also send two *programming pulses*, high-voltage strobes via the VCC pin. These strobes are detected internally, allowing the A1335 to boost the voltage on the EEPROM gates. For specific details about sensor programming and protocols, refer to the A1335 Programming Manual.

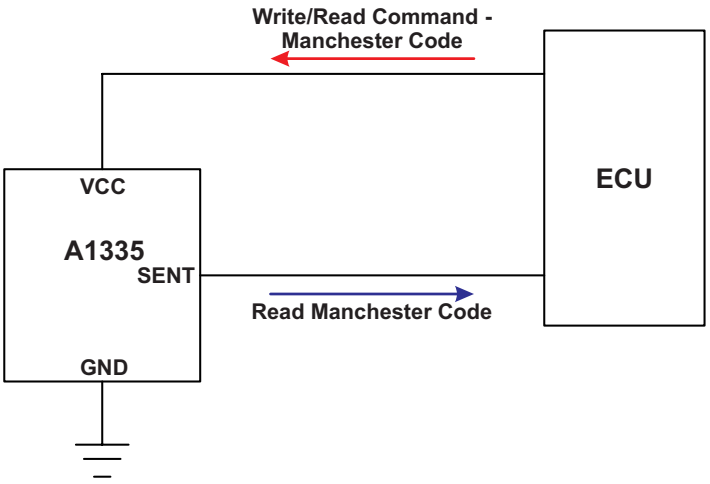

Figure 3: Top-Level Programming Interface

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Manchester Interface Reference

Table 3: Manchester Interface Protocol Characteristics [1]

Characteristics	Symbol	Note	Min.	Typ.	Max.	Unit
INPUT/OUTPUT SIGNAL TIMING						
Bit Rate		Defined by the input message bit rate sent from the external controller	4	–	100	kbps
Bit Time	t_{BIT}	Data bit pulse width at 4 kbps	243	250	257	µs
		Data bit pulse width at 100 kbps	9.5	10	10.5	µs
Bit Time Error	err_{TBIT}	Deviation in t_{BIT} during one command frame	–11	–	+11	%
Write Delay	$t_{WRITE(E)}$	Required delay from the end of the second EEPROM programming pulse to the leading edge of a following command frame	V_{CC} < 6.0 V	–	–	–
Read Delay	t_{START_READ}	Delay from the trailing edge of a read command frame to the leading edge of the read acknowledge frame	¼ × t_{bit}	–	¾ × t_{bit}	µs
EEPROM PROGRAMMING PULSE						
EEPROM Programming Pulse Setup Time	$t_{sPULSE(E)}$	Delay from last bit cell of write command to start of EEPROM programming pulse	40	–	–	µs
INPUT SIGNAL VOLTAGE						
Manchester Code High Voltage	$V_{MAN(H)}$	Applied to VCC line	7.8	–	–	V
Manchester Code Low Voltage	$V_{MAN(L)}$	Applied to VCC line	–	–	5.7	V
OUTPUT SIGNAL VOLTAGE (Applied on SENT Line)						
Manchester Code High Voltage	$V_{MAN(H)}$	Minimum R_{pullup} = 5 kΩ	0.9 × V_S	–	–	V
		Maximum R_{pullup} = 50 kΩ	0.7 × V_S	–	–	V
Manchester Code Low Voltage	$V_{MAN(L)}$	5 kΩ ≤ R_{pullup} ≤ 50 kΩ	–	–	0.1	V

[1] Determined by design.

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SENT Output Mode

The SENT output converts the measured magnetic field angle into a binary value mapped to the full-scale output (FSO) range of 0 to 4095, shown in Figure 4. This data is inserted into a binary pulse message, referred to as a frame, that conforms to the SENT data transmission specification (SAEJ2716 JAN2010).

The SENT frame may be configured via EEPROM. The A1335 may operate in one of three broadly defined SENT modes. (For details about SENT modes and settings, refer to the A1335 Programming Manual.)

- SAE J2716 SENT: Free-streaming SENT frame in accordance with industry specification. Additional programmability allows tick time adjustment from 0.5 µs to 7.9 µs.
- Triggered SENT (TSENT): User-defined sampling and retrieval.
- Shared SENT: Allows multiple devices to share a common SENT line. Devices may either be directly addressed (addressable SENT or ASENT) or sequentially polled (sequential SENT or SSENT).

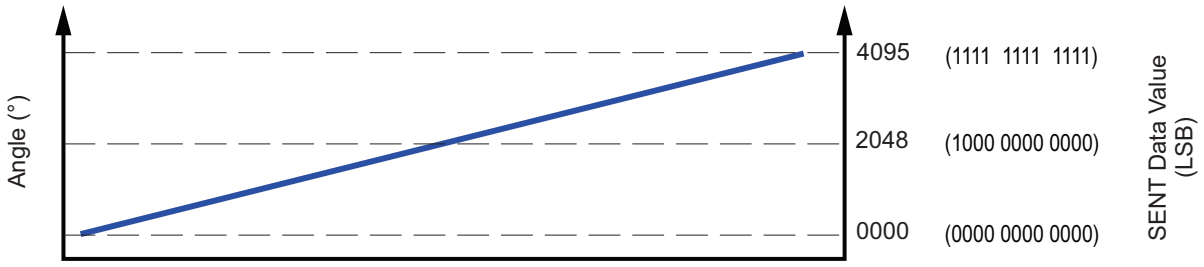

Figure 4: Angle is Represented as a 12-bit Digital Value

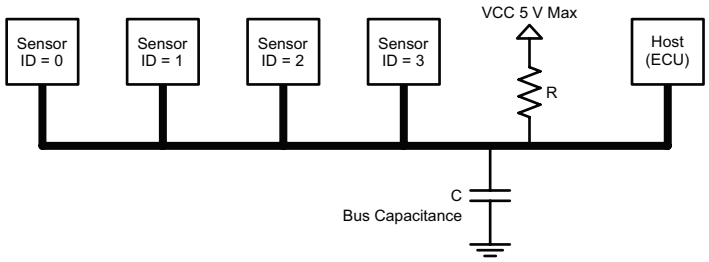

Figure 5: Allegro-proprietary SENT protocol allows multiple parts to share one common output bus.

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SENT MESSAGE STRUCTURE

Data within a SENT message frame is represented as a series of nibbles, with the following characteristics:

- Each nibble is an ordered pair of a low-voltage interval followed by a high-voltage interval.
- The low-voltage interval acts as the delimiting state, which acts as a boundary between each nibble. The length of this low-voltage interval is fixed at 5 ticks.
- The high-voltage interval performs the job of the information state and is variable in duration in order to contain the data payload of the nibble.
- The slew rate of the falling edge may be adjusted using the SENT_DRIVER parameter.

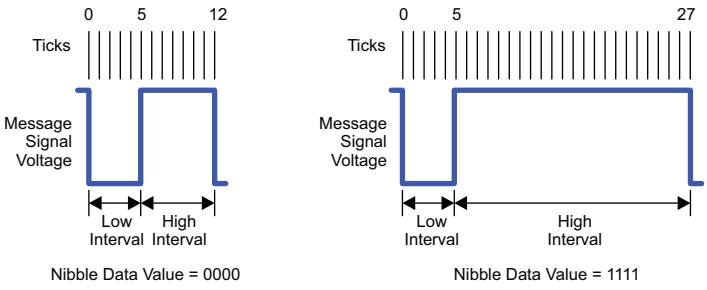

Figure 6: General Value Formation for SENT

0000 (left), 1111 (right)

The duration of a nibble is denominated in ticks. The period of a tick is set by the SENT_TICK parameter. The duration of the nibble is the sum of the low-voltage interval plus the high-voltage interval.

The parts of a SENT message are arranged in the following required sequence (see Figure 7):

1. **Synchronization and Calibration:** Flags the start of the SENT message.
2. **Status and Communication Nibble:** Provides A1335 status and the optional serial data determined by the setting of the SENT_SERIAL parameter.
3. **Data:** Angle information and optional data.
4. **CRC:** Error checking.
5. **Pause Pulse (optional):** Fill pulse between SENT message frames.

Table 4: Nibble Composition and Value

Quantity of Ticks			Binary (4-bit) Value	Decimal Equivalent Value
Low-Voltage Interval	High-Voltage Interval	Total		
5	7	12	0000	0
5	8	13	0001	1
5	9	14	0002	2
⋮	⋮	⋮	⋮	⋮
5	21	26	1110	14
5	22	27	1111	15

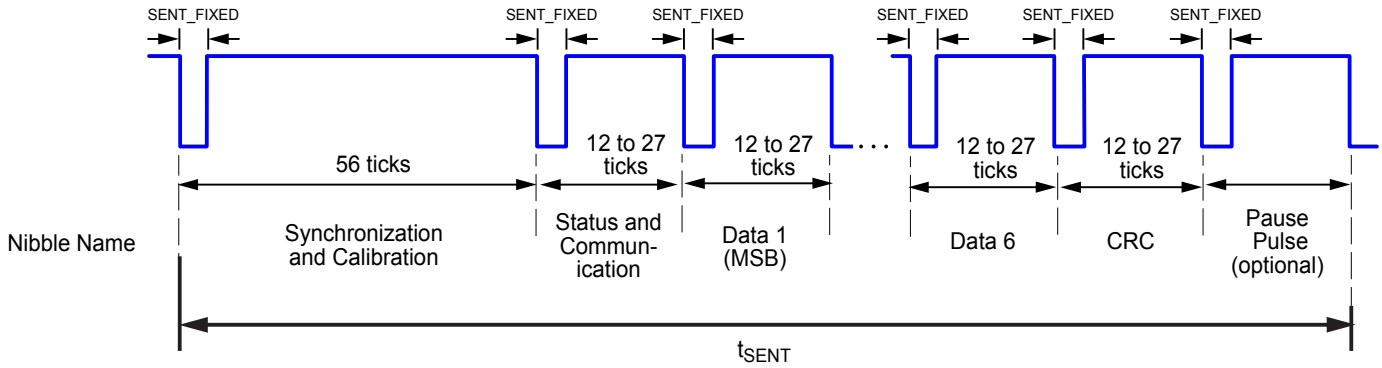

Figure 7: General Format for SENT Message Frame

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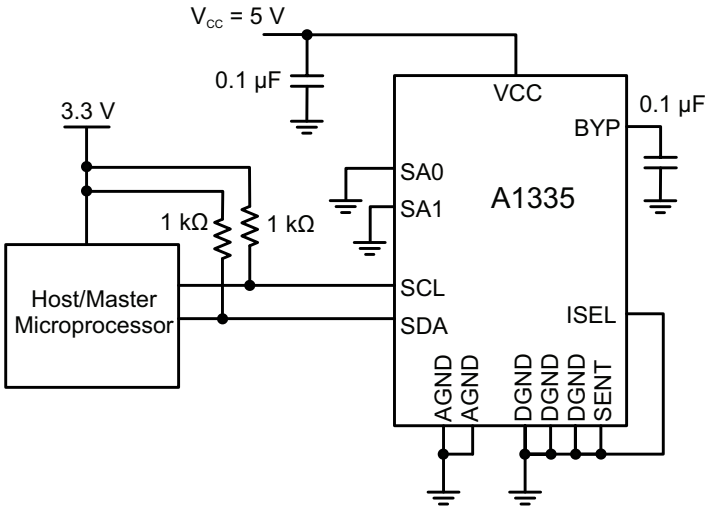
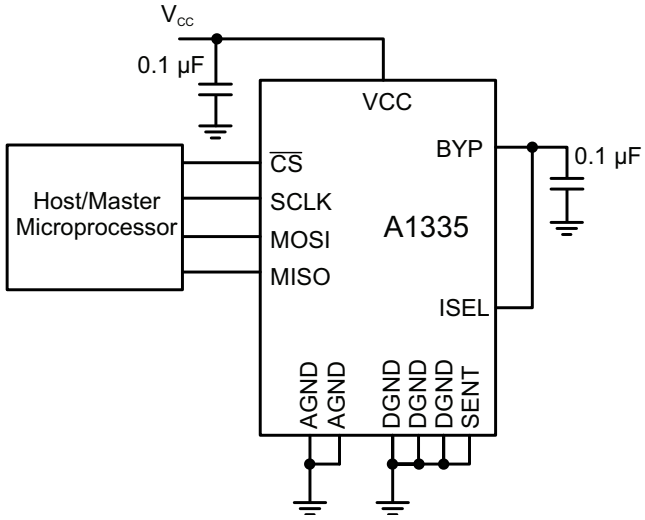
APPLICATION INFORMATION

Serial Interface Description

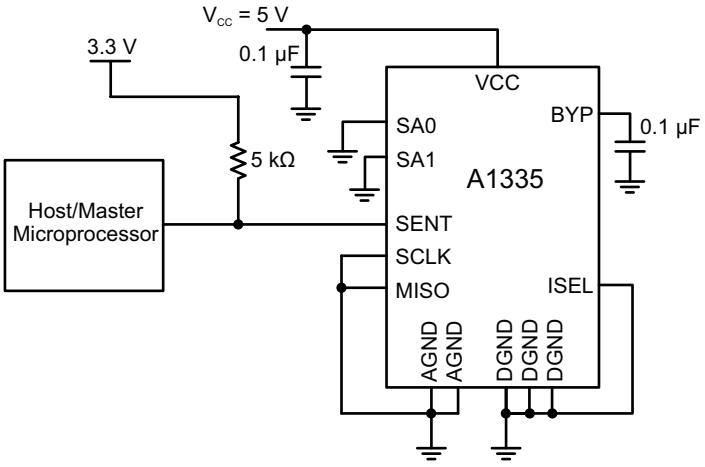
The A1335 features I²C-, SPI-, and SENT-compliant interfaces for communication with a host microcontroller or other controller. A basic circuit for configuring the A1335 package is shown in Figure 8. When not in use, the SENT pin should be grounded (as shown in A and B of Figure 8) and SENT disabled (SENT_MODE = 0 within EEPROM address 0x317).



(A) Typical A1335 configuration using I²C interface; A1335 set up for serial address 0xC



(B) Typical A1335 configuration using SPI interface



(C) Typical A1335 configuration using SENT interface (SA0/SA1 may be brought to BYP or GND to configure Manchester/Shared SENT address)

Figure 8: Typical A1335 configuration

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Magnetic Target Requirements

There are two main sensing configurations for magnetic angle sensing: on-axis and off-axis. On-axis (end of shaft) refers to when the center axis of a magnet lines up with the center of the sensing element. Off-axis (side shaft) refers to when the angle sensor is mounted along the edge of a magnet. On- and off-axis sensing configurations are illustrated in the Effect of Orientation on Signal section.

FIELD STRENGTH

The A1335 actively measures and adapts to its magnetic environment. This allows operation throughout a large range of field strengths (recommended range is 300 to 1000 G; operation beyond this range is allowed with no long-term impact). Due to the greater signal-to-noise ratio provided at higher field strengths, performance inherently increases with increasing field strength. Typical angle performance over applied field strength is shown in Figure 9 and Figure 10.

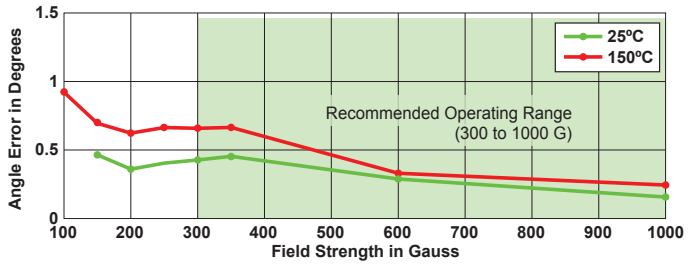


Figure 9: Typical Maximum Angle Error Over Field Strength

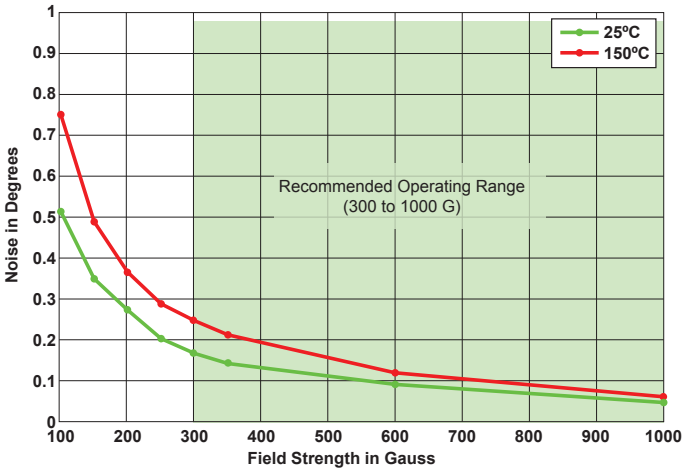
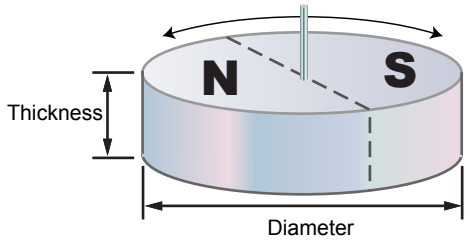


Figure 10: Typical One-Sigma Angle Noise Over Field Strength

Table 5: Target Magnet Parameters

Magnetic Material	Diameter (mm)	Thickness (mm)
Neodymium (bonded)	15	4
Neodymium (sintered) [1]	10	4
Neodymium (sintered)	8	3
Neodymium/SmCo	6	2.5



[1] A sintered neodymium magnet with 10 mm (or greater) diameter and 4 mm thickness is the recommended magnet for redundant applications.

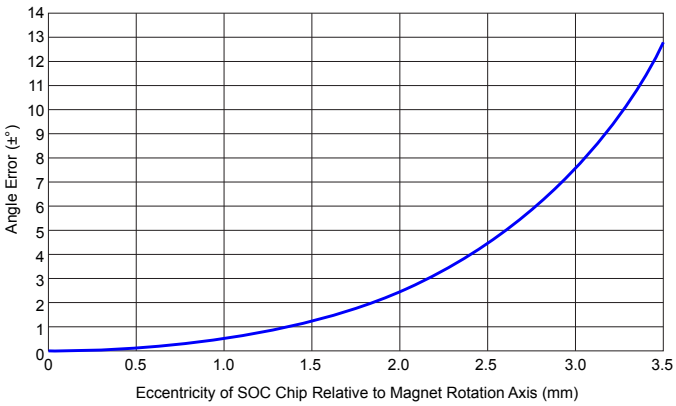


Figure 11: Simulated Error versus Eccentricity for a 10 mm × 4 mm Neodymium Magnet at a 2.7 mm Air Gap

Typical systemic error versus magnet to sensor eccentricity (d_{axial}), Note: “Systemic error” refers to application errors in alignment and system timing. It does not refer to sensor IC device errors. The data in this graph is simulated with ideal magnetization.

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Calculating Target Zero-Degree Angle

When shipped from the factory, the default angle value when oriented as shown in Figure 12, is approximately 0º (180º on secondary die). In some cases, the end user may want to program an angle offset in the A1335 to compensate for variation in magnetic assemblies, or for applications where absolute system-level readings are required.

The internal algorithm for computing the output angle is:

$$Angle_{OUT} = Angle_{postLin} - Zero\ Offset\ . \quad (1)$$

The procedure to "zero out" the A1335 follows.

During final application calibration, position the magnet above the sensor in the required zero-degree position and record the angle reading from the device. Program the Zero Offset field in EEPROM (0x306 bits 12:0) with this value (for additional details, refer to the A1335 Programming Manual).

It is important to keep in mind that the zero offset adjustment occurs after linearization within the A1335 signal path (see Figure 1). As a result, the zero offset adjustment should be performed following end-of-line linearization.

Bypass Pin Usage

The bypass pin is required for proper device operation and is intended to bypass internal IC nodes of the A1335. A 0.1 µF capacitor must be placed in close proximity to the bypass pin. It is not intended to be used to source external components.

Target alignment for default angle setting
• Target rotation axis intersects primary die
  • Primary die 0° default point
  • Secondary die 180° default point
(Example shows element E1 as primary die element E2 as secondary die)

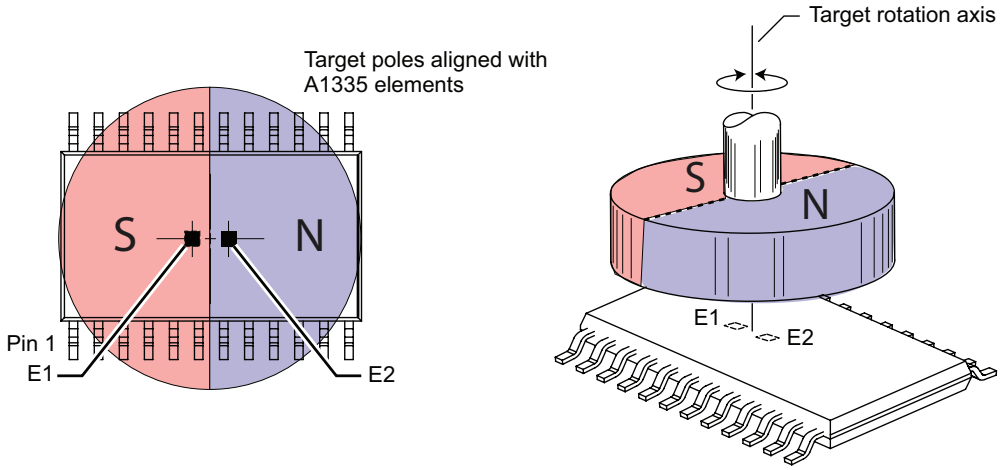

Figure 12: Orientation of Magnet Relative to Primary Die and Secondary Die

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ON-AXIS APPLICATIONS

Some common on-axis applications for the device include digital potentiometer, motor sensing, power steering, and throttle sensing. The A1335 is designed to operate with magnets constructed with a variety of magnetic materials, cylindrical geometries, and field strengths, as shown in Table 5. The device has two internal linearization algorithms that can compensate for much of the error due to alignment. For more-detailed information about magnet selection and theoretical error, contact Allegro.

OFF-AXIS APPLICATIONS

There are two major challenges with off-axis angle-sensing applications. The first is field strength. All efforts should be conducted to maximize magnetic signal strength obsrved by the device. The goal is a minimum of 300 G. Field strength can be maximized by using high-quality magnetic material, and by minimizing the distance between the sensor and the magnet. Another challenge is overcoming the inherent nonlinearity of the magnetic-field vector generated at the edge of a magnet. The device has two linearization algorithms that can compensate for much of the geometric error. Harmonic linearization is recommended for off-axis applications.

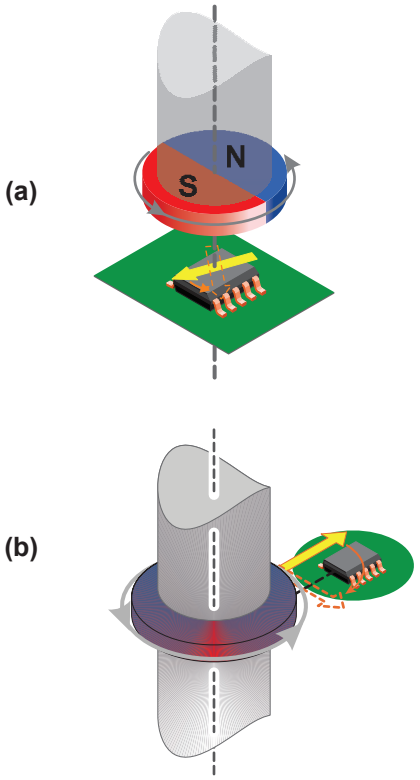

Figure 13: Typical On-Axis (a) and Off-Axis (b) Orientation

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Effect of Orientation on Signal

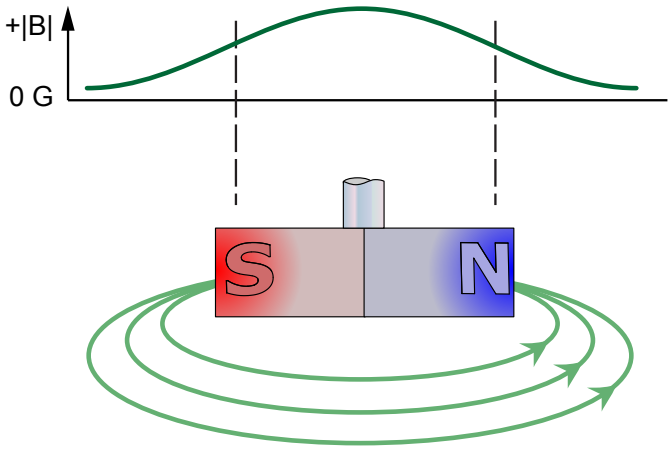

Figure 14: The magnetic field flux lines run between the north pole and south pole of the magnet. The peak flux densities are between the poles.

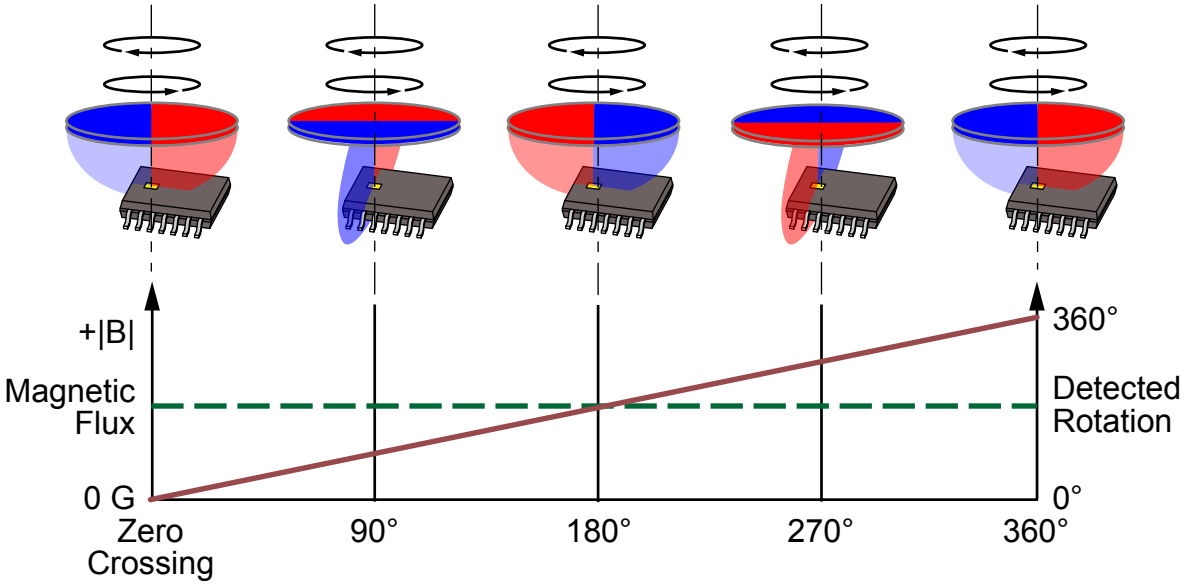

Figure 15: As the magnet rotates, the Hall element detects the rotating relative polarity of the magnetic field (solid line). When the center of rotation is centered on the Hall element, the magnetic flux amplitude is constant (dashed line).

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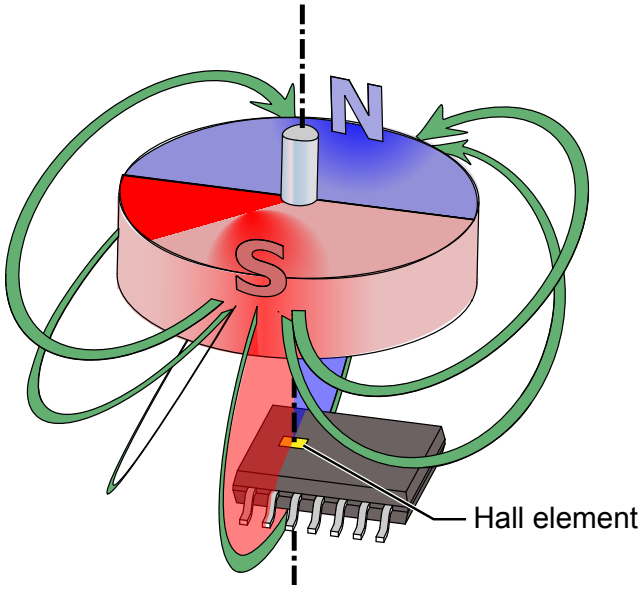

Figure 16: Centering the axis of magnet rotation on the Hall element provides the strongest signal in all degrees of rotation.

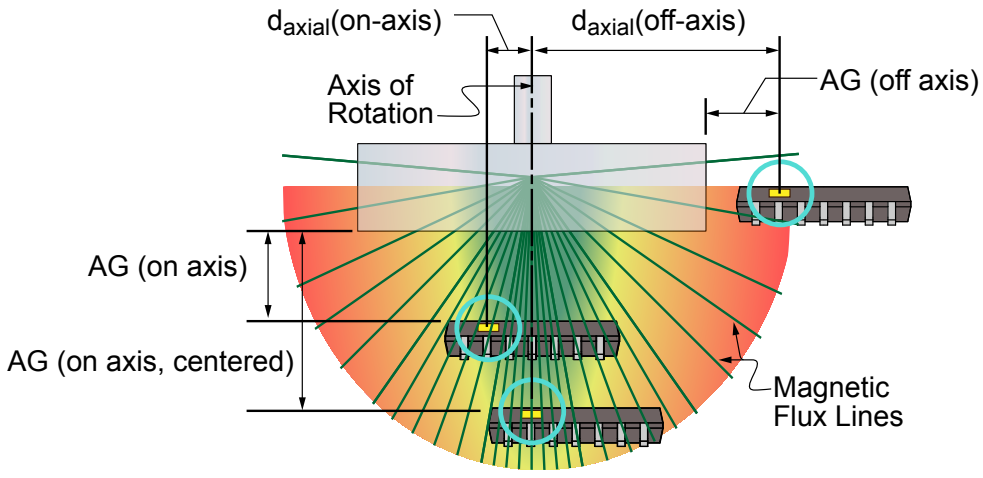

Figure 17: The magnetic flux density degenerates rapidly away from the plane of peak north-south polarity. When the axis of rotation is placed away from the Hall element, the device must be placed closer to the magnetic poles to maintain an adequate level of flux at the Hall element.

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Linearization

Magnetic fields are generally not completely linear throughout the full range of target positions. This can be the result of non-uniformities in mechanical motion or of material composition. In some applications, it may be required to apply a mathematical transfer function to the angle that is reported by the A1335.

The A1335 has built-in functions for performing linearization on the acquired angle data. It is capable of performing one of two different linearization methods: harmonic linearization and piecewise (segmented) linearization.

Segmented linearization divides the output dynamic range into 16 equal segments. Each segment is then represented by the equation of a straight line between the two endpoints of the segment. Using this basic principle, it is possible to tailor the output response to compensate for mechanical nonlinearity.

One example is a fluid-level detector in a vehicle fuel tank. Because of requirements to conform the tank and to provide stiffening, fuel tanks often do not have a uniform shape. A level detector with a linear sensor in this application would not correctly indicate the remaining volume of fuel in the tank without some mathematical conversion. The general concept is illustrated in Figure 18.

Harmonic linearization uses the Fourier series to compensate for periodic error components. In the most basic of terms, the Fourier series is used to represent a periodic signal using a sum of ideal periodic waveforms. The A1335 is capable of using up to 11 Fourier series components to linearize the output transfer function.

While it can be used for many applications, harmonic linearization is most useful for 360-degree applications. The error curve for a rotating magnet that is not perfectly aligned most often has an error waveform that is periodic. This phenomenon is especially true for systems where the sensor is mounted off-axis relative to the magnet. This periodic error is illustrated in Figure 19.

An initial set of linearization coefficients is created by characterizing the application experimentally. With all signal processing options configured, the device is used to sense the applied magnetic field at a target zero degrees of rotation reference angle and at regular intervals. For segmented linearization, 16 samples are taken: at nominal zero degrees and every 1/16 interval (22.5°) of the full 360° rotational input range. Each angle is read from the angle (ANG) register and recorded.

These values are loaded into the Allegro ASEK programming utility for the device, or an equivalent customer software program, to generate coefficients corresponding to the values. The user then uses the software load function to transmit the coefficients to the EEPROM. Each of the coefficient values can be individually overwritten during normal operation by writing directly to the corresponding SRAM.

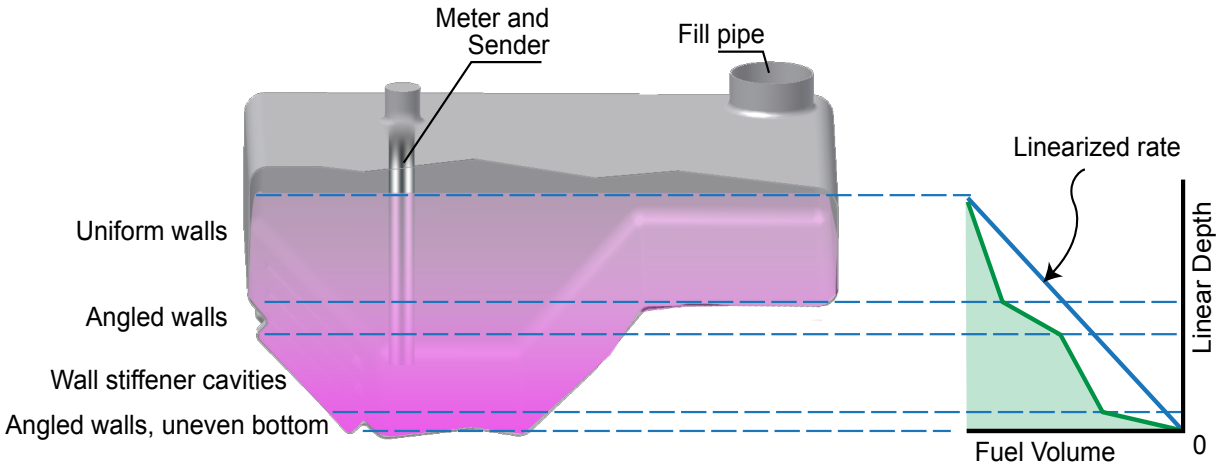

Figure 18: An integrated vehicle fuel tank has varying volumes according to depth due to structural elements. As shown in the chart, this results in a variable rate of fuel level change, depending on volume at the given depth, and a linearized transfer function can be used against the integral volume.

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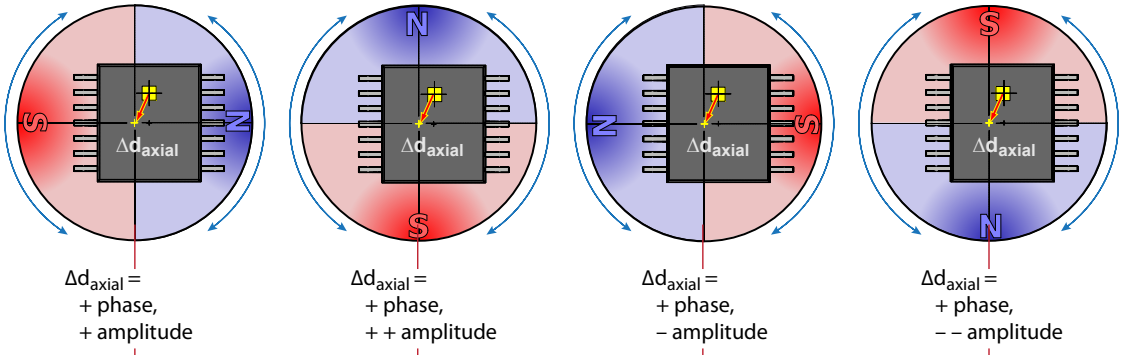

Δd_{axial} = + phase, + amplitude

Δd_{axial} = + phase, + + amplitude

Δd_{axial} = + phase, – amplitude

Δd_{axial} = + phase, – – amplitude

Figure 19a: With the axis of rotation aligned with the Hall element, linearization coefficients are a simple inversion of the input.

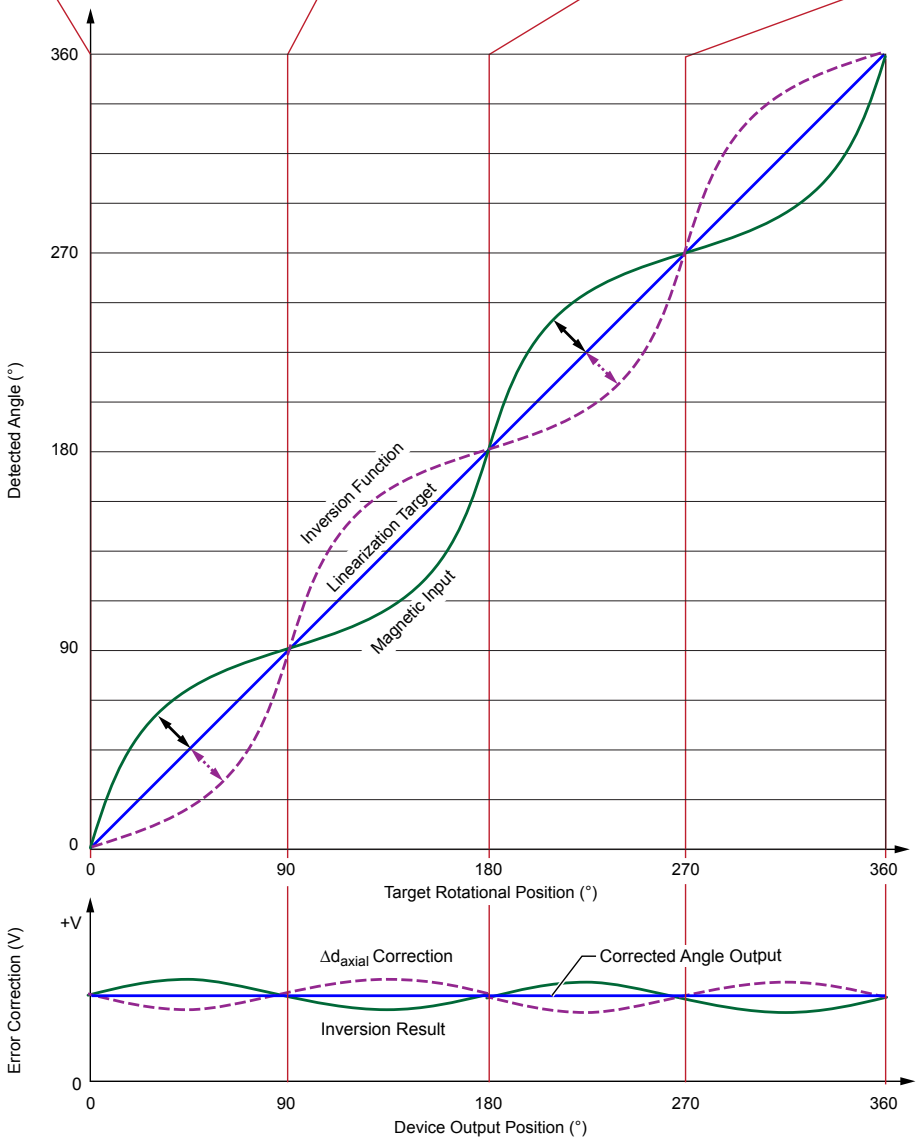

Figure 19b: Any eccentricity is evaluated as an error. Systematic eccentricity can be factored out by appropriate linearization coefficients. For off-axis applications, the harmonic linearization method is recommended.

Figure 19: Correction for Eccentric Orientation

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HARMONIC COEFFICIENTS

The device supports up to 11 harmonics. Each harmonic is characterized by an amplitude and a phase coefficient.

To apply harmonic linearization, the device:

1. Calculates the error factors.
2. Applies any programmed offsets.
3. Calculates the linearization factor as:

$$A_n \times sin(n \times t + \varphi_n)$$

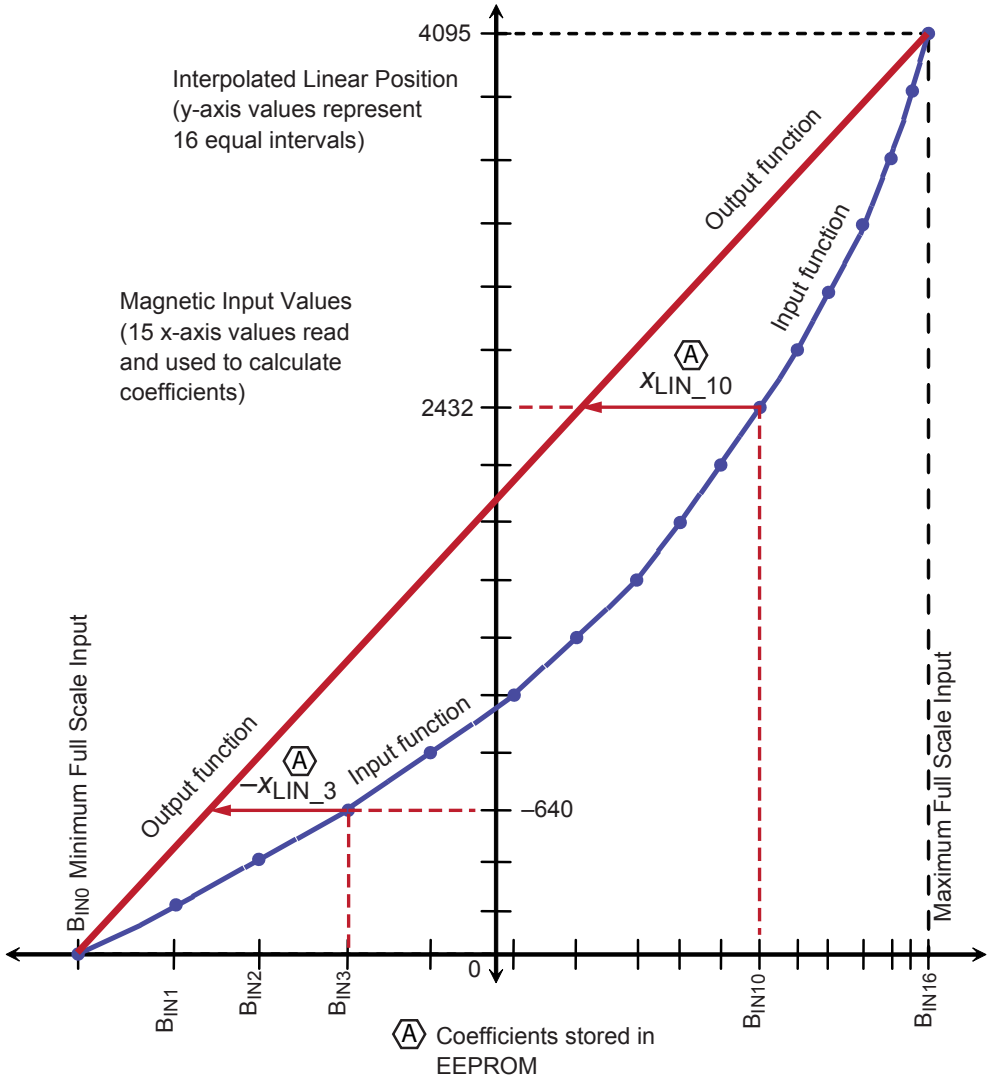

Figure 20: Sample of Linearization Function Transfer Characteristic

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TYPICAL PERFORMANCE CHARACTERISTICS

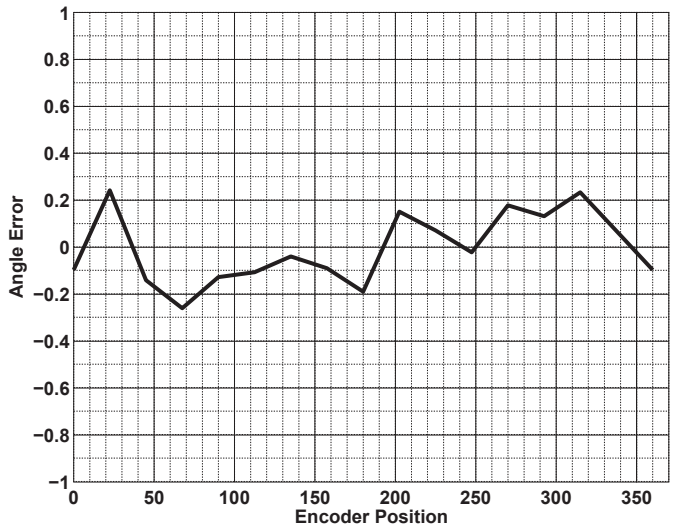

Figure 21: Typical Angle Error versus Encoder Position (300 G, 25ºC)

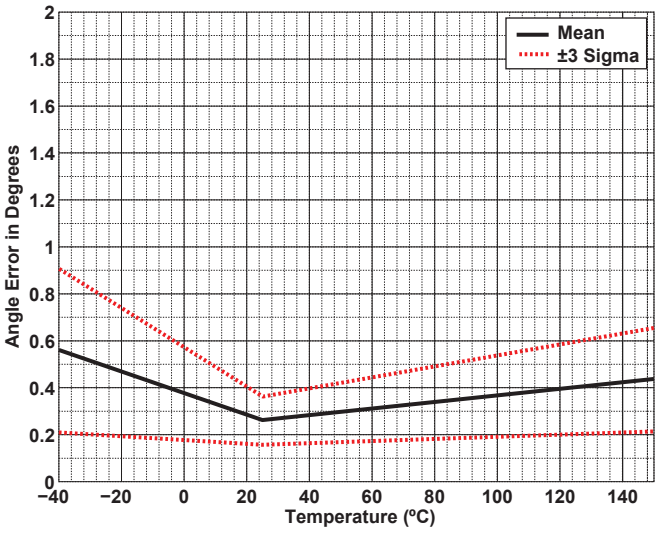

Figure 22: Peak Angle Error over Temperature (300 G)

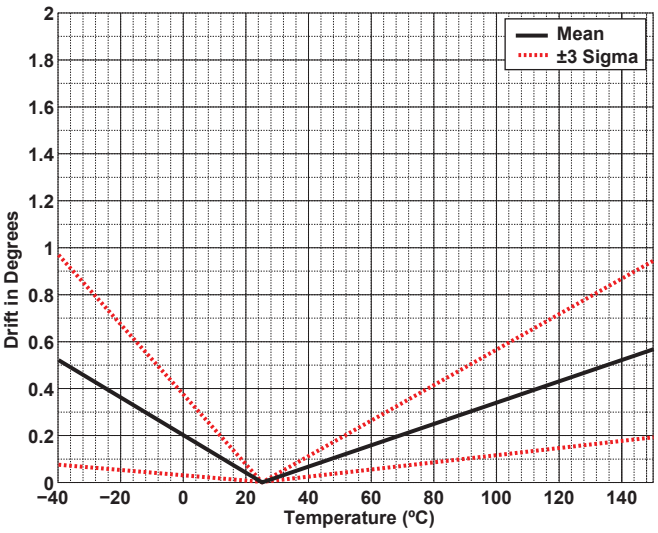

Figure 23: Maximum Temperature-Induced Drift from 25°C (300 G)

Note: Plots depict distributions taken from a production lot of ≈700 pieces. Data does not include shifts over lifetime.

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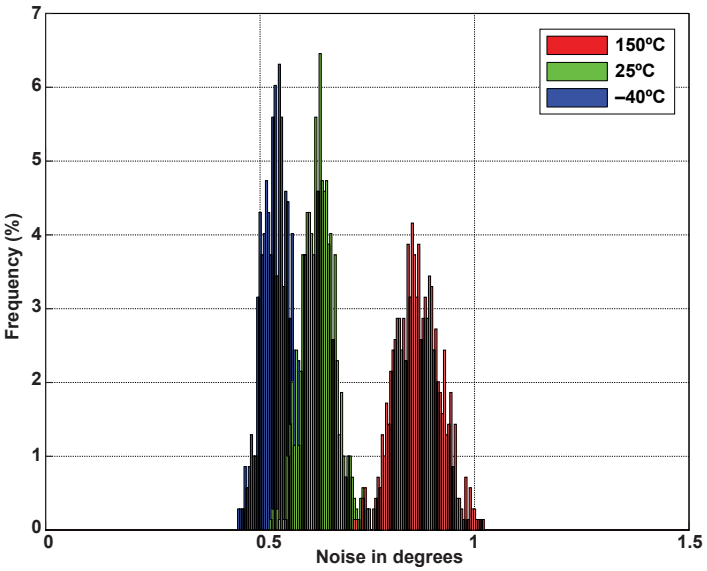

Figure 24: Noise Distribution over Temperature (3 Sigma, 300 G)

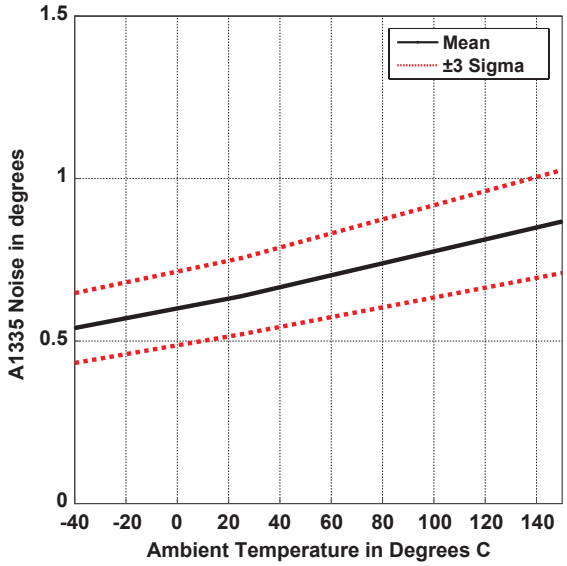

Figure 25: Noise Performance over Temperature (3 Sigma, 300 G)

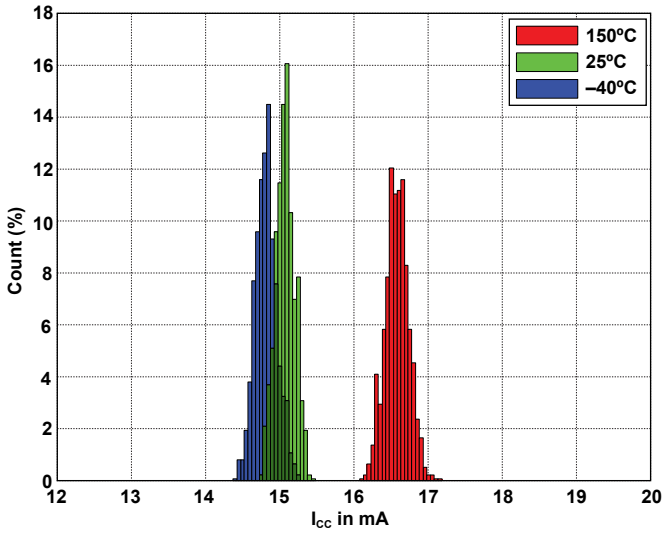

Figure 26: I_{CC} Distribution over Temperature (V_{CC} = 5.5 V)

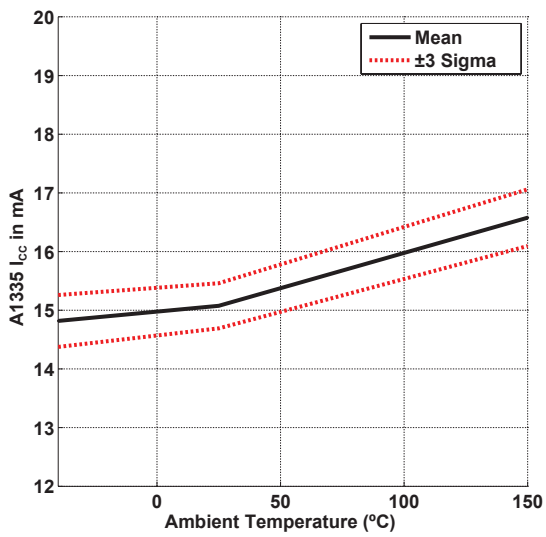

Figure 27: I_{CC} over Temperature (V_{CC} = 5.5 V)

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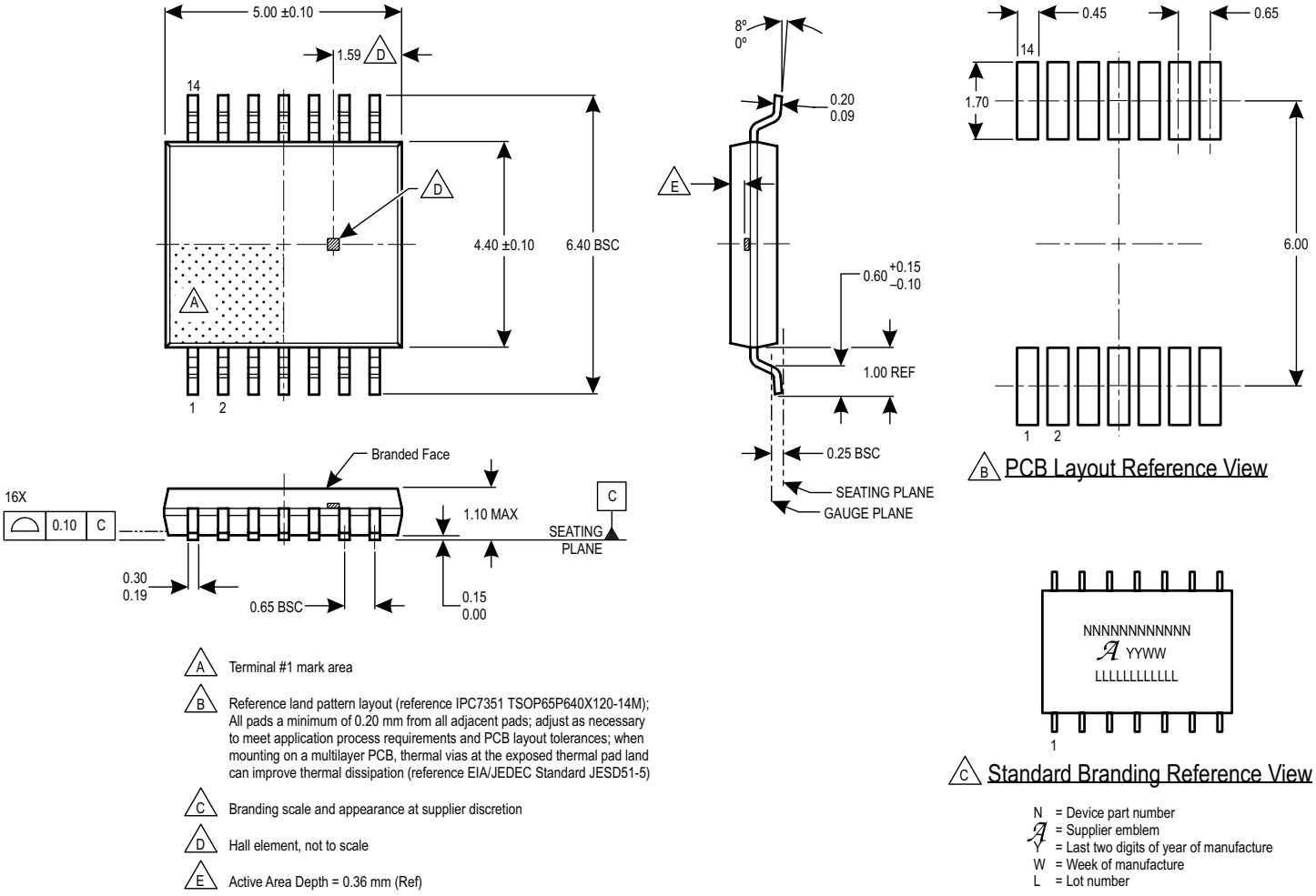
PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference MO-153 AB-1)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 TSOP65P640X120-14M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Branding scale and appearance at supplier discretion

D Hall element, not to scale

E Active Area Depth = 0.36 mm (Ref)

N = Device part number
A = Supplier emblem
Y = Last two digits of year of manufacture
W = Week of manufacture
L = Lot number

Figure 28: Package LE, 14-Pin TSSOP (Single-Die Version)

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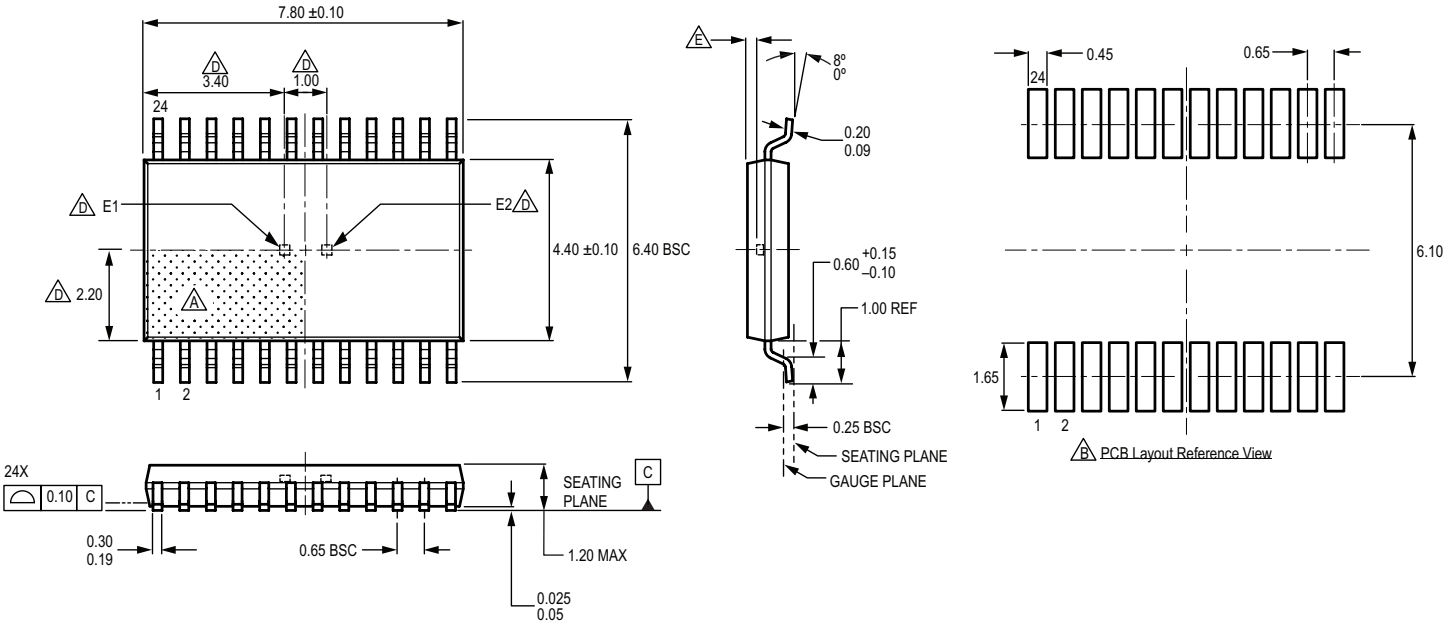
(Reference MO-153 AD)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



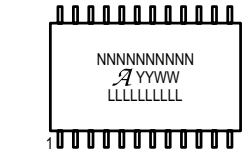
A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 TSOP65P640X120-25M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Branding scale and appearance at supplier discretion

D Hall elements (E1, E2), corresponding to respective die; not to scale

E Active Area Depth 0.36 mm REF



C Standard Branding Reference View

N = Device part number
A = Supplier emblem
Y = Last two digits of year of manufacture
W = Week of manufacture
L = Lot number

Figure 29: Package LE, 24-Pin TSSOP (Dual-Die Version)

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APPENDIX A: SPI INTERFACE ERROR FLAG DESCRIPTION

IER Flag

The IER flag is located in bit 9 of the ERR serial register (0x24:0x25). This flag is designed to assert when the IC detects an improper communication frame, via either SPI or Manchester. For the purposes of this appendix, only the behavior in regards to the SPI bus is discussed. The IER flag asserts upon the following conditions:

- An improper number of SPI clocks is detected.
- The MSB of the MOSI packet is a logic = 1.

Table 6: Err Serial Register

Addr.	0x24								0x25							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Register identifier				XER	XOV	IER	CRC	NR	AT	AH	AL	OV	UV	MH	ML

Behavior When Sharing SPI lines

The IER flag may provide an erroneous indication when sharing the SCLK line among multiple ICs. In the case where an IC is held inactive by bringing the CS line high, the inactive IC(s) continue to count falling SCLK edges. This results in an invalid number of observed SCLK edges, and assertion of the IER flag on the next SPI transaction of the IC. False IER flag assertions differ based on the size of the SPI packet.

SIXTEEN BIT SPI PACKETS

The IER flag always asserts if, during the CS high period, the SCLK line is brought low as follows:

- At least one time, if using a 16-bit SPI packet.

Impact of IER Flagging with 16-Bit Packets

When an incorrect number of SCLK edges is observed by the IC, the following occurs:

1. The IER flag triggers.
2. If the packet preceding the CS high time is a read:
   A. If SCLK drops low within 70 ns of the CS rising edge, there is a possibility the read will be discarded. If this occurs, the output corresponds to the last valid read request for that device.
   B. If the SCLK edge occurs after 70 ns of the CS rising edge, the read is not discarded, potentially corrupting the next immediate response from the device.
3. If the packet preceding the CS high time is a write:
   A. If SCLK drops low within 70 ns of the CS rising edge, there is a possibility the write will be discarded.
   B. If the SCLK edge occurs after 70 ns of the CS rising edge, the write occurs, but the IER flag still asserts.

TWENTY BIT SPI PACKETS

When using 20-bit SPI packets, the IER flag may occur when the SCLK line is brought low while CS is high. The probability of a false IER flag asserting is timing dependent and differs from device to device, but should not occur on more than 3.2% of all SPI transactions. Lab characterization has shown significantly lower assertion rates, with false flags on 0.00% to 0.80% of all SPI transactions.

Impact of IER Flagging with a 20-Bit Packet

When using a 20-bit SPI packet, if an incorrect number of SCLK edges is observed, the following occurs:

1. The IER flag triggers.
2. If the packet preceding the CS high time is a read:
   A. If SCLK drops low within 70 ns of the CS rising edge, there is a possibility the read will be discarded. If this occurs, the output corresponds to the last valid read request for that device.
   B. If the SCLK edge occurs after 70 ns of the CS rising edge, the read occurs as expected.
3. If the packet preceding the CS high time is a write:
   A. If SCLK drops low within 70 ns of the CS rising edge, there is a possibility the write will be discarded.
   B. If the SCLK edge occurs after 70 ns of the CS rising edge, the write occurs, but the IER flag still asserts.

Avoiding IER Flag Assertion

The following methods may be used to avoid false IER flag assertions:

1. Use dedicated SCLK lines for each IC and hold the SCLK line high when CS is high.
   A. This prevents the IC from observing SCLK edge transitions when CS is high.

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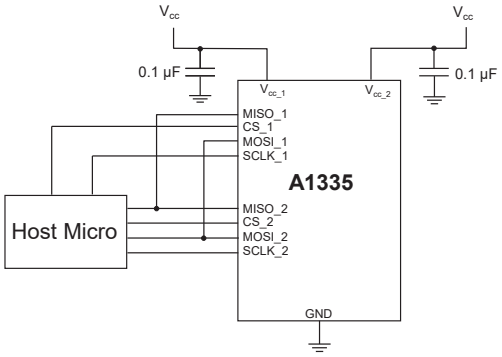

Figure 30: Separate SCLK Lines

2. Use a 21-bit SPI packet.

   A. When using a 21-bit SPI packet, the IC does not count SCLK edges when the CS pin is held high. This prevents the IER flag from improperly asserting, with the exception of power-on.

USING A 21-BIT SPI PACKET

No special EEPROM programming is required for the A1335 to support a SPI packet size of 21 bits; the controller must simply send 21 SCLK pulses during the CS low period. The format of the SPI message is shown in Figure 31.

The controller output-peripheral in (MOSI) signal consists of: a 1-bit SYNC bit defined as a logic of 0, 1-bit read/write (R/W), 6 address bits, 4 CRC bits, and an additional logic of 0. The extra logic of 0 sent on the 21st clock tick effectively shifts the standard 20-bit packet left by one place value.

The controller input-peripheral out (MISO) signal consists of: 16 data bits, the contents of which are determined by the address of the register being read, 4 CRC bits, and a repeat of the MSB of the CRC value. The repeated CRC bit shifted out on the 21st clock edge should be ignored by the controller when processing the CRC to validate the message contents.

POWER-ON BEHAVIOR WITH A 21-BIT SPI PACKET

If the SCLK line is shared on two or more ICs, the IER flag asserts on all idle A1335 die (CS held high) after the first SPI transaction (on the bus) following power-up. This occurs *independent* of the 21-bit SPI packet. This spurious IER flag asserts, on the idle die only during the first SPI transaction. All subsequent SPI transactions process correctly. This spurious assertion does not affect any future reads or writes to the device while power is maintained. If the IC is programmed to validate the CRC on MOSI, a CRC error flag (bit 8 of the ERR serial register) related to the spurious detection of a bad SPI packet also asserts.

To prevent an intial false error report that results from the initial assertion of the IER flag and risks the masking of real SPI communication issues, clear all error and warning flags on all A1335 ICs after power-on.

NOTE: This is a good practice that is also recommended independent of the false IER flag assertion.

By clearing the false IER flag, real SPI communication issues are not masked.

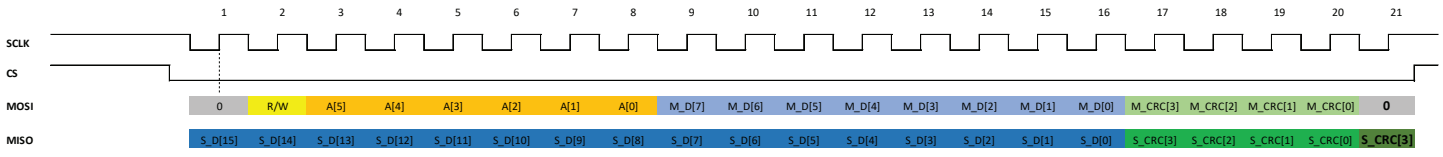

Figure 31: 21-bit SPI Packet Format

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Additional SPI Examples

The examples below show differing SPI implementations. All figures assume a shared SPI bus (MISO, MOSI, SCLK) between two sensors, with individual CS lines.

An example of pipelining SPI reads between two sensors, which can result in discarded packets or corrupted data when used with 16 SPI packets, is shown in Figure 32. In this example, SPI reads are bounced between Sensor 1 and Sensor 2, one frame at a time. During the interval in which the CS lines are high, the inoperative sensor detects an incorrect number of edges, asserting the IER flag and potentially corrupting the following read response.

A modified version of this pipelining approach is shown in Figure 33. The first read response from each sensor is known to be corrupt and is ignored. Because of this, the second read request (which results in the first read response on the next sequence) can be a NOP command, resulting in all zeros from the device (a NOP command is a read of serial register 0x0, which is hardcoded with all 0s). Inserting a NOP command between each valid read response ensures the data placed in the SPI buffers prior to the second response is valid.

It should be noted that the IER flag asserts on every changeover to a new die (CS line) when using this implementation due to the incorrect number of SCLK edges detected during the CS high period.

A 20-bit SPI packet is shown in Figure 34. This removes the potential for incorrect read data (assuming the SCLK edge occurs 70 ns or later following the CS rising edge), allowing the two sensors to be addressed in a sequential manner, one frame per sensor. This implementation has the added advantage of including a 4-bit CRC within each response. The IER flag may still assert when using a 20-bit packet.

Implementation of a 21-bit SPI packet is shown in Figure 35. This removes the false IER flag assertion and any potential for incorrect data interpretation. Allegro recommends using a 21-bit SPI packet when sharing SPI lines.

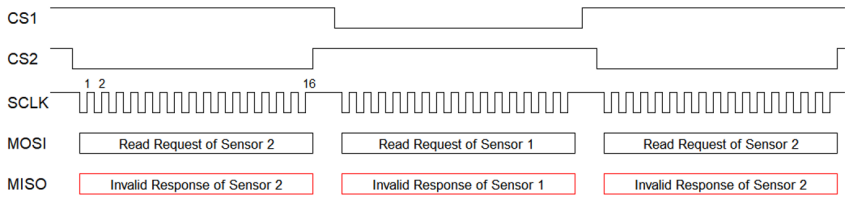

Figure 32: Implementation of SPI using 16-bit packets resulting in IER flag assertion and potentially corrupted data

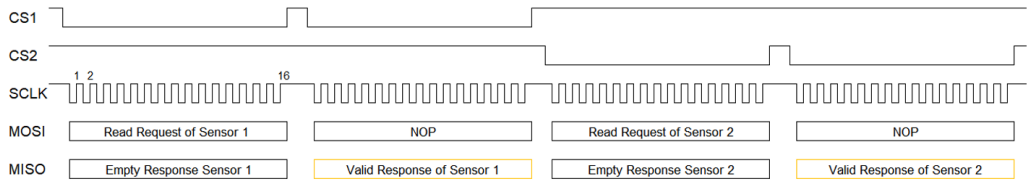

Figure 33: Implementation of SPI using 16-bit packets; valid data, IER flag still asserts

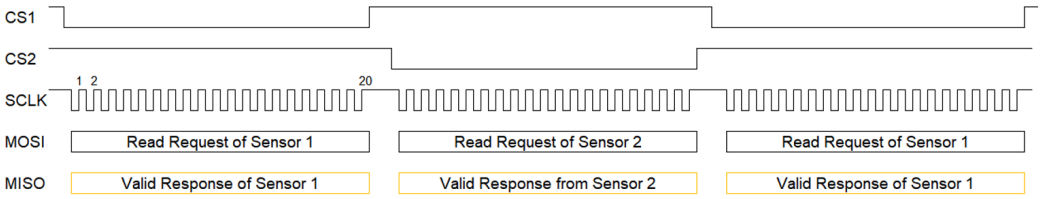

Figure 34: SPI Implementation using 20-bit packets; data contents are valid; however, IER flag may still assert

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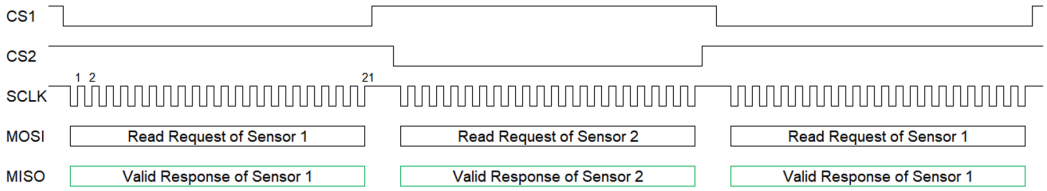

Figure 35: SPI Implementation using 21-bit packets; data contents are valid; no false IER flag generation

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Revision	Change	Pages	Responsible	Date
–	Initial release	All	W. Wilkinson	September 21, 2015
1	Updated Angle Characteristics; reduced SENT and Manchester information redundant with A1335 programming guide; added Field Strength section and charts; added on-axis and off-axis figures; corrected CVH location in single-die package outline drawing.	1, 7, 19, 20, 27	W. Wilkinson	December 17, 2015
2	Corrected LE-24 Package Outline Drawing dimensions	28	W. Wilkinson	April 15, 2016
3	Updated Magnetic Field values in Operating Characteristics table	6	W. Wilkinson	July 5, 2016
4	Added description of zero degree position, CS_idle time parameter; CVH self-test operation restricted to field ≤ 300 G, temperature ≥ 25°C; Noise plots and table entry updated with 3 sigma values.	4, 6, 10, 18, 24, 26	W. Wilkinson	July 30, 2018
5	Minor editorial updates	All	R. Couture	August 26, 2019
6	Added SPI Clock Duty Cycle characteristic	4	W. Wilkinson	November 1, 2021
	Updated footnote 4	6		
	Updated Serial Interface Description section	16		
	Added Appendix A	A-1 to A-4		
7	Updated Figure 23 title and added note	25	W. Wilkinson	April 19, 2022
8	Change to lifetime drift specification	6	W. Wilkinson	July 6, 2022
9	Correction to functional block diagram and lifetime drift specification note	1, 6	W. Wilkinson	August 4, 2022
10	Added notes to Operating Characteristics for SPI Clock Duty Cycle and Logic Input High Level	4	W. Wilkinson	August 19, 2022
11	Changed archaic terminology and made minor editorial changes, per revised Technical Writing Style Guidelines.	All	J. Henry	September 12, 2023

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