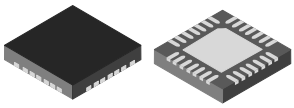
Automotive Three-Phase and Battery Isolator MOSFET Driver

FEATURES AND BENEFITS

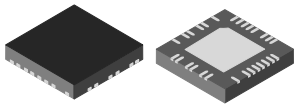
- Five floating N-channel MOSFET drives
- Maintains V_{GS} with 100 kΩ gate-source resistors
- Integrated charge pump controller
- 4.5 to 85 V supply voltage operating range
- Supports source-to-source and drain-to-drain battery MOSFET isolation
- V_{CP} and V_{GS} undervoltage protection
- 150°C ambient (165°C junction) continuous
- Fully integrated diagnostics for safe motor phase and battery disconnect
- Extensive programmable diagnostics
- Diagnostic verification
- Automotive AEC-Q100 qualified
- A^2-SIL™ product—device features for safety-critical system: Developed in accordance with ISO 26262 as a hardware safety element out of context with ASIL B capability for use in automotive safety-related systems when integrated and used in the manner prescribed in the applicable safety application note and datasheet.

PACKAGES

Not to scale



28-contact QFN with wettable flanks and exposed pad (suffix ET)



28-contact QFN with wettable flanks and exposed pad (suffix EV)

DESCRIPTION

The A89103 is an N-channel power MOSFET driver capable of controlling five MOSFETs to provide motor-phase isolation and supply isolation in three-phase BLDC applications. Three floating gate-drive outputs maintain phase-isolator power MOSFETs in the on state, over the full supply range, with high-phase voltage and high dv/dt on the motor-phase connection for 12 V and 48 V systems. Two additional floating gate drivers are provided to isolate the battery supply voltage during reverse-battery or short-circuit conditions. The A89103 supports both source-to-source and drain-to-drain battery MOSFET isolation. An integrated charge-pump regulator provides the above-battery-supply voltage necessary to continuously maintain the power N-channel MOSFETs in the on state. The charge pump maintains sufficient gate drive power (> 7.5 V) for battery voltages down to 4.5 V with 100 kΩ gate source resistors.

The five floating gate drives can be configured, monitored, and controlled through the SPI interface. When not in use, the A89103 can be placed in a low-power sleep mode.

Undervoltage monitors check that the pumped supply voltage and the gate drive outputs are high enough to ensure that the MOSFETs are maintained in a safe conducting state.

The A89103 is supplied in a 28-contact wettable-flank quad flat no-lead (QFN) package (suffix ET), and 28-contact wettable-flank QFN (suffix EV), both with exposed pads for enhanced thermal dissipation. They are lead (Pb) free, with 100% matte tin leadframe plating.

TYPICAL APPLICATIONS

- Three-phase and battery isolation for ASIL systems up to level B
- Electric power steering (EPS)
- Electric braking (EMB)
- Redundant motor-control systems

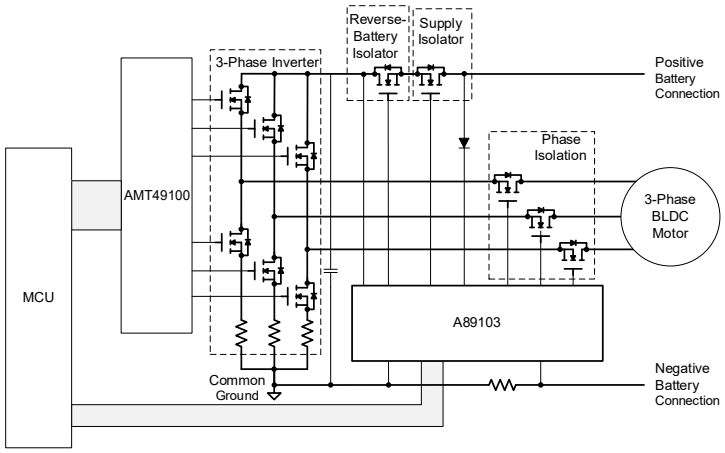


Figure 1: Typical Application Diagram

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SPECIFICATIONS

SELECTION GUIDE

Part Number	I/O Logic	Package
A89103KETSR-3	3.3 V	5 mm × 5 mm × 0.75 mm 28-contact QFN with exposed thermal pad
A89103KETSR-5	5 V	
A89103KEVSR-3	3.3 V	6 mm × 6 mm × 0.9 mm 28-contact QFN with exposed thermal pad
A89103KEVSR-5	5 V	

ESD RATINGS

ESD Information for Handling of ESDS in an ESD Protected Area
CDM (AEC-Q100-011JS-002: CDM withstand threshold of 1000 V; CDM Class C3
HBM (AEC-Q100-002/JS-00102017): HBM withstand threshold of 1500 V; HBM Class 2 NOTE: The HBM withstand threshold is determined by two pins (GREV and GBRG) that pass at 1500 V. All other pins pass at 2000 V.

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ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Conditions	Rating [1]	Units
Load Voltage Supply	V_{BB}		–0.3 to 85	V
Terminal VCP	V_{CP}		V_{BB} – 0.3 to V_{BB} + 12	V
Terminal CP1	V_{CP1}		V_{BB} – 12 to V_{BB} + 0.3	V
Terminal CP2	V_{CP2}		V_{BB} – 0.3 to V_{CP} + 1	V
Terminal CP3	V_{CP3}		V_{BB} – 12 to V_{BB} + 0.3	V
Terminal CP4	V_{CP4}		V_{BB} – 0.3 to V_{CP} + 1	V
Terminal CSn, SCK, MOSI, MISO, DIAG	V_{IO}	A89103KETSR-3	–0.3 to 4 [2]	V
Terminal CSn, SCK, MOSI, MISO, DIAG	V_{IO}	A89103KETSR-5	–0.3 to 6 [2]	V
Terminal SWIN	V_{SWIN}	$V_{SWINSCL}$ > 85 V	–0.3 to SCL [3]	V
Terminal SWIN	I_{SWIN}		–4 to 4	mA
Terminal SWOUT	V_{SWOUT}		–0.3 to 6	V
Terminal GU, GV, GW, GREV, GBRG	V_{GX}		V_{SX} – 0.3 to V_{SX} + 16	V
Terminal CSP, CSM	V_{CSN}		–4 to 6	V
Terminal LSS	V_{LSS}		–4 to 6	V
Terminal SU, SV, SW	V_{Sx}		–16 to 85	V
Terminal SREV, SBRG	V_{SREV},V_{SBRG}	$V_{SREVSCL}$ and $V_{SBRGSCL}$ < –16 V	–SCL [4] to 85	V
Terminal SREV, SBRG	I_{SREV}, I_{SBRG}	Limited by power dissipation	–150 to 10	mA
Terminal VBRG	V_{BRG}		–5 to 85	V
Operating Ambient Temperature	T_A	Limited by power dissipation	–40 to 150	°C
Maximum Continuous Junction Temperature	$T_{J(max)}$		165	°C
Transient Junction Temperature	T_{Jt}	Overtemperature event not exceeding 10 seconds; lifetime duration not exceeding 10 hours; guaranteed by design characterization	180	°C
Storage Temperature	T_{stg}		–55 to 150	°C

[1] With respect to GND, unless otherwise specified. Ratings apply when no other circuit operating constraints are present.
[2] The V_{IO} absolute maximum voltage ratings can be exceeded if the terminal currents are externally limited to ± 10 mA. The VIO terminals conduct when the voltage exceeds a diode below ground or a diode above V_{IO}.
[3] This terminal self-clamp sat a self-clamp level (SCL) of greater than 85 V. The resistor divider impedance should be chosen to ensure the terminal current does not exceed the I_{SWIN} absolute maximum rating under any condition.
[4] These terminals self-clamp at an SCL of less than –16 V. The terminal current during self-clamping must not exceed the I_{SREV} or I_{SBRG} absolute maximum ratings under any condition. The current level and duration may be limited by package power dissipation limits and transient junction temperature limits.

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THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [1]	Value	Units
Package Thermal Resistance, ET Package (Junction to Ambient)	$R_{\theta JA}$	Four-layer PCB based on JEDEC standard	32	°C/W
	$R_{\theta JP}$		2	°C/W
Package Thermal Resistance, EV Package (Junction to Pad)	$R_{\theta JA}$	Four-layer PCB based on JEDEC standard	27	°C/W
	$R_{\theta JP}$		2	°C/W

[1] Additional thermal information available on the Allegro website.

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PINOUT DIAGRAMS AND TERMINAL LIST TABLE

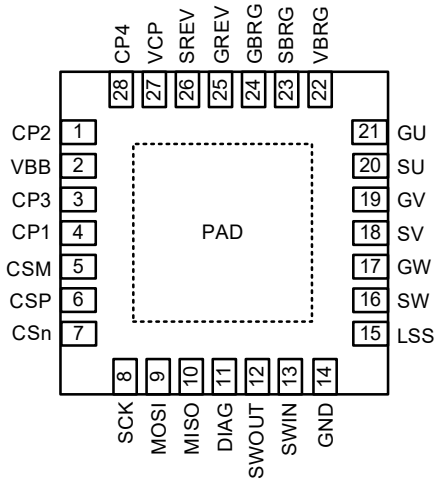

Figure 2: Package ET, 28-Pin, 5 × 5 QFN Pinouts

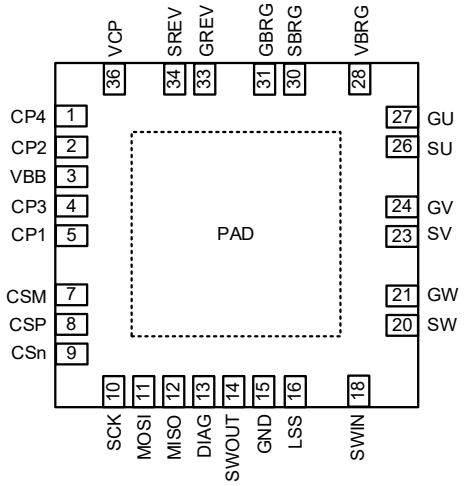

Figure 3: Package EV, 28-Pin, 6 × 6 QFN Pinouts

Terminal List Table

Name	Number (ET)	Number (EV)	Description
CP1	4	5	Charge-Pump Capacitor Connection
CP2	1	2	Charge-Pump Capacitor Connection
CP3	3	4	Charge-Pump Capacitor Connection
CP4	28	1	Charge-Pump Capacitor Connection
CSM	5	7	Current Sense, Negative Input
CSn	7	9	Chip Select (Active Low)
CSP	6	8	Current Sense, Positive Input
DIAG	11	13	Programmable Diagnostic Bidirectional Pin
GBRG	24	31	Bridge-Supply Isolator MOSFET Gate Drive
GND	14	15	Ground
GREV	25	33	Reverse-Battery Isolator MOSFET Gate Drive
GU	21	27	U-Phase MOSFET Gate Drive
GV	19	24	V-Phase MOSFET Gate Drive
GW	17	21	W-Phase MOSFET Gate Drive
LSS	15	16	Extra Pin
MOSI	9	11	Serial Data Input
MISO	10	12	Serial Data Output
SBRG	23	30	Bridge-Supply Isolator MOSFET Source Reference
SCK	8	10	Serial Clock Input
SREV	26	34	Reverse-Battery Isolator MOSFET Source Reference
SU	20	26	U-Phase MOSFET Source Reference
SV	18	23	V-Phase MOSFET Source Reference
SW	16	20	W-Phase MOSFET Source Reference
SWIN	13	18	VBAT Divider Switch Input
SWOUT	12	14	VBAT Divider Switch Output
VBB	2	3	Main Power Supply
VBRG	22	28	Bridge High-Side MOSFET Drain Reference
VCP	27	36	Pumped Supply
PAD	–	–	Exposed Pad, Connect to GND

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FUNCTIONAL BLOCK DIAGRAMS

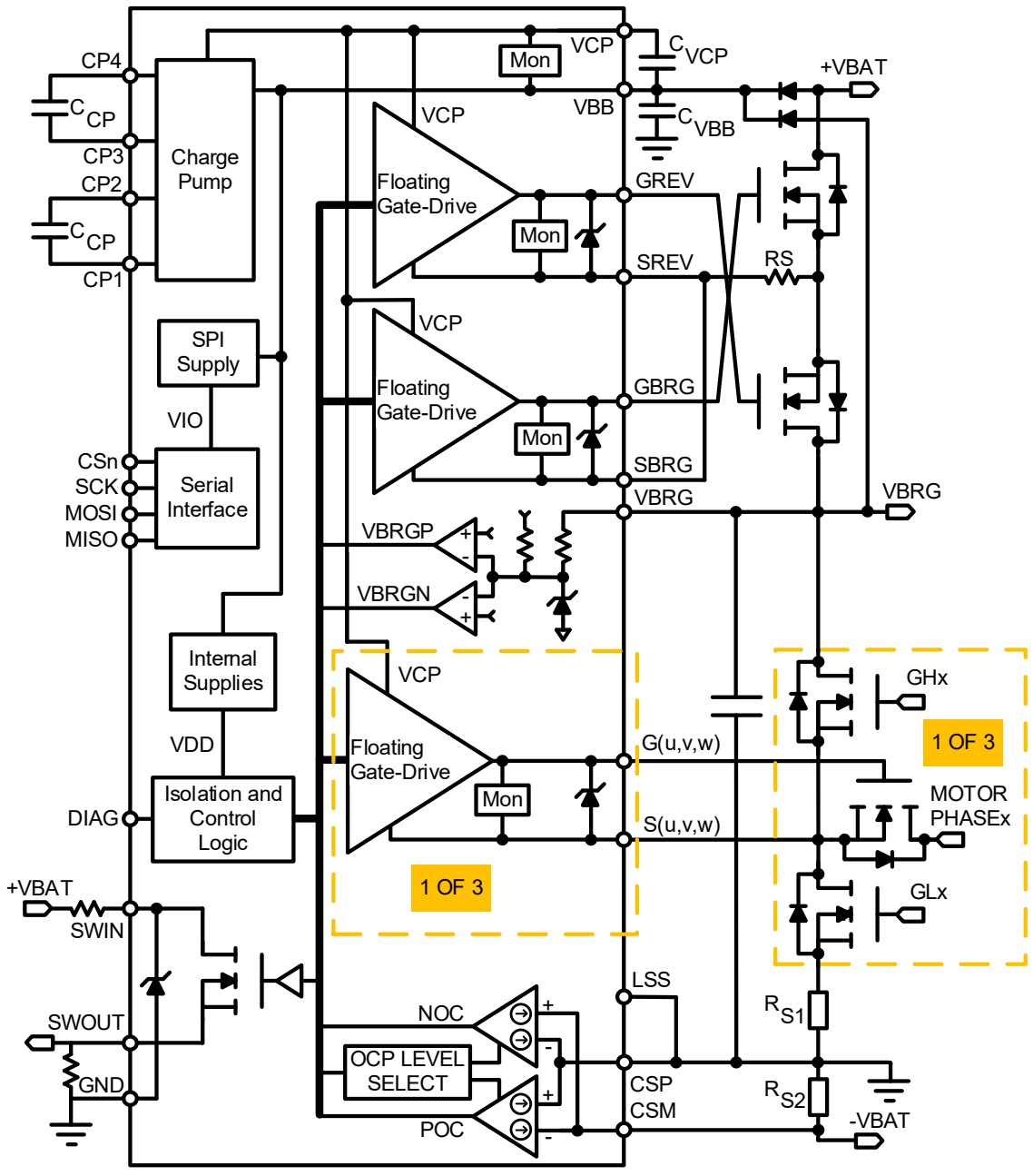

Figure 4: Battery-Disconnect Common-Source Configuration

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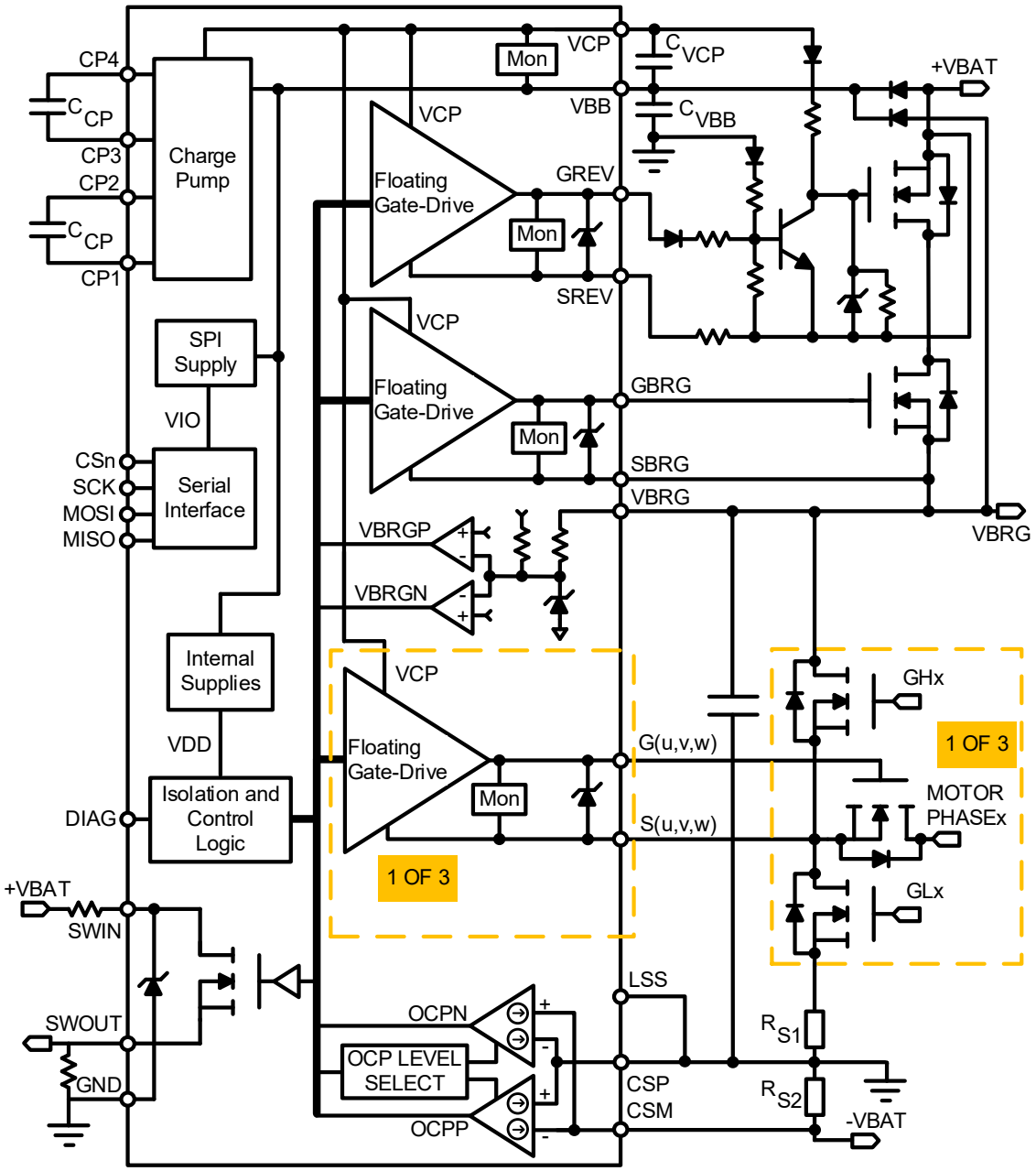

Figure 5: Battery-Disconnect Common-Drain Configuration

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CHARACTERISTIC PERFORMANCE

OPERATING CHARACTERISTICS: Valid at T_J = –40 to 150°C, V_{BB} = 4.5 to 85 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
SUPPLY						
VBB Functional Operating Range [1]	V_{BB}	Operating; outputs active	4.5	–	85	V
		Operating; outputs disabled	4	–	85	V
		No undefined states [1]	0	–	85	V
VBB Supply Current	I_{BB}	Gate drive off, V_{BB} = 12 V	–	–	20	mA
	I_{BBS}	Sleep mode, V_{BB} = 12, 48 V, T_J < 85°C, CSn < V_{CSnL} (0.66 V)	–	–	3	µA
VCP Output Voltage, with respect to VBB	V_{CP}	V_{BB} > 6 V, I_{VCP} > –1 mA [2][3]	9.5	10.5	11.5	V
		4.5 V < V_{BB} ≤ 6 V, I_{VCP} > –800 µA [2][3]	8	8.5	–	V
VBB Undervoltage	V_{BBON}	V_{BB} rising	3.85	4	4.15	V
	V_{BBOFF}	V_{BB} falling	3.6	3.75	3.9	V
VDD Undervoltage [4]	V_{DDON}	V_{DD} rising	2.7	–	3	V
	V_{DDOFF}	V_{DD} falling	2.6	–	2.8	V
VDD Undervoltage Hysteresis [4]	V_{DDUVH}		200	250	300	mV
Internal Logic I/O Regulator Voltage	V_{IO}	A89103KETSR-3, V_{BB} > 4 V	3.17	3.3	3.43	V
		A89103KETSR-5, V_{BB} > 5.5 V	4.8	5	5.2	V
DIAGNOSTICS AND PROTECTION						
Internal Timing Clock Frequency	f_{CLK}	Uncalibrated [5]	2.5	4	5.5	MHz
VGS Undervoltage Threshold Rising	V_{GSUV}	SDCFG = 0	5.7	6.5	7.35	V
VGS Undervoltage Threshold Hysteresis	V_{GShys}	SDCFG = 0	–	200	–	mV
VGS Undervoltage Filter Time	t_{GSUV}		3.7	–	18	µs
VCP Undervoltage Filter Time	t_{CPUV}		–	12.5	–	µs
VCP Startup Blank Timer	t_{CPON}		–	100	–	µs
VCP Undervoltage Lockout	V_{CPON}	V_{CP} with respect to V_{BB}, V_{CP} rising	6.5	7	7.5	V
	V_{CPOFF}	V_{CP} with respect to V_{BB}, V_{CP} falling	6.25	6.75	7.25	V
Current Comparator Input Open Threshold	V_{CD}		1.8	2.2	2.6	V
Current Sense Disconnect Filter Time	t_{CD}		6	10	14	µs
Temperature Warning Threshold	T_{JW}	Temperature increasing	–	160	–	°C
Temperature Warning Hysteresis	T_{JWHys}		–	15	–	°C

[1] Function is correct, but parameters are not guaranteed below the general limits (4.5 to 85 V).
[2] For input and output current specifications, negative current is defined as coming out of the specified device terminal (termed “sourcing”).
[3] Tested with all drivers in the on state. I_{VCP} current specified is the minimum average V_{CP} current available for driver on-/off-switching transitions, in addition to the static on-state current.
[4] Verified by design and characterization. Not production tested.
[5] The f_{CLK} frequency can be calibrated through the SPI interface to improve accuracy.

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OPERATING CHARACTERISTICS: Valid at T_J = –40 to 150°C, V_{BB} = 4.5 to 85 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
GATE DRIVE						
Turn-On Rise Time	t_r	C_{LOAD} = 2. 5 nF, 20% to 80%, S*x* < V_{BB}	–	1.2	2	µs
Turn-Off Fall Time	t_f	C_{LOAD} = 2. 5 nF, 20% to 80%, S*x* < V_{BB}	–	0.15	0.2	µs
Propagation Delay—Turn On	t_{PON}	C_{LOAD} = 2.5 nF, internal enable command to G*x* 20%	–	–	0.85	µs
Propagation Delay—Turn Off	t_{POFF}	C_{LOAD} = 2.5 nF, internal disable command to G*x* 80%	–	–	0.4	µs
Turn-On Pulse Current	I_{GPx}		8.5	11.5	14.5	mA
Turn-On Pulse Time	t_{GPx}		16	26	36	µs
On Hold Current	I_{GHx}		200	300	400	µA
Pull-Down On Resistance	$R_{DS(on)DN}$	T_J = 25°C, I_{Gx} = 10 mA	–	5	6.5	Ω
		T_J = 150°C, I_{Gx} = 10 mA	–	10	13	Ω
G*x* Output High Voltage, with respect to S*x*, when S*x* ≤ V_{BB}	V_{GH}	V_{BB} > 6 V	9	9.5	12	V
		4.5 V < V_{BB} ≤ 6 V	7.5	8	–	V
Gate Drive Static Load Resistor	R_{GS}	Between G*x* and S*x* (using ±1% tolerance resistor)	100	–	–	kΩ
G*x* Output Voltage Low	V_{GL}	–10 µA < I_{Gx} < 10 µA	–	–	V_{Sx} + 0.3	V
G*x* Passive Pull-Down	R_{GPD}	V_{Gx} – V_{Sx} < 0.3 V	–	950	–	kΩ
VBAT RESISTOR DIVIDER SWITCH						
Divider Switch On Resistance	R_{SW}		–	–	100	Ω
Divider Switch Off State Leakage	I_{LSW}	V_{SWIN} = 85 V, T_J < 85°C	–	–	1	µA
SWOUT Operational Range	V_{SWOR}		0	–	5.5	V

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Characteristics	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
OVERCURRENT PROTECTION						
OCP Comparator Threshold	V_{OCP}	OCP = 17	15	18	21	mV
		OCP = 63	59	64	69	mV
		OCP = 99	93	100	107	mV
		OCP = 127	118.8	128	137.5	mV
OCN Comparator Threshold	V_{OCN}	OCN = 17	–21	–18	–15	mV
		OCN = 63	–69	–64	–59	mV
		OCN = 99	–107	–100	–93	mV
		OCN = 127	–137.5	–128	–118.8	mV
OCP/OCN Common Mode Range	V_{CM}		–1.8	–	2	V
CSP Input Bias Current [1]	I_{BIASP}	V_{CM} in range	–160	–	–	µA
CSM Input Bias Current [1]	I_{BIASM}	V_{CM} in range	–160	–	–	µA
CSP/CSM Input Bias Current Matching [1]	I_{BIASCM}	V_{CM} in range, OCP = 127, OCN = 18	–15	–	+15	µA
Comparator Propagation Delay Time	t_{CPD}	V_{OD} = 25 mV, OCP = 99	–	–	500	ns
VBRG PROTECTION						
VBRG Comparator Positive-Voltage Threshold [2]	V_{VBRGP0}	VCMFG = 0	1.2	1.5	1.8	V
	V_{VBRGP1}	VCMFG = 1	5.75	6	6.4	V
VBRG Comparator Negative-Voltage Threshold [2]	V_{VBRGN0}	VCMFG = 0	–1	–0.75	–0.5	V
	V_{VBRGN1}	VCMFG = 1	–1	–0.75	–0.5	V
VBRG Comparator Filter Time	t_{CPBR}		–	1	–	µs
IO LOGIC (CSn, MOSI, MISO, SCK, DIAG)						
Input Low Voltage	V_{IL}		–	–	0.8	V
Input High Voltage	V_{IH}	All logic inputs	2	–	–	V
Input Hysteresis	V_{IHYS}	All logic inputs	250	550	–	mV
Input Negative Clamping Voltage	V_{ILNC}	I = –10 mA	–	–100	–	mV
MOSI and SCK Input Pull-Down	R_{PD}		37	50	63	kΩ
Logic Overvoltage Threshold	V_{LO}	V_{IO} rising	6.1	6.3	6.5	V
		Hysteresis	–	0.5	–	V
CSn Input Pull-Up to V_{IO}	R_{PU}	When device active	37	50	63	kΩ
Output Low Voltage	V_{OL}	(MISO) I_{OL} = 1 mA [1]	–	–	0.4	V
	V_{OL}	(DIAG) I_{OL} = 2 mA [1]	–	–	0.4	V
Output High Voltage (MISO)	V_{OH}	A89103-5, I_{OH} = –1 mA [1]	4	–	–	V
	V_{OH}	A89103-3, I_{OH} = –1 mA [1]	2.85	–	–	V

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (termed “sourcing”); positive current is defined as going into the node or pin (termed “sinking”).

[2] Comparator voltage thresholds are measured with respect to ground.

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OPERATING CHARACTERISTICS: Valid at T_J = –40 to 150°C, V_{BB} = 4.5 to 85 V, unless noted otherwise

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SERIAL INTERFACE TIMING						
SPI Clock Frequency	f_{SCK}	MISO pins, C_L = 20 pF	0.1	–	10	MHz
SPI Frame Rate	t_{SPI} [1]		3.15	–	181.8	kHz
Clock High Time	$t_{SCK,H}$	A in Figure 6	50	–	–	ns
Clock Low Time	$t_{SCK,L}$	B in Figure 6	50	–	–	ns
Chip Select Lead Time to SCK Low	t_{CSLD}	C in Figure 6	1			µs
Chip Select Lag Time	$t_{CSn,LG}$	D in Figure 6	30	–	–	ns
Chip Select High Time	$t_{CSn,H}$	E in Figure 6	1320	–	–	ns
Data Out (MISO) Enable Time [2]	$t_{MISO,EN}$	F in Figure 6	–	–	50	ns
Data Out (MISO) Disable Time [2]	$t_{MISO,D}$	G in Figure 6	–	–	30	ns
Data Out (MISO) Valid Time from SCK Falling [2]	$t_{MISO,V}$	H in Figure 6, A89103-5	–	–	50	ns
		H in Figure 6, A89103-3	–	–	75	ns
Data Out (MISO) Hold Time from SCK Falling	$t_{MISO,H}$	J in Figure 6	5	–	–	ns
Data In (MOSI) Set-Up Time to SCK Rising	$t_{MOSI,SU}$	K in Figure 6	15	–	–	ns
Data In (MOSI) Hold Time from SCK Rising	$t_{MOSI,H}$	L in Figure 6	10	–	–	ns
SCK High from CSn Rising	$t_{CSn,HCK}$	M in Figure 6	30	–	–	ns
SCK High to CSn Rising	$t_{CSn,LCK}$	N in Figure 6	30	–	–	ns
Wake Up from Sleep	t_{EN}				100	µs
CSn Wake-Up Threshold Rising	V_{CSnH}		0.8	1.33	1.68	V
CSn Wake-Up Threshold Falling	V_{CSnL}		0.66	1.12	1.43	V
CSn Wake-Up Threshold Hysteresis	V_{CSn}		128	215	300	mV

[1] $t_{SPI} = t_{CSLD} + t_{CSn,Lg} + t_{CSn,H} + (32 \times t_{SCK,L}) + (31 \times t_{SCK,H})$; $t_{SPI(min)}$ is calculated using a value of $t_{SCK,H}$ and $t_{SCK,L}$ = 5 µs.
[2] Verified by design and characterization. Not production tested.

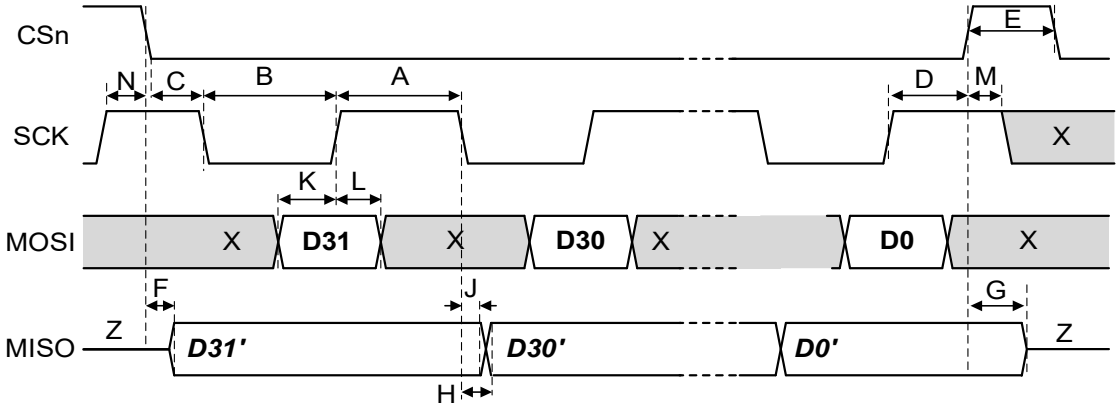

Figure 6: Serial Interface Timing for Write and Read Cycle

X = not relevant; Z = high impedance; MISO activity assumes the chip ID from the previous frame was correct

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FUNCTIONAL DESCRIPTION

Overview

The A89103 is an N-channel power MOSFET driver capable of controlling five MOSFETs to provide motor-phase isolation and power-supply isolation in three-phase BLDC applications.

Three floating gate drivers are capable of driving N-channel power MOSFETs for motor-phase isolation. These MOSFETs are placed in series with each motor phase and can be used to restrict current flowing into the motor, as shown in Figure 3 and Figure 4. The three-phase disconnect MOSFET can be turned on (enabled) through SPI and kept in the on state, over the full supply range. When enabled by SPI, the three floating gate-drive outputs maintain the phase-isolator power MOSFETs in the on state, over the full supply voltage range. When a system failure occurs, the phase-isolator power MOSFETs can be disabled to allow the motor to spin freely. The A89103 is capable of providing all the data required to safely disconnect the phase MOSFETs via the serial interface.

The two floating gate drivers for battery isolation are capable of independently controlling a wide range of N-channel MOSFETs in source-to-source or drain-to-drain configuration for battery disconnect. These MOSFETs are connected in series and are placed between the battery supply (VBB) and the DC bridge (VBRG) as shown in Figure 3 and Figure 4. When these MOSFETS are turned off, they block the current flowing to and from VBRG, isolating the bridge or inverter from the supply. This protects the bridge in the case of a negative battery and protects the battery in the case of a malfunction, such as a short in the bridge. These MOSFETs can be used independently for auxiliary functions as switches when battery-disconnect features are not required.

To facilitate battery isolation, two comparators are included to sense the bridge voltage, as well as two comparators used to sense positive and negative current for the negative battery connection. The two voltage comparators detect positive-undervoltage (UVP) and negative-undervoltage (UVN) nominal voltage conditions.

Detected UVP and UVN conditions are flagged in the SPI diagnostics and can be configured through the SPI to independently trigger the automatic disabling of the supply- and phase-disconnect MOSFETS.

The current sense comparator detects positive-overcurrent (OCP) and negative-overcurrent (OCN) conditions, and the thresholds can be controlled through the SPI interface.

The positive- and negative-overcurrent fault conditions are flagged in the SPI diagnostics and can be configured through the SPI to independently trigger the automatic disabling of the supply- and phase-disconnect MOSFETS.

When power is not applied to VBB, the MOSFET connected to GREV is held off by passive and active circuit elements to prevent reverse battery current flow.

DC link capacitor charging current can be limited by using a positive-overcurrent fault circuit to prevent a high inrush current spike when connecting VBRG. The charging current pulse and charging rate can be programmed through the SPI interface as described in the DC Link Charging section.

An integrated charge-pump regulator provides the voltage that is a larger magnitude than the battery supply voltage necessary to continuously maintain the power MOSFETs in the on state. The charge pump maintains sufficient gate drive power (> 7.5 V) for battery voltages down to 4.5 V with 100 kΩ gate source resistors.

Undervoltage monitors check that the pumped supply voltage (VCP) and the gate drive outputs are high enough to ensure that the MOSFETs are maintained in a safe conducting state. Both the gate driver and charge pump voltages are monitored. If the pumped supply voltage or any gate drive output voltage is less than the undervoltage threshold for longer than a fault filter time, a fault becomes set and can be read-back from the SPI.

A SPI-compatible serial interface with watchdog function is incorporated to configure, control, and monitor device operation.

The A89103 allows for the battery voltage to be measured. Two pins are dedicated to sense the voltage at the supply while minimizing the current drawn from the supply for sensing.

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Input and Output Terminal Functions

VBB

Main power supply for internal regulators and charge pump. The main power supply should be connected to VBB through a reverse voltage protection circuit as shown in Figure 3 and Figure 4 and should be decoupled with ceramic capacitors connected close to the supply and ground terminals.

VBRG

Sense input to the top of the external MOSFET bridge. Allows detection of a negative- or positive-undervoltage event.

CP1, CP2, CP3, CP4

Pump capacitor connection for charge pump. Connect a ceramic capacitor with a recommended nominal value of 680 nF between CP1 and CP2 and 680 nF between CP3 and CP4. These capacitors should have a rated working voltage of at least 25 V and a tolerance of ±20% or better.

VCP

Regulated voltage (10.5 V, typical), used to supply the five floating gate drivers and to provide current for the above supply charge pump. A sufficiently large storage capacitor must be connected to this terminal to provide the required transient charging current.

GND

Analog, digital, and inverter ground. This ground does not connect to the supply ground. For more information, refer to the Layout Recommendations section.

GREV

Gate-drive output for an external N-channel MOSFET used for reverse supply protection.

GBRG

Gate-drive output for an external N-channel MOSFET used for bridge supply protection.

GU, GV, GW

Floating gate-drive outputs for external N-channel MOSFETs used for phase disconnection.

SREV

Source connection for reverse-protection MOSFET that provides the negative-supply connections for the floating gate diver.

SBRG

Source connection for the bridge-protection MOSFET that provides the negative-supply connections for the floating gate diver.

SU, SV, SW

Source connection for the phase-disconnection MOSFETs that provide the negative-supply connections for the floating gate divers.

LSS

An extra pin for future development. This pin must be connected to ground.

CSP, CSM

Current sense monitor inputs.

SWIN, SWOUT

Input and output terminals for the VBAT resistor divider switch.

MOSI

Serial data logic input with pull-down. 32-bit serial word input, most-significant-bit (msb) first.

MISO

Serial data output. High impedance when CSn is high. Outputs the STATUS_0 register of the previous frame when CSn is pulled low if a read was not requested. Otherwise, the data of the selected register is output.

SCK

Serial clock logic input with pull-down. Data is latched-in from the serial digital interface (SDI) on the rising edge of SCK. There must be 32 rising edges per write, and SCK must be held high when CSn changes.

CSN

Serial data strobe and serial access enable logic input with pull-up. When CSn is high, any activity on SCK or MOSI is ignored and MISO is high impedance, allowing multiple SPI peripherals to have common MOSI, SCK, and MISO connections.

DIAG

Diagnostic output. Provides general fault flag output and can be programmed to output the internal clock frequency.

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Power Supply

A reverse-polarity-protected power-supply voltage (V_{BB}) is required to provide power to the A89103. This power supply is connected to the VBB pin. The VBB pin is internally isolated from the VBRG pin and can be driven from separate power supplies. In this scenario, VBRG can be disconnected and the supply to the A89103 can be simultaneously maintained. A good practice is to introduce a path from VBRG to VBB through a diode, as shown in Figure 3 and Figure 4. This allows the device to be temporarily back-powered from the large DC link capacitors connected to VBRG when the VBB connection is lost. Decoupling of the supply is recommended using a ceramic capacitor connected close to the device supply (VBB) and ground (GND) terminals. This decoupling capacitor must be rated to remove the DC current ripple that occurs due to the switching of the charge pump. A 470 nF ceramic capacitor is recommended because it gives a good balance of speed and current decoupling. The method for calculating the size of the decoupling capacitor can be found in the Application Information section.

An energy-storage capacitor (C_{VBB}) is also recommended, connected close to the device. This capacitor should be sized to provide sufficient supply during supply isolation or loss of power that it can hold-up to allow the system to complete the required isolation operation. Typically, a 220 µF electrolytic capacitor is used. Sizing of this capacitor is described in the Application Information section.

The A89103 operates within specified parameters with V_{BB} from 4.5 V to 85 V and can maintain the external phase-isolator MOSFETs in the off condition down to 4 V. The A89103 operates without any undefined states down to 0 V to ensure deterministic operation during power-up and power-down events. As the supply voltage rises from 0 V, the gate-drive outputs are maintained in the off state until the charge pump voltage is sufficiently high to ensure conduction and enablement of the outputs via the SPI interface.

The A89103 input/output (I/O) voltage can be selected by ordering the A89103-5 part number for 5 V operation or the A89103-3 part number for 3.3 V operation. The device selected determines the digital high output voltage on the MISO terminals and the logic input high threshold.

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DC LINK CHARGING

When charging the DC link capacitor, it is common to encounter a large inrush current drawn from the power supply at startup. A typical RC charging circuit with a switch, where the capacitor is the DC link capacitor and the resistor represents the sum of the turn-on gate resistance of the bridge supply and the reverse battery MOSFETs, is shown in Figure 7. The switch represents the bridge supply MOSFET When the switch is closed at time 0, the uncontrolled current flowing into the capacitor decays as shown in Figure 8. This large current is known as the inrush current and can damage components in the system.

Overcurrent protection circuitry can be used to limit the charge current for the DC link capacitor. This is accomplished by providing a series of programmable magnitude current pulses through successive SPI commands. Current limits and overcurrent timeouts can be used to enable controlled-mode charging of the the DC link capacitor from the battery supply. When controlled, the DC link capacitor current decays as shown in Figure 8. The voltage drop across the DC link capacitor increases in small steps that correspond to the current pulses. To calculate the required magnitude of the pulses and to charge the DC link capacitance, refer to the Application Information section.

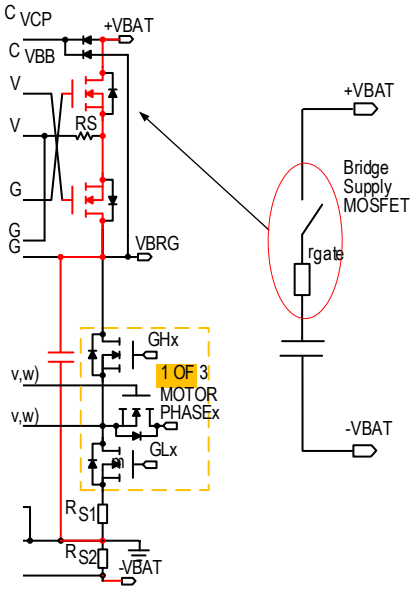

Figure 7: DC Link Capacitor Charging Circuit

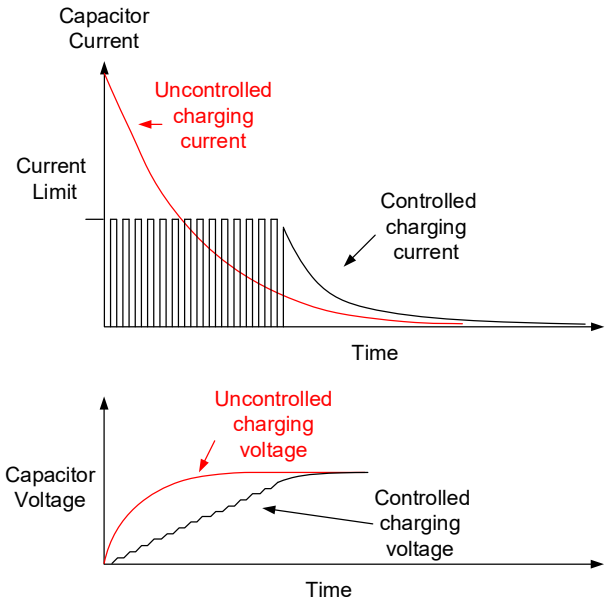

Figure 8: DC Link Capacitor Charging Voltage and Current Waveforms

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Charge Pump Regulator

The gate drivers are powered by a regulated charge pump, which provides the voltage above V_{BB} to ensure that the MOSFETs are fully enhanced with low on-resistance when the source of the MOSFET is at the same voltage as V_{BB}.

This regulator uses a charge-pump scheme with a switching frequency of 62.5 kHz and operates as a regulated doubler/tripler or a step-down regulator, depending on the input voltage on the VBB terminal. The charge pump voltage is regulated based on the difference between the VBB and VCP pins. The pumped voltage, V_{CP}, is available at the VCP terminal and is limited to 12 V maximum with respect to V_{BB}. This removes the need for external clamp diodes on the power MOSFETs to limit the gate-source voltage.

To provide the continuous low-level current required when gate-source resistors are connected to the external MOSFETs, a storage capacitor can be connected between the VCP and VBB terminals. Typically, a 1.5 µF capacitor of tolerance 5% is used. Pump capacitors, typically 680 nF ceramic capacitors of tolerance 10%, must be connected between the CP1 and CP2 terminals and between the CP3 and CP4 terminals to provide sufficient charge transfer, especially at low supply voltage.

The charge pump can be disabled through the SPI interface by writing 0 to the ENVCP configuration bit. When the charge pump is disabled, the MOSFETs being driven do not remain on and the state is indicated by a V_{GS} undervoltage fault. The charge pump is inactive during sleep mode.

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Gate Drives

The A89103 is designed to drive external, low on-state resistance, power N-channel MOSFETs when used in supply- and phase-isolation applications.

One of the five drivers in the A89103 is illustrated in Figure 9. The gate driver contains two current sources. The pulsed current source I_{GPx} is required to provide the MOSFET charge current, and the hold current source I_{GHx} is required to hold the MOSFET in the on state. When LENx goes high, the upper half of the drivers are turned on (low sides are turned off) and a current (I_{GPx} + I_{GHx} = 11.5 mA + 300 µA, typically) is sourced to the gate for a duration of t_{GPx}. Because drain-to-source voltage does not change during this period, in typical operations these parameters should be set to quickly charge the MOSFET input capacitance to the start of the Miller region. After this period, an on-hold current (I_{GHx} = 300 µA, typically) is sourced to the gates of the MOSFETs to keep them in the on state. The gate drive outputs accomplish turn-on of the MOSFETs in 8 µs (typically) and maintain the on state during voltage transients on the source of the MOSFETs. This is guaranteed as long as Sx is within its rated operating range.

When LENx goes low, the lower half of the drivers are turned on (high side is turned off) and current from the external MOSFET's gates to the respective Sx terminal sinks, which turns them off. To enable rapid, safe, on-demand opening of the circuit, turn-off is performed without current control. The gate drive outputs achieve turn-off of the MOSFETs in less than 300 ns (typically) and hold them in the off state during transients on the source.

An integrated hold-off circuit ensures that the gate source voltage of the MOSFET is held close to 0 V, even when power is disconnected. This can remove the need for additional gate-source resistors on the isolation MOSFETs. If gate-source resistors are mandatory for the application, the pump regulator can provide sufficient current to maintain the MOSFET in the on state using a gate-source resistor as low as 100 kΩ with 1% tolerance.

The floating gate-drive outputs for external N-channel MOSFETs are provided on pins GU, GV, GW, GREV, and GBRG. The reference points for the floating drives are the load phase connections SU, SV, and SW, and the sources of the reverse battery and bridge isolation MOSFETs, SREV and SBRG, respectively. The discharge current from the floating MOSFET gate capacitance flows through these connections.

For a detailed explanation of the circuit operation and a calculation of the external components, refer to the Application Information section.

When operating in the battery-disconnect common-drain configuration, the polarity of the reverse-battery gate driver is inverted, which drives the external discrete components. This ensures there is sufficient reverse-voltage protection in the common-drain configuration.

Each driver has independent internally latched control signals (LENx).

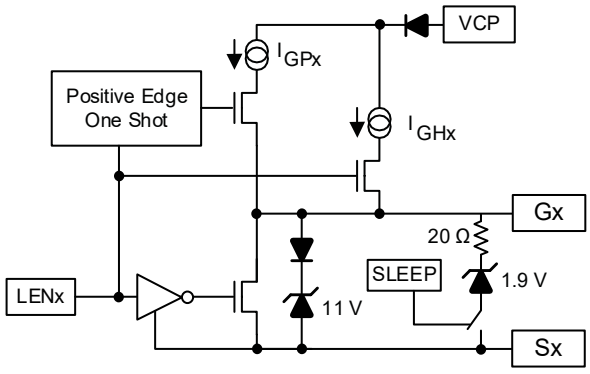

Figure 9: Operational Output Drive

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Driver Control via Serial Interface

The gate drivers are controlled by setting control bits in the enable/disable 0 register. These bis are ENU, ENV, ENW, ENBRG, ENREV, DISU, DISV, DISW, DISBRG, and DISREV.

When these bits are set or cleared accordingly, they toggle the internal signal LENx that controls turn-on and turn-off of the gate driver, as shown in Figure 9.

At power-on, the gate-driver-latched enable signals, LENx, and the serial driver control registers, ENx, are reset, disabling all gate drives. The gate-driver LENx enable signals can be directly enabled and disabled by serial command but may also be controlled by internal A89103 disconnect and protection functions.

To avoid unintended serial driver reactivation, the serial interface uses independent enable and disable control bits for each MOSFET driver. The enable (ENx) disable (DISx) control bits—ENBRG, ENREV, ENU, ENV, ENW, DISBRG, DISREV, DISU, DISV, and DISW—can be written in a single SPI word to command the drivers to turn on and turn off. Truth tables that summarize the operation of the gate driver are shown in Table 1.

For a driver to be turned on, LENx must be enabled, ENx must be set to 1, and DISx must be set to 0. For a driver to be turned off, LENx must be disabled, ENx must be set to 0, and DISx must be set to 1. After the commanded state is latched, the ENx and DISx bits are automatically reset to 0. Therefore, when these bits are read, they always appear to be zero.

Individual driver LENx control signals can be latched in the disable state by writing ENx = 0 and DISx = 1 in a single SPI command. After the commanded state is latched, the ENx and DISx bits are reset to 0.

If a serial command is received where ENx = DISx, the state of LENx for that driver retains the previous state. After the commanded state is latched, the ENx and DISx bits are reset to 0.

Each gate driver control is independent such that a single serial command can enable some drivers while disabling others.

During any operating condition, if any LENx signal is commanded through the SPI to be disabled, the respective driver switches off without delay. The only exception to this operation occurs when SPI control bit IDISREV is set to 1. In that case, if the LENREV signal is commanded through the SPI to be disabled, the transition to the disable state is blocked until the OCP sensed current is greater than the programmed OCN level (I > OCN). This feature ensures that, when the reverse MOSFET is turning off, the reverse current is small.

The status of the LENx control signals can be read from the SPI data registers STATx.

Table 1: Gate Driver Control Truth Table

Phase U				Phase V				Phase W			
ENU	DISU	LENU	GU	ENV	DISV	LENV	GV	ENW	DISW	LENW	GW
0	0	Latched	No change	0	0	Latched	No change	0	0	Latched	No change
0	1	0	Lo	0	1	0	Lo	0	1	0	Lo
1	0	1	Hi	1	0	1	Hi	1	0	1	Hi
1	1	Latched	No change	1	1	Latched	No change	1	1	Latched	No change

Bridge Driver				Reverse-Battery Driver			
ENBRG	DISBRG	LENBRG	GBRG	ENREV	DISREV	LENREV	GREV
0	0	Latched	No change	0	0	Latched	No change
0	1	0	Lo	0	1	0	Lo
1	0	1	Hi	1	0	1	Hi
1	1	Latched	No change	1	1	Latched	No change

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Common-Source/Drain Driver Configuration

There are two supported configurations when connecting the bridge and reverse supply MOSFETs. When the sources of both MOSFETs are connected together, this is known as a common-source configuration. Connecting the drain pins of both MOSFETs together creates the common-drain configuration. Because both configurations block the reverse and battery currents, the choice of common-drain or common-source configuration depends on the system layout.

The common-source configuration is the default configuration of the A89103. When operating in the common-source configuration, the SPI control bit SDCFG should be set to 0. This configuration offers simpler design and requires fewer external components. When common source is selected, the GREV gate driver operates with the same polarity as the other gate drivers.

The common-drain configuration is selected by setting the SPI control bit SDCFG to 1. The GREV gate driver operates with an inverted polarity to drive the external discreet components in the common-drain configuration diagram shown in Figure 5. In this configuration, the gate driver status indication bit STATREV does not monitor the status of the GREV gate monitor. STATREV monitors the status of the reverse MOSFET. The V_{GS} undervoltage fault is also masked in this configuration because the monitor cannot produce accurate results.

VBAT Resistor Divider Switch

The VBAT resistor divider switch between the SWIN and SWOUT terminals can be used to reduce the battery current draw when sensing VBAT is not required.

The switch can be enabled or disabled through the SPI interface by writing 1 or 0, respectively, to the ENSW configuration bit.

The resistor divider switch is inactive during sleep mode. When the switch is disabled, if +VBAT is greater than 85 V and the top half of the resistor divider is chosen to limit the current into the terminal to less than 4 mA, the ESD structure on the SWIN terminal conducts to clamp the terminal voltage to an allowable level.

The SWOUT terminal operating range is limited to –0.3 to 5.5 V.

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DIAGNOSTIC MONITORS

Multiple diagnostic features provide three levels of fault monitoring. These diagnostics can be categorized into three levels of protection:

- **Chip-level protection:** Chip-wide parameters critical for correct operation of the A89103 are monitored. These include maximum internal logic supply voltage, minimum internal logic and terminal supply voltage, and serial interface transmission. These three monitors are necessary to ensure that the A89103 is able to respond as specified.
- **Operational Monitors:** Parameters related to the safe operation of the A89103 in a system are monitored. These include parameters associated with external active and passive components, power supplies, and interaction with external controllers.
- **System Level Protection:** These include the detection of power bridge and load fault conditions.

All diagnostics remain operational and cannot be masked when the A89103 is in its typical operating range. The diagnostics and their functions are summarized in Table 2.

Except for the temperature warning, power-on-reset, and internal logic overvoltage monitors, the fault is reported through two mechanisms—DIAG output terminal and the STATUS_0 register accessed through the serial interface, which provide the status of the respective faults.

Table 2: Diagnostic Functions

Name	Diagnostic	Level
FDIAG	Externally triggered fault on the DIAG terminal	System
VIO	Internal logic supply overvoltage	Chip
FRESET	Terminal supply undervoltage or internal logic supply undervoltage causing a power-on-reset operation	Chip
FSPI	Serial transmission error	Chip
TW	High chip junction temperature warning	Monitor
FUVP	VBRG supply positive undervoltage	Monitor
FUVN	VBRG supply negative undervoltage	Monitor
FWD	Watchdog timeout	Monitor
FOCP	Positive overcurrent	Monitor
FOCN	Negative overcurrent	Monitor
FVCP	Charge pump undervoltage	Monitor
FGBRG	Bridge driver V_{GS} undervoltage	Monitor
FGREV	Reverse-battery driver V_{GS} undervoltage	Monitor
FGW	Phase-W driver V_{GS} undervoltage	Monitor
FGV	Phase-V driver V_{GS} undervoltage	Monitor
FGU	Phase-U driver V_{GS} undervoltage	Monitor

DIAG Diagnostic Output

The DIAG terminal is a single diagnostic output signal that can be configured through the serial interface by writing to the DIAG [1:0] configuration bits. The list of configured functions is:

- **DIAG_0—Digital Open-Drain Output:** Output pulled low in case of a fault.

  At power-up, or after a power-on-reset event, the DIAG terminal outputs a general logic-level fault flag that is active-low if a fault is present. This fault flag remains low while the fault is present or if one of the latched faults has been detected. When all the faults are reset, the DIAG output returns to high.
- **DIAG_1—Digital Open-Drain Output:** Clock signal derived from the internal chip clock.

  The clock output option provides a logic level square wave proportional to the digital clock frequency FCLK to allow for accurate configuration of the system clock. This is useful for obtaining accurate timing measurements that depend on the system clock.
- **DIAG_2—Tristate:** Input only.
- **DIAG_3—Tristate:** Input only.

When the DIAG terminal is not driven low by the A89103, the terminal can be externally pulled low. This is known as an external fault trigger. A DIAG fault appears and is represented by the setting of the FDIAG bit in the STATUS_0 register.

When DIAG is externally pulled low, FDIAG is set in the STATUS_0 register. The DIAG terminal is pulled low if the bit DMFDIAG is set to 0 and remains low until the fault is cleared in the status register by writing 1 to FDIAG. If DMFDIAG is set to 1, the DIAG terminal remains high.

The A89103 can be configured to respond to a DIAG fault in three fault mechanisms:

- Bridge-supply MOSFET turns off.
- Reverse-battery MOSFET turns off.
- Phase MOSFETs latch (cannot be turned on).

if the fault action bit ENBFTDIAG is set to 1, the bridge-supply MOSFET latches in the off state. If ENBFTDIAG is set to 0, the bridge-supply MOSFET remains in the on state.

If the fault action bit ENRFTDIAG is set to 1 and current-dependent isolation is disabled, the reverse supply MOSFET latches off. This is achieved by setting IDISREV to 0.

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Current-dependent isolation can be activated by setting IDISREV to 1. For this scenario, the reverse-supply MOSFET latches in the off state only when the voltage of the negative-overcurrent monitor is greater than the negative-threshold overcurrent voltage. The DIAG fault can be cleared when the positive-overcurrent event has passed and 1 is written to FDIAG.

For both isolation cases described above, if the fault action bit ENRFTDIAG is set to 0, the reverse-supply MOSFET remains in the on state. Because the magnitude and direction of phase currents is unknown, a positive-undervoltage fault does not cause the phase MOSFETs to turn off. If the fault action bit ENPFTDIAG is set to 1 and the phase MOSFETs are already off, they remain latched in the off state until the DIAG fault is cleared.

If the fault action bit ENPFTDIAG is set to 0, the phase MOSFETs do not latch to the off state.

The fault action for a DIAG fault is summarized in the flowchart in Figure 10.

When the A89103 pulls the DIAG terminal low and the low state is then deserted, the DIAG trigger function is blanked for 10 µs to prevent false tripping.

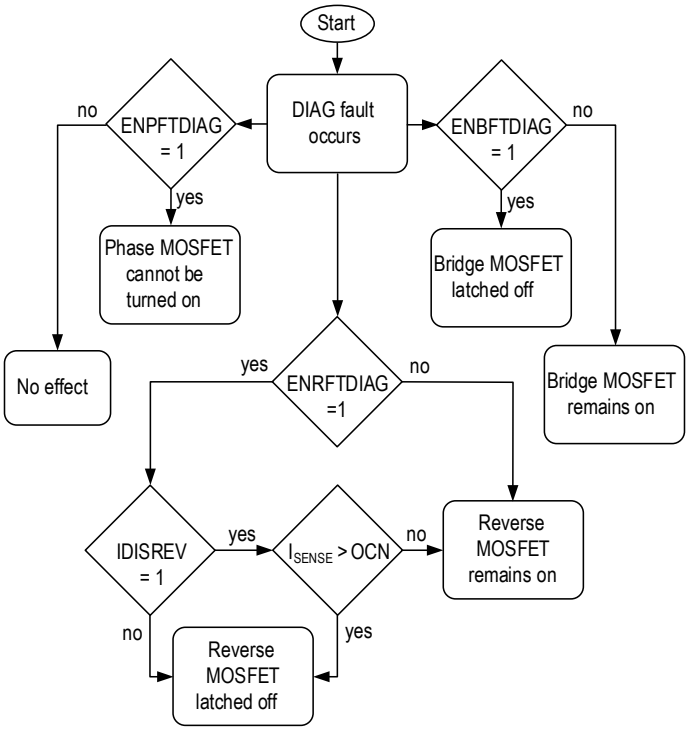

Figure 10: DIAG Fault-Action Scenarios

Diagnostic Registers

The serial interface allows detailed diagnostic data to be read from the diagnostic registers on the MISO output terminal at any time.

A system status register, STATUS_0, provides a summary of all faults in a single read transaction. The status register is always output on MISO when any register is written. In all cases, the fault bits in the status register are latched and are only cleared by writing 1 to the corresponding bit.

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Chip Fault State: Internal Logic Overvoltage

The A89103 has two independent integrated logic regulators, as shown in Figure 11. The SPI supply regulator provides power to the serial interface and the internal supply regulator provides power to the isolation and control logic. This supply architecture ensures that external events, other than loss of supply, do not prevent the A89103 from operating correctly. For example, during transient load event, if the main supply voltage drops below the V_{BB} undervoltage falling threshold (V_{BBOFF}), the internal logic supply regulator continues to operate with a low supply voltage.

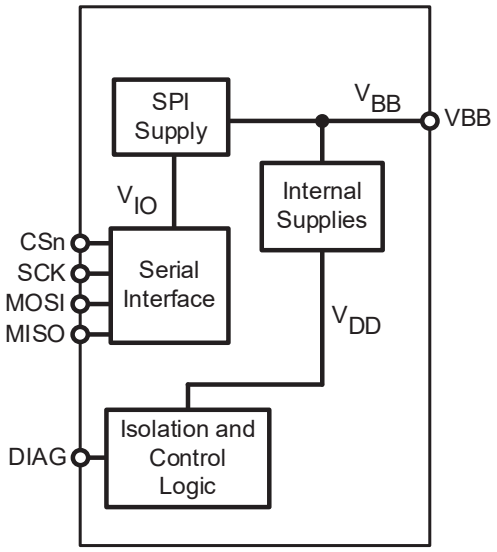

Figure 11: A89103 Internal Regulators

The A89103 monitors the internal supply voltage to detect when it exceeds the logic overvoltage threshold (V_{LO}). In the event of a logic overvoltage, the DIAG terminal is pulled low and remains low unless the regulated voltage supplying the serial interface, V_{IO}, recovers to the typical operating voltage. There is no SPI fault for V_{LO}, and the fault action on DIAG cannot be masked.

Chip Fault State: Internal Logic and Supply Undervoltage

When supply voltage is extremely, or during power-up or power-down, two undervoltage detectors ensure that the A89103 operates correctly. Neither the V_{DD} logic supply undervoltage lockout nor the VBB terminal supply undervoltage lockout can be masked: Both are essential to guarantee correct operation over the full supply range.

When power is first applied to the A89103, the internal logic is prevented from operating, and all gate drive outputs are held in the off state until both the V_{DD} logic supply exceeds its undervoltage rising threshold (V_{DDON}) and the VBB terminal exceeds its undervoltage rising threshold (V_{BBON}). At this point, all serial control registers are reset to their power-on state and all fault states are reset. The FFRESET bit in the STATUS_0 register becomes set to one to indicate that a power-on-reset operation has occurred. The A89103 then goes into its fully operational state and begins to operate as specified.

Once the A89103 is operational, the V_{DD} logic supply and the VBB terminal supply continue to be monitored. During operation, if V_{DD} drops below the logic supply undervoltage lockout falling (turn-off) threshold, or if V_{DDOFF} or V_{BB} drops below the terminal-supply undervoltage-lockout falling (turn-off) threshold, the logical function of the A89103 cannot be guaranteed and the outputs are immediately disabled. If there is sufficient voltage present to drive the pull-down device, the DIAG terminal is pulled low. The A89103 enters a power-down state and all internal activity, other than the V_{DD} and V_{BB} voltage monitors, are suspended. If the V_{BB} or V_{DD} undervoltage is a transient event, then the A89103 follows the power-up sequence above as the voltage rises.

Chip Fault State: Serial Error

The data transfer into the A89103 through the serial interface is monitored for two fault conditions:

- **Transfer length:** A transfer length fault is detected if there are more than 32 rising edges on SCK, or if CSn goes high and there have been fewer than 32 rising edges on SCK.
- **Cyclic redundancy check (CRC) checksum:** A CRC checksum error occurs when the calculated CRC does not match the received CRC. For a more-detailed explanation of the CRC calculation and operation, refer to the Application Information section.

In both cases, the write process is cancelled without writing data to the register. In addition, the FSPI bit becomes set to indicate a data transfer error. Due to the nature of out-of-frame communication, the contents of the register during the last valid serial transaction are still able to be read.

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Operational Monitors

Voltages related to the driving of external power MOSFETs are monitored—specifically, the V_{CP} and V_{GS} of each gate drive output as well as the logic voltages. The inverter bridge voltage, V_{BRG}, is monitored for positive- and negative-undervoltage events. In addition, a watchdog timer can be applied to the serial input to verify continued operation of the SPI interface.

Gate-Drive Output Monitor

For each gate driver, the gate-to-source voltage between the Gx terminal and the Sx terminal is monitored during the on state for the presence of an undervoltage condition. This monitor ensures that the gate-drive output is operating correctly and that the drive voltage is sufficient to fully enhance the power MOSFET to which it is connected. The undervoltage threshold, V_{GSUV}, has a typical value of 6.5 V.

If V_{GS} on any active gate-drive output is lower than the gate-drive undervoltage warning threshold, V_{GSUV}, the fault condition becomes latched in the appropriate gate-drive undervoltage status bit—FGREV, FGBRG, FGU, FGV, or FGW. All gate-drive outputs remain in the on state. The gate-drive undervoltage bits FGREV, FGBRG, FGU, FGV, and FGW can only be reset by writing 1 to the appropriate status bit or via a power-on-reset operation.

The output of each V_{GS} undervoltage comparator is filtered by a V_{GS} fault-qualifier circuit. This circuit uses a timer to verify that the output from the comparator has indicated a valid V_{GS} fault. The duration of the V_{GS} qualifying timer, t_{GSUV}, is specified in the Characteristic Performance section.

Charge Pump Output Monitor

The external voltage on the VCP terminal with respect to V_{BB}, identified as V_{CP}, is monitored.

When the voltage at the charge pump output, V_{CP}, drops below the undervoltage threshold, V_{CPOFF}, a timer starts. If V_{CP} remains below V_{CPON} for the duration of the V_{CP} undervoltage filter time, t_{CPUV}, the fault status (FVCP) bit becomes set to 1. When this occurs, the charge pump remains operative and the DIAG terminal indicates a fault until the FVCP fault is cleared. Because this is a latched fault, the fault action remains active until the FVCP bit is cleared by writing 1 to the FVCP status bit or via a power-on reset.

When the FVCP fault bit is set and the SPI control bit ENVCPD is set to 1, if a VCP fault occurs, the gate drivers become disabled.

Temperature Warning

If the chip temperature rises beyond the temperature warning threshold, T_{JW}, the hot warning bit, TW, becomes set in the STATUS_0 register. Because this bit is for indication only, no fault actions are taken. When the temperature drops below T_{JW} by more than the hysteresis value, T_{JWHys}, the temperature warning goes away. The TW bit remains in the status register until it is reset by writing 1 to the TW status bit.

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Negative-Overcurrent Sensing

A negative-overcurrent event occurs when current flows into the positive terminal of the battery. Common scenarios that may cause are when the motor enters generation mode, where kinetic energy is released, or when the battery is connected in the reverse direction, which is common to jump-start a vehicle.

The negative-overcurrent monitor is referenced to the negative-overcurrent threshold voltage, V_{OCN}, to provide an indication of the negative-overcurrent events. V_{OCN} has a resolution of 1 mV and is defined by the contents of the OCN [6:0] variable. V_{OCN} is approximately defined as:

$$V_{OCN} = V_{CSM} - V_{CSP} = (1\ mV \times OCN) + 1,$$

where OCN = 0 to 127.

The output from the negative-overcurrent comparator is filtered by an overcurrent qualifier circuit designed to prevent false tripping. The qualifier circuit has a timer to verify that the output from the comparator has indicated a valid overcurrent event.

The timer is started each time a comparator indicates an overcurrent event. When the comparator changes back, this timer is reset to indicate typical operation. If the timer reaches the end of the timeout period set by t_{OCNQ}, the overcurrent event is considered valid and the overcurrent bit FOCN becomes set in the STATUS_0 register.

The duration of the overcurrent qualifying timer, t_{OCNQ}, is determined by the contents of the OCND [2:0] variable and is defined as:

$$t_{OCNQ} = n \times 250\ ns,$$

where n is a positive integer defined by OCND [2:0]

When a valid overcurrent event is detected, FOCN is set in the STATUS_0 register. If DMFOCN is set to 0, the DIAG terminal is pulled low; it remains low until the fault is cleared in the status register by writing 1 to the FOCN bit. If DMFOCN is set to 1, the DIAG terminal remains high.

If the fault action bit ENBFTOCN is set to 1, the bridge-supply MOSFET latches in the off state. If ENBFTOCN is set to 0, the bridge-supply MOSFET remains in the on state.

If the fault action bit ENRFTOCN is set to 1, The reverse supply MOSFET latches in the off state, and current-dependent isolation becomes disabled, indicated by IDISREV set to 0.

Current-dependent isolation can be activated by setting IDISREV to 1. For this scenario, the reverse supply MOSFET is latched in the off state only when the voltage of the negative-overcurrent monitor is greater than the negative-threshold overcurrent voltage. This feature ensures that the reverse-battery MOSFET is sufficiently small to reduce the risk of avalanching. The OCN fault can be cleared when the negative-overcurrent event is no longer present and 1 is written to FOCN.

For both isolation cases described, the reverse supply MOSFET remains on if the fault action bit ENRFTOCN is set to 0.

Because the magnitude and direction of phase currents is unknown, a negative-overcurrent fault does not cause the phase MOSFETs to turn off. If the fault action bit ENPFTOCN is set to 1 and the phase MOSFETs are already in the off state, they remain latched in the off state until the OCN fault is cleared.

If the fault action bit ENPFTOCN is set to 0, the phase MOSFETs do not latch to the off state.

The fault action for an overcurrent fault is summarized in the flowchart in Figure 12.

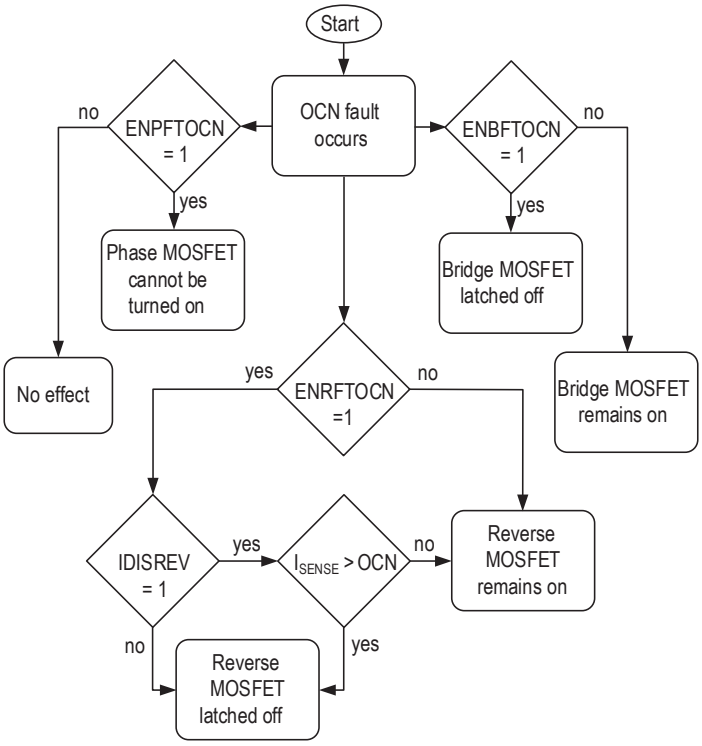

Figure 12: Negative-Overcurrent Fault-Action Scenarios

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Positive-Overcurrent Sensing

Positive-overcurrent events can occur when there is a fault in the three-phase inverter that results in a short to ground in one phase or during startup when the DC link capacitor is being charged. The positive-overcurrent monitor is referenced to the positive-overcurrent threshold voltage, V_{OCP}, to provide an indication of the positive-overcurrent events in the battery. V_{OCP} has a resolution of 1 mV and is defined by the contents of the OCP [6:0] variable. V_{OCP} is approximately defined as:

$$V_{OCP} = V_{CSP} - V_{CSM} = (1\ mV \times OCP) + 1,$$

where OCP = 0 through 127.

The output from the positive-overcurrent comparator is filtered by an overcurrent qualifier circuit designed to prevent false tripping. The qualifier circuit has a timer to verify that that the output from the comparator has indicated a valid overcurrent event.

The timer is started each time a comparator indicates an overcurrent event. When the comparator changes back, this timer is reset to indicate typical operation. If the timer reaches the end of the timeout period set by t_{OCPQ}, the overcurrent event is considered valid and the overcurrent bit FOCP becomes set in the STATUS_0 register.

The duration of the overcurrent qualifying timer, t_{OCPQ}, is determined by the contents of the OCPD [2:0] variable and is defined as:

$$t_{OCPQ} = n \times 250\ ns,$$

where n is a positive integer defined by OCPD [2:0].

When a valid overcurrent event is detected, the FOCP bit is set in the STATUS_0 register. If DMFOCP is set to 0, the DIAG terminal becomes pulled low and remains low until the fault is cleared in the status register by writing 1 to the FOCP bit. If DMFOCP is set to 1, the DIAG terminal remains high.

If the fault action bit ENBFTOCP is set to 1, the bridge-supply MOSFET becomes latched in the off state. If ENBFTOCP is set to 0, the bridge-supply MOSFET remains on.

If the fault action bit ENRFTOCP is set to 1, the reverse supply MOSFET becomes latched in the off state and current-dependent isolation becomes disabled. Current-dependent isolation can also be disabled by setting IDISREV to 0.

Current-dependent isolation can be activated by setting IDISREV to 1. For this scenario, the reverse-supply MOSFET is only latched in the off state when the voltage of the negative-overcurrent monitor is greater than the negative-threshold overcurrent voltage. The OCP fault can be cleared when the positive-overcurrent event is no longer present and 1 is written to FOCP.

For both isolation cases described, if the fault action bit ENRFTOCP is set to 0, the reverse-supply MOSFET remains in the on state.

Because the magnitude and direction of phase currents is unknown, a positive-overcurrent fault does not cause the phase MOSFETs to turn off. If the fault action bit ENPFTOCP is set to 1 and the phase MOSFETs are already off, they will remain latched in the off state until the OCP fault is cleared.

If the fault action bit ENPFTOCP is set to 0, the phase MOSFETs do not latch in the off state.

The fault action for an overcurrent fault is summarized in the flowchart in Figure 13.

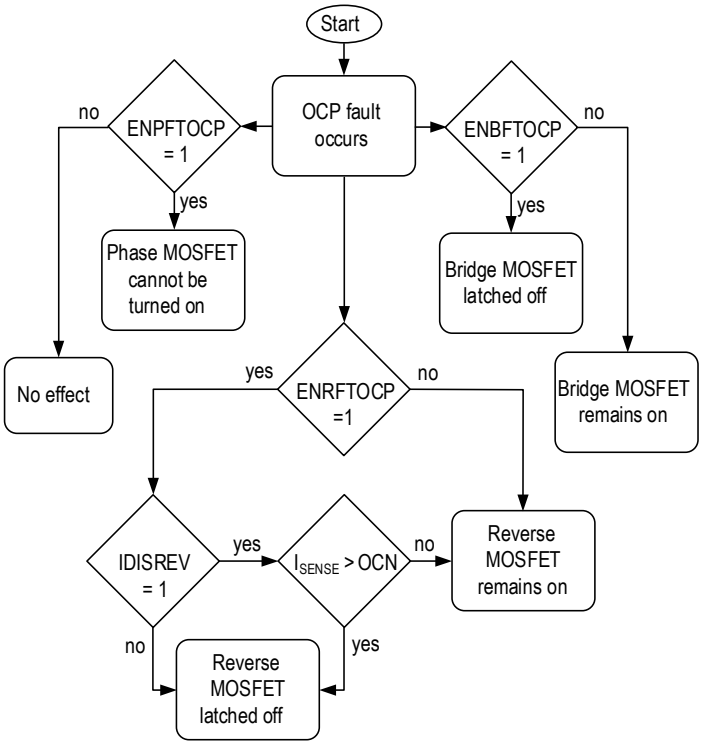

Figure 13: Positive-Overcurrent Fault-Action Scenarios

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OCP Timer

The A89103 contains an overcurrent timer. This timer can be enabled to measure the time between overcurrent events, known as the overcurrent timed value, t_{OC}. This feature is useful for charging of the DC link capacitor and is further detailed in the Application Information section. The timer is started by writing 1 to the overcurrent timer enable bit (ENOCT). A multiple of the time elapsed between a rising edge of ENOCT and the detection of a filtered negative- or positive-overcurrent fault is stored in the register variable OCT [7:0]. The overcurrent timed value t_{OC} can be estimated using:

$$(p \times n)/f_{CLK} < t_{OC} < [p \times (n + 1)]/f_{CLK},$$

where n is a positive integer defined by OCT [7:0], p is a clock prescalar defined by OCTP [1:0], and f_{CLK} is the internal timing clock frequency.

The clock prescalar has a default value of 1 and varies in the range of 1 to 8 according to the value set by OCTP [1:0].

If the OCT register overflows, it returns the maximum count value. The timer can be reset by writing 1 to the ROCT bit. After reset, the ROCT bit is automatically cleared to 0 and the timer does not run until a new ENABLE/DISABLE_0 write is received and ENOCT is 1. When ENOCT is set to 0, the timer is unconditionally reset. ROCT is set in the STATUS_0 register after ENOCT is changed to 1. The timing of the t_{OC} measurement is shown in Figure 14

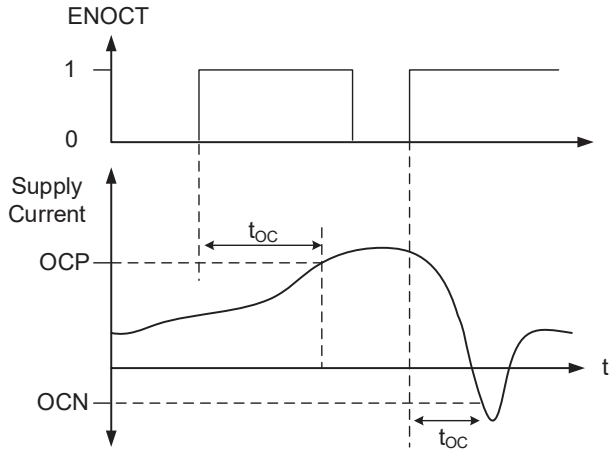

Figure 14: OCP Timer Measurement

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VBRG Voltage Monitoring

The main battery supply to the bridge, V_{BRG}, is monitored by the A89103 on the VBRG terminal to determine if the supply voltage is below its minimum typical operating voltage. An undervoltage event can be either positive (for example, loss of battery power) or negative (for example, bridge in regenerative mode). Voltage is monitored by two voltage comparators to detect positive-undervoltage (UVP) and negative-undervoltage (UVN) conditions.

The A89103 is designed to operate in both 12 V and 48 V systems. Both systems have different positive-voltage thresholds, V_{VBRGP0} and V_{VBRGP1}. The positive-undervoltage monitor threshold is programmed by writing to the nominal voltage bit, VCMFG. The nominal voltage bit defaults to 0, which is the correct setting for 12 V operation. For 48 V operation, VCMFG must be set to 1.

If the nominal voltage bit VCMFG = 0, intended for 12 V operation, the UVP condition is detected when V_{BRG} is less than V_{VBRGP0} nominally, and the UVN condition is detected when V_{BRG} is less than V_{VBRGN0} nominally. If VCMFG = 1, intended for 48 V operation, the UVP condition is detected when V_{BRG} a less than V_{VBRGP1} nominally, and the UVN condition is detected when V_{BRG} is less than V_{VBRGN1} nominally. These voltage thresholds are defined in the Characteristic Performance section.

When a valid positive-undervoltage event is detected, the FUVP bit is set in the STATUS_0 register. If DMFUVP is set to 0, the DIAG terminal is pulled low and remains low until the fault is cleared in the status register by writing 1 to FUVP. If DMFUVP is set to 1, the DIAG terminal remains high.

If the fault action bit ENBFTUVP is set to 1, the bridge-supply MOSFET becomes latched in the off state. If ENBFTUVP is set to 0, the bridge supply MOSFET remains in the on state.

If the fault action bit ENRFTUVP is set to 1, the reverse-supply MOSFET will be latched off and the current-dependent isolation becomes disabled. Current-dependent isolation can also be achieved by setting IDISREV to 0.

Current-dependent isolation can be activated by setting IDISREV to 1. For this scenario, the reverse supply MOSFET latches in the off state only when the voltage of the negative-overcurrent monitor is greater than the negative-threshold overcurrent voltage. The UVP fault can be cleared when the positive-overcurrent event is no longer present and 1 is written to FUVP.

For both isolation cases described, if the fault action bit ENRFTUVP is set to 0, the reverse-supply MOSFET remains in the on state.

Because the magnitude and direction of phase currents is unknown, a positive-undervoltage fault does not cause the phase MOSFETs to turn off. If the fault action bit ENPFTUVP is set to 1 and the phase MOSFETs are already off, they remain latched in the off state until the UVP fault is cleared.

If the fault action bit ENPFTUVP is set to 0, the phase MOSFETs do not latch to the off state.

The fault action for a positive-undervoltage fault is summarized in the flowchart in Figure 15.

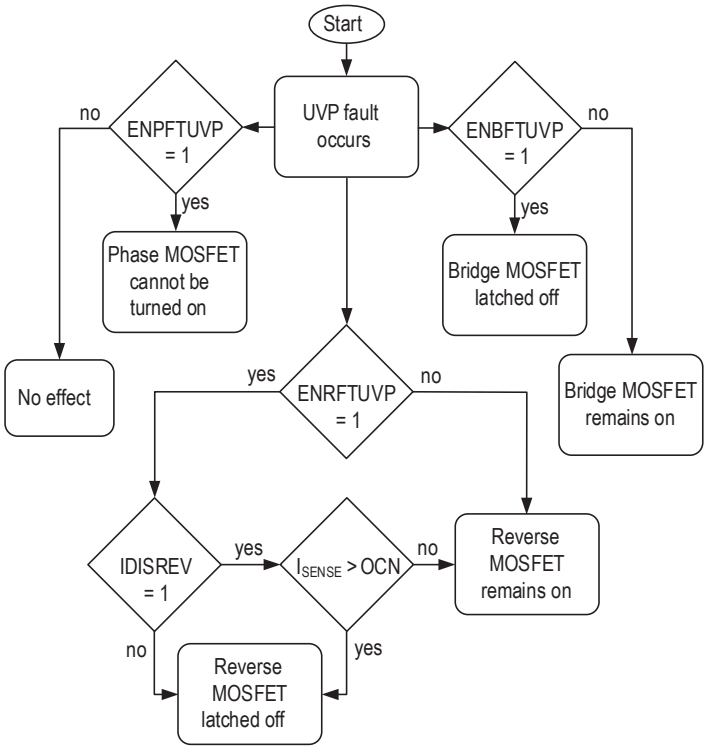

Figure 15: Positive-Undervoltage Fault-Action Scenarios

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When a valid negative-undervoltage event is detected, FUVN is set in the STATUS_0 register. If DMFUVN is set to 0, the DIAG terminal is pulled low and remains low until the fault is cleared in the status register by writing 1 to FUVN. If DMFUVN is set to 1, the DIAG terminal remains high.

If the fault action bit ENBFTUVN is set to 1, the bridge-supply MOSFET latches in the off state. The bridge supply MOSFET will remain on if ENBFTUVN is set to 0.

If the fault action bit ENRFTUVN is set to 1, the reverse-supply MOSFET latches in the off state and current-dependent isolation is disabled. current-dependent isolation can also be disabled by setting IDISREV to 0.

Current-dependent isolation can be activated by setting IDISREV to 1. For this scenario, the reverse supply MOSFET latches in the off state only when the voltage of the negative-overcurrent monitor is greater than the negative-threshold overcurrent voltage. The UVN fault can be cleared when the negative-overcurrent event is no longer present and 1 is written to FUVN.

For both isolation cases described, if the fault action bit ENRFTUVN is set to 0, the reverse-supply MOSFET remains in the on state.

Because the magnitude and direction of phase currents is unknown, a negative-undervoltage fault does not cause the phase MOSFETs to turn off. If the fault action bit ENPFTUVN is set to 1 and the phase MOSFETs are already off, they remain latched in the off state until the UVN fault is cleared.

If the fault action bit ENPFTUVN is set to 0, the phase MOSFETs do not latch in the off state.

The fault action for a negative-undervoltage fault is summarized in the flowchart in Figure 16.

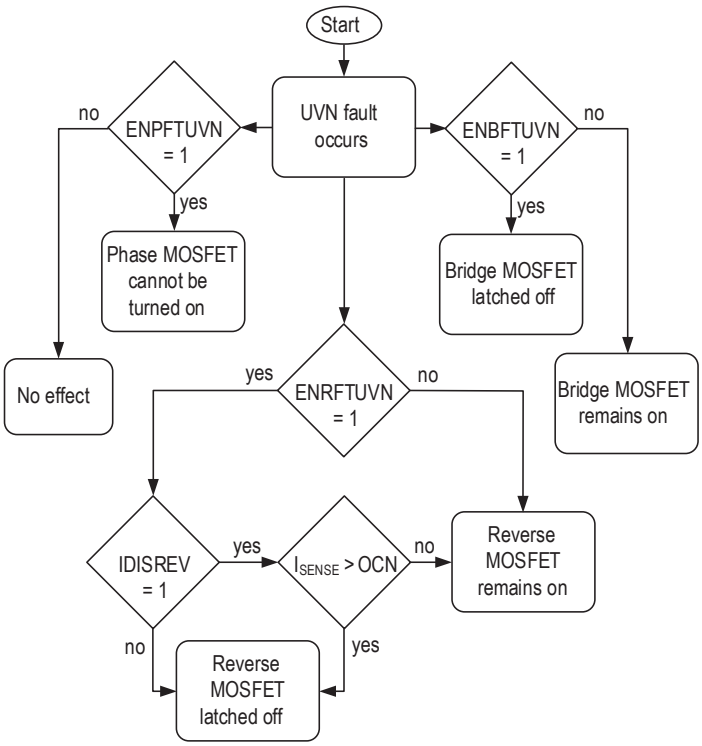

Figure 16: Negative-Undervoltage Fault-Action Scenarios

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Fault Action

The action taken when one of the diagnostic functions indicates a fault is listed in Table 3.

When a fault is detected, a corresponding fault state is considered to exist. In some cases, the fault state only exists during the time the fault is detected. In other cases, when the fault is only detected for a short time, the fault state is latched (held in the fault state) until reset. The faults that are latched are indicated in Table 3. Latched fault states are always reset when a power-on-reset state is present or when 1 is written to the associated fault bit in the status register. Any fault bits that have been set in the status register are only reset when a power-on-reset state is present or when 1 is written to the associated fault bit.

For most diagnostic functions, the action taken when a fault state is detected can be programmed to force the gate drive output into the inactive (low) state or to keep the output active. The action is selected by setting a 1 or 0 in the specific fault action bit associated with the diagnostic. The specific fault action bit for each diagnostic and the action taken for each setting is shown in Table 3.

If a power-on-reset state is detected, all gate drive outputs are driven low and all MOSFETs are held in the off state. This persists until the power-on-reset state is cleared.

Setting any of the bits in the ENABLE/DISABLE_2 register to 0 such that the gate drive outputs are not disabled in the event of the corresponding fault being detected results in the A89103 not taking any action to protect itself, the supply MOSFETs, or the phase MOSFETs: Damage may occur. In all cases, appropriate action must be taken by the external controller.

Table 3: Fault Action

Fault Description	Fault Action Bit Name	Disable Outputs		Fault State Latched
		Fault Action Bit = 0	Fault Action Bit = 1	
Power-On-Reset	–	Yes	No	
Enable WD Timeout	–	Yes	No	
V_{IO} Undervoltage	–	Yes	no	
Bridge-Supply MOSFET UVP Trigger	ENBFTUVP	No	Yes	Yes
Bridge-Supply MOSFET UVN Trigger	ENBFTUVN	No	Yes	Yes
Bridge-Supply MOSFET Positive-Overcurrent Trigger	ENBFTOCP	No	Yes	Yes
Bridge-Supply MOSFET Negative-Overcurrent Trigger	ENBFTOCN	No	Yes	Yes
Bridge-Supply MOSFET Trigger by DIAG	ENBFTDIAG	No	Yes	Yes
Reverse-Supply MOSFET UVP Trigger	ENRFTUVP	No	Yes	Yes
Reverse-Supply MOSFET UVN Trigger	ENRFTUVN	No	Yes	Yes
Reverse-Supply MOSFET Positive-Overcurrent Trigger	ENRFTOCP	No	Yes	Yes
Reverse-Supply MOSFET Negative-Overcurrent Trigger	ENRFTOCN	No	Yes	Yes
Reverse-Supply MOSFET Trigger by DIAG	ENRFTDIAG	No	Yes	Yes
Phase-Isolator UVP Trigger	ENPFTUVP	No	No	Yes
Phase-Isolator UVN Trigger	ENPFTUVN	No	No	Yes
Phase-Isolator Positive-Overcurrent Trigger	ENPFTOCP	No	No	Yes
Phase-Isolator Negative-Overcurrent Trigger	ENPFTOCN	No	No	Yes
Phase-Isolator Trigger by DIAG	ENPFTDIAG	No	No	Yes

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SPI Watchdog

The A89103 contains an SPI watchdog monitor that provides an added level of safety for serial communication. When enabled, the time between consecutive valid SPI communications is measured. If the time exceeds the programmed watchdog timeout period (WDT), the A89103 enters a fault state and disables all gate drives. The watchdog timeout period is configured by writing to the WDT [2:0] variable. The estimated WDT that can be programmed is shown in Table 4. These values assume that the system clock frequency is 4 MHz.

Table 4: Watchdog Timeout Period

WDT2	WDT1	WDT0	Timeout
1	1	1	1310 ms
1	1	0	655 ms
1	0	1	328 ms
1	0	0	82 ms
0	1	1	41 ms
0	1	0	30.8 ms
0	0	1	20.5 ms
0	0	0	10.2 ms

At power-on the watchdog function is enabled with a default value of 1310 ms. The watchdog function can be disabled by writing 0 to the ENWD control bit.

A multiple of the elapsed watchdog time between successive valid communications, t_{WDC}, is stored in the SPI register variable WDC [15:0]. The elapsed watchdog time between successive valid communications, t_{WDC}, is estimated using:

$$t_{WDC} = n \times 40\ \mu s,$$

where n is the decimal equivalent of the WDC register value.

When a valid watchdog timeout occurs, the FWD bit in the status register is set. If DMFWD is set to 0, the DIAG terminal is pulled low and remains low until the fault is cleared in the status register by writing 1 to FWD. If DMFWD is set to 1, the DIAG terminal remains high.

The shut-down sequence of the gate drivers is selected using the WDSO bit. If WDSO is set to its default value of 0, the phase-isolation MOSFET drivers are disabled first, followed by the supply-isolation MOSFET drivers.

If WDSO is set to 1, the supply-isolation MOSFET drivers are disabled first, followed by the phase-isolation MOSFET drivers.

After all gate drivers are disabled, the A89103 enters an idle state. If CSn is less than the wakeup threshold falling (V_{CSnL}) for more than 1 ms, the A89103 enters sleep mode.

During either sequence, if a valid SPI communication is received that clears the SPI FWD bit, the isolation process halts. All MOSFET drivers remain in the state they were in when the process was halted. If, prior to FWD being set, another source has already triggerd isolation, the device waits for that isolation to complete before entering the idle state.

The FWD status bit remains set until it is cleared by writing 1 to the FWD status bit in the STATUS_0 register.

The watchdog disabling sequence is depicted in Figure 17.

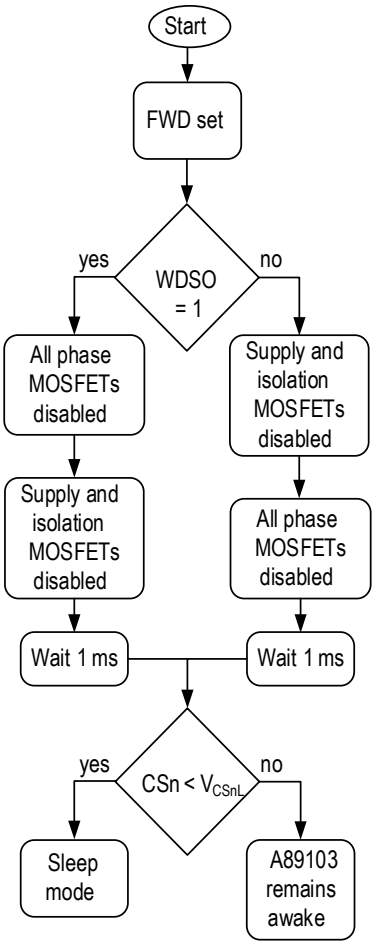

Figure 17: SPI Watchdog Timeout Disabling Sequence

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Sleep State

The A89103 provides a low-power sleep state where the consumption from the supply is reduced to a minimum by disabling all typical functions including the charge pump regulator and all internal logic circuitry. The A89103 can only be put into sleep mode via the SPI watchdog fault. Two conditions must be met to enter sleep mode:

- The ENWD bit must be set in the ENABLE/DISABLE_1 register, such that a watchdog timeout occurs that sets the FWD bit.
- CSn must be held below the wakeup threshold falling (V_{CSnL}) for at least 1 ms after all gate drives are disabled.

If both of the above conditions are not met, sleep mode will be inactive regardless of the CSn or watchdog state. The A89103 wakes from sleep when CSn rises beyond the wakeup threshold rising (V_{CSnH}). If CSn is between V_{CSnL} and V_{CSnH}, the device may draw current exceeding I_{BBS}; however, continued operation is not guaranteed. When exiting sleep mode, all configuration and control registers are reset to the default values. All fault states are cleared, and—with exception to FRESET—all fault bits in the status register are set to 0.

When the device powers up, it remains powered if one of two conditions is met—the CSn terminal remains above the wakeup threshold rising (1.33 V, nominal) or the device does not initiate a power down sequence due to a SPI watchdog timeout.

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DIAGNOSTIC AND SYSTEM VERIFICATION

To comply with various aspects of safe system design, it is necessary for higher-level safety systems to verify that any diagnostics or functions used to guarantee safe operation are operating within specified tolerances.

There are four basic aspects to verification of diagnostic functions:

- Verify connections
- Verify comparators
- Verify thresholds
- Verify fault propagation

Completion of these verifications is required for each diagnostic. Operation of system functions not directly covered by diagnostics should also be verified.

The A89103 includes additional verification functions to help the system design comply with any safety requirements. Many such functions can only be completed when the diagnostics are not required and can only be commanded to run by the main system controller. These are referred to as offline verification functions.

A few of the functions can be continuously active, but the results must be checked by the main system controller on a regular basis. These are referred to as online verification functions.

Table 5: Verification Functions

Verification Type	Function Verified	Operation	
		Offline	Online
Connection	Current sense disconnect		Y
Diagnostic	Temperature warning	Y	
Diagnostic	V_{CP} undervoltage	Y	
Diagnostic	Watchdog timer	Y	
Diagnostic	Current sense overvoltage	Y	
Diagnostic	VBRG undervoltage	Y	

The frequency with which offline verification functions are run or online verifications results are checked depends on the safety requirements of the system using the A89103.

Online Verification

Online verification functions are permanently active. An online verification function sets the appropriate bit in the verification result registers to indicate that the verification has failed. No other action is taken by the A89103. These functions are used to verify that certain parts of the A89103 terminals are correctly connected to the power bridge circuit. Online verification functions in the A89103 include:

- **Current Sense Disconnect:** The current sense comparator terminals include continuous current sources that allow detection of an input open circuit condition. If an input open circuit occurs, the terminal voltage rises above the comparator open-load detect threshold, the V_{CD} and the CD bit are set in the VERIFY_RESULT_0 register. To prevent false tripping, these comparators have an analog filter with a typical filter time of 10 µs.

Offline Verification

The following functions are only active when commanded by setting the appropriate bit in the verification command registers in addition to any required gate-drive commands. If the function only verifies a connection, a fail causes the appropriate bit to be set in the verification result register. No other action is taken by the A89103. If the function is to verify one of the diagnostic circuits in the A89103, the verification is completed by checking that the associated fault bit is set in the diagnostic registers.

- **Verify Temperature Warning:** The temperature warning detector is verified by setting the YTW bit in the VERIFY_COMMAND_0 register to 1. This applies a voltage to the comparator that is lower than the temperature warning threshold and should cause the temperature warning fault bit, TW, to be latched in the STATUS_0 register. When YTW is reset to 0, the TW bit remains set in the status register until reset. If the TW bit is not set, the verification has failed.
- **Verify V_{CP} Undervoltage:** The VCP input undervoltage detector is verified by setting the YCP bit in the VERIFY_COMMAND_0 register to 1. This applies a voltage to the VCP undervoltage comparator that is lower than the corresponding undervoltage threshold and should cause the FVCP fault bit to be set in the STATUS_0 register. The

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charge pump must be enabled (ENVCP = 1) to conduct this verification because, when the charge pump is disabled, the monitor is also disabled. When YCP is reset to 0, the FVCP bit remains set, indicating a successful verification. If the FVCP bit is not set, the verification has failed.

- **Verify Watchdog Timer:** The watchdog timer is verified by setting the YWD bit in the VERIFY_COMMAND_0 register to 1. This creates a watchdog fault. The watchdog timer (ENWD = 0) must be disabled to conduct this verification because, when the watchdog timer is enabled, it initiates the full watchdog shut-down sequence. When YWD is reset to 0, the FWD bit remains set, indicating a successful verification. If FWD is not set, the verification process failed.
- **Current Sense Overvoltage:** The overcurrent detector is verified by setting the YOCP and/or YOCN bits in the VERIFY_COMMAND_0 register to 1. This forces a voltage across the comparator that exceeds the trip threshold. Consequently, the overcurrent fault bits, FOCP and FOCN in STATUS_0 register, should be set. When YOCP and/or YOCN are reset to 0, the sense amplifier outputs return to typical operation and/or the FOCP and FOCN bits remain latched until reset. Unless the FOCP and/or FOCN bits are set, the verification has failed.
- **Verify VBRG Undervoltage:** The VBRG positive- and negative-undervoltage detectors are verified by setting the YUVP and/or YUVN bits in the VERIFY_COMMAND_0 register to 1. This forces a voltage across the V_{BRG} comparator that is higher than the trip threshold and V_{BRG} undervoltage fault bits, FUVP and FUVN, to become latched in the STATUS_0 register. When the YUVP and/or YUVN bits are reset to 0, the FUVP and/or FUVN bits remain set in the STATUS_0 register until reset. If the FUVP or FUVN bit is not set, the verification has failed for the corresponding comparator.

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SERIAL INTERFACE

A four-wire synchronous serial interface, operating as a SPI-compatible peripheral, is used to configure and control the features of the A89103 as a SPI peripheral and to provide diagnostic feedback and readback of the register contents. The full list of register contents is specified in the Serial Registers Definition section. The serial interface timing requirements are specified in the Characteristic Performance section and illustrated in Figure 4.

The chip-select control signal from the SPI controller, input on the CSn terminal, controls access to the serial interface. CSn is typically held high and is only brought low to initiate a serial transfer. When CSn is high, the output terminal of the A89103, MISO, is high impedance and no data is clocked in or out.

Data from the SPI controller is received by the A89103 on the MOSI terminal. Each bit is sampled and clocked through a shift register on the rising edge of the clock signal input on the SCK terminal when CSn is low.

Data is transmitted from the A89103 through the MISO terminal. When CSn is brought low, bit [31] output data becomes valid on MISO. After the first rising edge of the clock signal, each subsequent bit to be transmitted from MISO is updated on the falling edge of the SCK terminal signal input so long as CSn remains low.

Each pair of input and output serial words, referred to as a frame, is exactly 32 bits in length and is defined by the number of rising edges between CSn going low and CSn going high. After 32 bits have been clocked into the shift register, CSn must be taken high to initiate any action to be taken by the A89103.

The serial interface operates using out-of-frame transfer and provides the ability to address up to four peripheral nodes or three peripheral nodes and broadcast on a single SPI bus with common MOSI, MISO, SCK, and CSn connections. Out-of-frame transfer means that the peripheral addressed in one frame responds in the following frame. The controller can transmit sequential frames to different peripherals with each peripheral responding in the following frame. The addressed peripheral starts driving the MISO output as soon as CSn goes low to start the frame following the frame in which it was addressed.

Each complete frame consists of a 32-bit header sent from the controller to the peripheral on MOSI and a 32-bit response frame from the selected peripheral node to the controller on MISO. All data are transmitted most-significant-bit (msb) first, at the same time, by the clock signal input on the SCK terminal. The serial frame structure is shown in Figure 18.

		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Header	MOSI	NAD			CMD				ADDRESS				DATA																CRC				
Response	MISO	NAD		V	FF	0				COUNT			STATUS/DATA																CRC				

Figure 18: Serial Frame Structure

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Header Frame

The first two bits of the header frame [31,30], are the node address bits, NAD. These two bits provide the ability to address up to four peripheral nodes, 3 to 0, independently while sharing a common SPI bus, including CSn. For the A89103, the NAD is fixed at 1 [0,1], and broadcast on NAD 3 is not supported. Each peripheral that shares a common CSn signal must have a unique address. Only the node addressed by the first two bits of the header frame respond on MISO in the following frame. If the A89103 does not detect its own peripheral node address, it ignores the complete transfer until CSn goes high.

The next 2 bits, [29:28], are the command (CMD) bits. When CMD = 0 (write), the A89103 writes the header data bits to the addressed register and sends the status register contents in the response-frame data bits. When CMD = 1 (read), the A89103 ignores the header bits and sends the data in the addressed register in the response-frame data bits.

CMD = 2 and CMD = 3 are reserved and provide no function in the A89103. If CMD = 2 or 3 is detected, the following header address and data are ignored and, if uniquely addressed by NAD, the A89103 responds with all zeroes in the response data. The header frame must otherwise comply with all frame-verification checks; if compliance is not achieved, a serial error is reported. Likewise, to ensure that the controller does not detect a framing error, the response frame complies with all frame-verification checks.

The next 7 bits of the header frame, [27:21], are the address bits for the register address where data is to be written to the A89103 from the controller or read back from the A89103 to the controller. Data from the controller is only written to the addressed register in the A89103, and any resulting action is only taken, when CSn goes high.

The register address is followed by the 16-bit header data in bits [20:5] that is to be written to the addressed register. If CMD = 1, indicating a register read, the data bits in the header frame are ignored.

The last 5 bits in the header frame are the cyclic redundancy checksum (CRC). The checksum is based on the standard USB-5 token checksum with a polynomial $x^5 + x^2 + 1$ and calculated over the full transmission, including the NAD bits.

Response Frame

If the node address in the preceding header frame does not match the contents of the NAD [1:0] variable, the A89103 is not the directly addressed peripheral node and maintains the MISO terminal in the high-impedance state for the complete frame.

If the A89103 detects its own unique peripheral node address in the header of the preceding frame, it first responds by sending its node address in the first two bits of the response frame. This permits the controller to check that the correct peripheral is responding.

The next bit, V, verifies that the previous transmission received by this A89103 node was correct. If V = 1, the previous transmission was received correctly. If V = 0, an error has occurred in the previous transmission, and no action has been taken with any received data.

This is followed by the general fault flag, FF, which indicates if a fault has been detected since the last transmission. FF is derived from a logical OR of bits in the status register. FF = 1 indicates that a fault has been detected and should be verified by reading the contents of the status register.

The FF bit is followed by three 0 bits, then by a 4-bit count value. The count value is provided by a 4-bit modulo counter that is incremented after the end of the frame each time a valid header frame is received with a matching node address. The counter value starts at 0 following each power-on-reset event and rolls over from the maximum count of 15 back to 0. If the node address in the header does not match the node address of the A89103, the count does not increment.

The content of the next 16 bits, [20:5], in the response frame depends on the command in the header frame. For a write command, these bits are the contents of the status register. For a read command, these bits are the contents of the addressed register.

NOTE: The status register can also be read directly with a read command to register 0, the address of the status register.

The last 5 bits in the header frame are the CRC. The checksum is based on the standard USB-5 token checksum with a polynomial $x^5 + x^2 + 1$ and calculated over the full transmission including the NAD bits. A detailed description of how to create and use the checksum is provided in the Application Information section (to be added at a later date).

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F_{CLK}-Dependent Timing Configuration

The A89103 uses a 4 MHz nominal digital clock frequency, f_{CLK}, for digitally timed functions. The accuracy of f_{CLK}-timed functions can be improved by adjusting the f_{CLK} frequency through the SPI interface. To determine the adjustment necessary, set the SPI configuration bits DIAG [1:0] to 1, which applies a 4.1 ms nominal period clock signal, proportional to f_{CLK}, on the DIAG terminal. To determine what adjustment is needed, this signal can be measured by the MCU and compared to the ideal 4.1 ms value. The adjustment to the f_{CLK} period is made by programing the SPI configuration bits CFCLK [4:0]. Bits CFCLK [4] to CFCLK [0] adjust the period by –36%, +18%, +9%, +4.5%, and +2.25% nominal values, respectively. After programing, the DIAG clock signal can be measured to confirm the desired result.

Device Identification Register

An additional feature of the A89103 is the device identification register IDENT_0. This register ensures that the device complies with future cybersecurity requirements and that the variant and revision history are tracked.

The IDENT_0 register is a read only register. An 8-bit integer stores the unique chip identification number (CID) [7:0]. The VIO bit indicates the logic level of the variant. If VIO is 0, the device operates with 3.3 V logic. If VIO is 1, the device operates with 5 V logic. REV [3:0] is a 4-bit integer that stores the silicon revision. This number is split into two parts:

- REV [1:0] stores the minor revision number.
- REV [3:2] stores the major revision.

For example, a device with revision 2.1 stores the value 1001 in the REV register.

Transmission Error Handling

If, during a frame transfer sequence, there are more than 32 rising edges on SCK or if CSn goes high and there are fewer than 32 rising edges on SCK, a framing error has been detected. If a framing error has been detected and/or the CRC checksum of any received transfer indicates an error in the transmission, the FSPI and FF bits are set to 1 and the V bit is set to 0 to indicate a data transfer error. In addition, any data write is cancelled without latching data to the register. The contents of the register can still be read even if the previous frame header contained the wrong CRC. This fault condition can be cleared by a subsequent valid serial transmission or by a power-on-reset.

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Sequential Transmissions

It is possible to have multiple sequential transmissions of read and/or write combinations to a single peripheral or to combinations of different peripherals. As a simple example, a basic write to register 0 for sequential nodes in typical mode is shown in Figure 19, where:

- U indicates bit is undefined.
- X indicates bit is not relevant.
- Single digit in parentheses indicates the associated node [e.g., Status(1) indicates the status information from node 1].
- Comma-separated digits in parentheses indicates the associated node and the register address [e.g., Data(3,0) indicates the data read from or written to register 0 in node 3].

In Figure 3, frame 1, data is sent from the controller to peripheral node 0 on MOSI to be written to register 0. In this example the header of the previous frame is unknown, so the response from MISO in frame 1 is unknown or undefined and is ignored.

In frame 2 data is sent from the controller to peripheral node 1 on MOSI to be written to register 0. Node 0 responds on MISO with the peripheral node 0 status.

The sequence continues through frames 3 and 4 for writing to nodes 2 and 3 and reading the status from nodes 1 and 2, respectively.

In frame 5, the controller sends a read request to node 1, register 23, and reads the status from node 3. The data bits in the header of frame 5 are unimportant, but the CRC must still be correct.

In frame 6, the controller sends a dummy read request to node 0, register 0, to permit the node 1 peripheral to respond in the frame with the requested contents of register 23.

			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		MOSI	**NAD**		**CMD**		**Address**							**Data**																**CRC**				
		MISO	**NAD**		**V**	**FF**	**0**			**Count**				**Status/Data**																**CRC**				
Frame 1	**Header**	MOSI	0		0		0							Data(0,0)																CRC				
	Response	MISO	U		U	U	U			U				U																U				
Frame 2	**Header**	MOSI	1		0		0							Data(1,0)																CRC				
	Response	MISO	0		1	0	0			1				Status(0)																CRC				
Frame 3	**Header**	MOSI	2		0		0							Data(2,0)																CRC				
	Response	MISO	1		1	0	0			1				Status(1)																CRC				
Frame 4	**Header**	MOSI	3		0		0							Data(3,0)																CRC				
	Response	MISO	2		1	0	0			1				Status(2)																CRC				
Frame 5	**Header**	MOSI	1		1		23							X																CRC				
	Response	MISO	3		1	0	0			1				Status(3)																CRC				
Frame 6	**Header**	MOSI	0		1		0							X																CRC				
	Response	MISO	1		1	0	0			2				Data(1,23)																CRC				

Figure 19: Sequential Node Write to Register 0—Typical Mode

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REGISTER MAPS

HEX	DEC	REGISTER NAME	TYPE	15	14	13	12	11	10	9	8
				7	6	5	4	3	2	1	0
0x00	0	STATUS_0	RW1C	ROCT	TW	FRESET	FDIAG	FUVP	FUVN	FSPI	FWD
				FOCP	FOCN	FVCP	FGBRG	FGREV	FGW	FGV	FGU
0x01	1	ENABLE/DISABLE_0	RW	ENOCT						DISBRG	DISREV
				DISW	DISV	DISU	ENBRG	ENREV	ENW	ENV	ENU
0x02	2	ENABLE/DISABLE_1	RW								
								ENWD	ENSW	ENVCP	ENVCPD
0x03	3	ENABLE/DISABLE_2	RW		ENBFTUVP	ENBFTUVN	ENBFTOCP	ENBFTOCN	ENBFTDIAG	ENRFTUVP	ENRFTUVN
				ENRFTOCP	ENRFTOCN	ENRFTDIAG	ENPFTUVP	ENPFTUVN	ENPFTOCP	ENPFTOCN	ENPFTDIAG
0x04	4	CONFIG_0	RW		OCP [6:0]						
					OCN [6:0]						
0x05	5	CONFIG_1	RW	CFCLK [4:0]					WDT [2:0]		
							VCMFG	SDCFG	WDSO	IDISREV	
0x06	6	CONFIG_2	RW								
				OCTP [1:0]		OCPD [2:0]			OCND [2:0]		
0x07	7	CONFIG_3	RW								
0x08	8	CONFIG_4	RW		DIAG [1:0]		DMFDIAG	DMFUVP	DMFUVN	DMFSPI	DMFWD
				DMFOCP	DMFOCN	DMFVCP	DMFGBRG	DMFGREV	DMFGW	DMFGV	DMFGU
0x09	9	VERIFY_COMMAND_0	RW		YUVP	YUVN	YWD				
								YOCP	YOCN	YTW	YCP
0x0A	10	DIAGNOSTIC_0	R				STATBRG	STATREV	STATW	STATV	STATU
				OCT [7:0]							
0x0	11	DIAGNOSTIC_1	R	WDC [15:8]							
				WDC [7:0]							
0x0E	14	VERIFY_RESULT_0	RW1C								
											CD
0x0F	15	READ-BACK	RW	READ-BACK_[15:8]							
				READ-BACK_[7:0]							
0x10	16	IDENT_0	R		VIO	REV3	REV2	REV1	REV0		
				CID7	CID6	CID5	CID4	CID3	CID2	CID1	CID0

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Serial Interface Default Values

SERIAL REGISTERS DEFINITION

For each input register, the first row shows the bit name and the second row shows the power-on-reset value for that input register bit.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0 STATUS_0	ROCT	TW	FRESET	FDIAG	FUVP	FUVN	FSPI	FWD	FOCP	FOCN	FVCP	FGBRG	FGREV	FGW	FGV	FGU
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1 ENABLE/ DISABLE_0	ENOCT						DISBRG	DISREV	DISW	DISV	DISU	ENBRG	ENREV	ENW	ENV	ENU
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2 ENABLE/ DISABLE_1													ENWD	ENSW	ENVCP	ENVCPD
	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
3 ENABLE/ DISABLE_2		ENBFTUVP	ENBFTUVN	ENBFTOCP	ENBFTOCN	ENBFTDIAG	ENRFTUVP	ENRFTUVN	ENRFTOCP	ENRFTOCN	ENRFTDIAG	ENPFTUVP	ENPFTUVN	ENPFTOCP	ENPFTOCN	ENPFTDIAG
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4 CONFIG_0		OCP6	OCP5	OCP4	OCP3	OCP2	OCP1	OCP0		OCN6	OCN5	OCN4	OCN3	OCN2	OCN1	OCN0
	0	1	1	0	0	0	1	1	0	0	0	1	0	0	0	1
5 CONFIG_1	CFCLK4	CFCLK3	CFCLK2	CFCLK1	CFCLK0	WDT2	WDT1	WDT0				VCMFG	SDCFG	WDSO	IDISREV	
	1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0
6 CONFIG_2									OCTP1	OCTP0	OCPD2	OCPD1	OCPD0	OCND2	OCND1	OCND0
				0	0	0	0	0	0	0	1	0	0	1	0	0
7 NOT USED																
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8 CONFIG_4		DIAG1	DIAG0	DMFDIAG	DMFUVP	DMFUVN	DMFSPI	DMFWD	DMFOCP	DMFOCN	DMFVCP	DMFGBRG	DMFGREV	DMFGW	DMFGV	DMFGU
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9 VERIFY_ COMMAND_0		YUVP	YUVN	YWD									YOCP	YOCN	YTW	YCP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10 DIAGNOSTIC_0				STATBRG	STATREV	STATW	STATV	STATU	OCT7	OCT6	OCT5	OCT4	OCT3	OCT2	OCT1	OCT0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11 DIAGNOSTIC_1	WDC15	WDC14	WDC13	WDC12	WDC11	WDC10	WDC9	WDC8	WDC7	WDC6	WDC5	WDC4	WDC3	WDC2	WDC1	WDC0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14 VERIFY_ RESULT_0																CD
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15 READ-BACK																
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16 IDENT_0		VIO	REV3	REV2	REV1	REV0			CID7	CID6	CID5	CID4	CID3	CID2	CID1	CID0
	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1

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Status Register

There is one status register. The contents of this register can be read, and are cleared only when a 1 is written to the specific bits. The status register provides a summary of the status of the device by indicating if any diagnostic monitors have detected a fault. These faults are summarized in Table 6.

The most significant bit in the status register is the overcurrent timer reset bit, ROCT. The overcurrent timer is reset by writing 1 to this bit.

The second most significant bit is the TW bit. When the junction temperature of the A89103 rises beyond the temperature warning threshold, the TW fault condition becomes set; however, all gate drives remain in the on state. This fault can be cleared by writing 1 to the TW bit.

The third bit is the FRESET bit. During a reset event, the latched fault status bit FRESET becomes set, indicating to the external controller that a power-on-reset has taken place. All other diagnostic bits are reset, and all other registers are returned to their default state.

NOTE: A power-on-reset only occurs when the V_{BB} or V_{DD} supply monitors are below their specified thresholds.

The fourth bit is the FDIAG bit. This bit is set when the DIAG pin is externally pulled low.

The fifth and sixth bits are FUVP and FUVN, respectively. These bits indicate when a positive- or negative-undervoltage event occurs on VBRG.

The FSPI bit indicates that the previous serial transmission was not completed successfully.

The FWD bit indicates when the watchdog timer is exceeded.

Bits FOCP and FOCN indicate when a positive- or negative-overcurrent event has been triggered.

Charge-pump undervoltage detection is indicated by the FVCP status bit.

The remaining bits, FGBRG, FGREV, FGW, FGV, and FGU, all indicate faults on the gate drivers. When a gate-to-source undervoltage fault occurs on the gate driver, the corresponding bit becomes set.

Table 6: Status Register Mapping

Status Register Bit	Diagnostic
ROCT	Overcurrent Timer
TW	Temperature Warning
FRESET	Supply Voltage Monitors
FDIAG	External DIAG Trigger
FUVP	Positive VBRG Monitor
FUVN	Negative VBRG Monitor
FSPI	Serial Error
FWD	Watchdog Error
FOCP	Positive Overcurrent
FOCN	Negative Overcurrent
FVCP	Charge Pump Monitor
FGBRG	Bridge Driver V_{GS} UV
FGREV	Reverse Battery V_{GS} UV
FGW	Phase W Driver V_{GS} UV
FGV	Phase V Driver V_{GS} UV
FGU	Phase U Driver V_{GS} UV

UV = Undervoltage, OV = Overvoltage

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Enable/Disable Registers

Three registers are used to enable or disable the different functionalities within the A89103.

- ENABLE/DISABLE_0

  Individual bits for enabling (ENx) and disabling (DISx) the gate drivers and the overcurrent timer. The ENx and DISx bits can only change the state of the LENx signal when they are not the same value in a single SPI word. Therefore, to turn on LENx, ENx must be 1 and DISx must be 0 in the same SPI word. Similarly, to turn off LENx, ENx must be 0 and DISx must be 1 in the same SPI word.

- ENABLE/DISABLE_1

  Individual bits for enabling the charge-pump undervoltage monitor, the charge-pump regulator, the VBAT resistor-divider switch, and the SPI watchdog trigger.

- ENABLE/DISABLE_2

  Individual bits for disabling the gate drivers due to the following faults: positive-supply undervoltage, negative-supply undervoltage, positive overcurrent, negative overcurrent, and external DIAG trigger.

Configuration Registers

Four configuration registers are used to configure the functionalities within the A89103:

- CONFIG_0
  - OCP [6:0], a 7-bit integer to set the positive-overcurrent sense comparator threshold in 1 mV increments.
  - OCN [6:0], a 7-bit integer to set the negative-overcurrent sense comparator threshold in 1 mV increments.
- CONFIG_1
  - FCLK [4:0], a 5-bit integer to calibrate the digital clock period between –36% and +18% of the nominal value.
  - WDT [2:0], a 3-bit integer to set the watchdog timeout between 10.2 ms and 1310 ms.
  - VCMFG, selects the nominal voltage of VBRG.
  - SDCFG, sets the driver configuration to common drain or common source.
  - WDSO, sets the sequence of operation for watchdog timeout.
  - IDISREV, disables reverse supply MOSFET current-dependent isolation.
- CONFIG_2
  - OCTP [1:0], a 2-bit integer to set the OCT clock prescalar between 1 and 8.
  - OCPD [2:0], a 3-bit integer to set the deglitched overcurrent positive-filter time in 250 ns increments.
  - OCND [2:0], a 3-bit integer to set the deglitched overcurrent positive-filter time in 250 ns increments.
- CONFIG_4
  - DIAG [1:0], a 2-bit integer to select the signal output on the DIAG terminal.
  - Individual mask bits to disable diagnostics from being output on the DIAG terminal.

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Verification Registers

Two registers are used to manage the diagnostic and system verifications:

- VERIFY_COMMAND_0

  Individual bits to initiate verification tests for VBRG, watchdog, overcurrent, temperature warning, and charge pump diagnostics.

- VERIFY_RESULT_0

  Individual bit holding the result of the current disconnect verification test. This is a read/write-1-to-clear register. Therefore, the contents of this register can only be cleared by writing 1 to the CD bit.

Diagnostic Registers

Two read-only diagnostic registers provide detailed diagnostic management and reporting:

- DIAGNOSTIC_0 (read only)
  - The latched enable gate driver signal status for each gate driver and the OCP timed value.
- DIAGNOSTIC_1 (read only)
  - Watchdog counter elapsed time.

Data written to the STATx registers is ignored.

Readback

A register to write and read data to the A89103 without affecting its operation. This register can be used to test the read and write capability of the device.

Device Identification

- CID [7:0], an 8-bit integer to display the unique chip ID.
- Rev [3:0], a 4-bit integer to store the minor and major silicon revision.
- VIO, records the internal logic voltage levels.

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Status Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0 STATUS_0	ROCT	TW	FRESET	FDIAG	FUVP	FUVN	FSPI	FWD	FOCP	FOCN	FVCP	FGBRG	FGREV	FGW	FGV	FGU
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

STATUS_0

ROCT	Overcurrent timer
TW	Temperature warning
FRESET	Supply-voltage monitors
FDIAG	External DIAG trigger
FUVP	Positive VBRG monitor
FUVN	Negative VBRG monitor
FSPI	Serial error
FWD	Watchdog error
FOCP	Positive overcurrent
FOCN	Negative overcurrent
FVCP	Charge-pump monitor
FGBRG	Bridge-driver V_{GSUV}
FGREV	Reverse-battery V_{GSUV}
FGW	Phase-W driver V_{GSUV}
FGV	Phase-V driver V_{GSUV}
FGU	Phase-U driver V_{GSUV}

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Enable/Disable Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1 ENABLE/ DISABLE_0	ENOCT						DISBRG	DISREV	DISW	DISV	DISU	ENBRG	ENREV	ENW	ENV	ENU
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2 ENABLE/ DISABLE_1													ENWD	ENSW	ENVCP	ENVCPD
	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
3 ENABLE/ DISABLE_2		ENBFTUVP	ENBFTUVN	ENBFTOCP	ENBFTOCN	ENBFTDIAG	ENRFTUVP	ENRFTUVN	ENRFTOCP	ENRFTOCN	ENRFTDIAG	ENPFTUVP	ENPFTUVN	ENPFTOCP	ENPFTOCN	ENPFTDIAG
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ENABLE/DISABLE_0

ENOCT	Overcurrent timer
DISBRG	Disable bridge-supply isolator gate drive
DISREV	Disable reverse-battery isolator gate drive
DISW	Disable phase-W isolator gate drive
DISV	Disable phase-V isolator gate drive
DISU	Disable phase-U isolator gate drive
ENBRG	Enable bridge-supply-isolator gate drive
ENREV	Enable reverse-battery-isolator gate drive
ENW	Enable phase-W isolator gate drive
ENV	Enable phase-V isolator gate drive
ENU	Enable phase-U isolator gate drive

ENABLE/DISABLE_1

ENWD	SPI watchdog isolation
ENSW	VBAT resistor-divider switch
ENVCP	Charge-pump regulator
ENVCPD	Charge-pump output monitor

ENABLE/DISABLE_2 (Stop on Fault)

ENBFTUVP	Bridge-supply MOSFET UVP trigger
ENBFTUVN	Bridge-supply MOSFET UVN trigger
ENBFTOCP	Bridge-supply MOSFET positive-overcurrent trigger
ENBFTOCN	Bridge-supply MOSFET negative-overcurrent trigger
ENBFTDIAG	Bridge-supply MOSFET trigger by DIAG
ENRFTUVP	Reverse-supply MOSFET UVP trigger
ENRFTUVN	Reverse-supply MOSFET UVN trigger
ENRFTOCP	Reverse-supply MOSFET positive-overcurrent trigger
ENRFTOCN	Reverse-supply MOSFET negative-overcurrent trigger
ENRFTDIAG	Reverse-supply MOSFET trigger by DIAG
ENPFTUVP	Phase-isolator UVP trigger
ENPFTUVN	Phase-isolator UVN trigger
ENPFTOCP	Phase-isolator positive-overcurrent trigger
ENPFTOCN	Phase-isolator negative-overcurrent trigger
ENPFTDIAG	Phase-isolator trigger by DIAG

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Configuration Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4 CONFIG_0		OCP6	OCP5	OCP4	OCP3	OCP2	OCP1	OCP0		OCN6	OCN5	OCN4	OCN3	OCN2	OCN1	OCN0
	0	1	1	0	0	0	1	1	0	0	0	1	0	0	0	1
5 CONFIG_1	CFCLK4	CFCLK3	CFCLK2	CFCLK1	CFCLK0	WDT2	WDT1	WDT0				VCMFG	SDCFG	WDSO	IDISREV	
	1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0

CONFIG_0

OCP [6:0]

Positive-current sense comparator threshold:

$$V_{OCP} = V_{CSP} - V_{CSM} = (1\ mV \times OCP) + 1,$$

where OCP is a positive integer defined by OCP [6:0]; e.g., for the default condition OCP [6:0] = 99, V_{OCP} = 100 mV, the range of V_{OCP} is 1 mV to 128 mV.

OCN [6:0]

Negative-current sense comparator threshold:

$$V_{OCN} = V_{CSM} - V_{CSP} = (1\ mV \times OCP) + 1,$$

where OCN is a positive integer defined by OCN [6:0]; e.g., for the default condition OCN [6:0] = 17, V_{OCN} = –18 mV, the range of V_{OCP} is –1 mV to –128 mV.

CONFIG_1

CFCLK [4:0]

Digital clock period configuration.

CFCLK	Period Adjustment (%)	Default
[0]	+2.25	D
[1]	+4.5	
[2]	+9	D
[3]	+18	D
[4]	–36	D

WDT [2:0]

SPI watchdog timeout, where WDT is a positive integer defined by WDT [2:0].

WDT	Timeout (ms)	Default
0	10.2	
1	20.5	
2	30.8	
3	41	
4	82	
5	328	
6	655	
7	1310	D

VCMFG

V_{BRG} nominal voltage.

VCMFG	VBRG Nominal Voltage	Default
0	12 V	D
1	48 V	

SDCFG

Common-source/common-drain driver configuration

SDCFG	Driver Configuration	Default
0	Common source	D
1	Common drain	

WDSO

Watchdog-timeout sequential operation.

WDSO	Sequence	Default
0	Disable phase isolators, then disable supply isolation MOSFETs.	D
1	Disable supply isolation MOSFETs, then disable phase isolators.	

IDISREV

Reverse-supply MOSFET current-dependent isolation.

WDSO	Reverse Supply MOSFET Current-Dependent Isolation	Default
0	Disabled	D
1	Enabled	

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CONFIGURATION—SERIAL REGISTER REFERENCE

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
6 CONFIG_2									OCTP1	OCTP0	OCPD2	OCPD1	OCPD0	OCDN2	OCDN1	OCDN0
			0	1	1	0	1	1	0	0	1	0	0	1	0	0
8 CONFIG_4		DIAG1	DIAG0	DMFDIAG	DMFUVP	DMFUVN	DMFSPI	DMFWD	DMFOCP	DMFOCN	DMFVCP	DMFGBRG	DMFGREV	DMFGW	DMFGV	DMFGU
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CONFIG_2

OCTP [1:0]

OCT clock prescalar, where OCTP is a positive integer defined by OCTP [1:0].

OCTP	Prescalar	Default
0	1	D
1	2	
2	4	
3	8	

OCPD [2:0]

Deglitched overcurrent positive-filter counter.

Produces a positive-filter time of 250 ns × n, where n is a positive integer defined by OCPD [2:0]; e.g., for the default condition, if OCPD [2:0] = 4, the positive-filter time is 1000 ns.

The range of positive-filter time is 0 ns to 1750 ns.

OCND [2:0]

Deglitched overcurrent negative-filter counter.

Produces a negative-filter time of 250 ns × n, where n is a positive integer defined by OCND [2:0]; e.g., for the default condition, if OCND [2:0] = 4, the positive-filter time is 1000 ns.

The range of negative-filter time is 0 ns to 1750 ns.

CONFIG_4 (Mask Register)

DIAG [1:0]

Diagnostic terminal configuration, where DIAG is a positive integer defined by DIAG [1:0].

DIAG	Configuration	Default
0	Fault indicator	D
1	Clock output for calibrating f_{CLK}	
2	Tristate: input only	
3	Tristate: input only	

DMFDIAG	Mask DIAG fault indicator
DMFUVP	Mask positive VBRG monitor
DMFUVN	Mask negative VBRG monitor
DMFSPI	Mask serial error
DMFWD	Mask watchdog error
DMFOCP	Mask positive overcurrent
DMFOCN	Mask negative overcurrent
DMFVCP	Mask charge pump monitor
DMFGBRG	Mask bridge driver V_{GS} UV
DMFGREV	Mask reverse battery V_{GS} UV
DMFGW	Mask phase W driver V_{GS} UV
DMFGV	Mask phase V driver V_{GS} UV
DMFGU	Mask phase U driver V_{GS} UV

DMFx	Fault mask	Default
0	Fault detection on DIAG permitted (DIAG pulled low)	D
1	Fault detection on DIAG disabled (DIAG not pulled low)	

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Verify Command Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
9 VERIFY_ COMMAND_0		YUVP	YUVN	YWD									YOCP	YOCN	YTW	YCP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VERIFY_COMMAND_0

YUVP	Verify positive VBRG monitor
YUVN	Verify negative VBRG monitor
YWD	Verify watchdog monitor
YOCP	Verify positive-overcurrent monitor
YOCN	Verify negative-overcurrent monitor
YTW	Temperature warning
YCP	Charge pump undervoltage

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Diagnostic Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
10 DIAGNOSTIC_0				STATBRG	STATREV	STATW	STATV	STATU	OCT7	OCT6	OCT5	OCT4	OCT3	OCT2	OCT1	OCT0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11 DIAGNOSTIC_1	WDC15	WDC14	WDC13	WDC12	WDC11	WDC10	WDC9	WDC8	WDC7	WDC6	WDC5	WDC4	WDC3	WDC2	WDC1	WDC0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DIAGNOSTIC_0 (Read Only)

STATBRG	Latched enable bridge driver signal status
STATREV	Latched enable reverse-battery driver signal status
STATW	Latched enable phase W driver signal status
STATV	Latched enable phase V driver signal status
STATU	Latched enable phase U driver signal status

OCT [7:0]

OCP timed value (t_{OC}):

$$(p \times n)/f_{CLK} < t_{OC} < [p \times (n + 1)]/f_{CLK},$$

where n is a positive integer defined by OCT [7:0], p is a clock prescalar defined by OCTP [1:0], and f_{CLK} is the internal timing clock frequency; e.g., for the default condition, if OCT [7:0] = 0 and the clock prescalar is set to 1 with an internal timing clock frequency of 4 MHz, the OCP timed value is 0 µs < t_{OC} < 0.25 µs.

DIAGNOSTIC_1 (Read Only)

WDC [15:0]

Watchdog elapsed time (t_{WDC}):

$$t_{WDC} = n \times 4\ \mu s,$$

where n is a positive integer defined by WDC [15:0]; e.g., for the default condition, if WDC [15:0] = 0, the watchdog elapsed time is 0 µs. The watchdog elapsed time ranges from 0 µs to 262.14 ms.

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Verify Result Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
14 VERIFY_ RESULT_0																CD
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VERIFY_RESULT_0

CD	Current sense comparator open circuit

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Readback Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
15 READ-BACK																
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

READ_BACK

Write and read contents of this register to test read-write functionality.

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Identification Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
16 IDENT_0		VIO	REV3	REV2	REV1	REV0			CID7	CID6	CID5	CID4	CID3	CID2	CID1	CID0
	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1

IDENT_0

CID [7:0]

Unique chip ID

REV [3:0]

Silicon revision, where:

- REV [1:0] stores the minor revision number and
- REV [3:2] stores the major revision number

VIO

Internal logic voltage level

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APPLICATION INFORMATION

Isolation Current Considerations

When using the A89103 for battery and phase isolation, care must be taken to ensure that the current is safely disconnected. If it is not safely disconnected, transients from the inductive load can avalanche the phase MOSFETs. An understanding of the overall system is required to safely implement isolation.

The current flow in the circuit during isolation is shown in Figure 20 and Figure 21 and described next.

Battery Isolation

A single MOSFET can be used to isolate the current flowing from the battery supply. This provides unidirectional current isolation because the body diode of the power MOSFET allows current to flow back into the supply.

The isolation MOSFET should be placed where it can obstruct the flow of current into the bridge. The path to VBB must be left unobstructed to ensure that the A89103 has enough power to complete the isolation process. Current flowing into VBRG is interrupted by the battery MOSFET when it is turned off, as shown in Figure 20. The current path is highlighted in red.

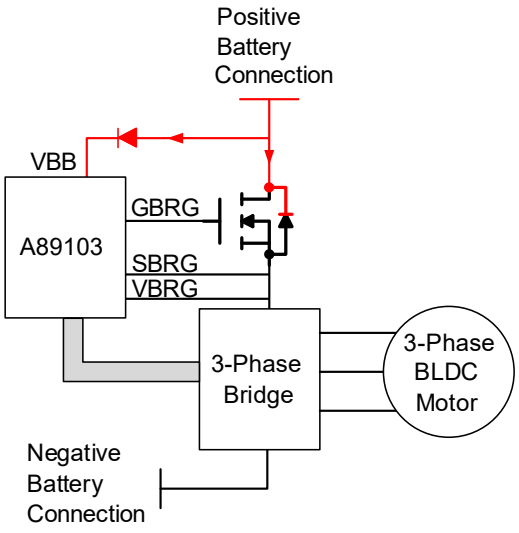

Figure 20: Bridge MOSFET Placement

Reverse Battery Isolation

The reverse battery isolation MOSFET provides protection of the battery and the A89103 from negative currents. These negative currents result from energy released by the motor when it enters generating mode. This is known as the regeneration current. A reverse battery connection also produces negative currents.

The isolation MOSFET must be placed such that it blocks the current flow when turned off. The MOSFET can be placed both upstream or downstream from the three-phase bridge, as shown in Figure 21, where the current paths are highlighted in red.

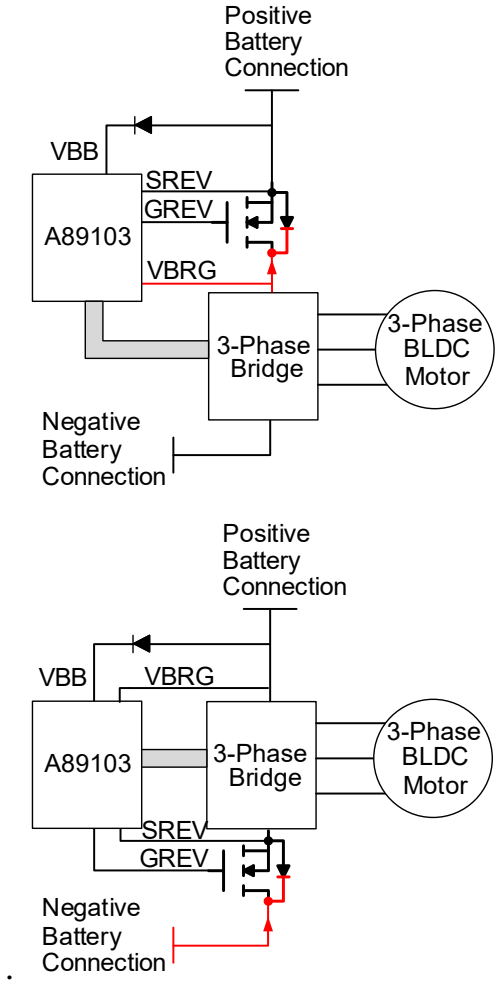

Figure 21: Reverse-Supply Protection MOSFET Placement

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Phase-Current Isolation

Because each MOSFET can only block current in one direction, the current flowing is always blocked by at least one MOSFET.

The configuration of the MOSFETs for phase-current isolation can be either drain-to-motor or source-to-motor. The sequence of disconnection changes according to which configuration is used. The configuration of optional clamping circuitry is also affected.

The direction of current flow for phase isolation in three possible scenarios is shown in Figure 22, where the current paths are highlighted in red.

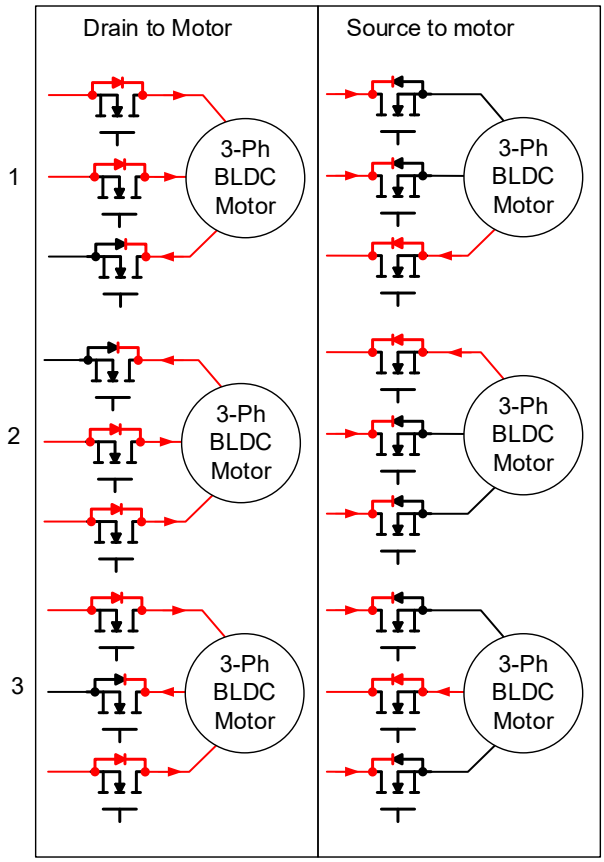

Figure 22: Current Flow Through Phase-Isolation MOSFETs

MOSFET Avalanche Protection

The phase MOSFETs must be appropriately protected to ensure that they do not suffer permanent damage during isolation. If the energy stored in the motor does not dissipate properly, a large voltage drop—greater than the breakdown voltage—occurs across the MOSFET. This can be prevented by either using additional external components or using control algorithms.

External Protection

One common practice for using external components is the inclusion of clamping diodes. These diodes provide a path for the current to safely recirculate when the phase MOSFETs are switched off. This prevents the voltage drop across the MOSFETs from entering the avalanche region. The diode clamps are oriented differently for the drain-to-motor and source-to-motor configurations, as shown in Figure 23, where the current paths are highlighted in red.

High-power diodes are selected with a reverse voltage that exceeds the rating of the motor and bridge voltage. This ensures that, during typical operation, the clamping diodes survive any voltage transients in the system.

Digital Protection

The use of algorithms is a digital approach to MOSFET avalanche protection. Two assumptions are made about the overall system to successfully execute the phase-isolation algorithms:

- The MCU has a real time update of the magnitude and direction of the current flowing through each phase MOSFET.
- The MCU has the ability to execute the algorithm and send the appropriate SPI signals to the A89103 within the specified watchdog timeout period.

Considering each phase MOSFET individually, each can be safely turned off in three main scenarios:

- When there is no current flowing in the phase, the MOSFET can be turned off immediately because there is no risk of avalanche.
- If the measured current is flowing from the source to the drain, the MOSFET can be turned off immediately. This is because the current can safely decay through the body diode.
- If the phase current is flowing from the drain to the source but its magnitude is lower than the avalanche current threshold for the MOSFET.

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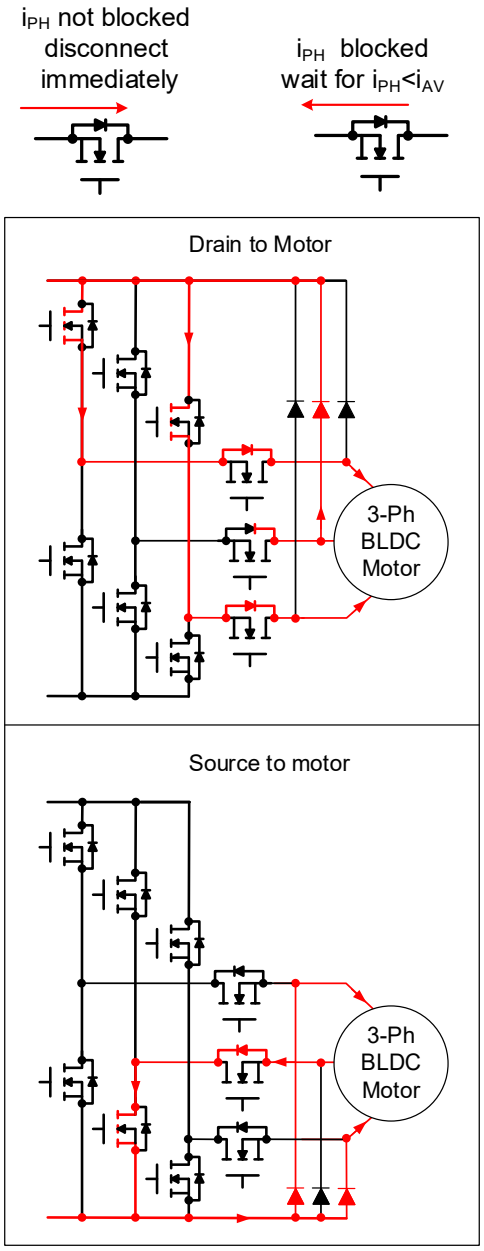

Figure 23: Phase-Isolation MOSFET Connection Options

MOSFET Avalanche Allowance

A common method of phase isolation is to allow the phase MOSFETs to enter the avalanche region. This is performed by using the arrangement with the source of the isolation MOSFET connected to the motor. The source voltage is allowed to go negative until it reaches the avalanche breakdown voltage of the MOSFET.

This well-documented mode of operation is specified in the MOSFET datasheet and has the added advantage of quickly reducing the phase current.

Because this method can quickly reduce the phase current with well-defined MOSFET capability at no extra cost, this has become the most popular solution for phase isolation. This solution requires the driver for the isolating MOSFET to withstand the negative voltage at the gate and source. However, since the gate pins of the A89103 have a similar negative-voltage capability as the source pins, this is not an issue.

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ADDITIONAL FEATURES

An additional feature of the A89103 is its ability to achieve automatic isolation according to different faults sensed in the system. The following sections describe how the device can be configured to achieve this.

Current-Dependent Isolation

The A89103 can be configured to automatically disconnect the battery and reverse MOSFETs when a positive- or negative-overcurrent event occurs. The phase MOSFETS cannot be automatically turned off, but they can be configured to be latched in their off state during the fault.

The configuration process for positive-overcurrent fault is:

1. Write 1 to ENVCP to turn on the charge pump.
2. Read the status register to determine if there are any startup faults.
3. Clear all startup faults by writing 1 to the corresponding fault bits in the STATUS_0 register.
4. Set one or a combination of the following bits, as desired:
   - □ To enable bridge MOSFET isolation, set ENBFTOCP to 1.
   - □ To enable reverse-battery isolation, set ENRFTOCP to 1.
   - □ To enable phase latching, set ENPFTOCP to 1.
5. Turn on the bridge MOSFET by writing 1 to ENBRG and 0 to DISBRG.
6. Turn on the reverse-supply MOSFET by writing 1 to ENREV and 0 to DISREV.
7. Turn on the phase MOSFETs by writing 1 to ENx (where x = U,V,W) and 0 to DISx.

The configuration process for negative-overcurrent fault is as follows:

1. Write 1 to ENVCP to turn on the charge pump.
2. Read the status register to determine if there are any startup faults.
3. Clear all startup faults by writing 1 to the corresponding fault bits in the STATUS_0 register.
4. Set one or a combination of the following bits, as desired:
   - □ To enable bridge MOSFET isolation, set ENBFTOCN to 1.
   - □ To enable reverse-battery isolation, set ENRFTOCN to 1.
   - □ To enable phase latching, set ENPFTOCN to 1.
5. Turn on the bridge MOSFET by writing 1 to ENBRG and 0 to DISBRG.
6. Turn on the reverse supply MOSFET by writing 1 to ENREV and 0 to DISREV.
7. Turn on the phase MOSFETs by writing 1 to ENx (where x = U,V,W) and 0 to DISx.

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Reverse-Supply MOSFET Current-Dependent Isolation

An additional feature of the reverse-battery driver is its ability to add an additional current requirement before automatic isolation takes place. This feature ensures that the reverse-battery MOSFET is not damaged due to large reverse currents.

The isolation process is as follows:

1. Configure the reverse-battery driver for one or more of the automatic isolation triggers (OP, OCN, UVP, UVN, DIAG).
2. Set IDISREV to 1.
3. Turn on GREV by writing 1 to ENREV and 0 to DISREV.

The current-dependent isolation algorithm functions as shown in the block diagram in Figure 24.

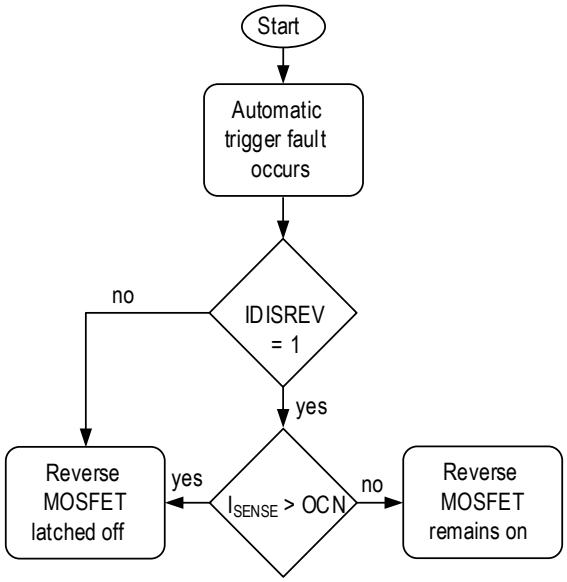

Figure 24: Current-Dependent Isolation Flowchart

Voltage-Dependent Isolation

Positive- and negative-undervoltage faults on VBRG can be used to achieve automatic isolation of the battery and reverse MOSFETs. The phase MOSFETS cannot be automatically turned off but they can be configured to be latched in their off state during the fault.

The configuration process for a positive-undervoltage fault is as follows:

1. Write 1 to ENVCP to turn on the charge pump.
2. Read the status register to determine if there are any startup faults.
3. Clear all startup faults by writing 1 to the corresponding fault bits in the STATUS_0 register.
4. Set one or a combination of the following bits, as desired:
   - □ To enable bridge MOSFET isolation, set ENBFTUVP to 1.
   - □ To enable reverse-battery isolation, set ENRFTUVP to 1.
   - □ To enable phase latching, set ENPFTUVP to 1.
5. Turn on the bridge MOSFET by writing 1 to ENBRG and 0 to DISBRG.
6. Turn on the reverse-supply MOSFET by writing 1 to ENREV and 0 to DISREV.
7. Turn on the phase MOSFETs by writing 1 to ENx (where x = U,V,W) and 0 to DISx

The configuration process for a negative-undervoltage fault is as follows:

1. Write 1 to ENVCP to turn on the charge pump.
2. Read the status register to determine if there are any startup faults.
3. Clear all startup faults by writing 1 to the corresponding fault bits in the STATUS_0 register.
4. Set one or a combination of the following bits, as desired:
   - □ To enable bridge MOSFET isolation, set ENBFTUVN to 1.
   - □ To enable reverse-battery isolation, set ENRFTUVN to 1.
   - □ To enable phase latching, set ENPFTUVN to 1.
5. Turn on the bridge MOSFET by writing 1 to ENBRG and 0 to DISBRG.
6. Turn on the reverse supply MOSFET by writing 1 to ENREV and 0 to DISREV.
7. Turn on the phase MOSFETs by writing 1 to ENx (where x = U,V,W) and 0 to DISx.

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External Triggering Isolation

The DIAG pin can be used for external triggering. When this pin is externally pulled low, a fault state is triggered. A DIAG fault can be used to automatically turn off the battery and reverse MOSFETs. The phase MOSFETs can be latched off.

The configuration process for a positive-undervoltage fault is:

1. Write 1 to ENVCP to turn on the charge pump.
2. Read the status register to determine if there are any startup faults.
3. Clear all startup faults by writing 1 to the corresponding fault bits in the STATUS_0 register.
4. Set one or a combination of the following bits, as desired:
   - □ To enable bridge MOSFET isolation, set ENBFTDIAG to 1.
   - □ To enable reverse-battery isolation, set ENRFTDIAG to 1.
   - □ To enable phase latching, set ENPFTDIAG to 1.
5. Turn on the bridge MOSFET by writing 1 to ENBRG and 0 to DISBRG.
6. Turn on the reverse supply MOSFET by writing 1 to ENREV and 0 to DISREV.
7. Turn on the phase MOSFETs by writing 1 to ENx (where x = U,V,W) and 0 to DISx.

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Automatic Isolation Combinations

A combination of fault triggers can be configured to automatically turn off the bridge or reverse MOSFET driver. Connection of these drivers is shown in the control logic diagrams in Figure 25 and Figure 26.

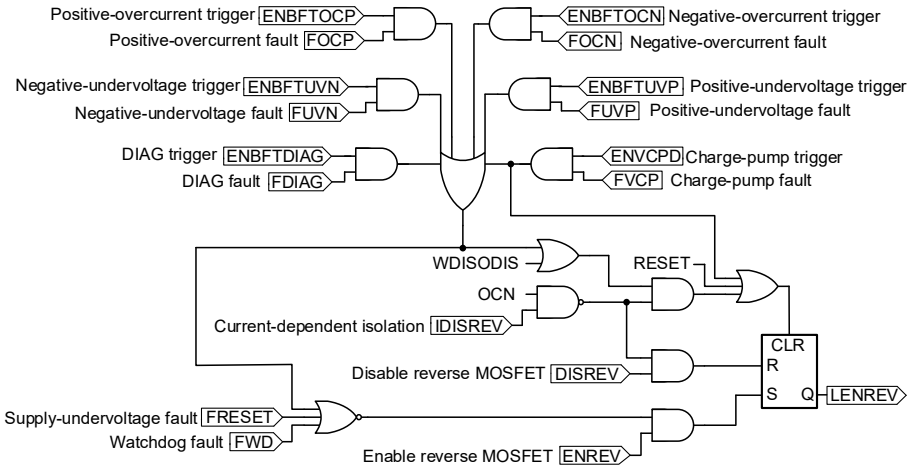

Figure 25: GREV Driver Latched Enable Control

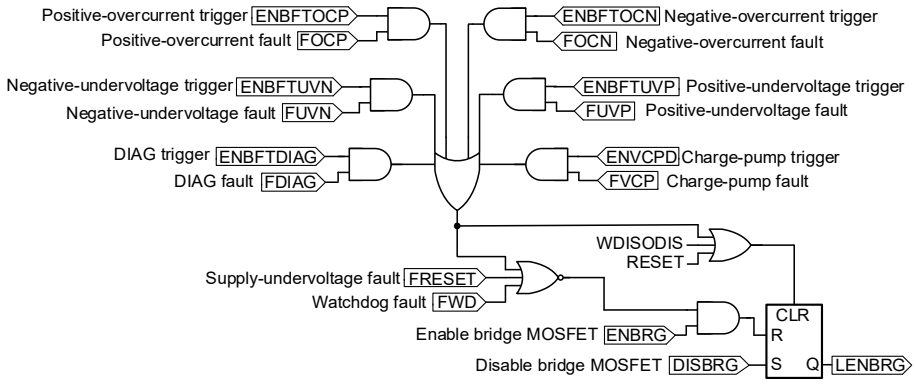

Figure 26: GBRG Driver Latched Enable Control

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Battery MOSFET Driver Basic Configuration

For the basic configuration, the GBRG driver is operated as an independent gate driver. All faults are ignored, and the driver can only be turned on and off via the SPI control bits ENBRG and DISBRG, respectively.

ENERGIZING SEQUENCE

1. Turn on the battery supply VBAT.
2. To operate the A89103 with SPI watchdog enabled, all subsequent SPI transactions must be sent within the default watchdog timeout period of 1310 ms. Otherwise, the SPI watchdog must be disabled by writing 0 to ENWD. Because this bit defaults to 1, the watchdog must be disabled within the watchdog timeout period. For further explanation of the disabling process, refer to the Watchdog Monitor Basic Configuration section.
3. Enable the charge pump by setting ENVCP to 1. This bit has a default value of 0.
4. Ensure that all the fault action bits found in the ENABLE/DISABLE _2 register are set to the default value of 0.

MOSFET DRIVING

To turn on the MOSFET driver, simultaneously write 1 to ENBRG and 0 to DISBRG. Similarly, to turn off GBRG, simultaneously write 0 to ENBRG and 0 to DISBRG.

HARDWARE CONSIDERATIONS

The gate driver is designed for isolation MOSFETs. Therefore, it can turn off the MOSFET within 2 µs. However, the driver does not have the capability for high-frequency PWM switching. The gate-to-source voltage of the GBRG driver is internally monitored to ensure it provides sufficient voltage to turn on the external MOSFET. It is recommended that the FGBRG bit be monitored to ensure that there is no V_{GS} undervoltage event present while the MOSFET is in the on state.

If a V_{GS} undervoltage event occurs, further action must be taken to protect the overall system.

Reverse MOSFET Driver Basic Configuration

For the basic configuration, the GREV driver is operated as an independent gate driver. All faults are ignored, and the driver can only be turned on and off via the SPI control bits ENREV and DISREV, respectively.

ENERGIZING SEQUENCE

1. Turn on the battery supply VBAT.
2. To operate the A89103 with SPI watchdog enabled, all subsequent SPI transactions must be sent within the default watchdog timeout period of 1310 ms. Otherwise, the SPI watchdog must be disabled by writing 0 to ENWD. Because this bit defaults to 1, the watchdog must be disabled within the watchdog timeout period. For further explanation of the disabling process, refer to the Watchdog Monitor Basic Configuration section.
3. Enable the charge pump by setting ENVCP to 1. This bit has a default value of 0.
4. Ensure that all the fault action bits found in the ENABLE/DISABLE _2 register are set to 0.

MOSFET DRIVING

To turn on the MOSFET driver, simultaneously write 1 to ENREV and 0 to DISREV. Similarly, to turn off GREV, simultaneously write 0 to ENREV and 0 to DISREV.

HARDWARE CONSIDERATIONS

The gate driver is designed for isolation MOSFETs. Therefore, it can turn off the MOSFET within 2 µs. However, the driver does not have the capability for high-frequency PWM switching. The gate-to-source voltage of the GREV driver is internally monitored to ensure it provides sufficient voltage to turn on the external MOSFET. It is recommended that the FGREV bit be monitored to ensure that there is no V_{GS} undervoltage event present while the MOSFET is in the on state.

If a V_{GS} undervoltage event occurs, further action must be taken to protect the overall system.

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Phase MOSFET Driver Basic Configuration

Each phase driver can be configured to operate as an independent gate driver that is turned on or off via the serial interface.

ENERGIZING SEQUENCE

1. Turn on the battery supply VBAT.
2. To operate the A89103 with SPI watchdog enabled, all subsequent SPI transactions must be sent within the default watchdog timeout period of 1310 ms. Otherwise, the SPI watchdog must be disabled by writing 0 to ENWD. Because this bit defaults to 1, the watchdog must be disabled within the watchdog timeout period. For further explanation of the disabling process, refer to the Watchdog Monitor Basic Configuration section.
3. Enable the charge pump by setting ENVCP to 1. This bit has a default value of 0.
4. Ensure that all fault action bits found in the ENABLE/DISABLE_2 register are set to 0.

MOSFET DRIVING

To turn on a phase MOSFET driver (GU, GV,GW), simultaneously write 1 to the ENx bit (ENU, ENV, ENW) and 0 to the DISx bit (DISU, DISV, DISW). Similarly, to turn off GU, GV, GW, simultaneously write 0 to ENx (ENU, ENV, ENW) and 1 to the DISx (DISU, DISV, DISW) bit.

HARDWARE CONSIDERATIONS

The gate driver is designed for isolation MOSFETs. Therefore, it can turn off the MOSFET within 2 µs. However, the driver does not have the capability for high-frequency PWM switching. The gate-to-source voltage of the Gx (GU GV GW) driver is internally monitored to ensure that it provides sufficient voltage to turn on the external MOSFET. It is recommended that the FGx (FGU FGV FGW) bit be monitored to ensure that no V_{GS} undervoltage event is present while the MOSFET is in the on state.

If a V_{GS} undervoltage event occurs, further action must be taken to protect the overall system.

Watchdog Monitor Basic Configuration

The watchdog monitor has a default on state and a default time-out period of 1310 ms. This means that, if a valid SPI transaction does not occur within 1310 ms of turn-on, a watchdog timeout occurs. Additionally, if consecutive SPI transactions do not occur within the default watchdog time, a watchdog fault occurs.

DISABLING THE WATCHDOG MONITOR

1. Send the following consecutive patterns to the A89103 within 1310 ms:
   A. Write 0 ENWD in the ENABLE/DISABLE_1 register.
   B. Read the ENABLE/DISABLE_1 register.
2. After this process, the latched watchdog fault bit can be cleared by writing 1 to FWD in the STATUS_0 register.

SETTING WATCHDOG TIMEOUT PERIOD

For a shorter watchdog timeout period, write the desired value to the WDT [2:0] variable in the CONFIG_1 register. This action can be performed when the watchdog monitor is disabled or enabled. If the monitor is enabled during the timeout configuration, ensure that the time between consecutive SPI transactions is faster that the new watchdog timeout period.

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DC Link Capacitor Charging

The A89103 includes features to control the charge cycle of the DC link capacitor.

An equivalent RC circuit can be used to represent the DC link capacitor, as shown in Figure 27.

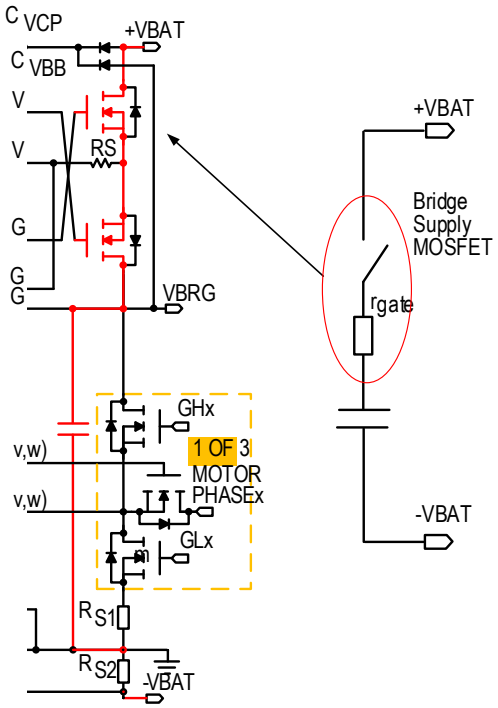

Figure 27: Equivalent DC Link Capacitor Charging Circuit

In fixed current charging, the fastest charge time is achieved by setting the current limit to the maximum value.

To charge the DC link capacitor with a fixed current:

1. Set OCP current limit according to system and MOSFET ratings.
2. Turn on the reverse MOSFET.
3. Configure the supply MOSFET to turn off automatically due to an OCP event.
4. Turn on the supply MOSFET, GBRG.
5. When the overcurrent event occurs, clear the fault and turn on on GBRG again.
6. Repeat this process until the overcurrent event does not occur.

The charging current and capacitor voltage can be represented as shown in Figure 28.

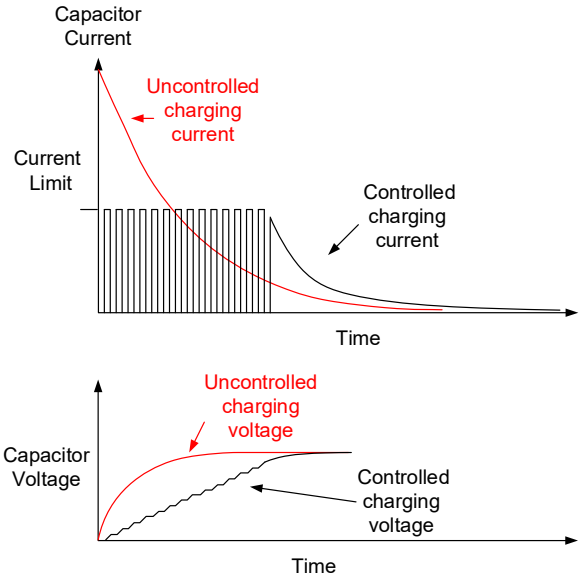

Figure 28: Controlled Capacitor Charging Current and Voltage

As shown in Figure 28, using a current limited charging approach results in a stepwise increase in the capacitor voltage.

The equation for capacitor current is:

$$I = (C\Delta v_C)/\Delta t,$$

where Δv_C is the small change in capacitor voltage during the charging cycle and Δt is the small change in time, as shown in Figure 29. When the equation is rearranged as $\Delta v_C = I\,\Delta t/C$, the total voltage on the capacitor can be estimated by measuring the total time that the capacitor is charging; this is the sum of the overcurrent timed value, t_{OC}, for each overcurrent event.

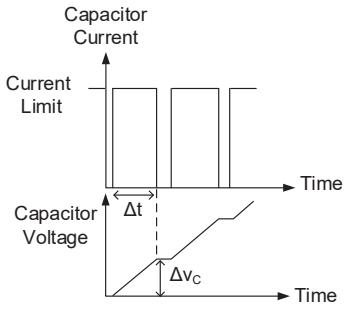

Figure 29: Incremental Change in Capacitor Voltage During Charging Event

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DC LINK CHARGING EXAMPLE

The following example considers a system with a DC link capacitor of capacitance 0.003 F that has to be charged to a DC voltage of 45 V with a maximum charging current of 5 A.

Using this information, the time for charging can be estimated as:

$$t = (C\Delta v_C)/I = 0.003\ F \times 45\ V/5\ A = 27\ ms$$

The process to set the time for charging is:

1. Set OCP current limit to 5 A.
2. Turn on the reverse MOSFET.
3. Configure the supply MOSFET to turn off automatically due to an OCP event.
4. In the same SPI command, set ENOCT to 1, ENBRG to 1, and DISBRG to 1.
5. When the overcurrent event occurs, clear the OCP fault in the STATUS_0 register and estimate t_{OC} using the equation:

   $$(p \times n)/f_{CLK} < t_{OC} < [p \times (n+1)]/f_{CLK},$$

   where n is a positive integer defined by OCT [7:0], p is a clock prescalar defined by OCTP [1:0], and f_{CLK} is the internal timing clock frequency.
6. Store the time in a register in the MCU. This time will be incremented by the value of t_{OC} for every overcurrent event.
7. Repeat steps 4 and 5, and add the time to the stored value until the stored value equals 27 ms.

This process is summarized in the flowchart in Figure 30.

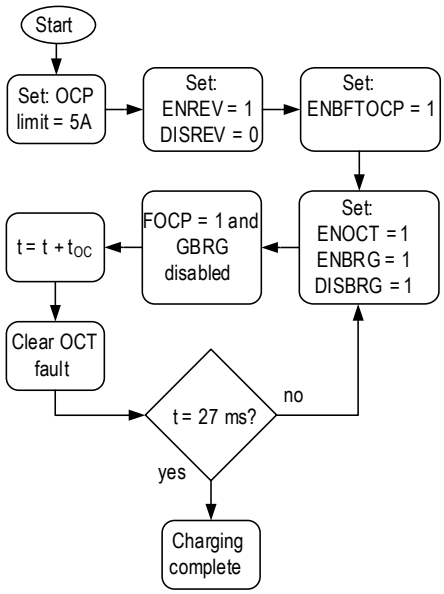

Figure 30: Flowchart for Charging DC Link Capacitor

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Fault Masking

Fault masking in the A89103 can be used to debug or to apply-application-specific faults. A fault is masked by setting the corresponding fault action bits to 0. These bits are found in the ENABLE/DISABLE_2 register.

Fault indication continues to appear in the status register and DIAG pin; however, no action is taken by the gate driver.

Fault indication on DIAG can also be masked by writing to the corresponding bit in the CONFIG_4 register. The response of the A89103 to masking a positive-overcurrent fault on the reverse-battery driver and DIAG pin is summarized in the flowchart in Figure 31.

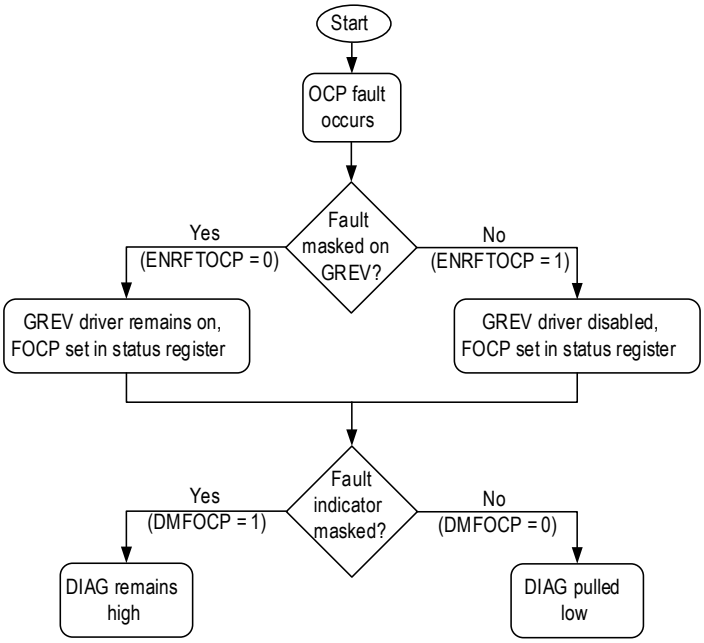

Figure 31: Fault-Masking Flowchart

Masking of the fault indicators is also a useful feature for redundant systems. This can be used to create specific secondary triggers to other parts of the system. An example of a secondary trigger is described in the flowchart for a redundant system containing two smart relays and a doubly wound motor, as shown in Figure 32.

When the primary relay (89103-A) detects a positive undervoltage, it begins the MOSFET isolation sequence.

All fault indicators other than FUVP are masked on DIAG.

When DIAG is pulled low due to FUVP, this trigger is used to disconnect the power supply to the primary GDU (GDU1) and to energize the secondary GDU (GDU2). The secondary relay turns on the isolation MOSFETs, energizing the secondary winding. A block diagram of the redundant drive system is shown in Figure 33.

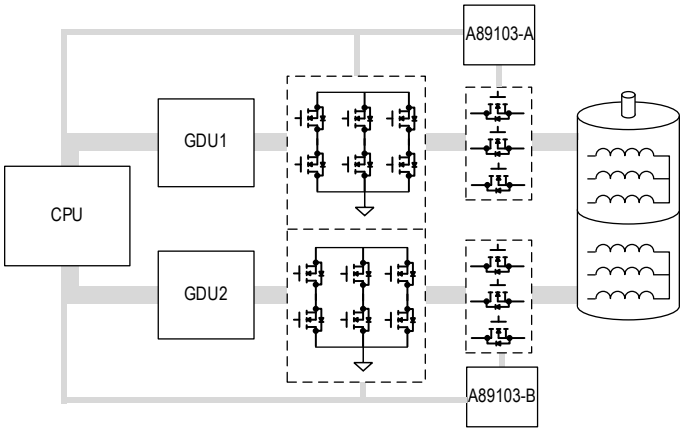

Figure 32: Example Redundant Drive System

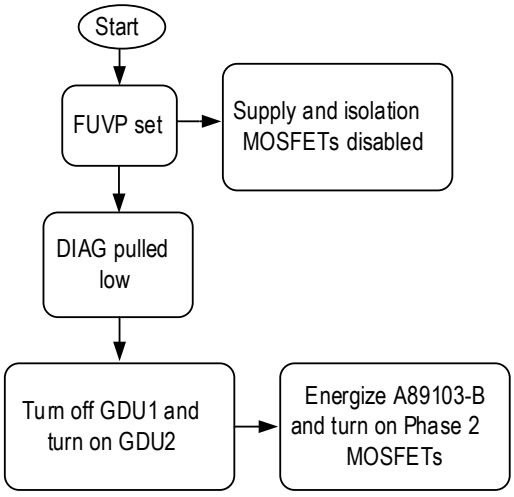

Figure 33: Secondary Triggering Flowchart

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Independent Drive Systems

The A89103 can be used in an independent drive system, as demonstrated in Figure 34. The phase drivers provide isolation of the motor while the battery isolators provide protection for the supply. This is achieved by monitoring the current in the battery and the voltage at the bridge.

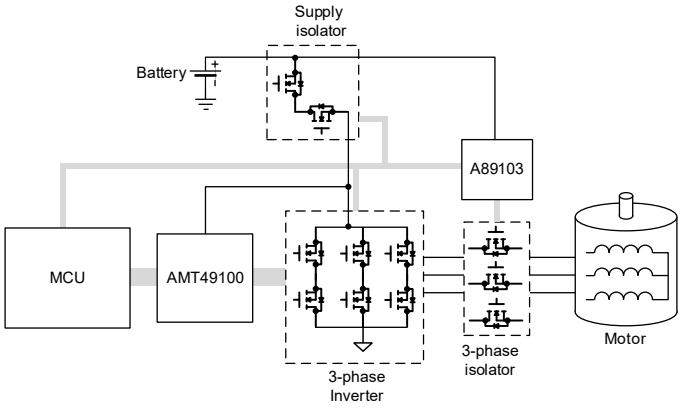

Figure 34: Independent Drive System Example

The example in Figure 34 incorporates the Allegro AMT49100 ASIL BLDC MOSFET gate driver for 48 V battery systems. [1] In this example, it is assumed that the AMT49100 is powered from the bridge terminal. An advantage of this configuration is that battery isolation also disconnects the supply to the AMT49100. One disadvantage of this configuration is that there is a risk that the six inverter MOSFETs do not turn off before the AMT49100 loses power. The energization sequence of this system is important for safe operation:

1. Energize the MCU and conduct any necessary startup tests.
2. Energize the A89103 and conduct any necessary startup tests.
3. Turn on the reverse-battery MOSFET.
4. Using the DC link charging process (see the DC Link Charging section), safely charge the DC link capacitor to the bridge voltage.
5. Turn on the bridge MOSFET using the A89103. This energizes the AMT49100.
6. Conduct any necessary startup tests on the AMT49100.
7. Turn on the three-phase isolator MOSFETs

An alternative configuration is to power the AMT49100 from the battery supply, as shown in Figure 35. The AMT49100 is independently powered, allowing all inverter MOSFET drivers to be turned off before the AMT491000 is turned off. An additional isolation circuit is required for disconnection of its supply from the battery. This system also has a different energizing sequence:

1. Energize the MCU and conduct any necessary startup tests.
2. Energize the A89103 and conduct any necessary startup tests.
3. Energize the AMT49100 and conduct any necessary startup tests.
4. Turn on the reverse-battery MOSFET.
5. Using the DC link charging process (see the DC Link Charging section), safely charge the DC link capacitor to the bridge voltage.
6. Turn on the bridge MOSFET using the A89103.
7. Turn on the three-phase isolator MOSFETs.

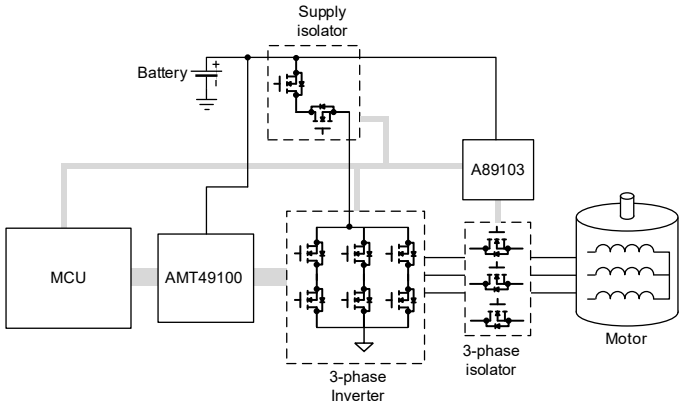

Figure 35: Alternative Independent Drive System

[1] https://www.allegromicro.com/en/products/motor-drivers/bldc-drivers/amt49100-amt49101

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Redundant Drive Systems

Redundancy is necessary in power steering systems to ensure that there is power steering assistance in most scenarios. Redundant systems reduce the rate of failure within the system. There are many different levels of redundancy that can be applied to systems. The redundancy level is determined by how safety-critical the feature is.

Another method to determine the redundancy required is by considering which component in the system has the highest failure rate.

The redundant part of the system must have the capability to fully replace the original system in terms of electrical parameters. However, the redundant part in power steering systems generally operate with reduced capability to ensure basic operation. This is known as “limp home” capability.

Based on the independent drive system described above, the three-phase inverter has the highest failure rate. There are three common redundant architectures that can be developed from this system:

- Single-Actuator Redundant Drive
- Redundant Drive and MCU
- Fully Redundant System

SINGLE-ACTUATOR REDUNDANT DRIVE

For this system architecture, a single motor and MCU is used with redundant inverters, gate drivers, and isolators, as shown in Figure 36.

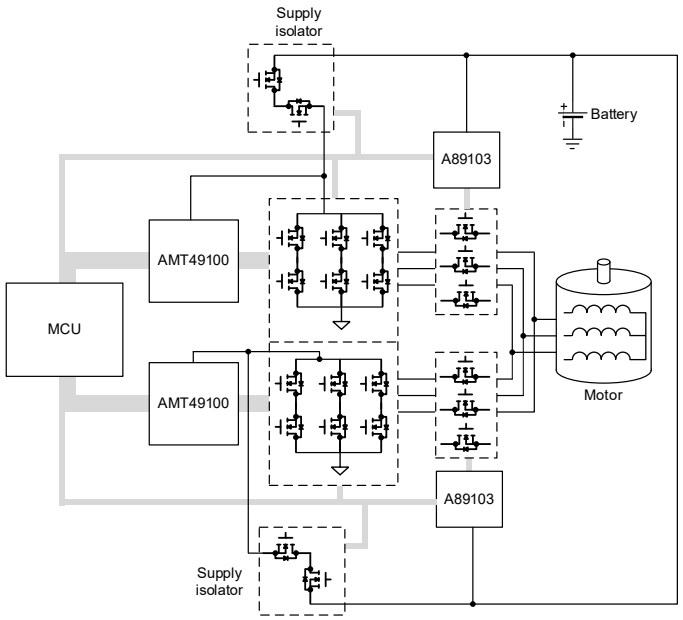

Figure 36: Example of Single-Actuator Redundant-Drive System

Switching from the primary gate driver to the secondary drive is triggered by a system fault. The following procedure is an example of how the secondary system can be energized.

1. Confirm that the primary phase and battery isolation MOSFETs are turned off.
2. Energize the secondary A89103.
3. Turn on the reverse battery MOSFET.
4. Turn on the bridge MOSFET using the A89103. This energizes the secondary AMT49100.
5. Turn on the three-phase isolator MOSFETs.

In this example, because it is assumed that the secondary system operates with reduced capability, the startup tests and DC link charging are not considered. These features can be included if necessary.

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REDUNDANT DRIVE AND MCU

Redundant MCU provides an additional protection against software failures. According to the system requirements, the second MCU operates as a backup or fully redundant system.

The processors usually operate together in one of the many dual, interlinked check modes. They are almost always from the same manufacturer and use the same software.

In this case, each processor drives its own powertrain down to the motor, but only one powertrain is active at any time.

The system layout is shown in the diagram in Figure 37.

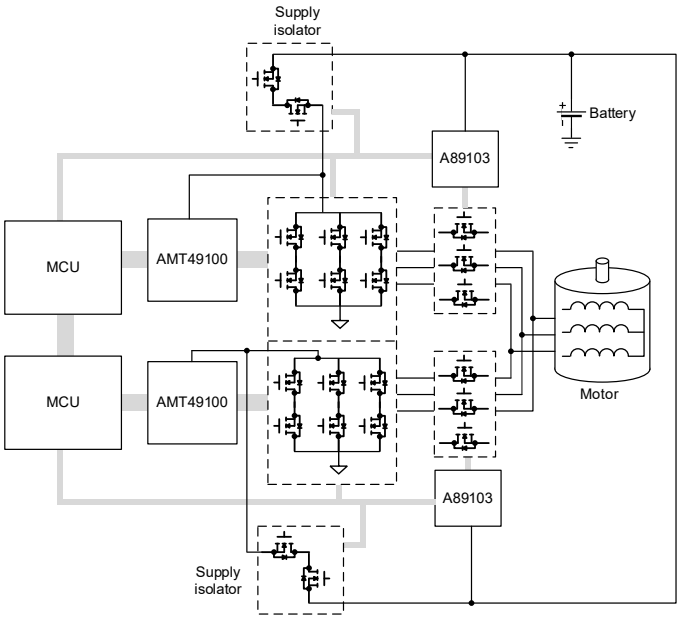

Figure 37: Example of Redundant Drive and MCU

FULLY REDUNDANT SYSTEM

For this system, a doubly wound motor is used with a redundant power supply. Although this system has a higher cost, it provides the greatest protection against failures. A block diagram of this system is shown in Figure 38.

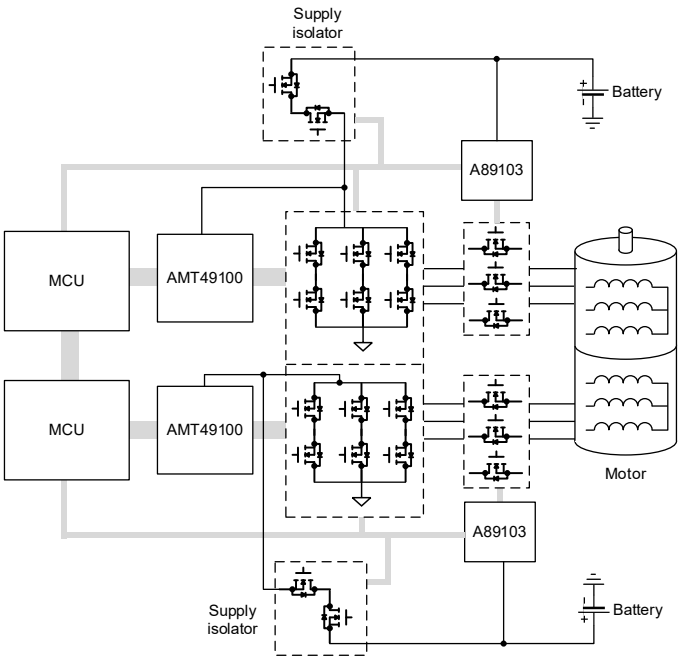

Figure 38: Fully Redundant Drive System

Digital Clock Frequency Configuration

Many functions in the A89103 depend on the digital clock, f_{CLK}. Improving the accuracy by calibrating the digital clock is a valuable additional feature.

The configuration process is as follows:

1. Energize the A89103 and clear all startup faults.
2. Set DIAG [2:0] to 1.
3. Measure the period of the signal at the DIAG pin.
4. Calculate the percentage difference between the measured period and the nominal clock period.
5. Adjust the frequency by a certain percentage by writing to CFCLK [4:0].
6. Measure the signal on DIAG and confirm it is within specified limits.

A combination of percentages can be used to achieve a desired configuration.

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Cyclic Redundancy Check

The cyclic redundancy checksum (CRC) is the error detection algorithm used in the A89103 to find unwanted changes in transmitted data. In this context, the MCU is the transmitter that sends the data to the A89103 via the serial interface and the A89103 is the receiver. The algorithm uses binary division to confirm that the transmitted and received data are identical.

The data frame is divided by a fixed number and the remainder is appended to the data frame. The receiver then divides this new frame by the same number to confirm that the remainder is zero. If the remainder is not zero, this means that the transmitted data was changed before it was received by the A89103. The CRC implementation is shown in the flowchart in Figure 39.

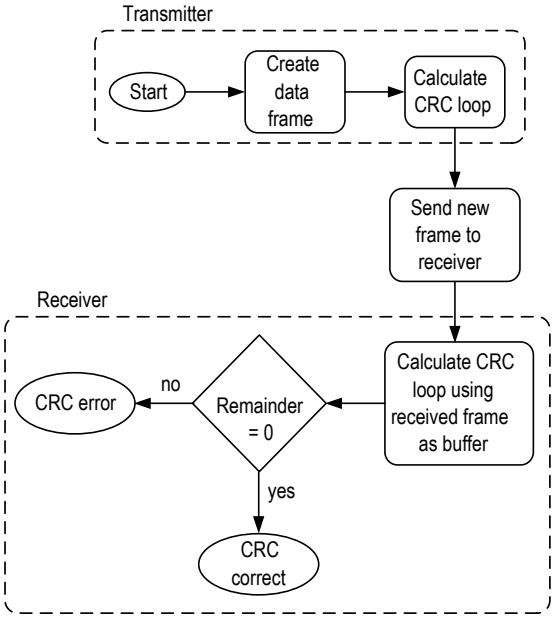

Figure 39: Flowchart Showing CRC Confirmation Sequence

The transmitter interprets the data to be sent as a binary number, N(x), and divides it by a polynomial, P(x), determined by the CRC format that is employed. The data and the division remainder, R(x), are sent to the receiver, which checks the message to verify if any errors were introduced during transmission.

P(x) is set by the CRC format chosen and, for the A89103, the USB CRC-5 is adopted. This format expresses the polynomial as:

$$P(x) = x^5 + x^2 + 1,$$

which is represented in binary form as 100101b.

N(x) comprises the data to be sent and, after the least significant bit of the data, a number of zeroes are padded equal to the degree of P(x). For an A89103 header message, N(x) consists of a header frame, address frame, command frame, data frame, and five zeroes for the CRC. For example, if the MOSI message has NAD equal to 01b, CMD of 00b, address of 0001111b, and data value of 0100011000011000b, then N(x) equals: 0100000111101000110000110000000000b.

A response message is composed similarly to the header message as described in the Serial Interface section. The structure of a serial frame is shown in Figure 18.

Dividing N(x) by P(x) results in a remainder, R(x). For example, dividing N(x), equal to 0100000111101000110000110000000000b, by P(x), equal to 100101b, gives remainder R(x) of 11010b.

The header frame is then completed with the remainder, substituting the zeros that were padded at the end of N(x). For example, if N(x) equals 0100000111101000110000110000000000b, the header frame transmitted is 0100000110101000110000110000000111b.

The receiver then performs a cyclic redundancy check, dividing the received message by P(x). If R(x) equals zero, the message has not been subjected to an unwanted change of bit.

CRC LOOP-DRIVEN IMPLEMENTATION

The loop-driven implementation of the CRC polynomial division uses a shift-register loop in conjunction with XOR gates and a buffer.

The shift registers are connected in series from bit 0 to bit 5. The number of shift registers is equal to the degree of P(x): For the A89103, six shift registers are necessary. The initial value of the shift registers is set to a non-zero value to preserve the leading zeros in N(x). For the A89103, the initial value of the shift registers is 010001. The buffer contains N(x). The initial setup used for the header frame example provided earlier in this section is shown in Figure 40.

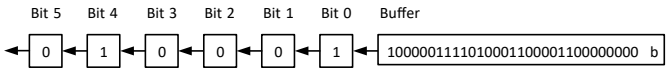

Figure 40: Initial Setup
The content of the shift registers is set to zero, and the buffer contains N(x).

The most significant bit in the buffer is pushed into the register loop, bit 0, sliding register contents to the left, toward bit 5. The content pushed left from bit 5 is disregarded. If bit 5 contains the value one, the register loop is XORed with the binary representa-

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tion of polynomial P(x); alternatively, if bit 5 contains the value zero, the previous step is repeated. See Figure 41.

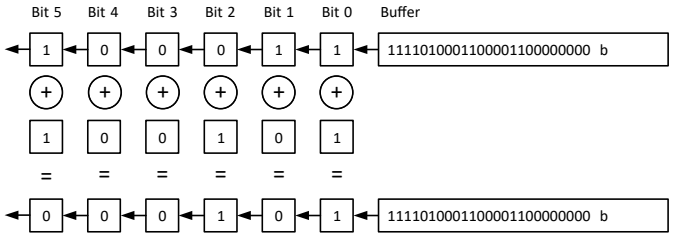

Figure 41: Bit 5 of Register Loop Contains Value 1 The register loop is XORed with the binary representation of P(x), and the new register-loop content becomes 000101b.

The process continues until the buffer is empty. Bits 4 to bit 0 of the register loop contain the remainder of the polynomial division, R(x). The resulting CRC frame is shown in Figure 42.

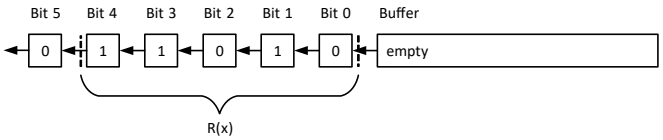

Figure 42: Once the Buffer Empties, Bit 4 to Bit 0 Contain the R(x) of the CRC Frame

The header frame is completed with the remainder, R(x), which must be substituted for the zeros that were padded at the end of N(x), as was explained in the introductory example.

The CRC loop implementation is explained in the flowchart in Figure 43.

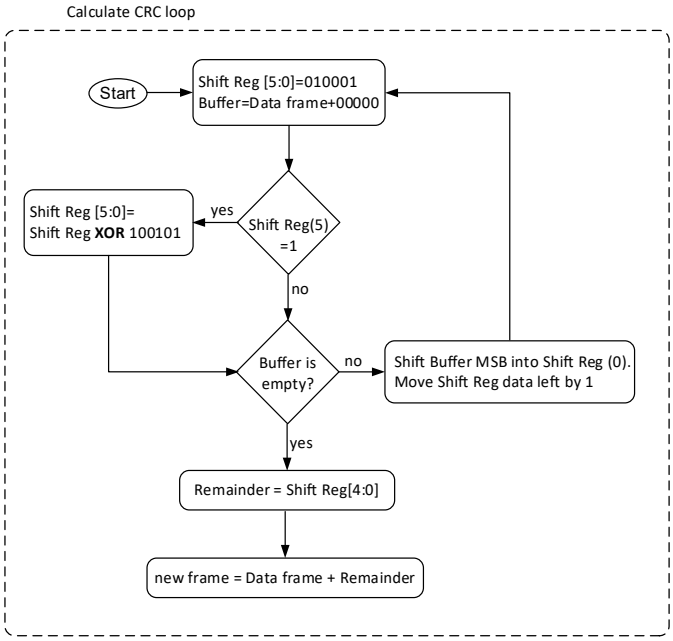

Figure 43: Flowchart Showing CRC Loop Algorithm

The receiver then performs a CRC test, repeating the steps above with the received message:

- If the message is devoid of errors, the register loop shows a zero for each of the bit 4 to bit 0 registers. This represents a correct CRC.
- If there is a remainder greater than zero, the A89103 determines that a CRC error occurred, and the FSPI and FF bits are set to 1. The V bit is set to 0 to indicate an error in the transmission.

		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Header	MOSI	NAD		CMD		Address							Data																CRC				
Response	MISO	NAD		V	FF	0			Count				Status/Data																CRC				

Figure 44: Serial Frame Structure

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Current Sense Monitor Configuration

Allowance must be made for both positive and negative current flows within the sense resistor.

The relationship between battery current, I_{BATT}, sense resistor value, R_S, and current sense monitor differential input voltage, V_{ID}, is given by:

$$V_{ID} = V_{CSP} - V_{CSM} = I_{BATT} \times R_S.$$

The sense resistor is selected to minimize power losses in the system. Typically, it is within the range of 0.5 to 1 mΩ.

V_{BB} CAPACITOR

The V_{BB} capacitor is present for two purposes—decoupling and V_{BB} holdup. Two separate capacitors are used to satisfy both requirements.

The decoupling capacitor is selected such that it can filter out high-frequency ripple of the charge pump. Therefore, selection depends on the acceptable DC voltage drop during the supply of a steady DC current, I. The capacitor value is calculated using:

$$C = I\Delta t/\Delta V,$$

where ΔV is the allowable DC voltage drop, and Δt is the time period. Considering a charge-pump frequency of 62.5 kHz and a current limit of 50 mA, the decoupling capacitor can be sized for a worst-case scenario of 1.5 V ripple as:

$$C = [(1/62.5\ kz) \times 50\ mA]/1.5\ V = \ 533\ nF$$

During typical operation, because the charge-pump capacitors do not fully discharge during every pump cycle, a decoupling capacitor with a fraction of this capacitance is suitable.

This decoupling capacitor should be placed as close to the device as possible.

The capacitance of the V_{BB} holdup capacitor is calculated using the same equation. In this case, ΔV is from the operating voltage to the minimum operating voltage (4.5 V), and Δt is the holdup time selected to allow the device to turn off in a safe manner. As good practice, Δt should be at least the minimum dead time (10.2 ms).

V_{BAT} RESISTOR-DIVIDER COMPONENTS

The resistor divider is designed to limit current flowing from the battery when V_{BAT} sensing is not required. Therefore, the resistors connected to SWIN and WSOUT must be selected for both current limiting and voltage biasing.

A resistance in the range of 80 to 120 kΩ sufficiently limits the current flowing into SWIN.

The value of the resistor connected to SWOUT can be 10 times less than SWIN to ensure the voltage at this pin is insignificant compared to V_{BAT}.

R_{S2} SENSE RESISTOR

R_{S2} is the sense resistor used by the A89103 to measure positive and negative battery current. The value of this resistor is calculated according to the power rating of the circuit and the acceptable voltage drop across this resistor. Because this sense resistor carries the DC current of the inverter at all times, it must be suitably rated to ensure that it can handle the dissipated power.

For example:

> If the maximum acceptable voltage drop is 50 mV and the expected maximum DC current is 40 A, the resistor value is:
>
> $$R_{S2} = 50\ mV/40\ A = 1.25\ m\Omega.$$

In the above example, the resistor dissipates 2 W of power at maximum current. Therefore, a 10 W resistor should comfortably handle the DC current without overheating.

COMMON-SOURCE CONFIGURATION

The reverse-supply and bridge MOSFET drivers can be configured to operate in either common-source or common-drain configuration. Selection of the mode of operation depends on the system architecture and budget for external components.

The common-source configuration is preferred for its simplicity because it only requires one additional component, R_S. This resistor is present to limit the current in case the battery is inadvertently connected with reverse polarity. The resistance is selected such that the I_R drop is not too large to decrease the gate drive. A resistance of 100 Ω ±20% works as a good balance between both requirements.

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COMMON-DRAIN CONFIGURATION

In the common-drain configuration, the GREV pin drives a transistor switch that operates in reverse polarity. When the transistor switch is in the on state, the gate of the external MOSFET is pulled to its source, turning it off. When the transistor switch is in the off state, the gate of the MOSFET is pulled to 12 V above its source, turning it on. The external components can be selected through a series of steps. The example circuit in Figure 45 is used to demonstrate the calculation process:

1. A 12 V Zener diode is selected to ensure that the reverse MOSFET is fully turned on when commanded.
2. When the transistor, T1, is turned on, all current flowing through R2 comes from the VCP pin. This pin is rated at 1 mA maximum. To ensure the pin is not stressed, 60 to 80% of this current can be used. In this example, 0.6 mA was selected. Therefore, R2 = (V_{CP} – 0.7 V – V_{BAT})/ 0.6 mA, where it is assumed that 0.7 V is dropped across all diodes.

   According to the Characteristic Performance section, V_{CP} is 10 V above V_{BB} during typical conditions and V_{BAT} is one diode drop above V_{BB}. Therefore:

   $V_{CP} – V_{BAT} = 9.3$ V

   R2 = (9.3 V – 0.7 V)/0.6 mA = 14.3 kΩ
3. Because R1 is a gate-source resistor present for biasing, resistances in the hundreds of kΩ are suitable. R1 should be 5 to 10 imes larger than R2,, ensuring minimal current flow through it when the MOSFET is in the on state. Therefore, a 150 kΩ resistor is suitable.
4. The remaining four resistors (R3, R4, R5, R6) are used to bias the transistor. R3 and R4 are set to identical values, creating a voltage divider between GREV – 0.7 V and V_{BAT}. The transistor base current, I_b, can be calculated using the DC current gain, hfe, as:

   $$I_b = ic/hfe$$

   Assuming that GREV goes to VCP when it is on and the DC current gain is 10:

   $$R3 = R4 = 0.5(GREV – 0.7 – V_{BAT})/I_b$$
   $$= 0.5(9.3\ V – 0.7\ V)50/0.6\ mA = 72.7\ k\Omega.$$
5. R5 is present to bias the transistor base. No current flows through this resistor except when reverse-battery operation occurs. A 10 kΩ resistor was selected.
6. R6 limits the current flowing into SREV as a form of protection from any V_{BAT} transients or reverse battery connection. A 10 kΩ resistor is suitable because it minimizes the current flowing into SREV. The example circuit is shown in Figure 45.

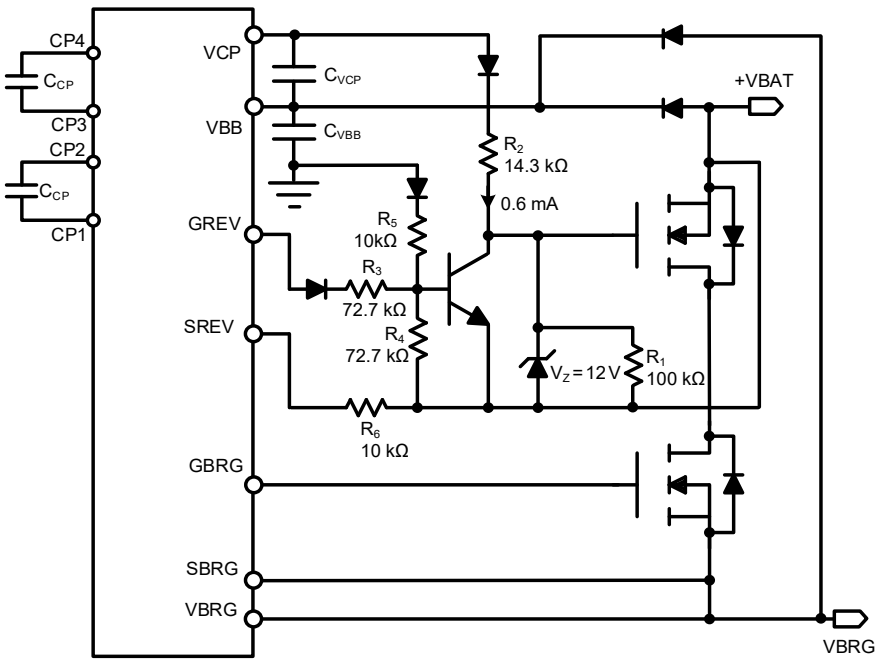

Figure 45: Recommended Circuit

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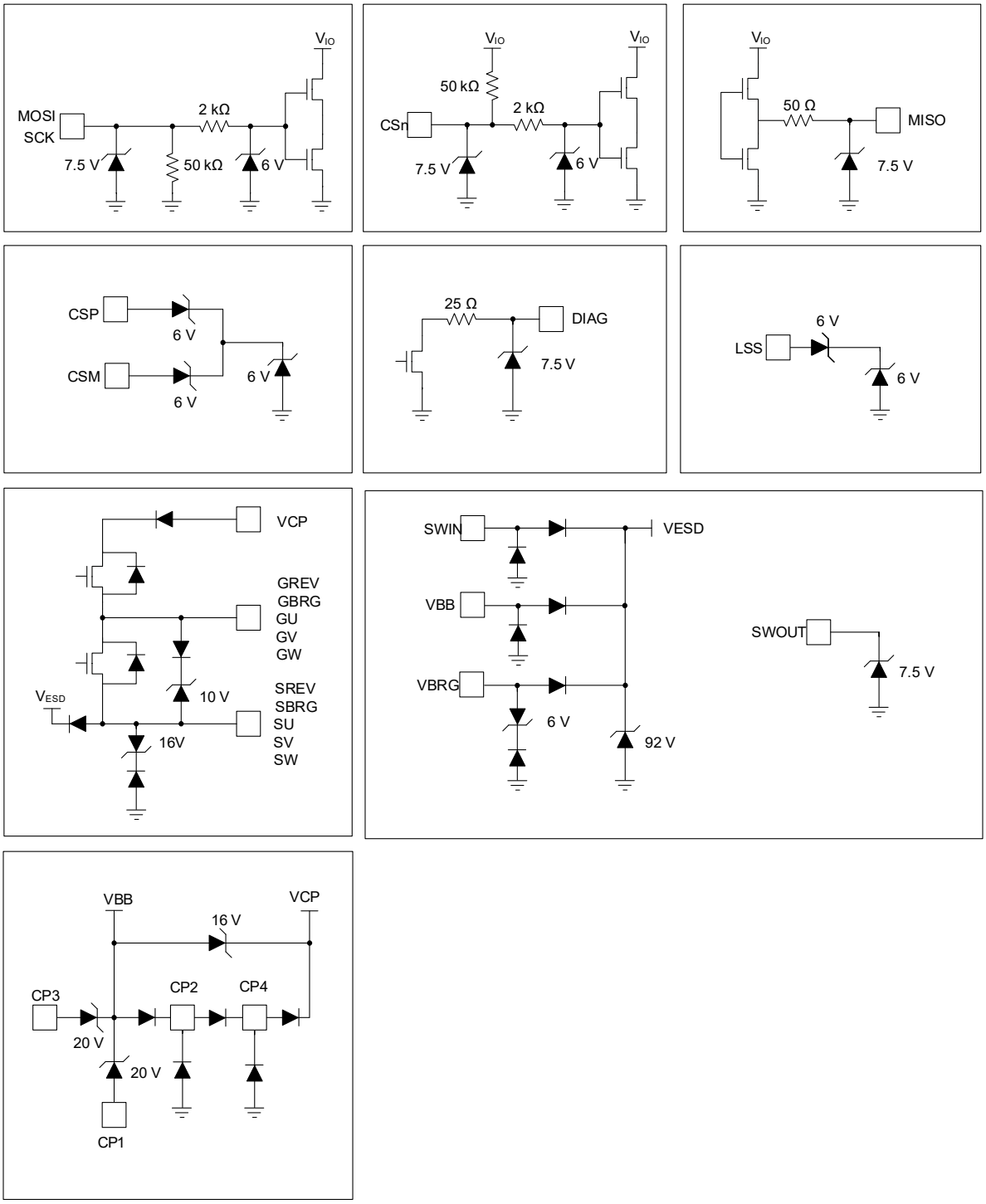
INPUT/OUTPUT STRUCTURES



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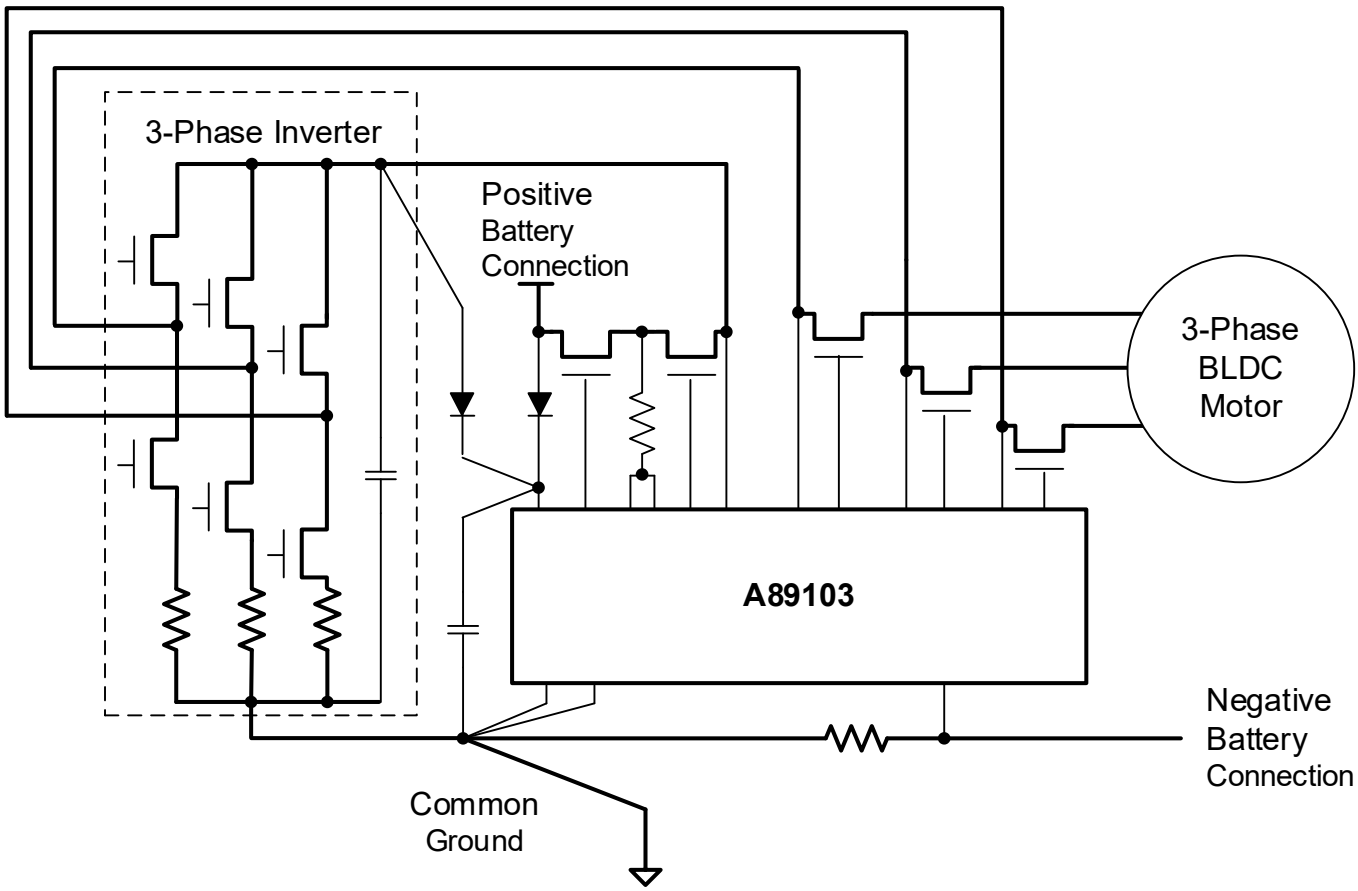
LAYOUT RECOMMENDATIONS

Careful consideration must be given to PCB layout when designing high-frequency, fast-switching, high-current circuits.

- The exposed thermal pad should be connected to the GND terminal.
- Minimize stray inductance by using short, wide copper tracks at the drain and source terminals of all power MOSFETs. This includes load lead connections to the input power bus. This minimizes voltages induced by fast switching of large load currents.
- Consider the addition of small (100 nF) ceramic decoupling capacitor across the source and drain of the power MOSFETs to limit fast transient voltage spikes caused by track inductance.
- Keep the gate discharge return connections as short as possible. Any inductance on these tracks causes negative transitions on the corresponding A89103 terminals, which may exceed the absolute maximum ratings. If this is likely, consider the use of clamping diodes to limit the negative excursion on these terminals with respect to the GND terminal.
- Supply decoupling, typically a 100 nF ceramic capacitor, should be connected between VBB and GND, as close to the A89103 terminals as possible. This is described in detail in the Application Information section.
- A gate-charge drive path or gate-discharge return path may carry a large transient current pulse. Therefore, the traces from Gx and Sx should be as short as possible to reduce the track inductance.



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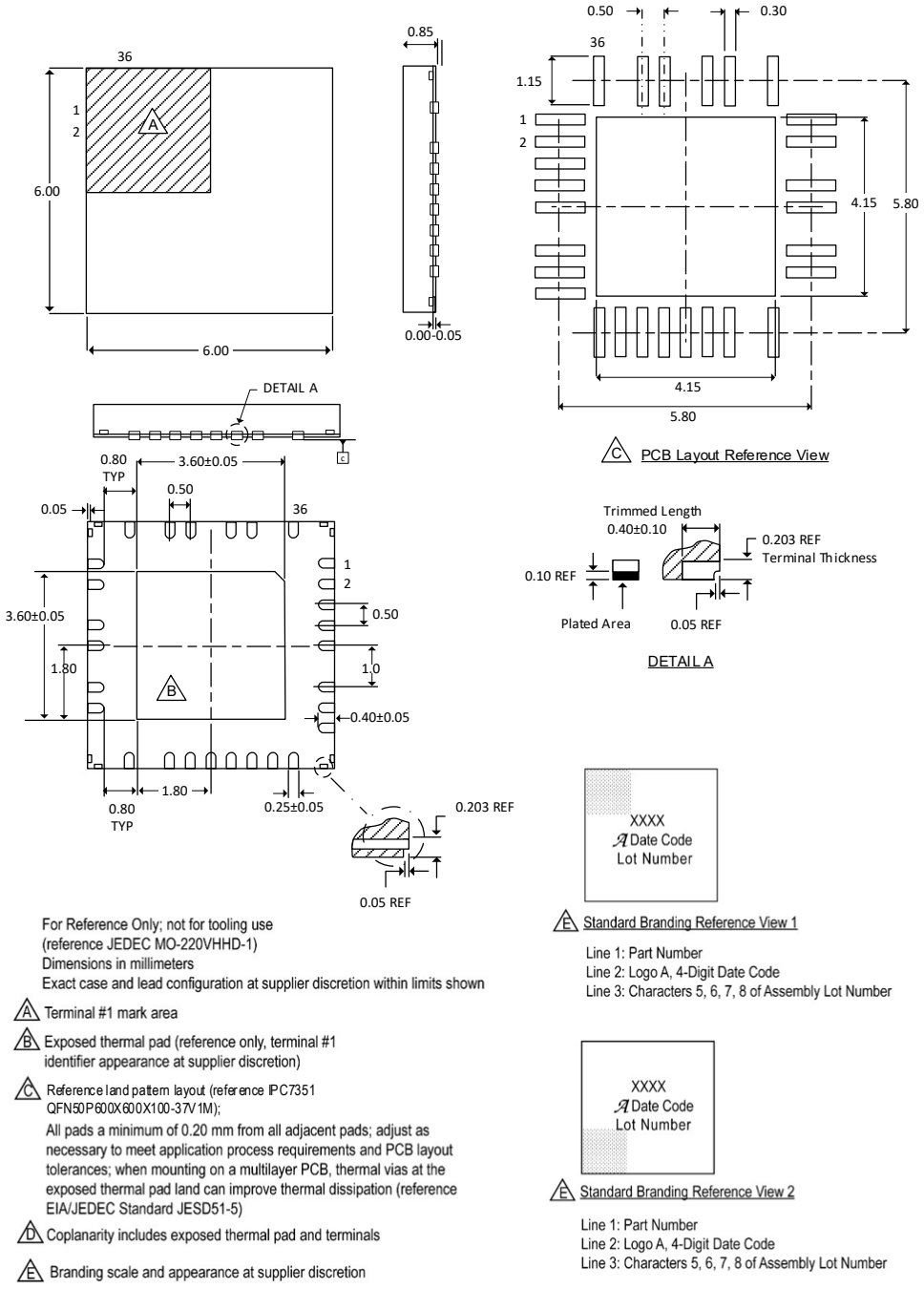
PACKAGE OUTLINE DRAWING



C PCB Layout Reference View

For Reference Only; not for tooling use
(reference JEDEC MO-220VHHD-1)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P600X600X100-37V1M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion

E Standard Branding Reference View 1
Line 1: Part Number
Line 2: Logo A, 4-Digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

E Standard Branding Reference View 2
Line 1: Part Number
Line 2: Logo A, 4-Digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Figure 46: Package EV, 28-Contact QFN with Exposed Pad

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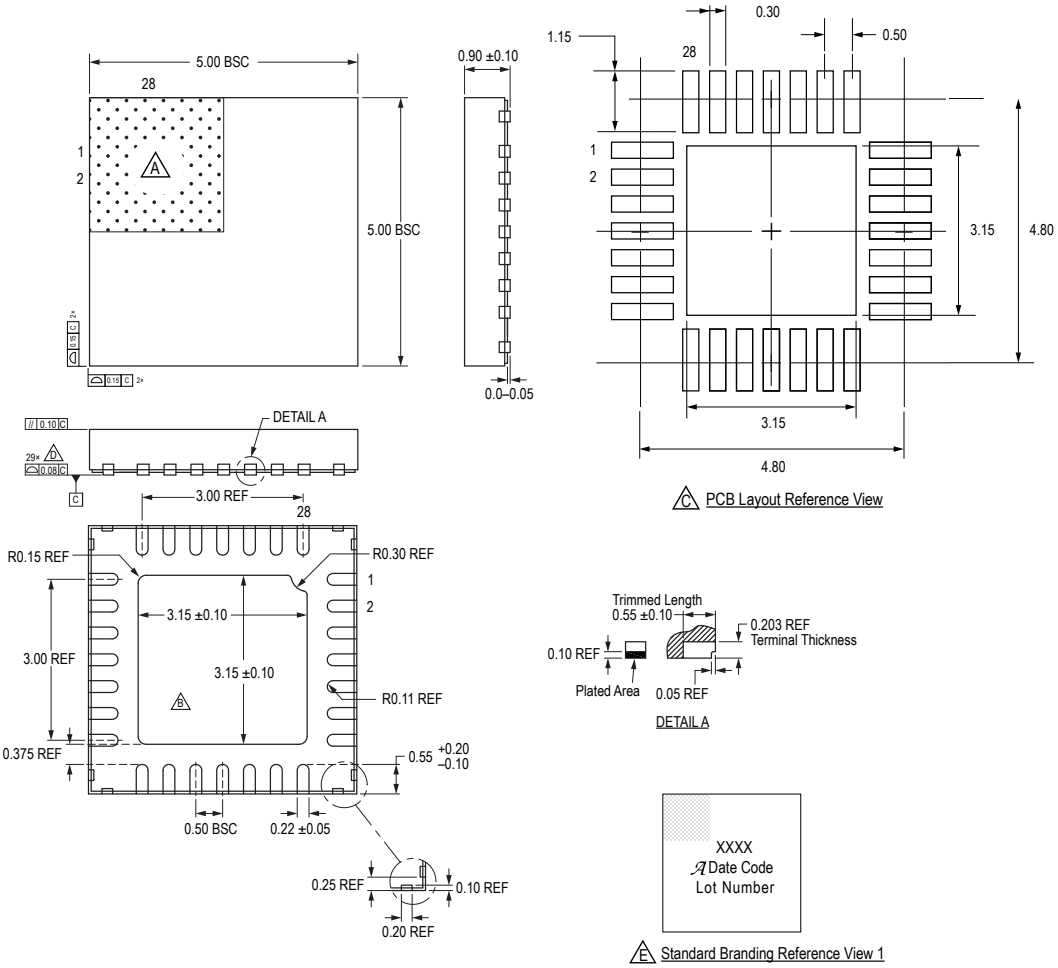
PACKAGE OUTLINE DRAWING

For Reference Only – Not For Tooling Use

(Reference Allegro DWG-0000378, Rev. 3 or JEDEC MO-220VHHD-1)
NOT TO SCALE
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown



C PCB Layout Reference View

E Standard Branding Reference View 1

Line 1: Part Number
Line 2: Logo A, 4-Digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

XXXX
Date Code
Lot Number

E Standard Branding Reference View 2

Line 1: Part Number
Line 2: Logo A, 4-Digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-29V1M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion

Figure 47: Package ET, 28-Contact QFN with Exposed Pad

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APPENDIX

Errata—Recommended Deglitch Filter Time Setting

DESCRIPTION

When overcurrent comparator thresholds of less than 63 mV are required and selected by the user, deglitch filter settings of 1000 ns and longer are recommended. If deglitch filter settings shorter than 500 ns are selected in combination with threshold voltages of 63 mV or less, false OCN/OCP triggering may occur due to noise. To avoid false triggers, filter settings of:

- 0 ns and 250 ns are not recommended for any comparator threshold setting
- 500 ns and 750 ns are only recommended for threshold voltages of 63 mV or greater
- 1000 ns (factory-programmed default value) or longer can be used for all comparator voltage thresholds.

DEVICES AFFECTED

- A89103-3
- A89103-5

SOLUTION

For comparator thresholds of less than 63 mV, OCPD [2:0] and OCND [2:0] must be set to 0xb100 (1000 ns) or higher. This prevents any unintended OCP or OCN comparator triggering. For deglitch filter settings of less than 0xb011 (750 ns) the comparator threshold must be set to 63 mV or higher.

NOTE: If the system is operating at 12 V, this issue is not present.

Current Datasheet

OPERATING CHARACTERISTICS: Valid at T_J = –40 to 150°C, V_{BB} = 4.5 to 85 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
OVERCURRENT PROTECTION						
OCP Comparator Threshold	V_{OCP}	OCP = 17	15	18	21	mV
		OCP = 63	59	64	69	mV
		OCP = 99	93	100	107	mV
		OCP = 127	118.8	128	137.5	mV
OCN Comparator Threshold	V_{OCN}	OCN = 17	–21	–18	–15	mV
		OCN = 63	–69	–64	–59	mV
		OCN = 99	–107	–100	–93	mV
		OCN = 127	–137.5	–128	–118.8	mV

Recommended Interpretation to Include Test Conditions for OCP/OCN Thresholds

OPERATING CHARACTERISTICS: Valid at T_J = –40 to 150°C, V_{BB} = 4.5 to 85 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
OVERCURRENT PROTECTION						
OCP Comparator Threshold	V_{OCP}	OCP = 17, OCPD [2:0] ≥ 0xb100	15	18	21	mV
		OCP = 63, OCPD [2:0] = 0xb100	59	64	69	mV
		OCP = 99, OCPD [2:0] = 0xb100	93	100	107	mV
		OCP = 127, OCPD [2:0] = 0xb100	118.8	128	137.5	mV
OCN Comparator Threshold	V_{OCN}	OCN = 17, OCND [2:0] ≥ 0xb100	–21	–18	–15	mV
		OCN = 63, OCND [2:0] = 0xb100	–69	–64	–59	mV
		OCN = 99, OCND [2:0] = 0xb100	–107	–100	–93	mV
		OCN = 127, OCND [2:0] = 0xb100	–137.5	–128	–118.8	mV

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Errata—SPI Watchdog Timeout Consideration

DESCRIPTION

When a short to ground occurs on the SCK input while the CSN input is high, a watchdog timeout expiration may not trigger. This is a known issue in the device and is planned to be corrected in a silicon revision with a minor change. A suitable datasheet update will be provided to remove this erratum after the change is complete. Little requalification to no requalification is expected with this change.

NOTE: If SCK is shorted to ground while CSn is low, a serial error is always detected, and a watchdog timeout is always triggered.

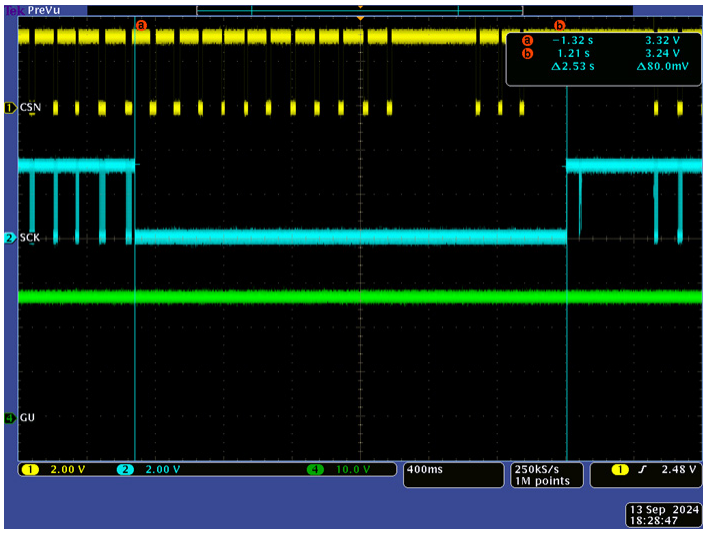

Figure 48: SCK Shorted to Ground, Without Occurrence of Watchdog Timeout

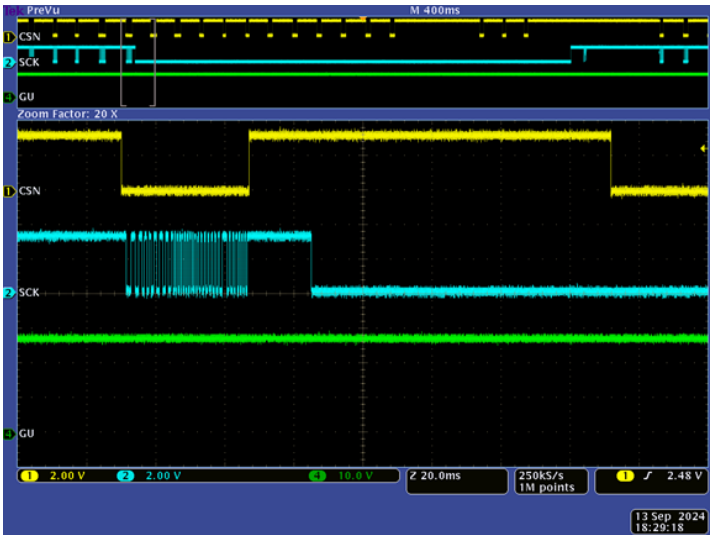

Figure 49: Short to GND Occurring When CSN is High (Zoomed-In View)

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Revision History

Number	Date	Description
–	October 31, 2023	Preliminary
1	January 3, 2024	Updated datasheet status to Final; updated Charge Pump Regulator section (page 17) and Package Drawing (page 74).
2	February 1, 2024	Removed “pending assessment” wording (page 1).
3	May 7, 2024	Minor editorial updates (pages, 11, 28, 40, 46), Updated Charge Pump Regulator wording (page 17), Cyclic Redundancy Check (pages 68, 69)
4	September 27, 2024	Corrected SPI watchdog timeout in WDT [2:0] configuration register (pages 42 and 46), corrected enable/disable serial register (page 45), and added errata appendix (pages 76 and 77).

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