

A81805 Demo Board

INTRODUCTION

The A81805 Demo Board is designed to aid system designers with evaluating the operation and performance of the A81805 and A81805-1 2.5 A synchronous buck regulators.

The A81805 Demo Board is a PCB that is available in two configurations: the A81805 with V_{OUT} of 3.3 V, and the A81805-1 with V_{OUT} of 5.0 V. The demo board will arrive with a mark on one of the two silkscreen boxes at the top right identifying the device for which the demo board is configured.

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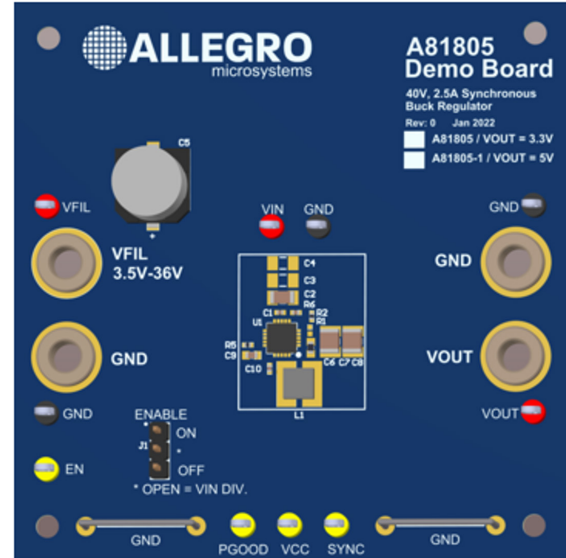


Figure 1: A81805 Demo Board

Table 1: A81805 Demo Board Configurations

Configuration Name	Part Number	V_{OUT}	f_{sw}	$I_{OUT Max}$
A81805 Version Demo Board	APEK81805KES-01-[MH or T]	3.3 V	2.2 MHz	2.5 A
A81805-1 Version Demo Board	APEK81805KES-01-[MH or T]-1	5.0 V	400 kHz	2.5 A

Table 2: General Specifications

Specification	Min	Nom	Max	Units
Absolute Maximum VIN Pin Voltage	-0.3	-	40	V
Absolute Maximum EN Pin Voltage	-0.3	-	40	V
Absolute Maximum SYNC Pin Voltage	-0.3	-	5.5	V
Operating Input Voltage Range	3.5	-	36	V
Output Voltage – A81805 Version Demo Board	-	3.3	-	V
Output Voltage – A81805-1 Version Demo Board	-	5.0	-	V
Maximum Output Current	-	2.5	-	A
Synchronous Frequency Range	0.4	-	2.5	MHz

GENERAL DESCRIPTION AND DEMO BOARD SETUP

This section provides instructions on proper setup and a basic overview of the configuration options and features of the demo board. The A81805 datasheet contains detailed information on the use and functionality of each IC pin and should be used in conjunction with this user manual.

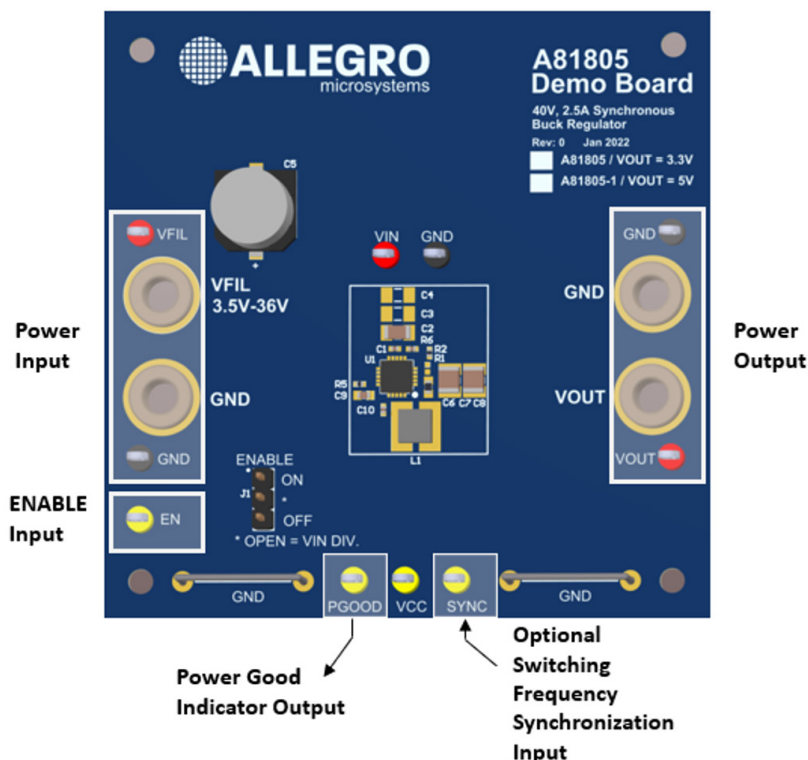


Figure 2: A81805 Demo Board Connections

Startup Procedure

Consult Figure 2 for details on interfacing hardware with the demo board. For more details on the demo board input and output connections, consult the Demo Board Inputs and Outputs section below.

For operation at lowest possible input voltage:

Step 1: Connect a suitable DC power supply to the VFIL and GND terminals. A suitable power supply will be able to provide the desired input voltage while sourcing a DC current of at least 3 A. Use **caution to avoid reversing the polarity when hooking up. Reversing the polarity on VFIL will result in a condition that exceeds VIN absolute maximum ratings and will likely damage the converter.**

Step 2: Connect the desired load to the VOUT and GND terminals. If an active electronic load is used, it may be necessary to apply the load after Step 4 to ensure proper operation of the active load.

Step 3: Set the ENABLE jumper to “ON” for converter operation at minimum input voltage or leave OPEN to use the *accurate enable* functionality.

Step 4: Increase the voltage at VFIL to 10 V. Verify that the output voltage is approximately:

- 3.3 V for A81805 Version Demo Board
- 5.0 V for A81805-1 Version Demo Board

The converter is now running. At this point, V_{IN} can be adjusted as desired. The maximum operating input voltage range is 36 V. The minimum operating input voltage is dependent upon the ENABLE jumper setting and the *accurate enable* resistor divider.

DEMO BOARD INPUTS AND OUTPUTS

Power Input

Connect a power supply using banana cables to the VFIL and GND through-hole banana jacks or with other suitable test leads to the VFIL and GND test points. VFIL is the power input to the board before the simple L-C input filter. Optionally, the VIN test point can be used to apply power directly to the VIN pin of the converter.

Power Output

Both versions of the demo board are capable of supplying 2.5 A of output current. For 2.5 A of continuous output current, a minimum input voltage of approximately 6.5 V for the A81805 Version Demo Board and approximately 7 V for the 81805-1 Version Demo Board is required. For consistent, stable converter operation, ensure the power supply can source 3 A of continuous current to the input of the demo board.

Switching Frequency and SYNC Input

Both the A81805 and A81805-1 have an internal oscillator that can generate the switching frequency. Additionally, they both have the capability of running from an external SYNC signal. If external synchronization is desired, a clock pulse can be applied to the SYNC test point on the demo board. However, erratic operation may occur if the FSET resistor (R1) is such that it sets the internal oscillator to a significantly different frequency than the externally applied synchronization signal. If external synchronization is desired, consult the datasheet for additional details on FSET selection and external synchronization.

PGOOD Output

The demo board has a PGOOD output that indicates the output voltage is in regulation. The datasheet provides details on the operation of the PGOOD output.

VCC Output

The demo board has a VCC test point which allows the user to monitor the output of the internal VCC regulators. No external loads should be applied to VCC.

Enable Jumper Configuration

The external circuitry around the Enable pin, EN, is tri-functional. If a shunt is placed in the “ON” position (shorting the upper two pins of J1) then EN is tied to VIN, forcing the converter to operate any time VIN is above UVLO. The Undervoltage Lockout section of the datasheet provides more details on VIN UVLO.

If a shunt is placed in the “OFF” position (shorting the lower two pins of J1), then EN is pulled to GND and the converter will remain disabled.

If no shunt is installed on J1, then EN is biased by a resistor divider from VIN to GND, and the *accurate enable* function of the converter is employed. The resistor divider sets the converter to turn on at a specific input voltage. The standard demo board setup will result in converter turn-on when V_{IN} reaches approximately 7.2 V. The VIN turn-on voltage can be adjusted by varying R3, R4, or both.

Table 3: ENABLE Jumper Configuration

Jumper	EN State	Description
ON	HIGH	Converter is on when $V_{IN} \geq V_{IN\ UVLO}$.
OFF	LOW	Converter remains disabled.
OPEN	PROPORTIONAL to VIN	Converter turns on once VIN reaches the set turn-on threshold.

Refer to the datasheet for detailed information about EN pin functionality and implementation of the *accurate enable* functionality.

THERMAL PERFORMANCE

The following figures show the thermal performance of both the A81805 and A81805-1 versions of the Demo Board.

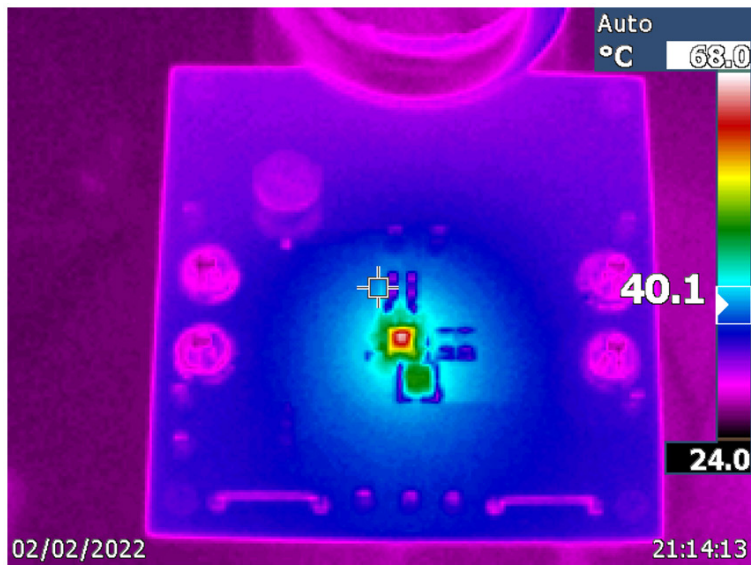


Figure 3: A81805 Version Demo Board Thermal Behavior.
 $V_{IN} = 13\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 2.5\text{ A}$.

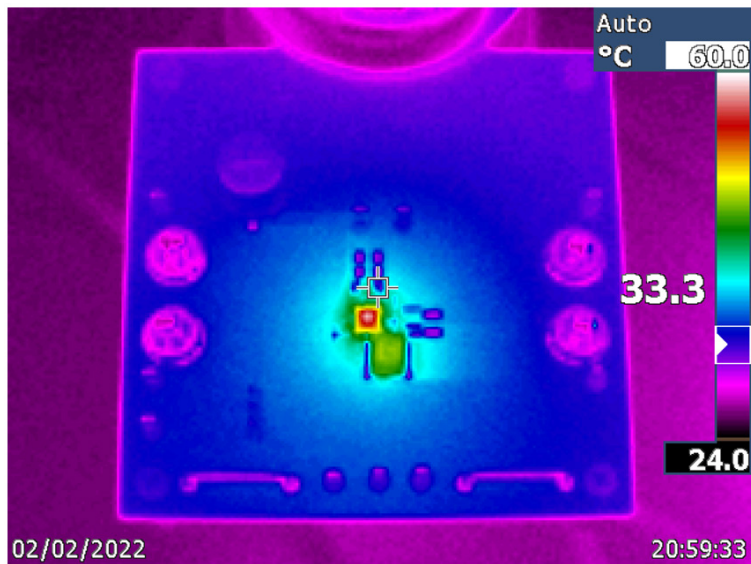


Figure 4: A81805-1 Version Demo Board Thermal Behavior.
 $V_{IN} = 13\text{ V}$, $V_{OUT} = 5.0\text{ V}$, $I_{OUT} = 2.5\text{ A}$.

EMI PERFORMANCE

The following figures show the EMI performance of the A81805-1 Version Demo Board under nominal V_{IN} conditions and maximum load. This does not reflect the overall EMI signature of an entire system containing the A81805 or A81805-1 but does show that the converter is capable of easily meeting even the stringent automotive CISPR25 Class 5 EMC standards.

NOTE: Allegro is not an accredited EMC laboratory. The information presented here is provided for reference only.

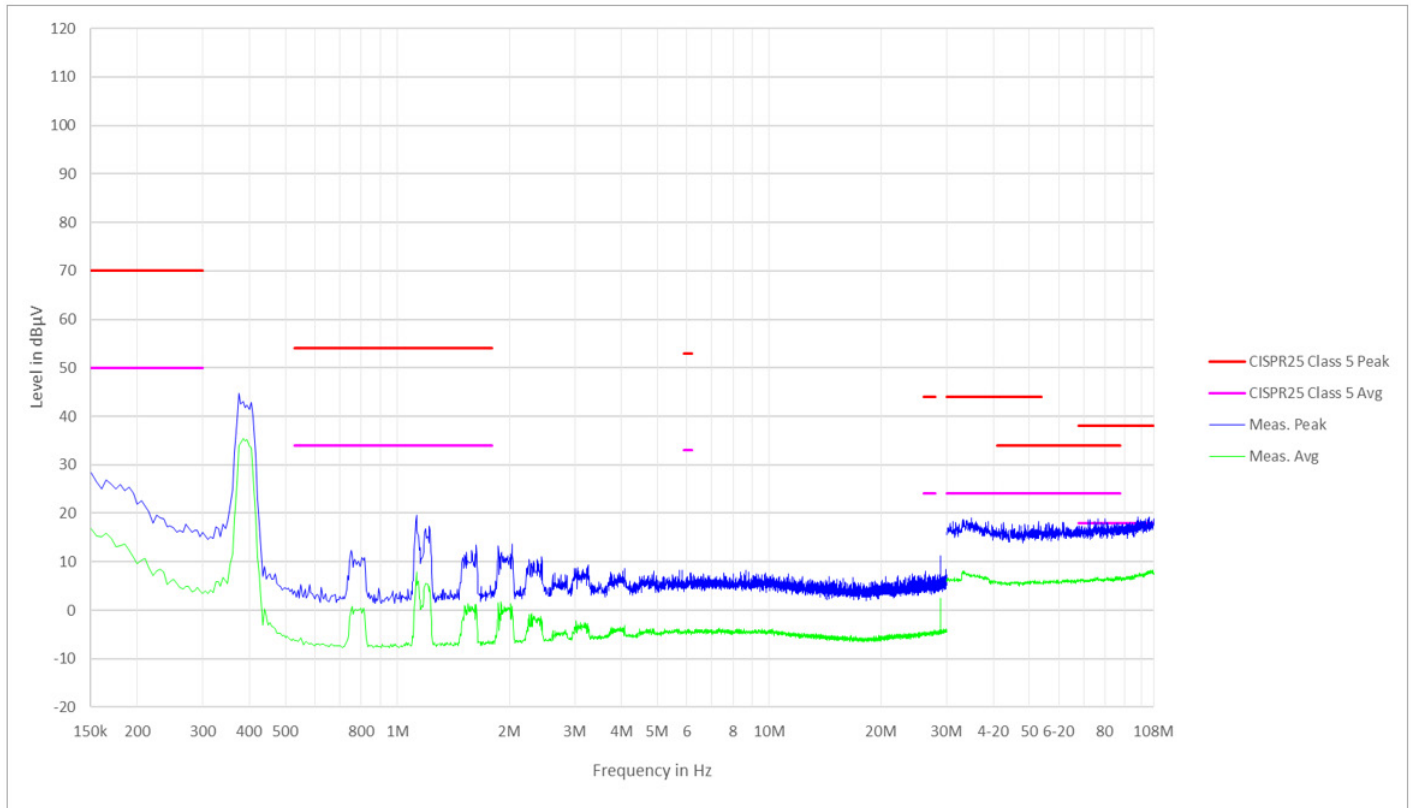


Figure 5: Conducted Emissions (150 kHz - 108 MHz)

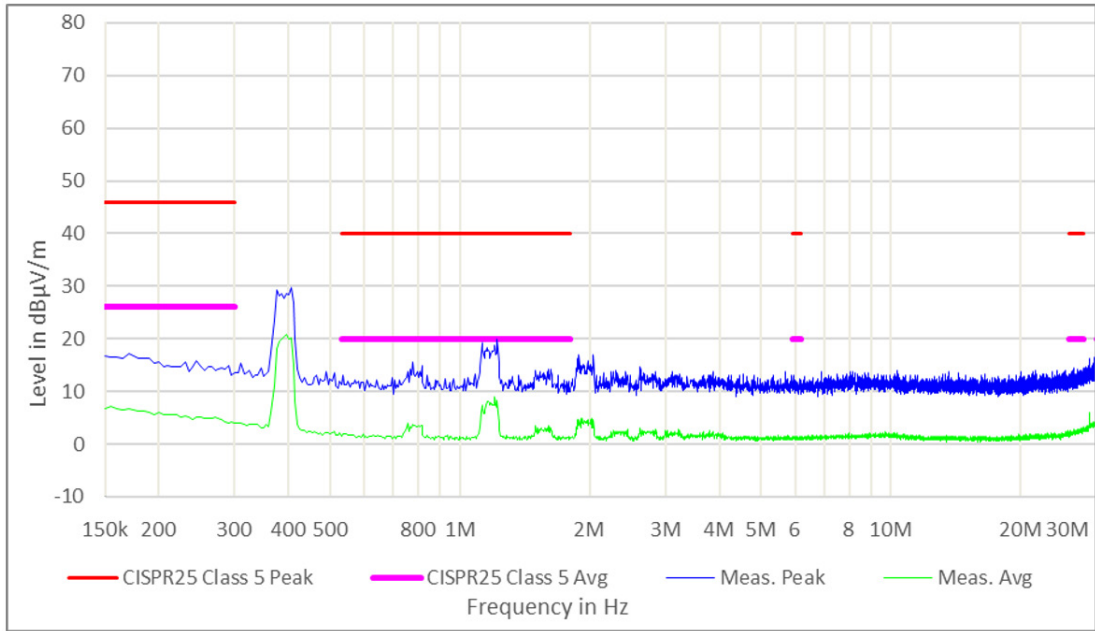


Figure 6: Radiated Emissions (150 kHz - 30 MHz)

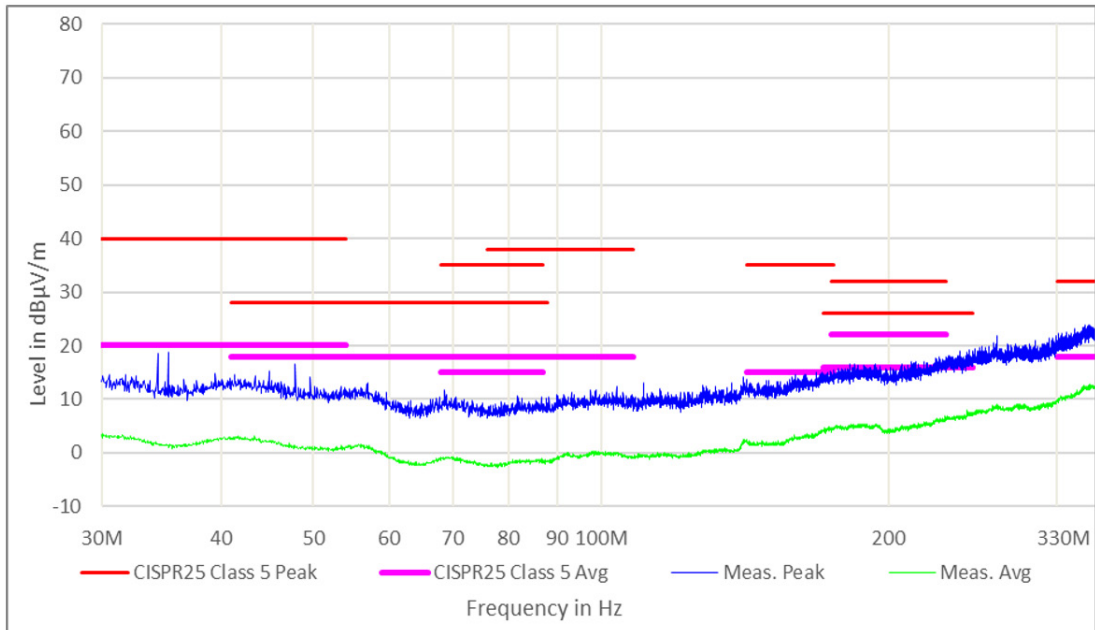


Figure 7: Radiated Emissions (30 MHz - 330 MHz)

A81805 VERSION DEMO BOARD SCHEMATIC

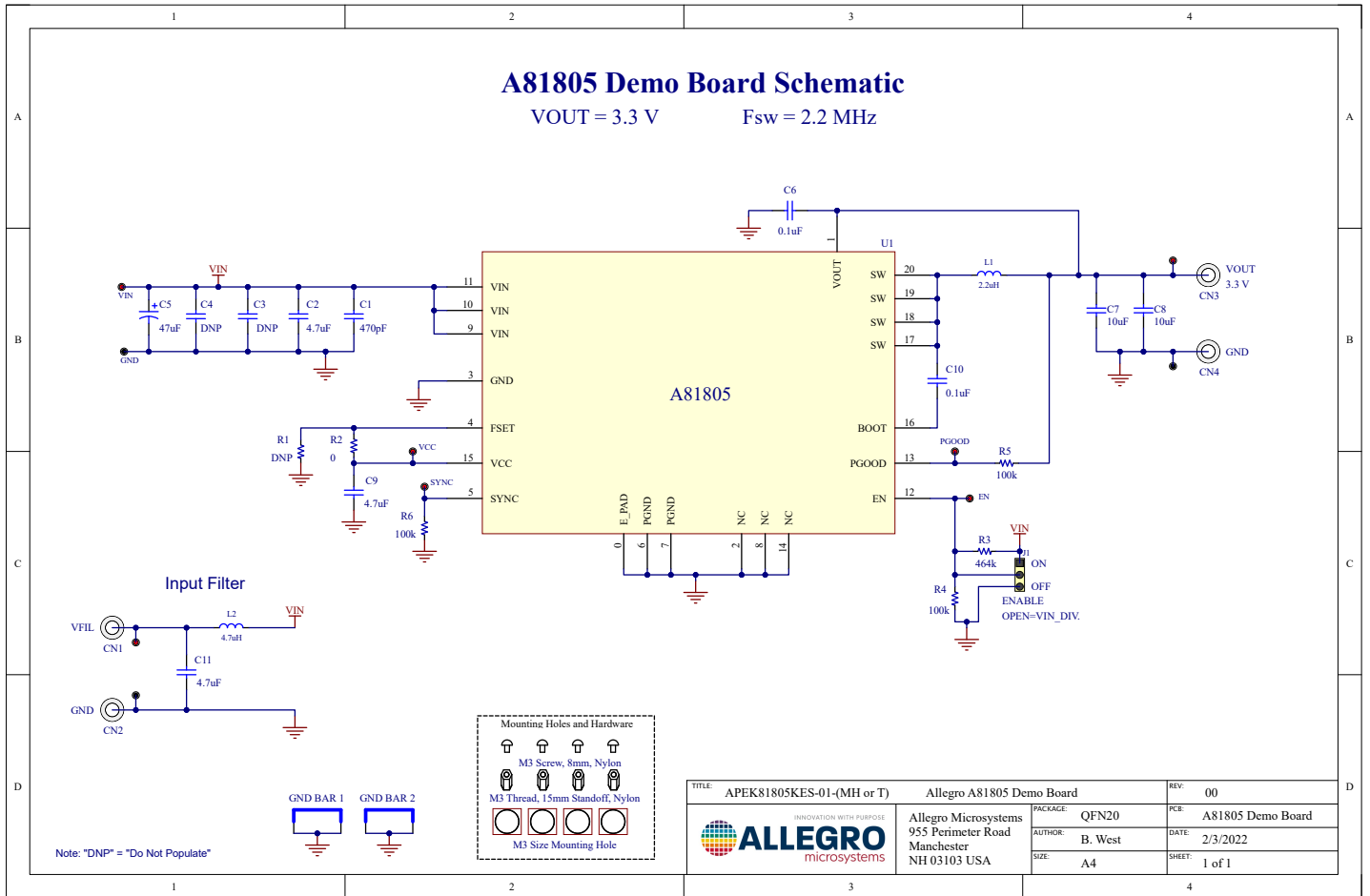


Figure 8: A81805 Version Demo Board Schematic

Table 4: A81805 Version Demo Board Bill of Materials

ELECTRICAL COMPONENTS						
Designator	Quantity	Comment	Description	Manufacturer	Manufacturer Part Number	Label on PCB
C1	1	470 pF	CAP, CER, 470 pF, 50 V, C0G, 0402	Kemet	C0603C471J5RACAUTO	C1
C2	1	4.7 μF	CAP, CER, 4.7 μF, 50 V, X7R, 1206	TDK	CGA4J1X7R1H475K125AC	C2
C3, C4	0	DNP				C3, C4
C5	1	47 μF	CAP, ALUM, 47 μF, 20%, 50 V, SMD	Nichicon	UBC1H470MNS1GS	C5
C6	1	0.1 μF	CAP, CER, 0.1 μF, 50 V, X7R, 0603	Murata	GCM155R71H104KE02J	C6
C7, C8	2	10 μF	CAP, CER, 10 μF, 16 V, X7R, 1210	Kemet	C1210C106K4RACTU	C7, C8
C9	1	4.7 μF	CAP, CER, 4.7 μF, 16 V, X7R, 0603	Murata	GCJ21BR71C475KA01L	C9
C10	1	0.1 μF	CAP, CER, 0.1 μF, 50 V, X7R, 0402	Murata	GCM155R71H104KE02J	C10
C11	1	4.7 μF	CAP, CER, 4.7 μF, 50 V, X7R, 1210	Murata Electronics	GRM32ER71H475KA88K	C11
L1	1	2.2 μH	FIXED IND 2.2 μH, 5.6 A, 35.2 mΩ, SMD	Coilcraft	XAL4020-222ME	L1
L2	1	4.7 μH	FIXED IND 4.7 μH, 4.5 A, 60 mΩ, SMD	Vishay Dale	IHL2020CZER4R7M11	L2
R1	0	DNP	RESISTOR, 1%, 0402	Panasonic		R1
R2	1	0 Ω	RESISTOR, 0 Ω, 1/10 W, 1%, 0402	Panasonic	ERJ-2GE0R00X	R2
R3	1	464 kΩ	RESISTOR, 464 kΩ, 1/10 W, 1%, 0402	Panasonic	ERJ-2RKF4643X	R3
R4, R5, R6	3	100 kΩ	RESISTOR, 100 kΩ, 1/10 W, 1%, 0402	Panasonic	ERJ-2RKF1003X	R4, R5, R6
U1	1	A81805	ALLEGRO IC, 40 V, 2.5 A, SYNCHRONOUS BUCK CONVERTER WITH 6 μA QUIESCENT CURRENT	Allegro MicroSystems	A81805KESJSR	U1
OTHER COMPONENTS						
Designator	Quantity	Comment	Description	Manufacturer	Manufacturer Part Number	Label on PCB
CN1	1	VFIL	BANANA JACK - NON-INSULATED, 0.218" LENGTH	Keystone Electronics	575-4	VFIL
CN2, CN4	2	GND	BANANA JACK - NON-INSULATED, 0.218" LENGTH	Keystone Electronics	575-4	GND
CN3	1	VOUT	BANANA JACK - NON-INSULATED, 0.218" LENGTH	Keystone Electronics	575-4	VOUT
J1	1	Header 1x3	CONN HEADER VERT 3 POS 2.54 MM	Würth Elektronik	61300311121	ENABLE
MS1, MS2, MS3, MS4	4	Standoff Screw	PAN HEAD SCREW, M3 X 8 MM, NYLON	Würth Elektronik	97790803111	N/A - mount in corner hole
PCB	1	Circuit Board	A81805 DEMO BOARD REV: 0 JAN 2022			N/A
STND1, STND2, STND3, STND4	4	Standoff	HEX STANDOFF, M3, NYLON	Keystone Electronics	25512	N/A - mount in corner hole
GND BAR1, GND BAR2	2	GND Connections	GND BAR : TINNED 18 AWG COPPER BUS WIRE			GND
EN, PGOOD, SYNC, VCC	4	Testpoint	PC TEST POINT, MULTIPURPOSE, YELLOW	Keystone Electronics	5014	EN, PGOOD, SYNC, VCC
VFIL, VIN, VOUT	3	Testpoint	PC TEST POINT, MULTIPURPOSE, RED	Keystone Electronics	5010	VFIL, VIN, VOUT
GND, GND	2	Testpoint	PC TEST POINT, MULTIPURPOSE, BLACK	Keystone Electronics	5011	GND

A81805-1 VERSION DEMO BOARD SCHEMATIC

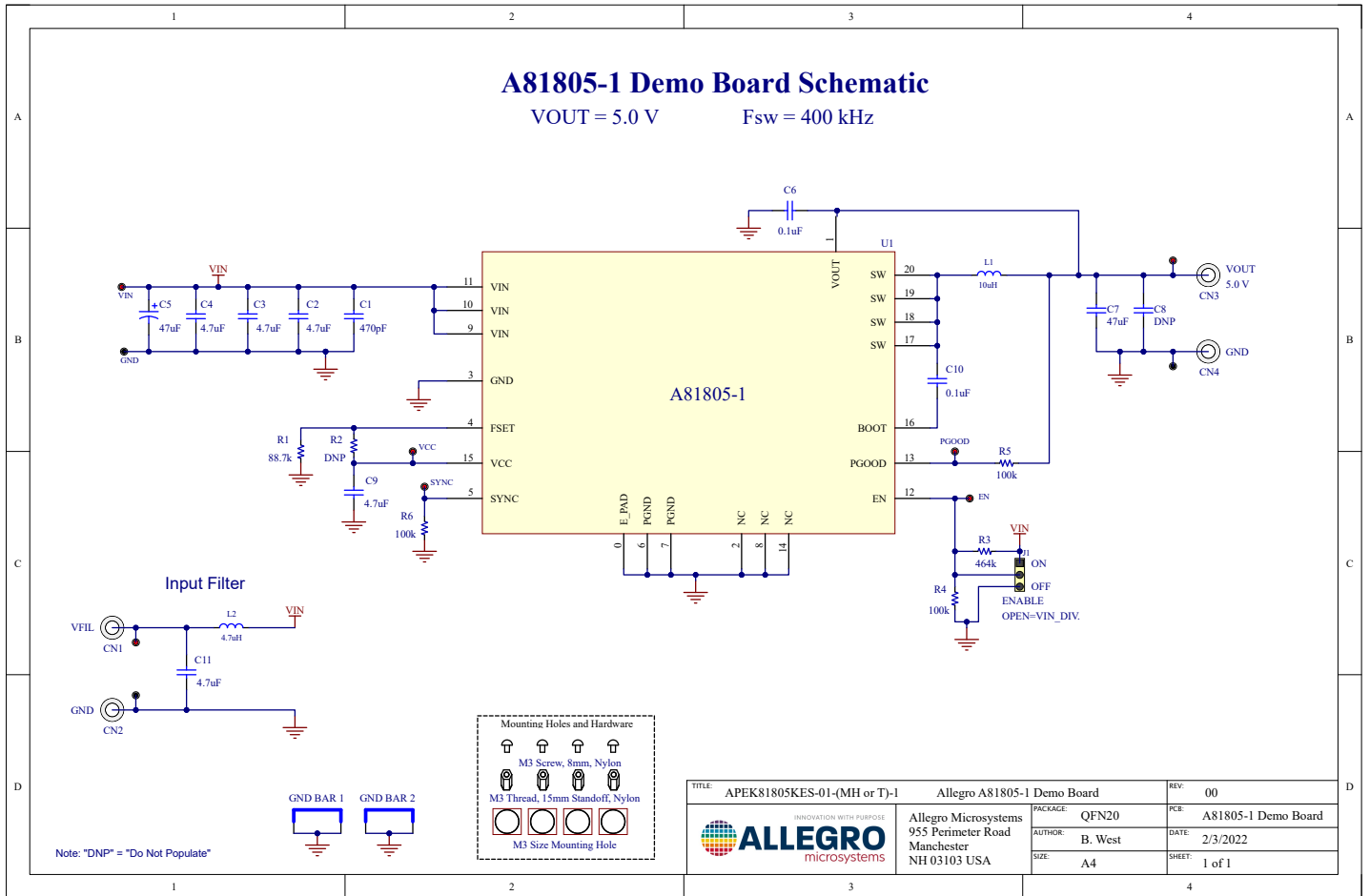


Figure 9: A81805-1 Version Demo Board Schematic

Table 5: A81805-1 Version Demo Board Bill of Materials

ELECTRICAL COMPONENTS						
Designator	Quantity	Comment	Description	Manufacturer	Manufacturer Part Number	Label on PCB
C1	1	470 pF	CAP, CER, 470 pF, 50 V, C0G, 0402	Kemet	C0603C471J5RACAUTO	C1
C2, C3, C4	3	4.7 µF	CAP, CER, 4.7 µF, 50 V, X7R, 1206	TDK	CGA4J1X7R1H475K125AC	C2
C5	1	47 µF	CAP, ALUM, 47 µF, 20%, 50 V, SMD	Nichicon	UBC1H470MNS1GS	C5
C6	1	0.1 µF	CAP, CER, 0.1 µF, 50 V, X7R, 0603	Murata	GCM155R71H104KE02J	C6
C7	1	47 µF	CAP, CER, 47 µF, 16 V, X5R, 1210	Murata	GRM32ER61C476ME15L	C7
C8	0	DNP	CAP, CER 1210			C8
C9	1	4.7 µF	CAP, CER, 4.7 µF, 16 V, X7R, 0603	Murata	GCJ21BR71C475KA01L	C9
C10	1	0.1 µF	CAP, CER, 0.1 µF, 50 V, X7R, 0402	Murata	GCM155R71H104KE02J	C10
C11	1	4.7 µF	CAP, CER, 4.7 µF, 50 V, X7R, 1210	Murata Electronics	GRM32ER71H475KA88K	C11
L1	1	10 µH	FIXED IND, 10 µH, 4.9 A, 40.9 mΩ, SMD	Coilcraft	XAL5050-103ME	L1
L2	1	4.7 µH	FIXED IND, 4.7 µH, 4.5 A, 60 mΩ, SMD	Vishay Dale	IHL2020CZER4R7M11	L2
R1	1	88.7 kΩ	RESISTOR, 88.7 kΩ, 1/10 W, 1%, 0402	Panasonic	ERJ-2RKF8872X	R1
R2	0	DNP	RESISTOR, 1%, 0402	Panasonic		R2
R3	1	464 kΩ	RESISTOR, 464 kΩ, 1/10W, 1%, 0402	Panasonic	ERJ-2RKF4643X	R3
R4, R5, R6	3	100 kΩ	RESISTOR, 100 kΩ, 1/10W, 1%, 0402	Panasonic	ERJ-2RKF1003X	R4, R5, R6
U1	1	A81805-1	ALLEGRO IC, 40 V, 2.5 A, SYNCHRONOUS BUCK CONVERTER WITH 6uA QUIESCENT CURRENT	Allegro MicroSystems	A81805KESJSR-1	U1
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CN3	1	VOUT	BANANA JACK - NON-INSULATED, 0.218" LENGTH	Keystone Electronics	575-4	VOUT
J1	1	Header 1x3	CONN HEADER VERT 3POS 2.54 MM	Wurth Elektronik	61300311121	ENABLE
MS1, MS2, MS3, MS4	4	Standoff Screw	PAN HEAD SCREW, M3 X 8 MM, NYLON	Wurth Elektronik	97790803111	N/A - MOUNT IN CORNER HOLE
PCB	1	Circuit Board	A81805 DEMO BOARD REV: 0 JAN 2022			N/A
STND1, STND2, STND3, STND4	4	Standoff	HEX STANDOFF, M3, NYLON	Keystone Electronics	25512	N/A - MOUNT IN CORNER HOLE
GND BAR1, GND BAR2	2	GND Connections	GND BAR : TINNED 18 AWG COPPER BUS WIRE			GND
EN, PGOOD, SYNC, VCC	4	Testpoint	PC TEST POINT, MULTIPURPOSE, YELLOW	Keystone Electronics	5014	EN, PGOOD, SYNC, VCC
VFIL, VIN, VOUT	3	Testpoint	PC TEST POINT, MULTIPURPOSE, RED	Keystone Electronics	5010	VFIL, VIN, VOUT
GND, GND	2	Testpoint	PC TEST POINT, MULTIPURPOSE, BLACK	Keystone Electronics	5011	GND

PCB LAYOUT

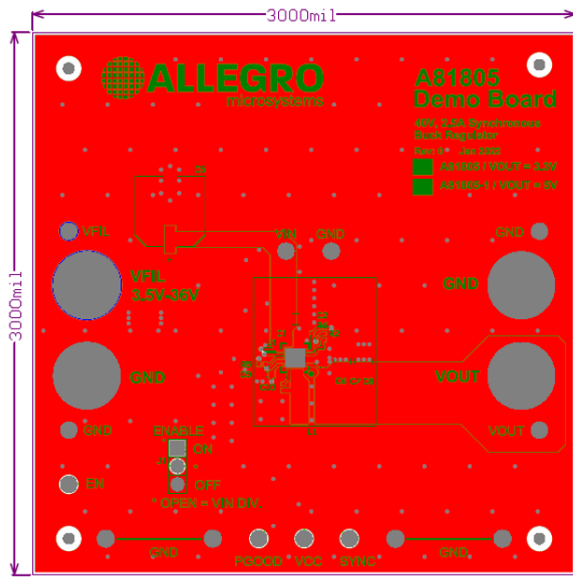


Figure 10: Top Layer

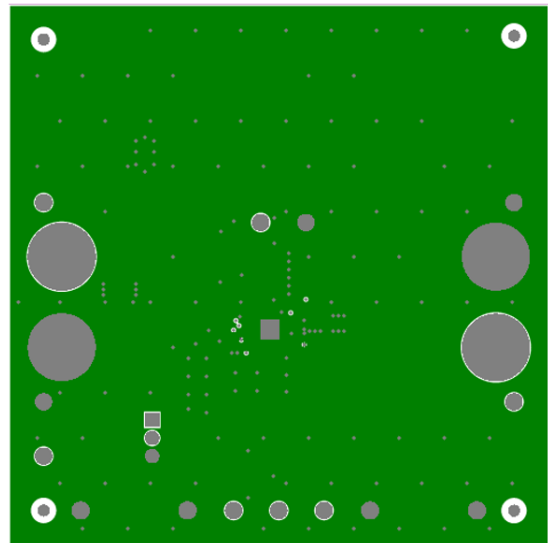


Figure 12: Inner Layer 1

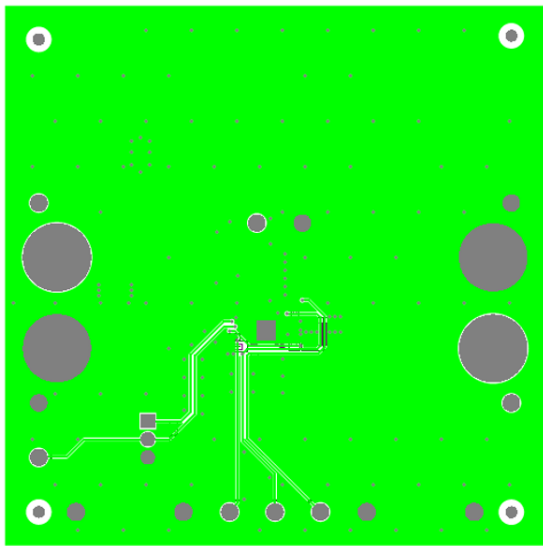


Figure 11: Inner Layer

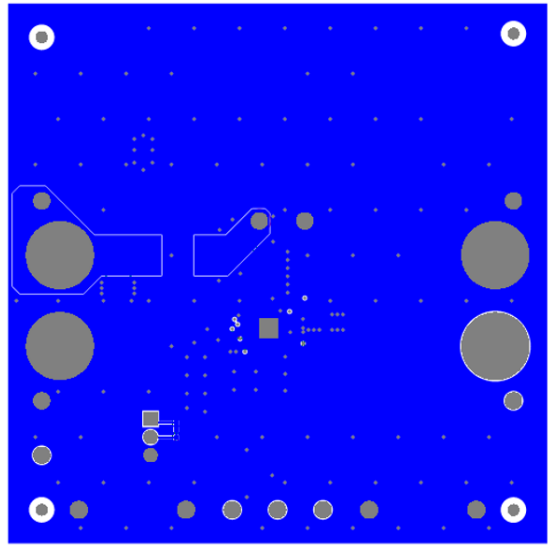


Figure 13: Bottom Layer

Revision History

Number	Date	Description
–	February 8, 2022	Initial release

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