APEK85110KNH-01-T-MH

AHV85110 Evaluation Board User Guide

DESCRIPTION

The Allegro MicroSystems Half-Bridge Driver-Switch APEK85110KNH-01-T-MH is a demonstration board containing two APEK85110KNH GaN FET drivers and two GaN FETs configured in a half-bridge configuration.

FEATURES

The APEK85110KNH-01-T-MH can be used to perform double-pulse tests, or to interface the half bridge to an existing LC power section, both as shown below.

The isolated APEK85110KNH driver does not require secondary side power or bootstrap components. Gate drive power is supplied to the secondary side from the primary side supply voltage V_{DRV}. The amplitude of the gate drive can be varied by changing V_{DRV} between 10.8 V and 13.2 V.

EVALUATION BOARD CONTENTS

- APEK85110KNH-01-T-MH evaluation board.

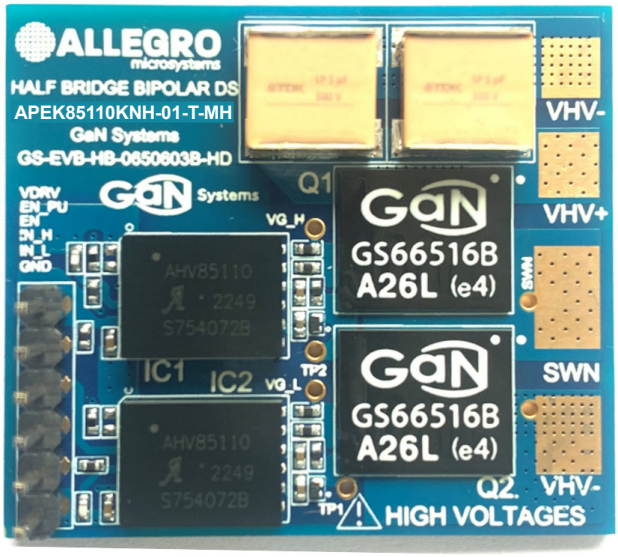

Figure 1: AHV85110 Evaluation Board

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DANGER

DO NOT TOUCH THE BOARD WHEN IT IS ENERGIZED AND ALLOW ALL COMPONENTS TO DISCHARGE COMPLETELY PRIOR HANDLING THE BOARD.

HIGH VOLTAGE CAN BE EXPOSED ON THE BOARD WHEN IT IS CONNECTED TO POWER SOURCE. EVEN BRIEF CONTACT DURING OPERATION MAY RESULT IN SEVERE INJURY OR DEATH.

Ensure that appropriate safety procedures are followed. This evaluation kit is designed for **engineering evaluation in a controlled lab environment and should be handled by qualified personnel ONLY.** Never leave the board operating unattended.

WARNING

Some components can be hot during and after operation. **There is NO built-in electrical or thermal protection on this evaluation kit.** The operating voltage, current, and component temperature should be monitored closely during operation to prevent device damage.

CAUTION

This product contains parts that are susceptible to damage by electrostatic discharge (ESD). Always follow ESD prevention procedures when handling the product.

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USING THE EVALUATION BOARD

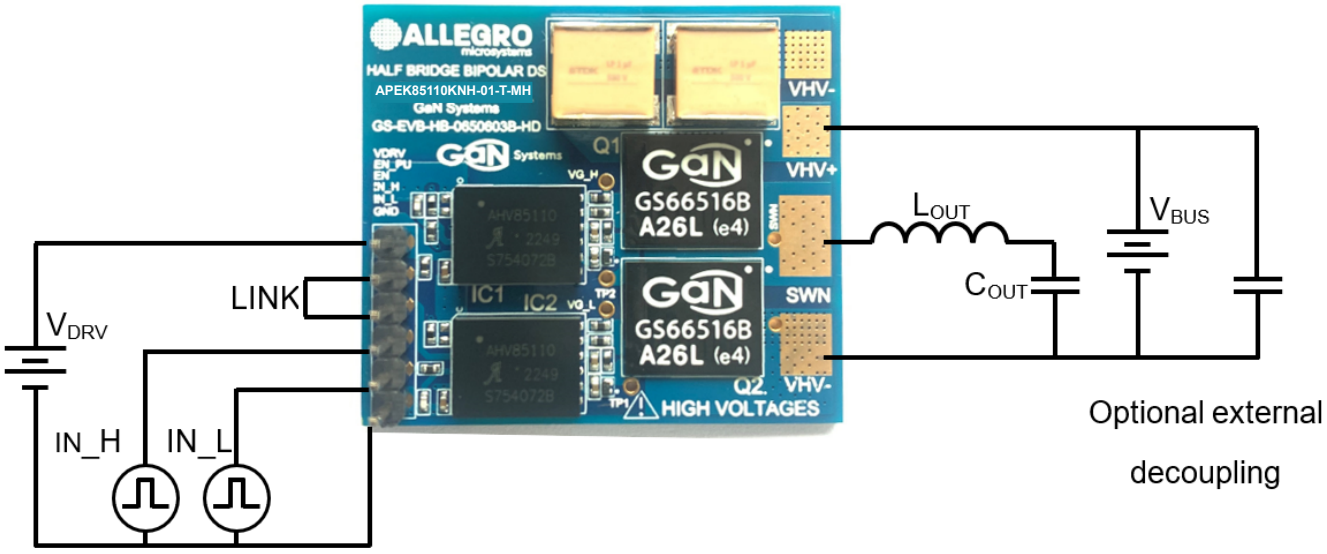

Figure 2: APEK85110KNH-01-T-MH Quick Start

1. Apply V_{DRV} = 12 V.
2. Link pins EN_PU and EN (if not using external Enable control).
3. Apply input gate signals, with adequate dead time, to the IN_L and IN_H inputs.
4. Convenient test points are located on the test board as shown in Figure 5 below. A suitable differential oscilloscope should be used to monitor the high-side gate signal from VGH to VSW.

GATE PULL-UP AND PULL-DOWN RESISTORS

The APEK85110KNH gate driver has independent output pins for the gate pull-up and gate pull-down allowing control of the turn-on and turn-off rise and fall times.

The default values for these resistors are:

OUTPU: R1 and R5 = 10 Ω

OUTPD: R3 and R7 = 1 Ω

These values can be modified to suit the application.

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ENABLE SEQUENCE

The APEK85110KNH has an open-drain enable pin (EN) to facilitate a system-level wired-AND startup.

When the enable pin is externally pulled low, the driver is forced into a low-power mode. The driver output is pulled low in this mode. In the event of an internal fault condition, such as UVLO or normal startup delay, the EN pin is actively pulled low internally by the driver.

During normal operation, the pin is released by the driver, and must be pulled high with an external pull-high resistor. This functionality can be used by the PWM controller as an indication that it can start sending IN pulses to the driver. It is typically wired-AND with the controller enable pin as shown in Figure 3 below.

The APEK85110KNH-01-T-MH EVM board provides direct access to the EN pin on connector CONN1. Internally the board contains a 100 kΩ pull-up resistor connected from VDRV to the EN_PU pin on connector CONN1—see schematic in Figure 12. If external control of the enable function is not required, pins EN and EN_PU must be linked together on CONN1 to make use of the internal 100 kΩ pull-up resistor to enable the driver. If the EN pin is left floating, the drivers will not respond to INL or INH input signals.

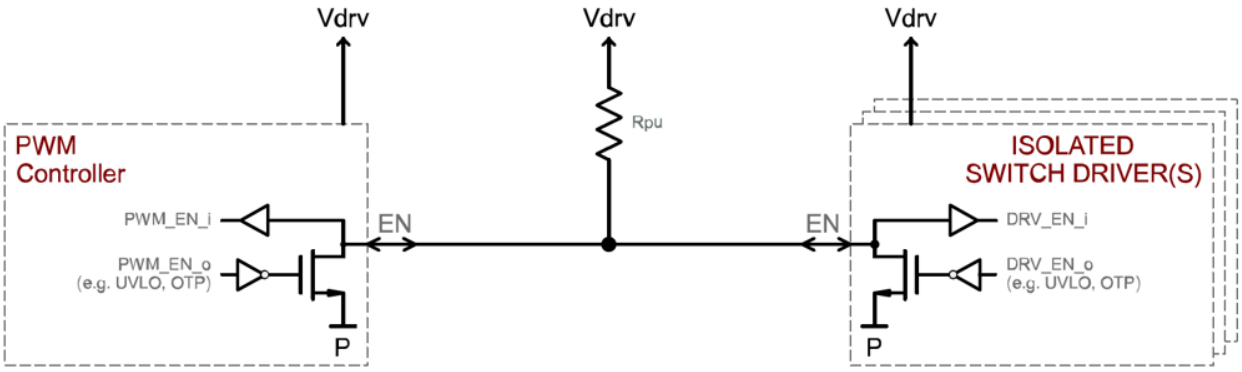

Figure 3: APEK85110KNH Wired-AND Enable

When the EN pin is pulled low, the driver output is disabled, and pulls down the OUTPD pin, regardless of the IN pin level (high or low). The driver goes to a low-power standby mode, and the isolated V_{SEC} bias rail is allowed to discharge. The rate of decay of V_{SEC} depends on the value of the C_{SEC} capacitor.

When the EN pin is subsequently pulled high, the driver will re-enable, and the isolated V_{SEC} bias rail will start to recharge.

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START SEQUENCE

The startup sequence of the APEK85110KNH is shown in Figure 4 below. Time t_{START} is defined as the time after which V_{DRV} reaches the UVLO rising level to the APEK85110KNH releasing the EN internal pull-down.

Any PWM signal applied to IN must remain low until V_{DRV} > UV threshold to avoid parasitic charging of the V_{DRV} rail through the IN pin internal ESD structures.

After V_{DRV} exceeds the UV enable threshold, a startup time delay t_{START} is required to charge V_{SEC} and allow all internal circuits to initialize and stabilize. During t_{START}, any IN signal inputs are ignored. EN internal pull-down will remain active during t_{START}, and will disable (i.e., go open-drain) only when V_{DRV} has reached its UVLO voltage level, all on-chip voltages are stabilized, and the internal t_{START} timer has elapsed. Thus, the EN pin can be used via a shared EN line to flag when t_{START} has elapsed, and the driver is ready to respond to PWM signals at the IN pin, as outlined above.

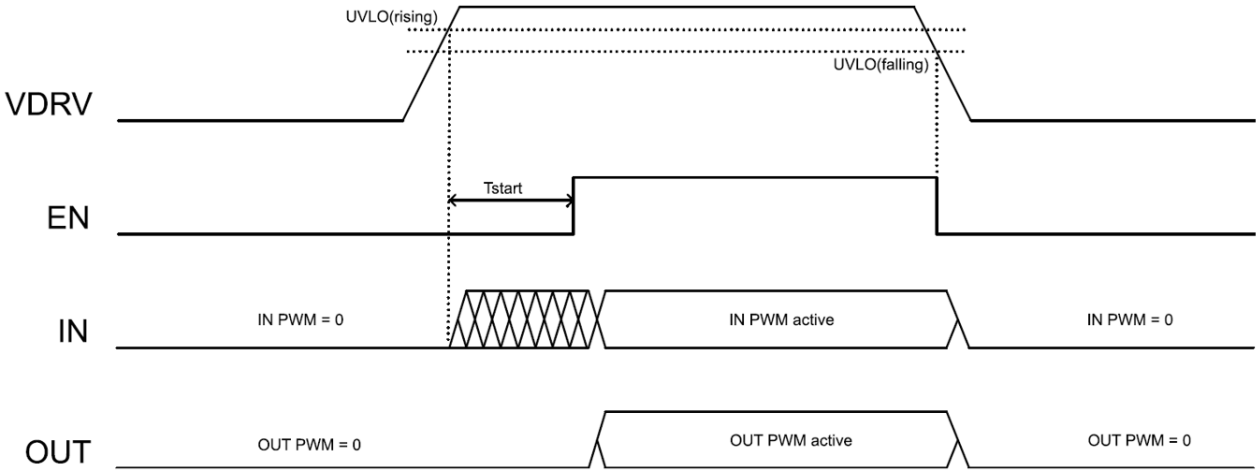

Figure 4: APEK85110KNH Startup Sequence

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MEASUREMENT POINTS

The APEK85110KNH-01-T-MH EVM contains convenient test points for monitoring the high- and low-side gate drives as well as the switch node as shown in Figure 5 below.

When measuring V_{GS_H}, use a differential probe with suitable ratings for the applied bus voltage. The APEK85110KNH-01-T-MH EVM uses a bipolar gate drive arrangement as shown in Figure 6 below. When measuring V_{GS}, both gate drives are measured relative to the source of their associated GaN FET. Therefore, the off-state voltage will be negative.

It is important to use a low-inductance scope probe ground lead as shown to avoid pickup of spurious switching noise.

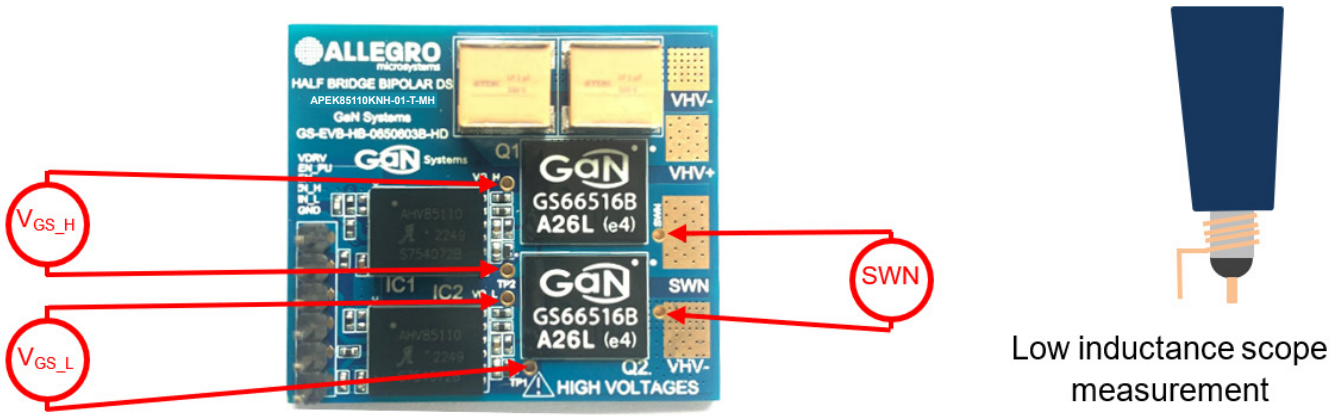

Figure 5: Measurements Points

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BIPOLAR GATE DRIVE

Due to the high rate of change of voltages and currents in power switching circuits, unwanted inductor currents and capacitor voltage drops can be created.

One such example is the false turn-on of a FET due to a dv/dt event. In a half-bridge circuit, after the low-side FET has been turned off and a suitable dead-time elapsed, the high-side FET is turned on. This produces a rapidly changing switch node voltage at the drain of the low-side FET. This voltage will produce a capacitor current:

$$i_{C_{GD}} = C_{GD} \frac{dV_{DS\_L}}{dt}$$

flowing in the gate-drain capacitance, C_{GD}, and driver output. It will cause the voltage on the gate of the low-side FET to rise. If this voltage spike peaks beyond the threshold voltage V_{TH}, the FET will conduct. Considering that the high-side FET is also conducting, this can result in a potentially destructive shoot-through event.

The APEK85110KNH-01-T-MH EVM uses a bipolar gate drive arrangement which is useful to mitigate against the effects of gate-drain capacitor currents. The secondary supply voltage V_{SEC} is a function of the primary supply voltage V_{DRV}. The zener diode, C_{R1}, will regulate the positive turn-on voltage of the GaN FET. During the turn-off period, the gate voltage will be negative with a value of:

$V_{GS\_OFF} = V_{SEC} - V_{ZENER}$. V_{SEC} is typically 9 V.

This negative V_{GS_OFF} voltage allows more margin before the threshold voltage can be reached.

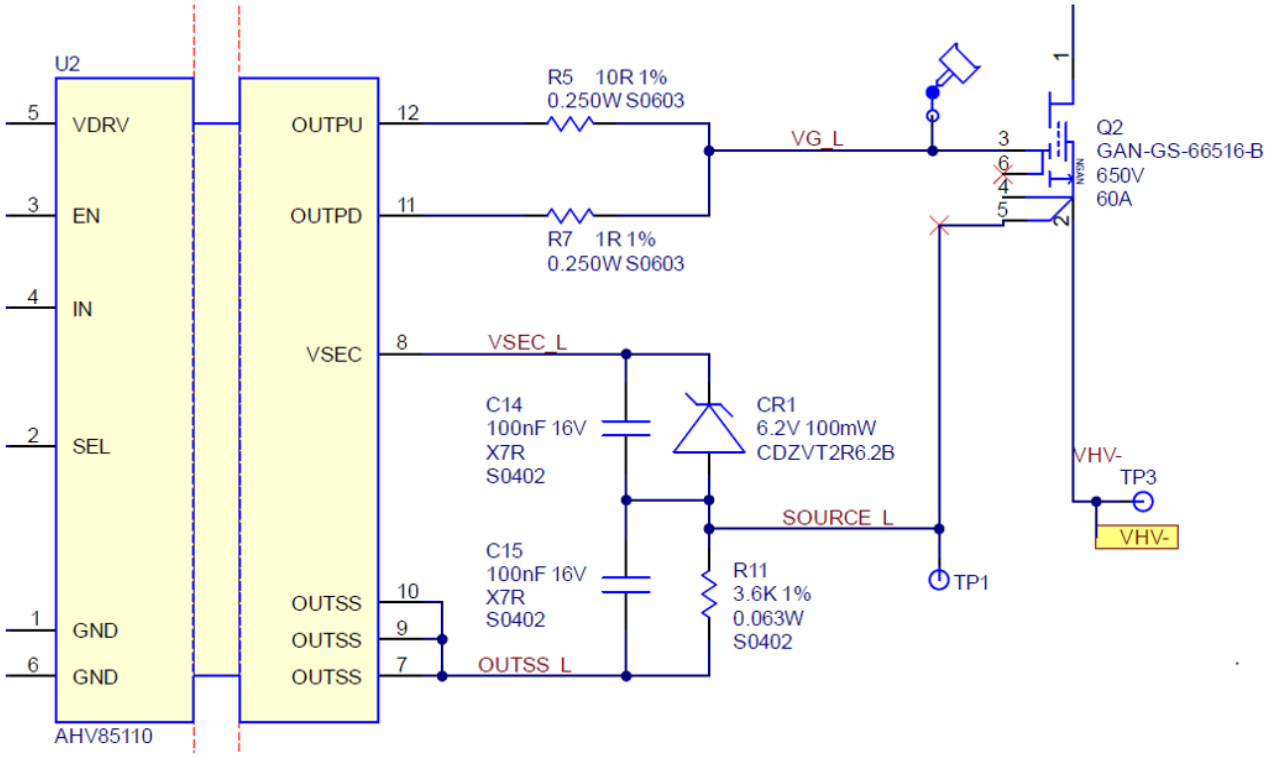

Figure 6: Bipolar Gate Drive Schematic

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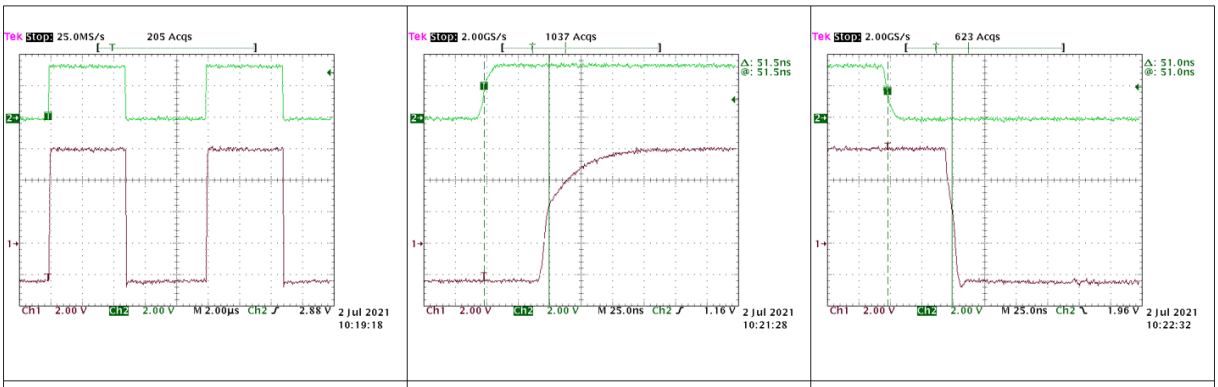
PROPAGATION DELAY

- V_{DRV} = 12 V
- Input = 100 kHz
- R_{PU} = 10 Ω, R_{PD} = 1 Ω
- Power train unloaded. That is, VHV+ = 0 V.



CH2: Low-side driver input **CH1:** Low-side driver (IC2) output wrt VHV-	**CH2:** Low-side driver input **CH1:** Low-side driver (IC2) output wrt VHV-	**CH2:** Low-side driver input **CH1:** Low-side driver (IC2) output wrt VHV-
Low-Side Driver Output	**Typical Turn-On Propagation Delay**	**Typical Turn-Off Propagation Delay**

Figure 7: Typical Driver Output at 100 kHz

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DOUBLE-PULSE TEST

The double-pulse test is used to evaluate the switching characteristics of a power switch under hard switching but in a safe manner.

For a low-side switch, the setup is as shown below:

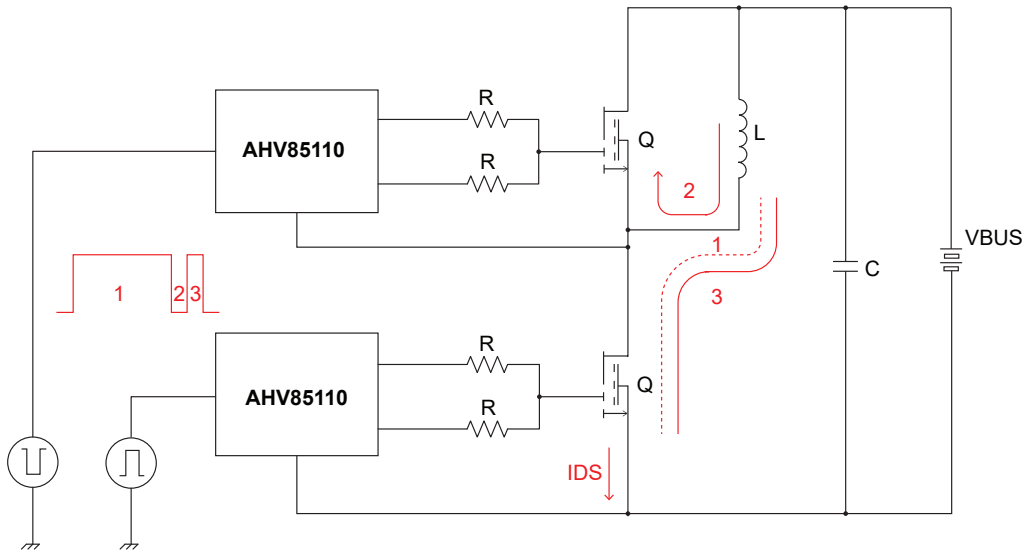

Figure 8: Double-Pulse Test

The low-side switch is driven with two pulses as shown below. The high-side switch can be held off or driven with the inverse of the low-side gate switch (with adequate dead time).

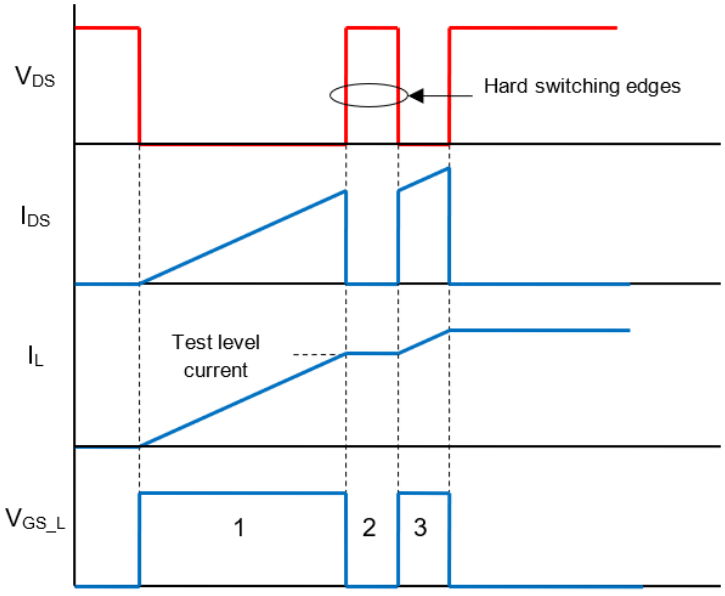

Figure 9: Double-Pulse Test Waveforms

An inductor is placed in parallel with the high-side switch. The goal of this inductor is to establish the test level current in the low-side switch at the end of the first on pulse (1). The magnitude of the test level current at the end of period 1 is given by:

$$I_L = V_{BUS} \frac{t_{ON\_1}}{L}$$

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During period 2, the inductor current will naturally decay. The duration of period 2 should not be so long that inductor current deviates significantly from the desired test level.

During period 3, the inductor current will again rise. Period 3 should not be so long that the inductor current rises to an excessive level.

The falling edge of pulse 1 is used to examine the hard turn off characteristics of the switch. The rising edge of pulse 3 is used to examine the hard turn on characteristics of the switch. By only applying these two pulses, the switches are only on for a very short time and should not overheat.

DOUBLE PULSE TEST RESULTS

DPT Result 100 V, 15 A

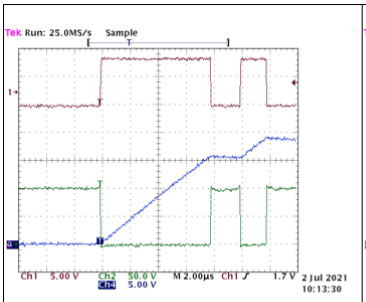	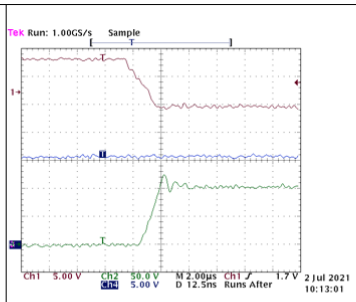	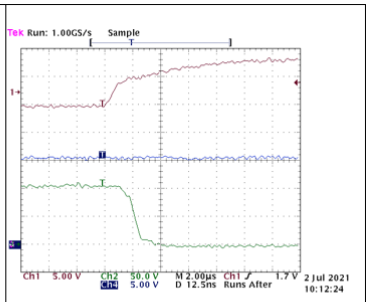
CH1 (Red): Low side output wrt VHV- **CH2 (Green):** Switch Node (500 MHz Probe) **CH4 (Blue):** Inductor Current (1 A/V)	**CH1 (Red):** Low side output wrt VHV- **CH2 (Green):** Switch Node (500 MHz Probe) **CH4 (Blue):** Inductor Current (1 A/V)	**CH1 (Red):** Low side output wrt VHV- **CH2 (Green):** Switch Node (500 MHz Probe) **CH4 (Blue):** Inductor Current (1 A/V)
DPT Overview	**DPT Hard Switching Turn-Off**	**DPT Hard Switching Turn-On Time Base (12.5 ns/div)**

Figure 10: DPT 100 V, 15 A

DPT Result 400 V, 62 A

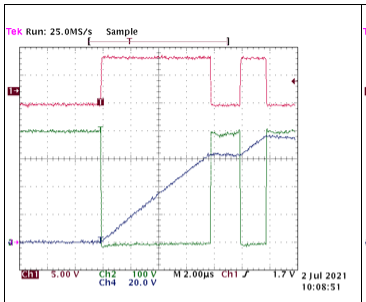	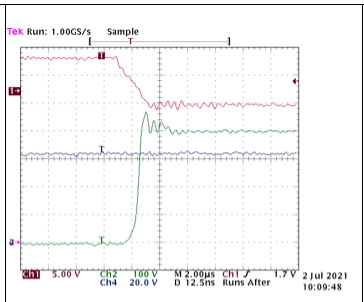	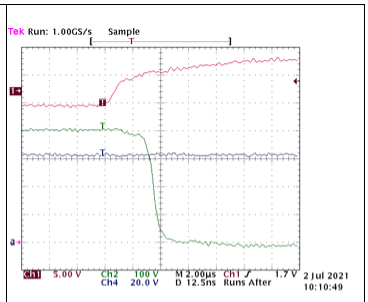
CH1 (Red): Low-side output wrt VHV- **CH2 (Green):** Switch Node (500 MHz Probe) **CH4 (Blue):** Inductor Current (1 A/V)	**CH1 (Red):** Low-side output wrt VHV- **CH2 (Green):** Switch Node (500 MHz Probe) **CH4 (Blue):** Inductor Current (1 A/V)	**CH1 (Red):** Low-side output wrt VHV- **CH2 (Green):** Switch Node (500 MHz Probe) **CH4 (Blue):** Inductor Current (1 A/V)
DPT Overview	**DPT Hard Switching Turn Off**	**DPT Hard Switching Turn-On Time Base (12.5 ns/div)**

Figure 11: DPT 400 V, 62 A

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SCHEMATIC

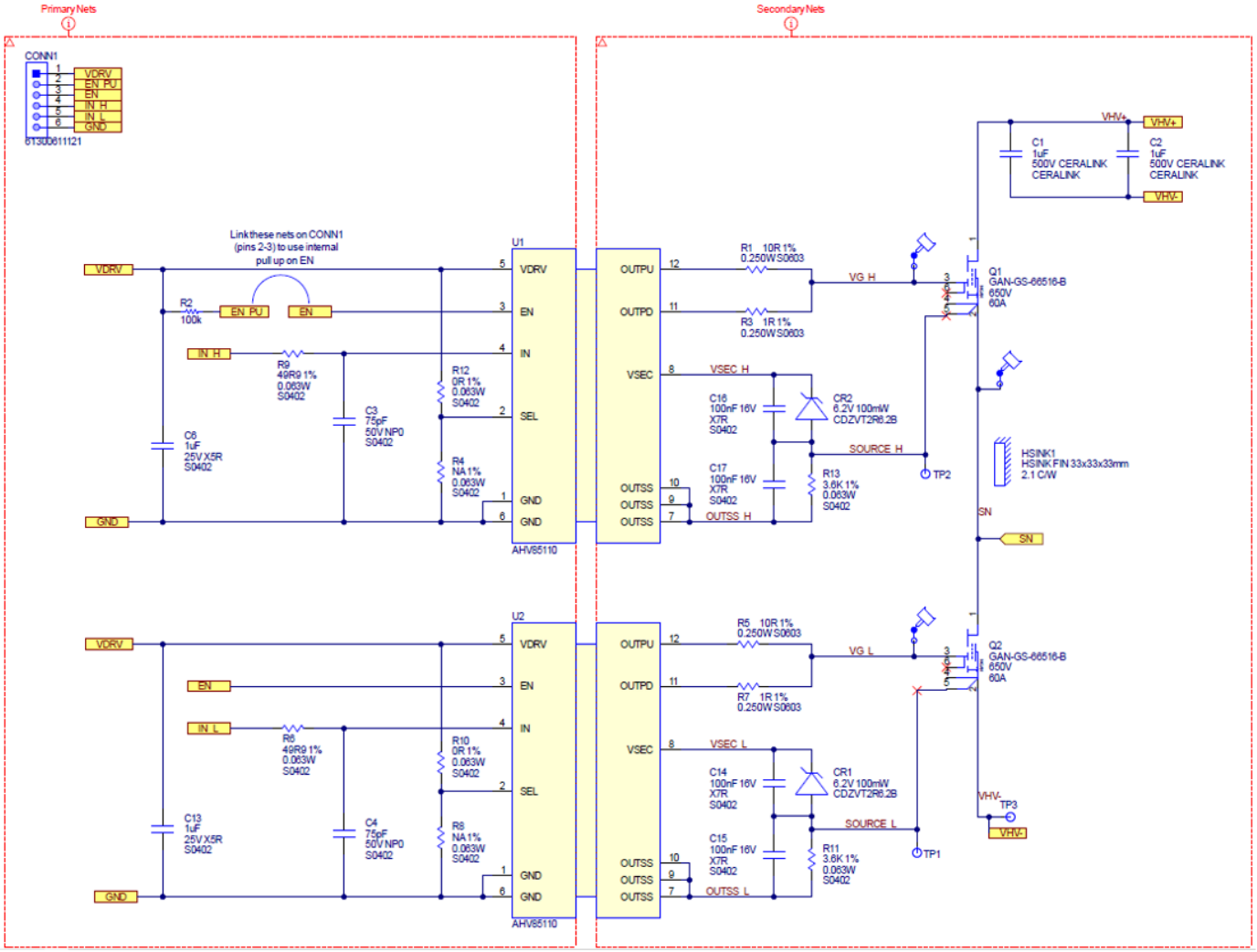

Figure 12: APEK85110KNH-01-T-MH Schematic

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PCB LAYOUT

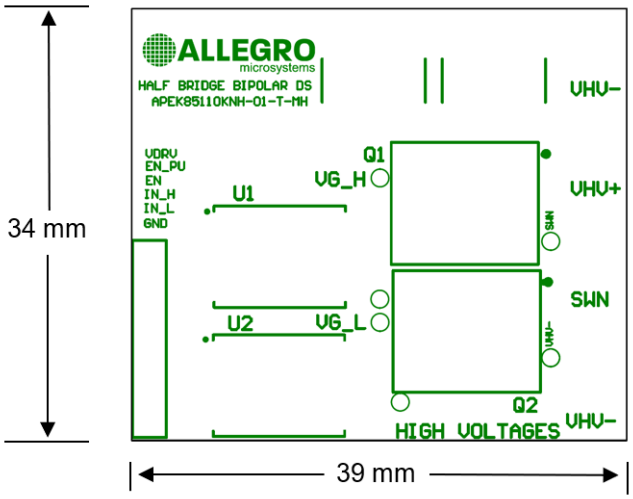

Figure 13: APEK85110KNH-01-T-MH Top Overlay

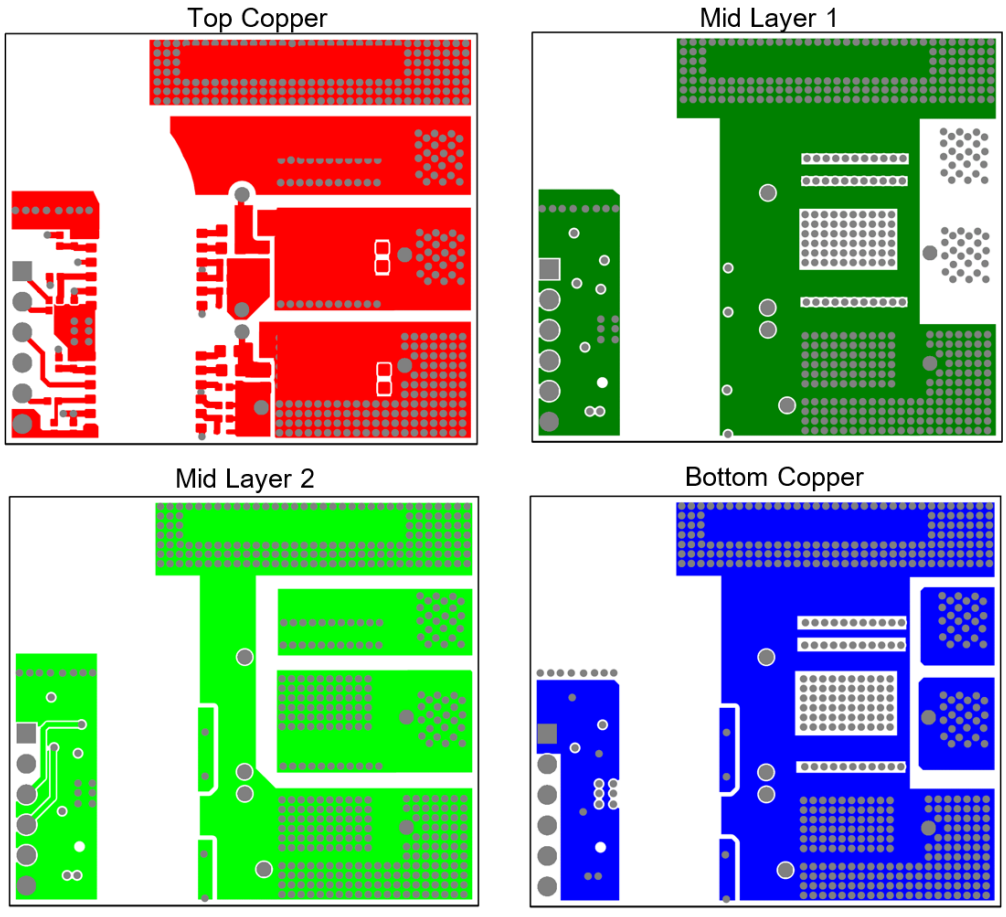

Figure 14: APEK85110KNH-01-T-MH PCB Copper Layers

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BILL OF MATERIALS

Table 1: APEK85110KNH-01-T-MH Evaluation Board Bill of Materials

Ref Name	Description	Value	Qty	Manufacturer	Manufacturer PN
C1, C2	CAP CERALINK, 1 µF, 500 V, PLZT	1 µF	2	TDK	B58031U5105M062
C14, C15, C16, C17	CAP, CER,100nF,16V, X7R, S0402	100 nF	4	KEMET	C0402C104K4RALTU
C3, C4	CAP, CER, 75 pF, 50 V, NP0, S0402	75 pF	2	KEMET	C0402C750J5GACTU
C6, C13	CAP, CER,1 µF, 25 V, X5R, S0402	1 µF	2	MURATA	GRM155R61E105KA12D
CONN1	HEADER, 6 WAY, 2.54 mm	6WAY, 2P54	1	WURTH	61300611121
CR1, CR2	DIO ZEN, 6V2, 100 mW, SOD-923	CDZVT2R6.2B	2	ROHM	CDZVT2R6.2B
IC1, IC2	Single-Channel Isolated GaN FET Driver	AHV85110	2	ALLEGRO	AHV85110KNHTR
Q1, Q2	GAN FET GS66516B 650 V, 60 A	GS66516B-MR	2	GAN SYSTEMS	GS-065-060-3-B
R1, R5	RES, SMD, 10 Ω, 0.063 W, 1%, S0603	10 Ω	2	BOURNS	CMP0603AFX-10R0ELF
R11, R13	RES, SMD, 3.6 kΩ, 0.063 W, 1%, S0402	3.6 kΩ	2	PANASONIC	ERJ2RKF3601X
R2	RES, SMD, 100 kΩ, 0.063 W, 1%, S0402	100 kΩ	1	PANASONIC	ERJ2GEJ104X
R3, R7	RES, SMD, 1 Ω, 0.063 W, 1%, S0603	1 Ω	2	ROHM	ESR03EZPJ1R0
R4, R8	RES, SMD, 0 Ω, 0.063 W, 1%, S0402	0 Ω	2	VISHAY	RCG04020000Z0ED
R6, R9	RES, SMD, 49.9 Ω, 0.063 W, 1%, S0402	49.9 Ω	2	VISHAY	CRCW040249R9FKED

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Revision History

Number	Date	Description
–	June 14, 2023	Initial release

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