APEK85110KNH-06-T-MH

AHV85110 Evaluation Board User Guide

DESCRIPTION

The Allegro MicroSystems half-bridge driver-switch APEK85110KNH-06-T-MH is a demonstration board containing two APEK85110KNH GaN FET drivers and two GaN FETs configured in a half-bridge configuration.

FEATURES

The APEK85110KNH-06-T-MH can be used to perform double-pulse tests or to interface the half bridge to an existing LC power section.

The isolated APEK85110KNH driver does not require secondary side power or bootstrap components. Gate-drive power is supplied to the secondary side from the primary-side supply voltage V_{DRV}. The amplitude of the gate drive can be varied by changing V_{DRV} between 10.8 V and 13.2 V.

EVALUATION BOARD CONTENTS

- APEK85110KNH-06-T-MH Evaluation Board

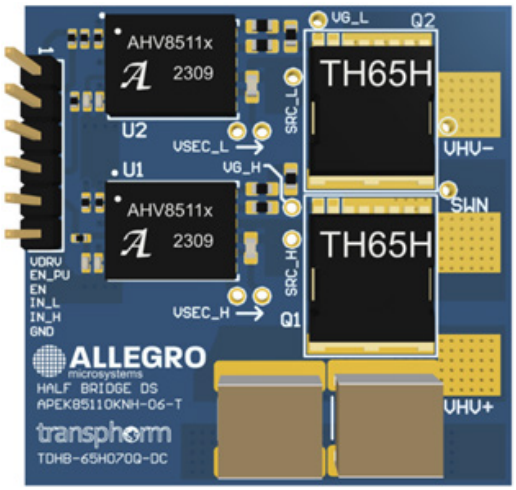

Figure 1: AHV85110KNH-06-T-MH Evaluation Board

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DANGER

DO NOT TOUCH THE BOARD WHEN IT IS ENERGIZED AND ALLOW ALL COMPONENTS TO DISCHARGE COMPLETELY PRIOR TO HANDLING THE BOARD.

HIGH VOLTAGE CAN BE EXPOSED ON THE BOARD WHEN IT IS CONNECTED TO THE POWER SOURCE. EVEN BRIEF CONTACT DURING OPERATION MAY RESULT IN SEVERE INJURY OR DEATH.

Ensure that appropriate safety procedures are followed. This evaluation board is designed for **engineering evaluation in a controlled lab environment and should be handled by qualified personnel ONLY.** Never leave the board operating unattended.

WARNING

Some components can be hot during and after operation. **There is NO built-in electrical or thermal protection on this evaluation board.** The operating voltage, current, and component temperature should be monitored closely during operation to prevent device damage.

CAUTION

This product contains parts that are susceptible to damage by electrostatic discharge (ESD). Always follow ESD prevention procedures when handling the product.

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USING THE EVALUATION BOARD

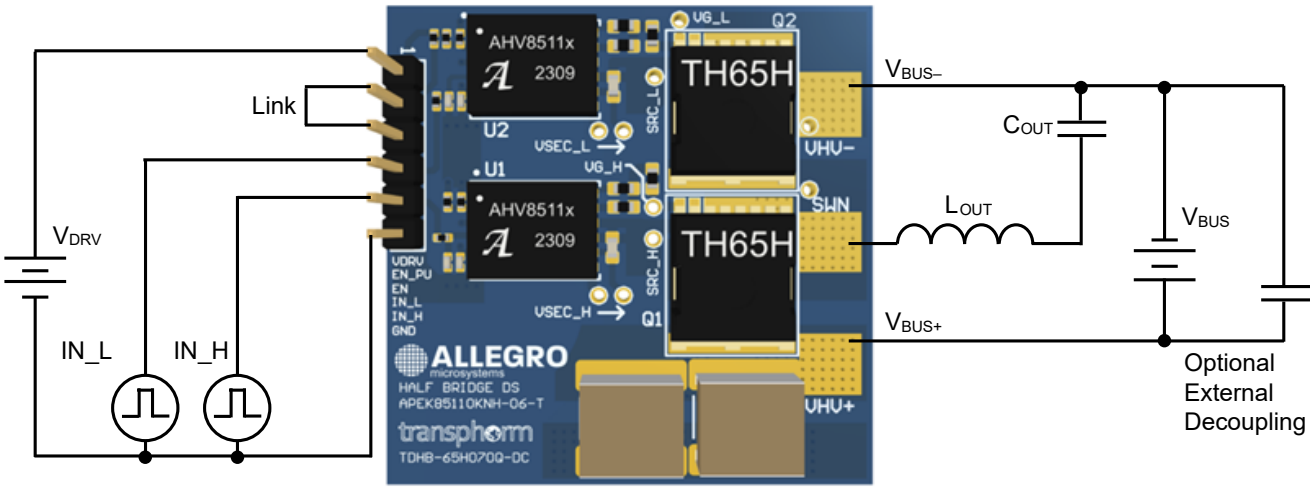

Figure 2: APEK85110KNH-06-T-MH Quick Start

1. Apply V_{DRV} = 12 V.
2. Link pins EN_PU and EN (if not using external Enable control).
3. Apply input gate signals, with adequate dead time, to the IN_L and IN_H inputs.
4. Convenient test points are located on the test board as shown in the Measurement Points section. A suitable differential oscilloscope should be used to monitor the high-side gate signal from VGH to VSW.

Gate Pull-Up and Pull-Down Resistors

The APEK85110KNH gate driver has independent output pins for the gate pull-up and gate pull-down, allowing control of the turn-on and turn-off rise and fall times.

The default values for these resistors are:

OUTPU: R7 and R13 = 33 Ω

OUTPD: R1 and R15 = 47 Ω

These values can be modified to suit the application.

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Enable Sequence

The APEK85110KNH has an open-drain enable pin (EN) to facilitate a system-level wired-AND startup.

When the enable pin is externally pulled low, the driver is forced into a low-power mode. The driver output is pulled low in this mode. In the event of an internal fault condition, such as UVLO or normal startup delay, the EN pin is actively pulled low internally by the driver.

During normal operation, the pin is released by the driver and must be pulled high with an external pull-high resistor. This functionality can be used by the PWM controller as an indication that it can start sending IN pulses to the driver. It is typically wired-AND with the controller enable pin as shown in Figure 3.

The APEK85110KNH-06-T-MH evaluation board provides direct access to the EN pin on connector CONN1. Internally, the board contains a 100 kΩ pull-up resistor connected from VDRV to the EN_PU pin on connector CONN1—see the Schematic section. If external control of the enable function is not required, pins EN and EN_PU must be linked together on CONN1 to make use of the internal 100 kΩ pull-up resistor to enable the driver. If the EN pin is left floating, the drivers do not respond to INL or INH input signals.

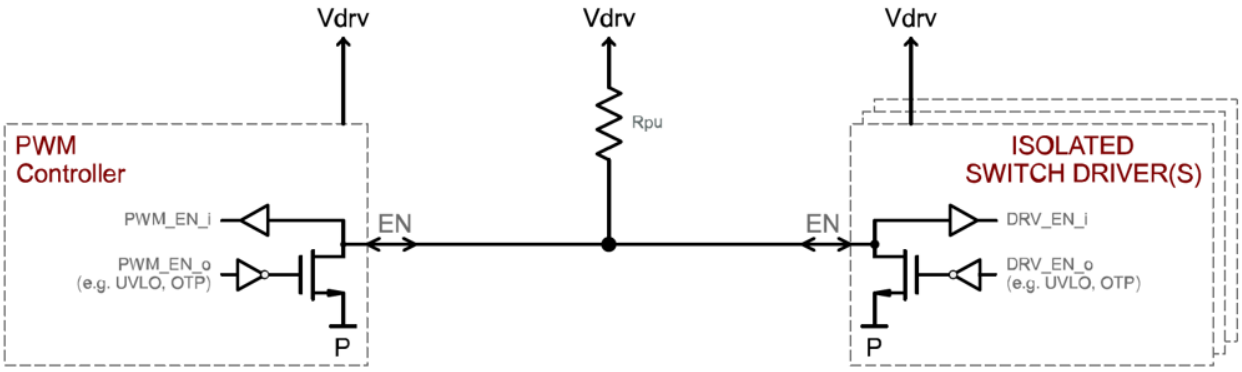

Figure 3: APEK85110KNH Wired-AND Enable

When the EN pin is pulled low, the driver output is disabled and pulls down the OUTPD pin regardless of the IN pin level (high or low). The driver goes to a low-power standby mode, and the isolated V_{SEC} bias rail is allowed to discharge. The rate of decay of V_{SEC} depends on the value of the C_{SEC} capacitor.

When the EN pin is subsequently pulled high, the driver becomes re-enabled, and the isolated V_{SEC} bias rail starts to recharge.

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Start Sequence

The startup sequence of the APEK85110KNH is shown in Figure 4. Time t_{START} is defined as the time after which V_{DRV} reaches the UVLO rising level of the APEK85110KNH, releasing the EN internal pull-down.

To avoid parasitic charging of the V_{DRV} rail through the IN pin internal ESD structures, any PWM signal applied to IN must remain low until V_{DRV} > UV threshold.

After V_{DRV} exceeds the UV enable threshold, a startup time delay t_{START} is required to charge V_{SEC} and allow all internal circuits to initialize and stabilize. During t_{START}, any IN signal inputs are ignored. EN internal pull-down remains active during t_{START}, and becomes disabled (i.e., goes open-drain) only when V_{DRV} has reached its UVLO voltage level, all on-chip voltages are stabilized, and the internal t_{START} timer has elapsed. Thus, the EN pin can be used via a shared EN line to flag when t_{START} has elapsed and the driver is ready to respond to PWM signals at the IN pin, as outlined above.

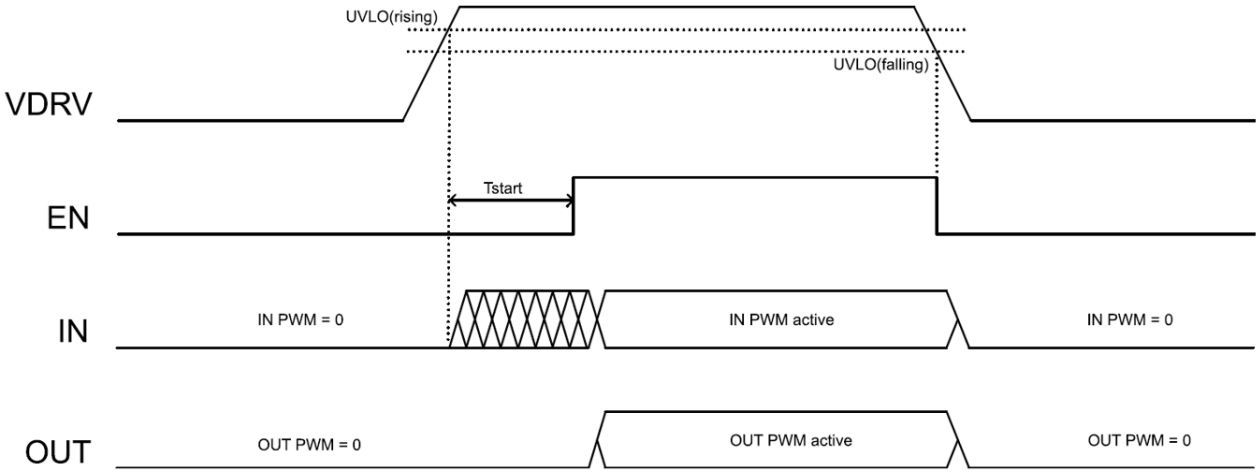

Figure 4: APEK85110KNH Startup Sequence

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Measurement Points

The APEK85110KNH-06-T-MH evaluation board contains convenient test points for monitoring the high- and low-side gate drives as well as the switch node, as shown in Figure 5.

When measuring V_{GS_H}, use a differential probe with suitable ratings for the applied bus voltage.

To avoid pickup of spurious switching noise, it is important to use a low-inductance-scope probe ground lead, as shown.

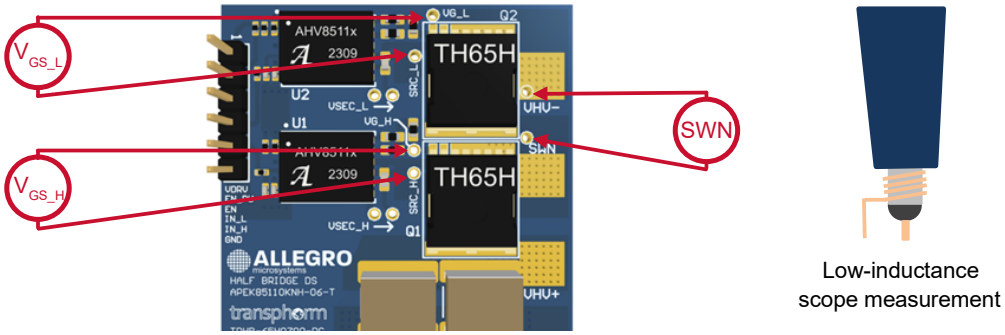

Figure 5: Measurement Points

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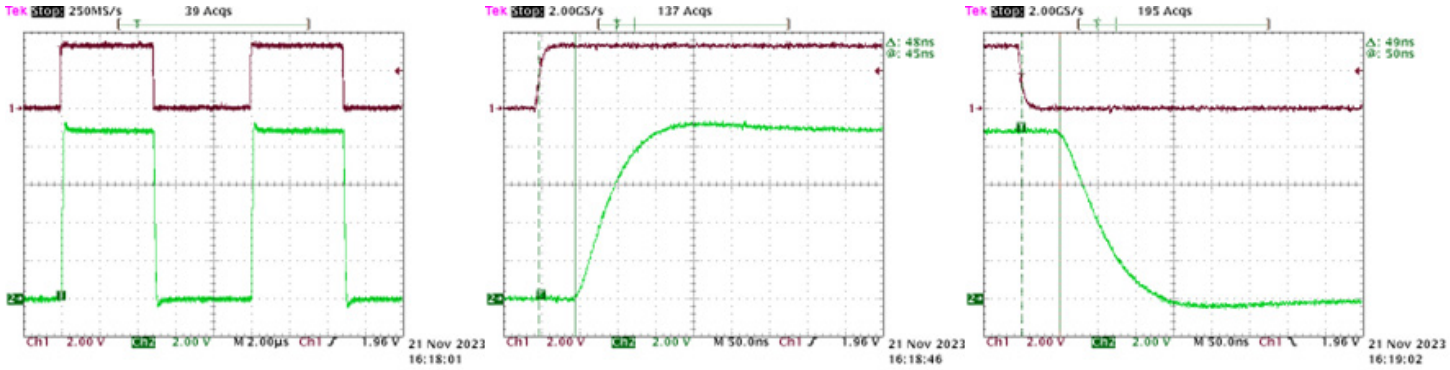
Propagation Delay

- V_{DRV} = 12 V
- Input = 100 kHz
- R_{PU} = 33 Ω, R_{PD} = 47 Ω
- Power train unloaded; that is, VHV+ = 0 V



CH1: Driver Input
CH2: Driver Output

Low-Side Driver Output

CH1: Driver Input
CH2: Driver Output

Typical Turn-On Propagation Delay

CH1: Driver Input
CH2: Driver Output

Typical Turn-Off Propagation Delay

Figure 6: Typical Driver Output at 100 kHz

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Double-Pulse Test

The double-pulse test is used to evaluate the switching characteristics of a power switch under hard switching but in a safe manner. For a low-side switch, the setup is shown in Figure 7.

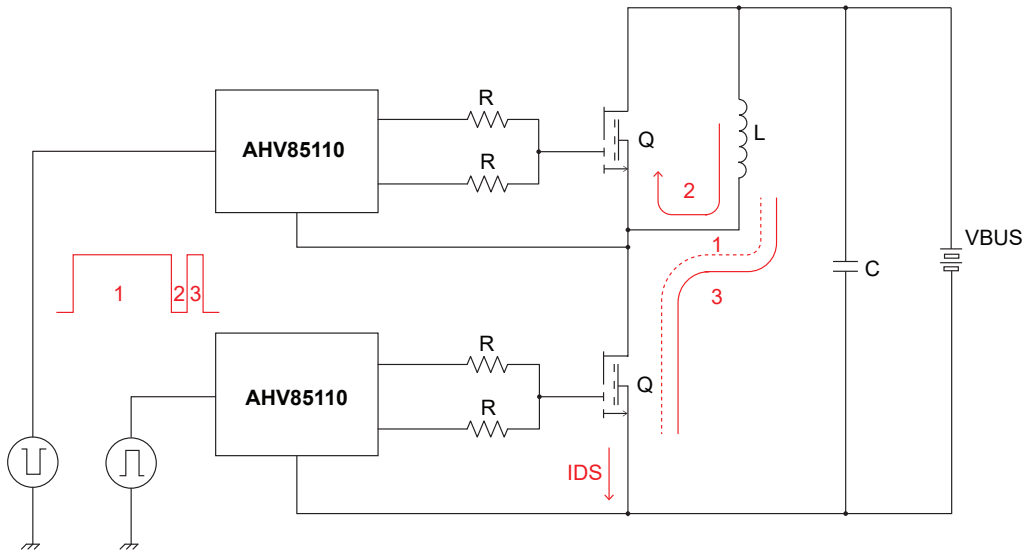

Figure 7: Double-Pulse Test

The low-side switch is driven with two pulses as shown in Figure 8. The high-side switch can be held off or driven with the inverse of the low-side gate switch (with adequate dead time).

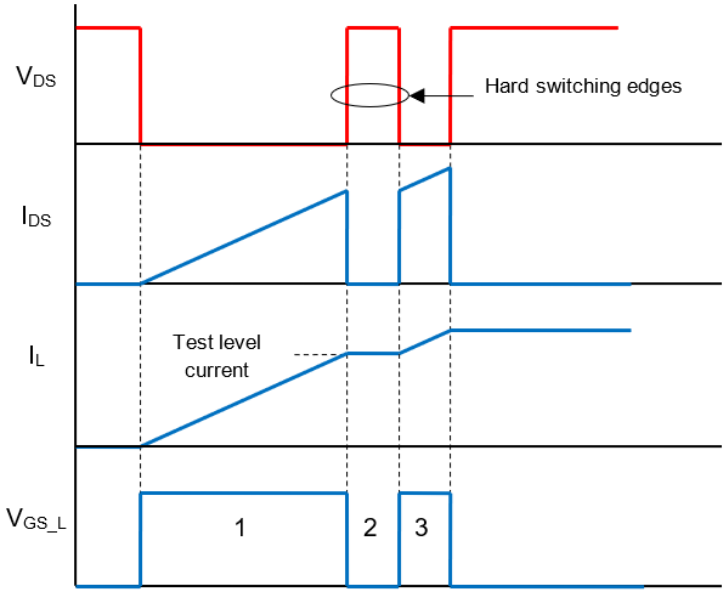

Figure 8: Double-Pulse Test Waveforms

An inductor is placed in parallel with the high-side switch. The goal of this inductor is to establish the test level current in the low-side switch at the end of the first on-pulse (1). The magnitude of the test level current at the end of period 1 is given by:

$$I_L = V_{BUS} \frac{t_{ON\_1}}{L}$$

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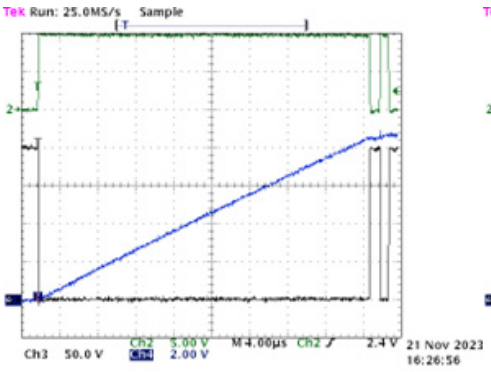
During period 2, the inductor current decays naturally. The duration of period 2 should not be so long that inductor current deviates significantly from the desired test level.

During period 3, the inductor current again rises. Period 3 should not be so long that the inductor current rises to an excessive level.

The falling edge of pulse 1 is used to examine the hard-turn-off characteristics of the switch. The rising edge of pulse 3 is used to examine the hard-turn-on characteristics of the switch. By only applying these two pulses, the switches are only in the on state for a very short period of time and should not overheat.

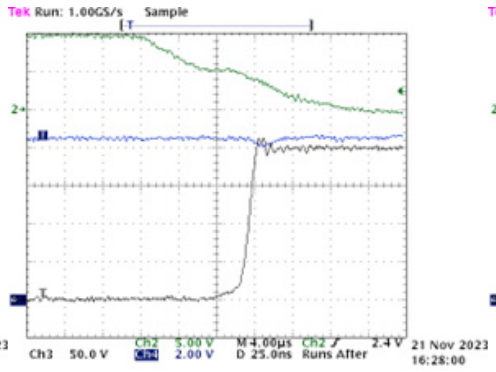
Double-Pulse Test (DPT) Results

DPT RESULT 200 V, 8 A



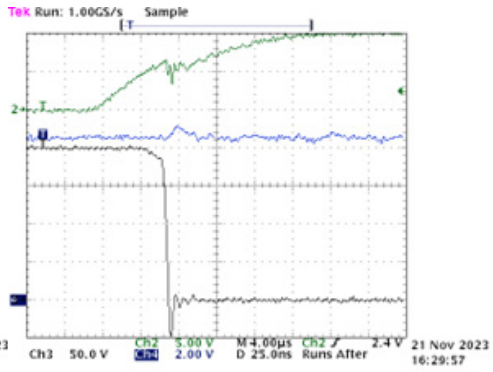
CH2: Low-Side V_{GS}
CH3: Switch Node
CH4: Inductor Current (1 A/V)

DPT Overview



CH2: Low-Side V_{GS}
CH3: Switch Node
CH4: Inductor Current (1 A/V)

DPT Hard-Switching Turn-Off
Time Base (25 ns/div)

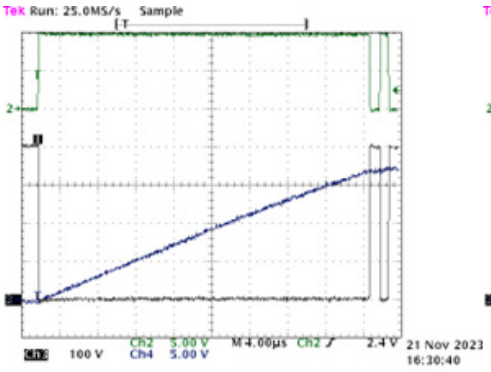


CH2: Low-Side V_{GS}
CH3: Switch Node
CH4: Inductor Current (1 A/V)

DPT Hard-Switching Turn-On
Time Base (25 ns/div)

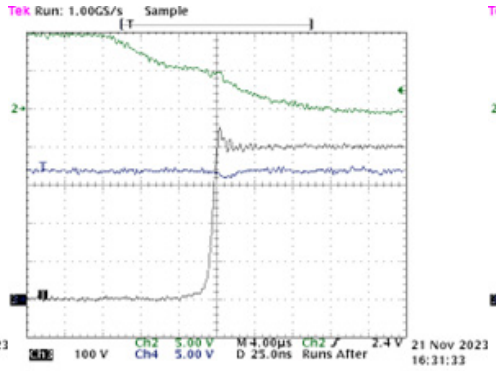
Figure 9: DPT 200 V, 8 A

DPT RESULT 400 V, 17 A



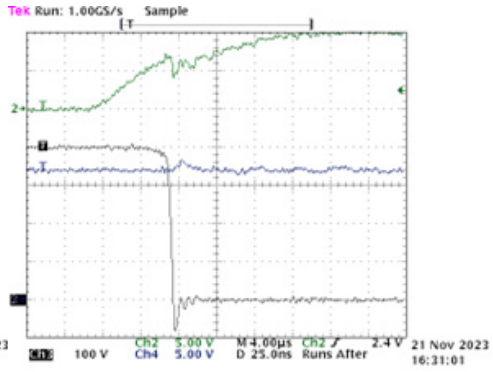
CH2: Low-Side V_{GS}
CH3: Switch Node
CH4: Inductor Current (1 A/V)

DPT Overview



CH2: Low-Side V_{GS}
CH3: Switch Node
CH4: Inductor Current (1 A/V)

DPT Hard-Switching Turn-Off
Time Base (25 ns/div)



CH2: Low-Side V_{GS}
CH3: Switch Node
CH4: Inductor Current (1 A/V)

DPT Hard-Switching Turn-On
Time Base (25 ns/div)

Figure 10: DPT 400 V, 17 A

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SCHEMATIC

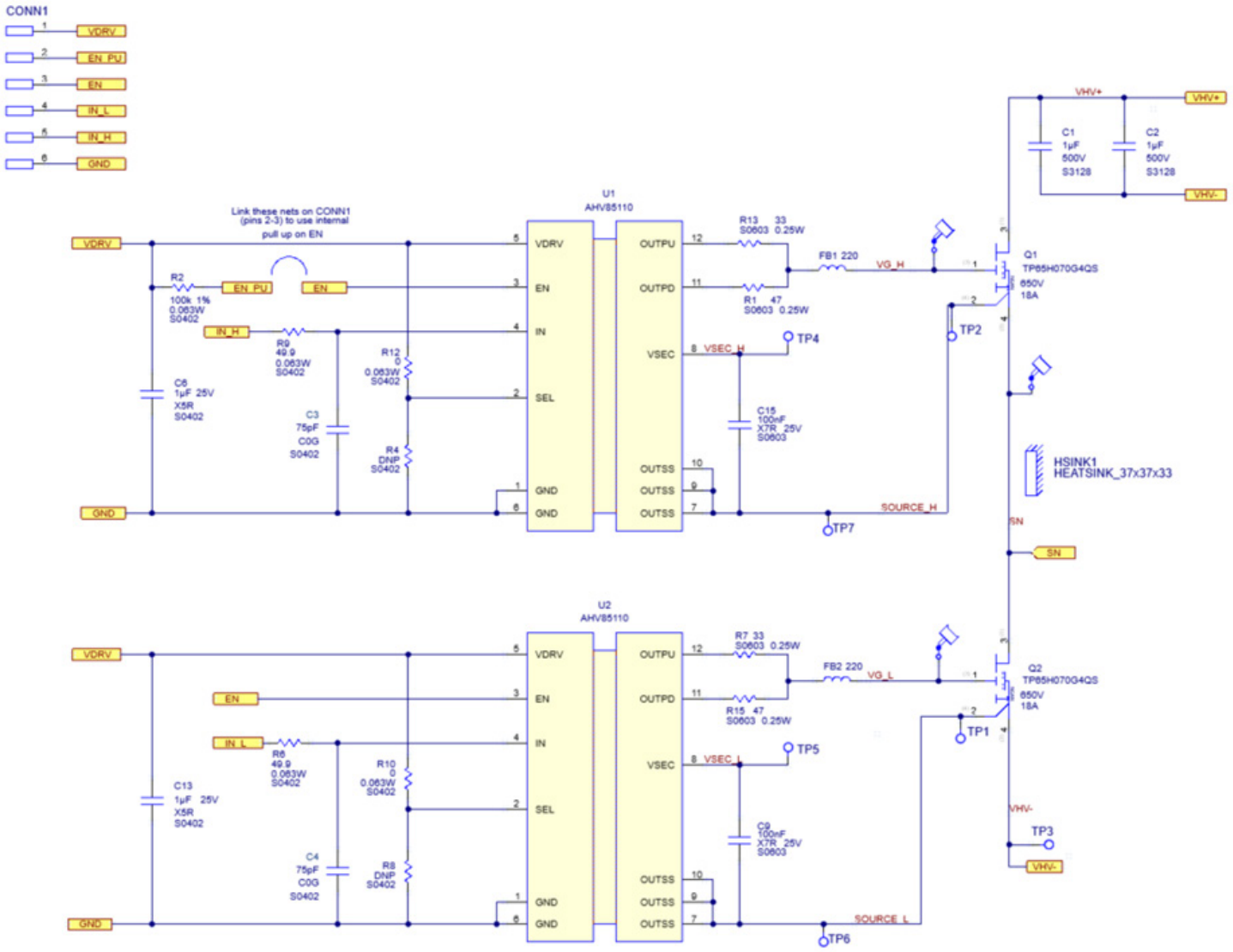

Figure 11: APEK85110KNH-06-T-MH Schematic

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LAYOUT

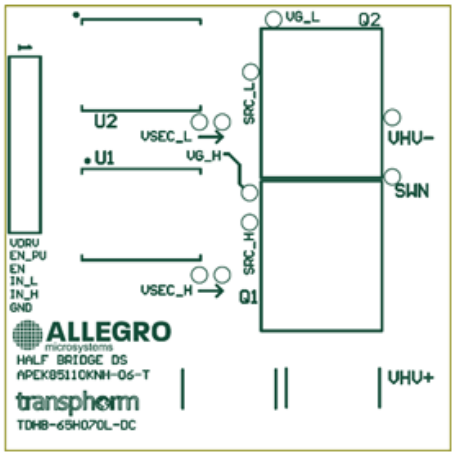

Figure 12: APEK85110KNH-06-T-MH Top Overlay

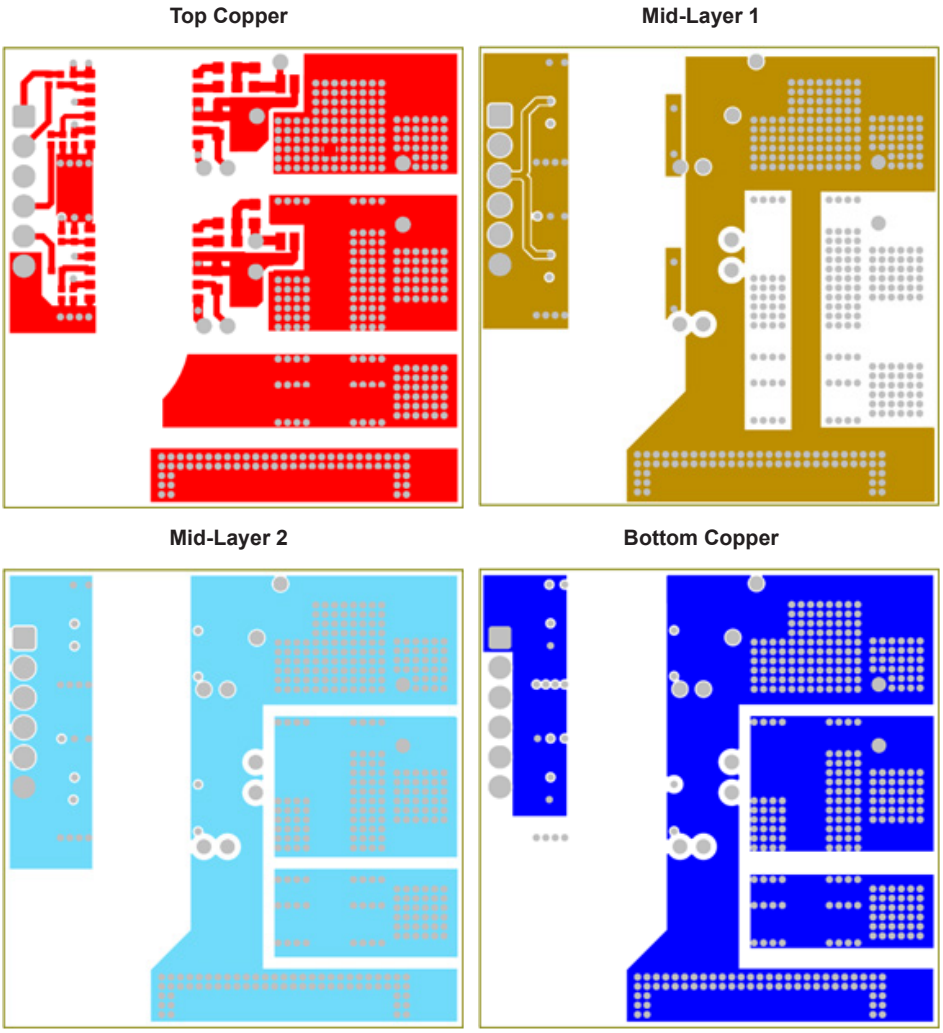

Figure 13: APEK85110KNH-06-T-MH PCB Copper Layers

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BILL OF MATERIALS

Table 1: APEK85110KNH-06-T-MH Evaluation Board Bill of Materials

Ref Name	Description	Value	Qty	Manufacturer	Manufacturer PN
CONN1	Pin Header, 2.54 mm, 6 Contacts	Connector 6 Way	1	Molex	22284065
R2	RES, 100 kΩ, 0.063 W, 1%, 0402	100 Ω	1	Walsin Technologies	SR04X1003FTL
U1, U2	AHV85110 Single-Channel Isolated GaN FET Driver	AHV85110	2	Allegro MicroSystems	AHV85110KNH
C6, C13	CAP, CER, 1 µF, 25 V, X5R, 0402	1 µF	2	Murata	GRT155R61E105KE01D
C3, C4	CAP, CER, 75 pF, 50 V, COG/NPO, 0402	75 pF	2	Multicomp	MC0402N750J500CT
C9, C15	CAP, CER, 100 nF, 25 V, X7R, 0603	100 nF	2	Murata	GCJ188R71E104KA12D
C1, C2	CAP, CERALINK, 1 µF, 500 V	1 µF	2	TDK EPCOS	B58031U5105M062
FB1, FB2	Ferrite Bead, 0603, 220 Ω at 100 MHz, 2.2 A	220 Ω	2	Murata	BLM18KG221SH1D
R10, R12	RES, 0 Ω, 0.063 W, 1%, 0402	0 Ω	2	Walsin Technologies	WR04X000PTL
R1, R15	RES, 47 Ω, 0603, 0.25 W, 5%, Anti-Surge	47 Ω	2	TE Connectivity	CRGS0603J47R
R7, R13	RES, 33 Ω, 0603, 0.25 W, 1%, Anti-Surge	33 Ω	2	ROHM	ESR03EZPF33R0
R6, R9	RES, 49.9 Ω, 0.063 W, 1%, 0402	49.9 Ω	2	Vishay	CRCW040249R9FKED
R4, R8	RES, 0402, Not Assembled		2		
Q1, Q2	Transphorm Cascode GaN FET 650 V, 18 A, 72 mΩ, 8.4 nC	TP65H070G4QS	2	Transphorm	TP65H070G4QS

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AHV85110 Datasheet: https://www.allegromicro.com/-/media/files/datasheets/ahv85110-full-datasheet.pdf?sc_lang=en

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Revision History

Number	Date	Description
–	November 29, 2023	Initial release

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