APEK85111KNH-02-T-MH

AHV85111 Evaluation Board User Guide

DESCRIPTION

The Allegro MicroSystems Half-Bridge Driver-Switch APEK85111KNH-02-T-MH is an evaluation board containing two APEK85111KNH GaN FET drivers and two GaN FETs configured in a half-bridge configuration.

FEATURES

The APEK85111KNH-02-T-MH can be used to perform double-pulse tests, or to interface the half-bridge to an existing LC power section, both as shown in this guide.

The isolated APEK85111KNH driver does not require secondary side power or bootstrap components. Gate drive power is supplied to the secondary side from the primary-side supply voltage, V_{DRV}. The amplitude of the gate drive can be varied by adjusting the voltage setting resistors as described in this guide.

EVALUATION BOARD CONTENTS

- APEK85111KNH-02-T-MH evaluation board.

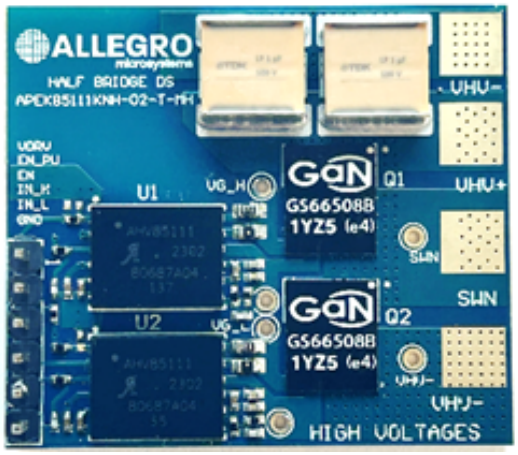

Figure 1: AHV85111 Evaluation Board

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DANGER

DO NOT TOUCH THE BOARD WHEN IT IS ENERGIZED AND ALLOW ALL COMPONENTS TO DISCHARGE COMPLETELY PRIOR HANDLING THE BOARD.

HIGH VOLTAGE CAN BE EXPOSED ON THE BOARD WHEN IT IS CONNECTED TO POWER SOURCE. EVEN BRIEF CONTACT DURING OPERATION MAY RESULT IN SEVERE INJURY OR DEATH.

Ensure that appropriate safety procedures are followed. This evaluation kit is designed for **engineering evaluation in a controlled lab environment and should be handled by qualified personnel ONLY.** Never leave the board operating unattended.

WARNING

Some components can be hot during and after operation. **There is NO built-in electrical or thermal protection on this evaluation kit.** The operating voltage, current, and component temperature should be monitored closely during operation to prevent device damage.

CAUTION

This product contains parts that are susceptible to damage by electrostatic discharge (ESD). Always follow ESD prevention procedures when handling the product.

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USING THE EVALUATION BOARD

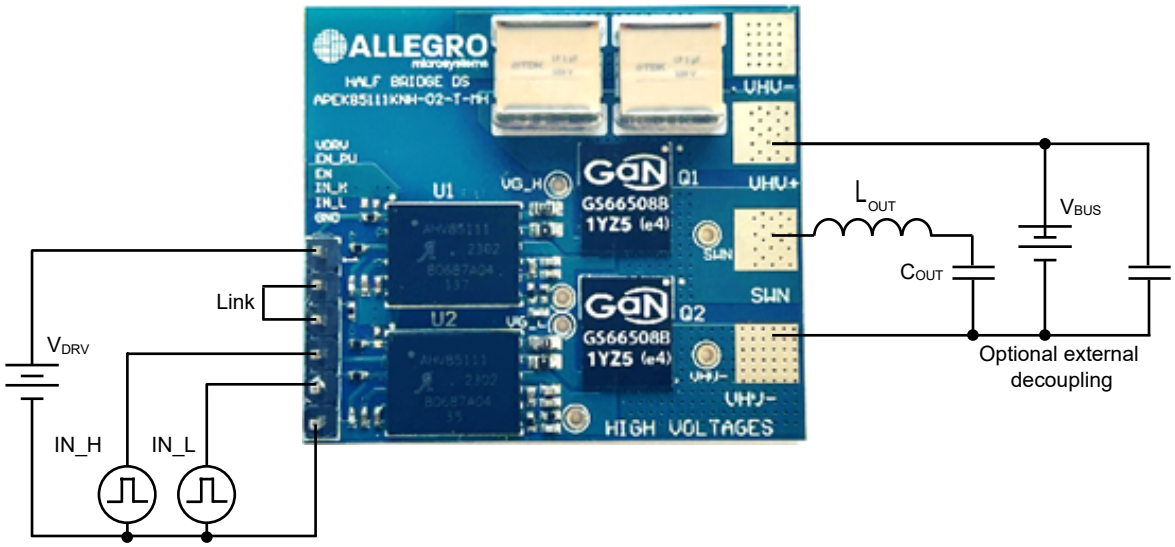

Figure 2: APEK85111KNH-02-T-MH Quick Start

1. Apply V_{DRV} = 12 V.
2. Link pins EN_PU and EN (if not using external enable control).
3. Apply input gate signals, with adequate dead time, to the IN_L and IN_H inputs.
4. Convenient test points are located on the test board as shown in the Measurement Points section. A suitable differential oscilloscope should be used to monitor the high-side gate signal from V_{GH} to V_{SW}.

GATE PULL-UP AND PULL-DOWN RESISTORS

The APEK85111KNH gate driver has independent output pins for the gate pull-up and gate pull-down, allowing control of the turn-on and turn-off rise and fall times.

The default values for these resistors are:

OUTPU: R7 and R13 = 10 Ω

OUTPD: R1 and R15 = 1 Ω

These values can be modified to suit the application.

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ENABLE SEQUENCE

The APEK85111KNH has an open-drain enable pin (EN) to facilitate a system-level wired-AND startup.

When the enable pin is externally pulled low, the driver is forced into a low-power mode. The driver output is pulled low in this mode. In the event of an internal fault condition, such as UVLO or typical startup delay, the EN pin is actively pulled low internally by the driver.

During typical operation, the pin is released by the driver and must be pulled high with an external pull-high resistor. This functionality can be used by the PWM controller as an indication that it can start sending IN pulses to the driver. It is typically wired-AND with the controller enable pin as shown in Figure 3.

The APEK85111KNH-02-T-MH evaluation board provides direct access to the EN pin on connector CONN1. Internally, the board contains a 100 kΩ pull-up resistor connected from V_{DRV} to the EN_PU pin on connector CONN1 (see the Schematic section). If external control of the enable function is not required, pins EN and EN_PU must be linked together on CONN1 to make use of the internal 100 kΩ pull-up resistor to enable the driver. If the EN pin is left floating, the drivers do not respond to IN_L or IN_H input signals.

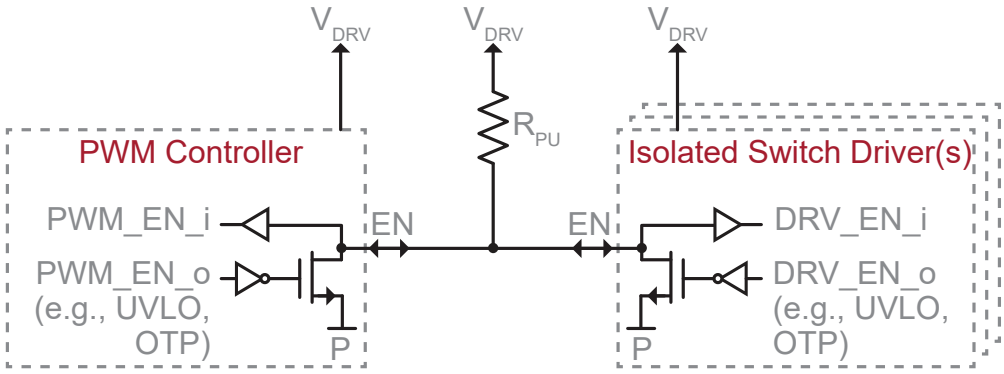

Figure 3: APEK85111KNH Wired-AND Enable

When the EN pin is pulled low, the driver output is disabled and pulls down the OUTPD pin, regardless of the IN pin level (high or low). The driver goes to a low-power standby mode, and the isolated V_{SEC} bias rails are allowed to discharge. The rate of decay of V_{SEC} depends on the value of the C_{SEC} capacitor.

When the EN pin is subsequently pulled high, the driver reenables, and the isolated V_{SEC} bias rails start to recharge.

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START SEQUENCE

The startup sequence of the APEK85111KNH is shown in Figure 4. Time t_{START} is defined as the time after which V_{DRV} reaches the UVLO rising level to the APEK85111KNH, releasing the EN internal pull-down.

Any PWM signal applied to IN must remain low until V_{DRV} > UV threshold to avoid parasitic charging of the V_{DRV} rail through the IN pin internal ESD structures.

After V_{DRV} exceeds the UV enable threshold, a startup time delay, t_{START}, is required to allow all internal circuits to initialize and stabilize. During t_{START}, any IN signal inputs are ignored. EN internal pull-down remains active during t_{START} and becomes disabled (i.e., go open-drain) only when V_{DRV} has reached its UVLO voltage level, all on-chip voltages have stabilized, and the internal t_{START} timer has elapsed. Thus, the EN pin can be used via a shared EN line to flag when t_{START} has elapsed and the driver is ready to respond to PWM signals at the IN pin, as outlined previously in this guide.

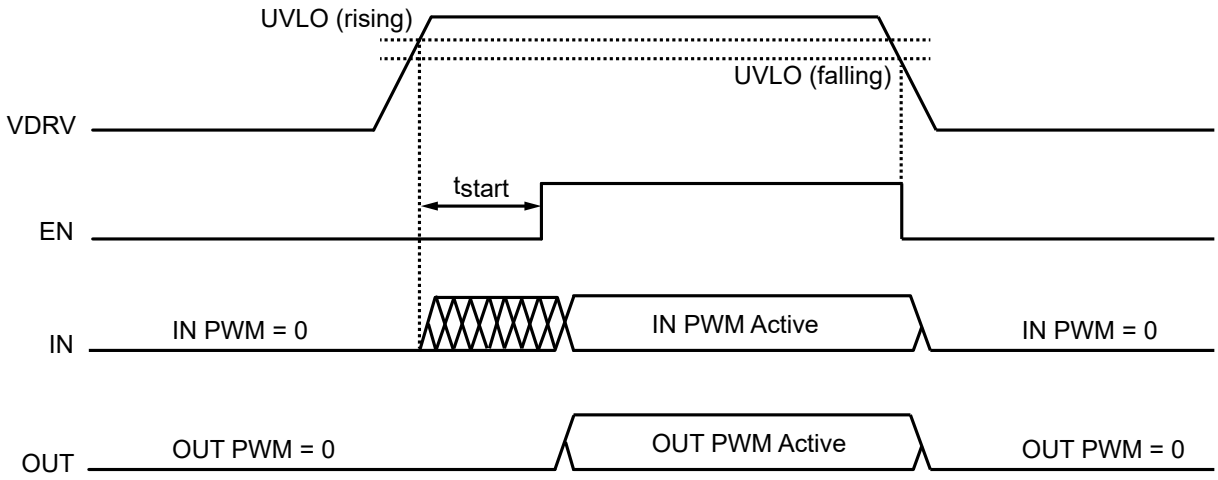

Figure 4: APEK85111KNH Startup Sequence

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MEASUREMENT POINTS

The APEK85111KNH-02-T-MH evaluation board contains convenient test points for monitoring the high- and low-side gate drives as well as the switch node, as shown in Figure 5.

When measuring V_{GS_H}, use a differential probe with suitable ratings for the applied bus voltage. The APEK85111KNH GaN FET drivers have bipolar output as shown in the Propagation Delay section. When measuring V_{GS}, both gate drives are measured relative to the source of their associated GaN FET. Therefore, the off-state voltage is negative.

To avoid pickup of spurious switching noise, it is important to use a low-inductance scope probe ground lead, as shown.

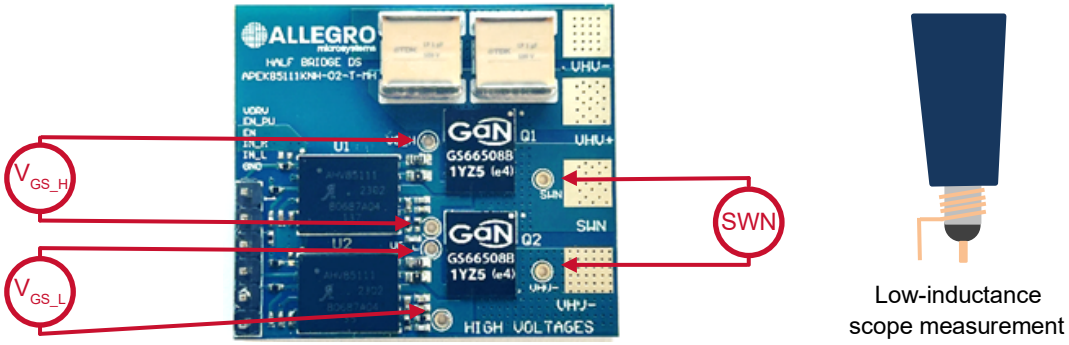
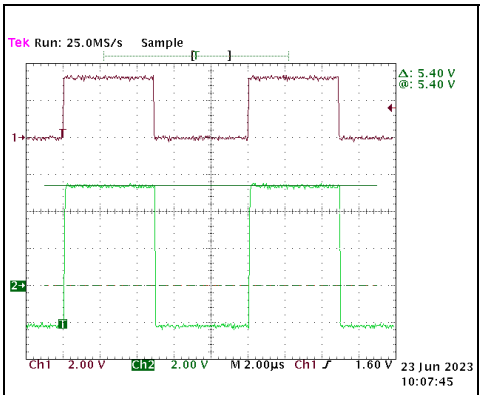


Figure 5: Measurements Points

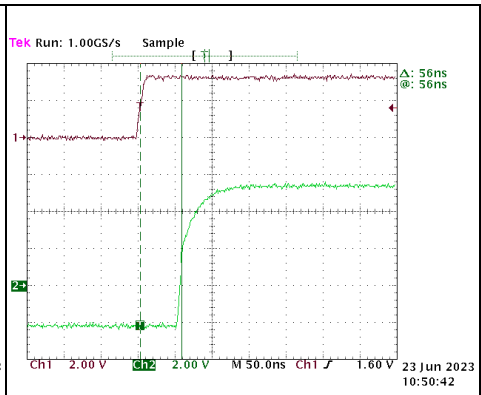
PROPAGATION DELAY

- V_{DRV} = 12 V
- Input = 100 kHz
- R_{PU} = 10 Ω, R_{PD} = 1 Ω
- Power train unloaded. That is, VHV+ = 0 V.



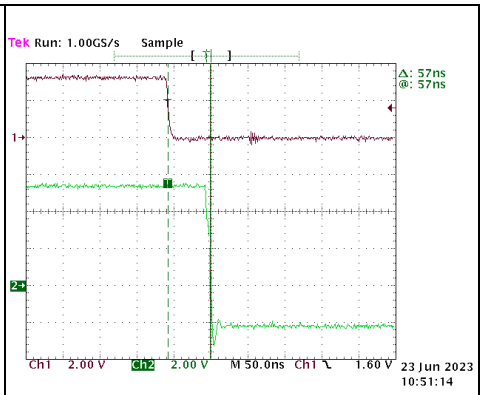
CH1 (Red): Driver Input
CH2(Green): Driver Output wrt VHV–

Low-Side Driver Output



CH1 (Red): Driver Input
CH2(Green): Driver Output wrt VHV–

Typical Turn-On Propagation Delay



CH1 (Red): Driver Input
CH2(Green): Driver Output wrt VHV–

Typical Turn-Off Propagation Delay

Figure 6: Typical Driver Output at 100 kHz

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THERMAL MANAGEMENT

The APEK85111KNH-02-T-MH is supplied without a heat sink. As such, do not continuously operate the board at high power levels.

To operate the evaluation board in continuous mode or at elevated power levels, a heat sink must be added to the underside of the PCB. The operating temperature of the AHV85111KNH driver and the GaN FETs must be maintained below their maximum temperatures.

When adding a heat sink, note that the heat sink may span the primary to secondary isolation boundary and the high voltage PCB traces on the secondary side. It is critical to use a suitable thermal interface material between the heat sink and the PCB.

Exercise caution when probing the test points to ensure that the integrity of the thermal interface material is not compromised.

DOUBLE-PULSE TEST

The double-pulse test is used to evaluate the switching characteristics of a power switch under hard switching but in a safe manner.

For a low-side switch, the setup is as shown in Figure 7.

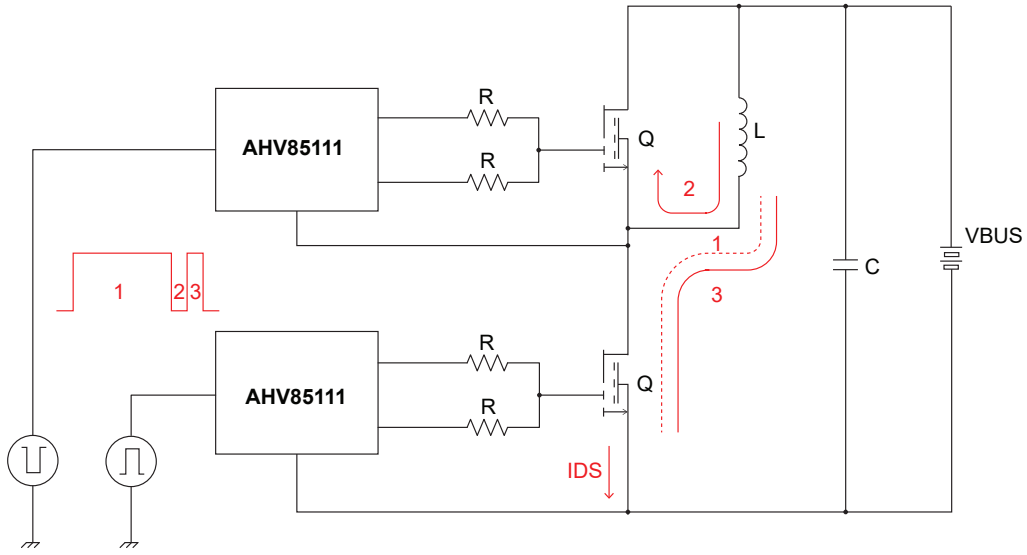

Figure 7: Double-Pulse Test

The low-side switch is driven with two pulses as shown in Figure 8. The high-side switch can be held off or driven with the inverse of the low-side gate switch (with adequate dead time).

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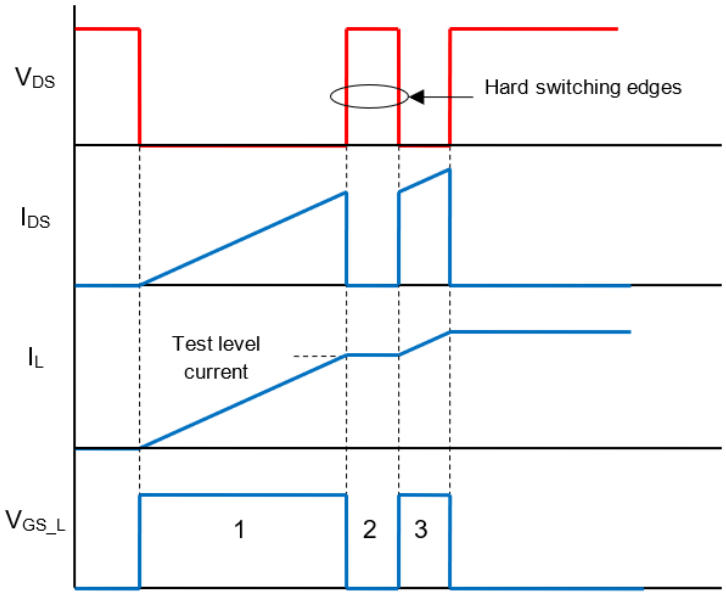

Figure 8: Double-Pulse Test Waveforms

An inductor is placed in parallel with the high-side switch. The goal of this inductor is to establish the test level current in the low-side switch at the end of the first on pulse (1). The magnitude of the test level current at the end of period 1 is given by:

$$I_L = \frac{V_{BUS}\, t_{ON\_1}}{L}$$

During period 2, the inductor current naturally decays. The duration of period 2 should not be so long that inductor current deviates significantly from the desired test level.

During period 3, the inductor current again rises. Period 3 should not be so long that the inductor current rises to an excessive level.

The falling edge of pulse 1 is used to examine the hard turn-off characteristics of the switch. The rising edge of pulse 3 is used to examine the hard turn-on characteristics of the switch. By only applying these two pulses, the switches are only on for a very short time and should not overheat.

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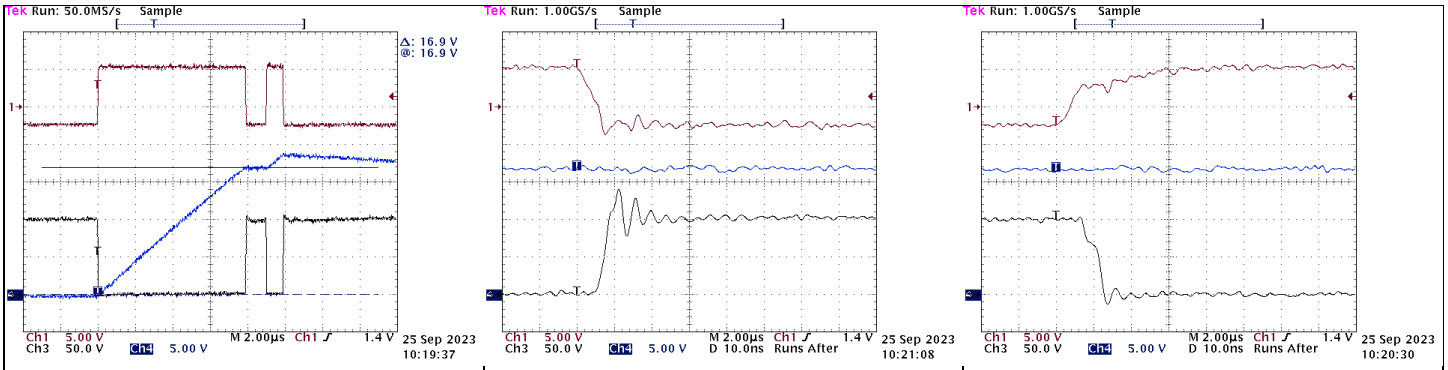
DOUBLE-PULSE TEST RESULTS

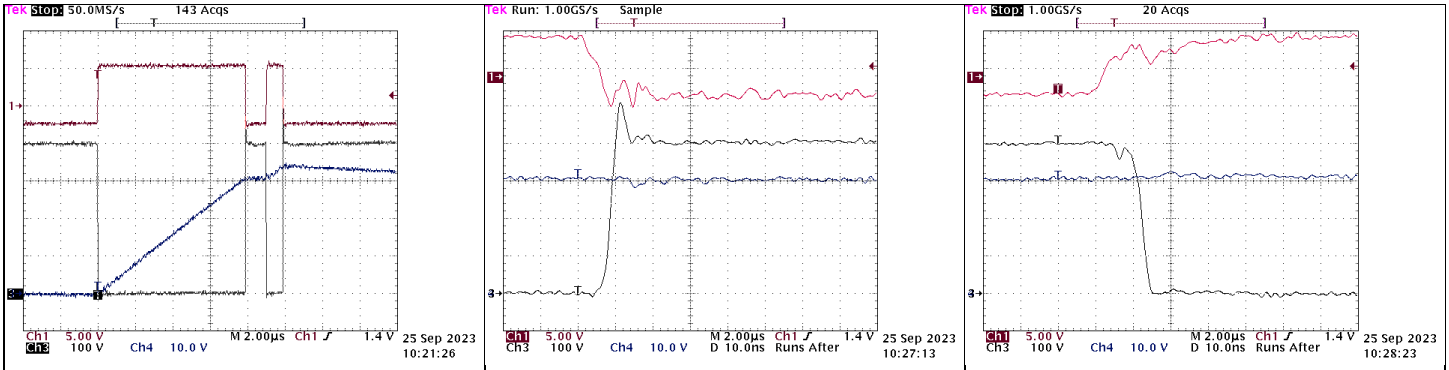
DPT Result 100 V, 16 A (R_{PU} = 10 Ω, R_{PD} = 1 Ω)



CH1(Red): Low side V_{GS} **CH3(Black):** Switch Node **CH4(Blue):** Inductor Current (1 A/V)	**CH1(Red):** Low side V_{GS} **CH3(Black):** Switch Node **CH4(Blue):** Inductor Current (1 A/V)	**CH1(Red):** Low side V_{GS} **CH3(Black):** Switch Node **CH4(Blue):** Inductor Current (1 A/V)
DPT Overview	**DPT Hard Switching Turn-Off**	**DPT Hard Switching Turn-On**

Figure 9: DPT 100 V, 16 A

DPT Result 400 V, 30 A (R_{PU} = 10 Ω, R_{PD} = 1 Ω)



CH1(Red): Low side V_{GS} **CH3(Black):** Switch Node **CH4(Blue):** Inductor Current (1 A/V)	**CH1(Red):** Low side V_{GS} **CH3(Black):** Switch Node **CH4(Blue):** Inductor Current (1 A/V)	**CH1(Red):** Low side V_{GS} **CH3(Black):** Switch Node **CH4(Blue):** Inductor Current (1 A/V)
DPT Overview	**DPT Hard Switching Turn-Off**	**DPT Hard Switching Turn-On**

Figure 10: DPT 400 V, 30 A

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SCHEMATIC

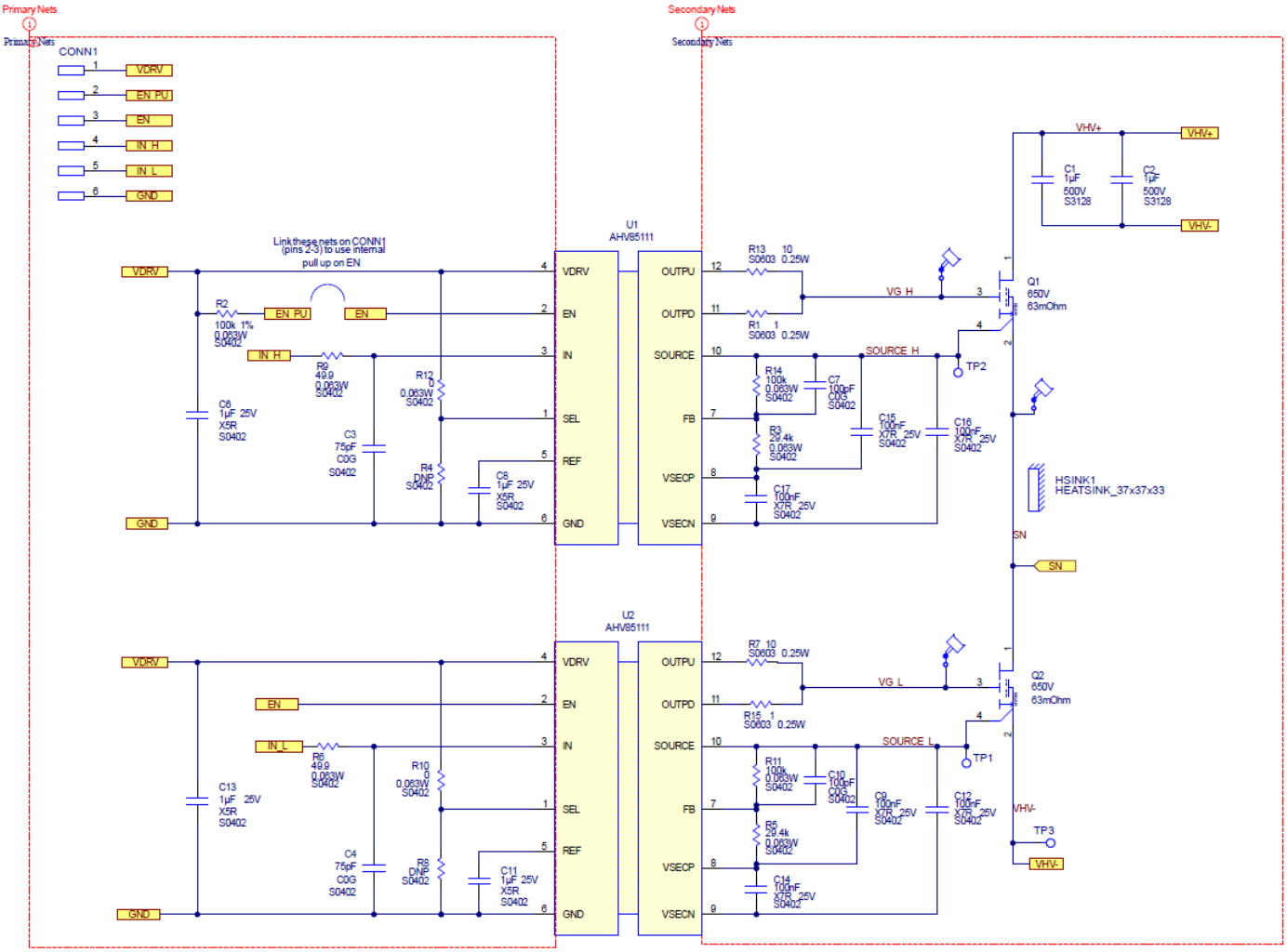

Figure 11: APEK85111KNH-02-T-MH Schematic

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PCB LAYOUT

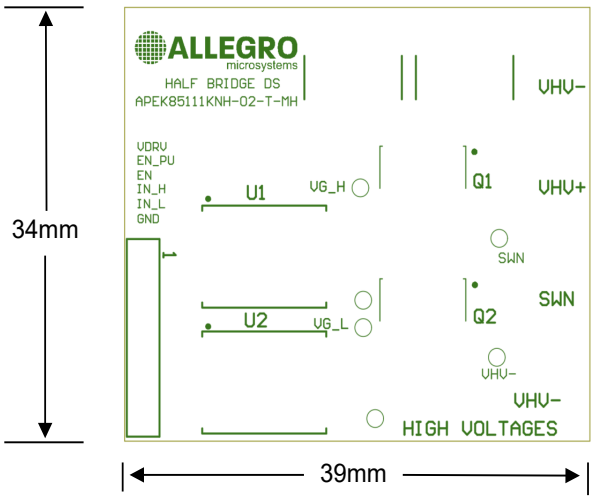

Figure 12: APEK85111KNH-02-T-MH Top Overlay

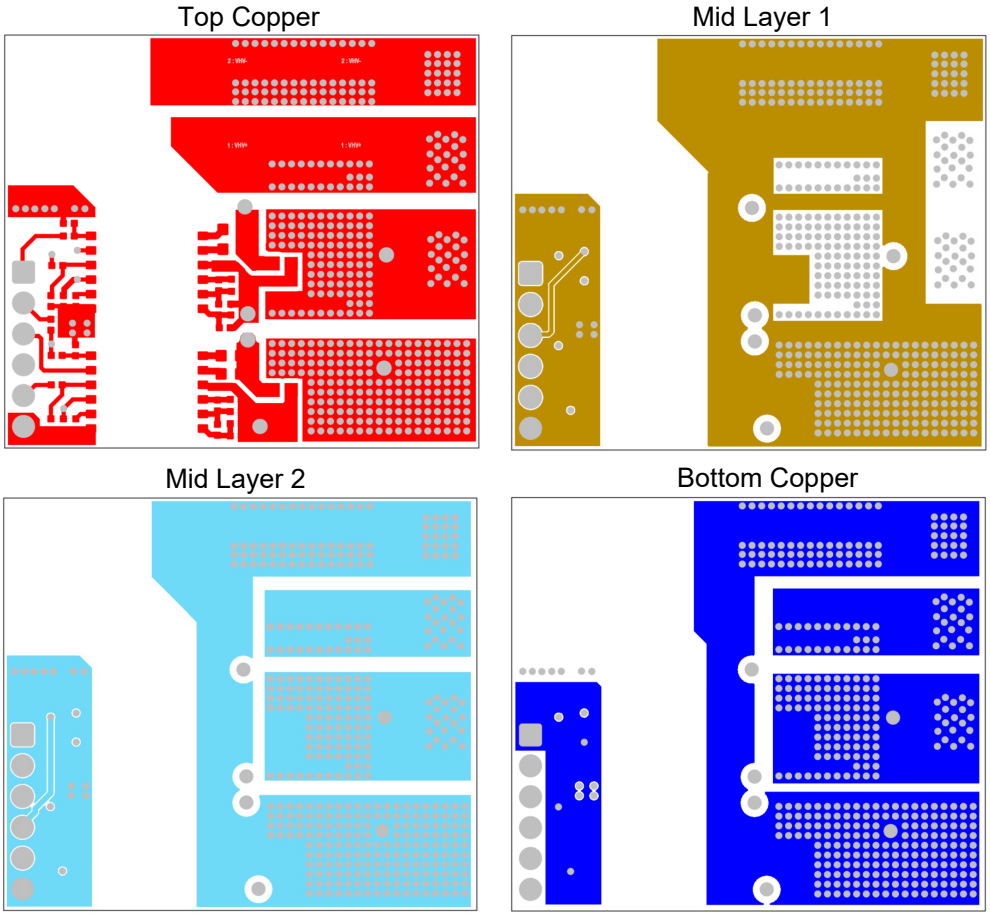

Figure 13: APEK85111KNH-02-T-MH PCB Copper Layers

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BILL OF MATERIALS

Table 1: APEK85111KNH-02-T-MH Evaluation Board Bill of Materials

Ref Name	Description	Value	Qty	Manufacturer	Manufacturer PN
C1, C2	CAP CERALINK, 1 µF,500 V PLZT	1 µF	2	TDK	B58031U5105M062
C3, C4	CAP, CER, 75 pF, 50 V, NP0, S0402	75 pF	2	MURATA	GCM1555C1H750FA16D
C6, C8, C11, C13	CAP, CER,1 µF,25 V, X5R, S0402	1 µF	4	MURATA	GRM155R61E105KA12D
C7, C10	CAP, CER, 100 pF,25 V, NP0, S0402	100 pF	2	AVX Interconnect	04023A101KAT2A
C9, C12, C14, C15, C16, C17	CAP, CER, 100 nF,16 V, X7R, S0402	100 nF	6	Yageo	CC0402KRX7R7BB104
CONN1	Header, 6-way, 2.54 mm	61300611121	1	Wurth Elektronik	61300611121
Q1, Q2	GaN FET GS66508B 650 V 30 A	GS66508B	2	GaN Systems	GS66508B-MR
R1, R15	RES, SMD, 1 Ω, 0.250 W, 1%, S0603	1 Ω ± 5%	2	ROHM	ESR03EZPJ1R0
R2, R11, R14	RES, SMD, 100 kΩ, 0.063 W, 1%, S0603	100 kΩ, 1%	3	Yageo / Phycomp	RC0402FR-07100KL
R3, R5	RES, SMD, 29.4 kΩ, 0.063 W, 1%, S0402	29.4 kΩ, 0.1%	2	Panasonic	ERA2AEB2942X
R4, R8	Not Installed	NA	2		
R6, R9	RES, SMD, 49.9 Ω, 0.063 W, 1%, S0402	49.9 Ω, 1%	2	Panasonic	ERJ2RKF49R9X
R7, R13	RES, SMD, 1 Ω, 0.250 W, 1%, S0603	10 Ω, 1%	2	BOURNS	CMP0603AFX-10R0ELF
R10, R12	RES, SMD, 0 Ω, 0.063 W, S0402	0 Ω	2	Panasonic	ERJ2GE0R00X
U1, U2	Single-Channel Isolated GaN FET Driver	AHV85111	2	Allegro MicroSystems	AHV85111KNHTR

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Revision History

Number	Date	Description
–	September 28, 2023	Initial release
1	February 15, 2024	Updated figures 1 and 2 (pages 1 and 3) and Bill of Materials (page 12)
2	July 10, 2024	Updated status for publishing to web

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