Revision History

AS4C128M32MD2 - 134 ball FBGA PACKAGE

Revision	Details	Date
Rev 1.0	Preliminary datasheet	Jun 2016

Specifications

- Density : 4G bits
- Organization :
  - 16M words x 32 bits x 8 banks
- Package :
  - 134-ball FBGA
  - Lead-free (RoHS compliant) and Halogen-free
- Power supply :
  - VDD1 = 1.8V (1.7V~1.95V)
  - VDD2/VDDQ/VDDCA = 1.2V (1.14V~1.3V)
- HSUL_12 interface (High Speed Unterminated Logic 1.2V)
- Data rate :
  - 1066Mbps RL=8
- Burst lengths (BL) : 4, 8 and 16
- Burst type (BT) : Sequential and interleave
- Read Latency (RL) : 3, 4, 5, 6, 7, 8
- Write Latency (WL) : 1, 2, 3, 4
- Output driver impedance: 34.3/40/48/60/80/120 Ω
- Operating case temperature range
  - Commercial Tc = -25°C to +85°C
  - Industrial Tc = -40°C to +85°C

Features

- JEDEC LPDDR2-S4B compliance
- Low power consumption
- Four-bit prefetch DDR architecture
- Eight internal banks for concurrent operation
- Double data rate architecture for command, address and data Bus
- Bidirectional and differential data strobe per byte of data (DQS and $\overline{DQS}$)
- DQS is edge-aligned with data for READs, center-aligned with data for WRITEs
- Differential clock inputs (CK and $\overline{CK}$)
- Data mask (DM) for write data
- Programmable READ and WRITE latencies (RL/WL)
- Auto Refresh and Self Refresh
- Per-bank refresh for concurrent operation
- Partial-array self refresh (PASR)
- On-chip temperature sensor to control self refresh rate for temperature compensated self refresh (TCSR)
- Deep power-down mode (DPD)
- Selectable output drive strength (DS)
- Clock stop capability
- DQ calibration offering specific DQ output patterns
- ZQ calibration

Table 1. Ordering Information

Part Number	Org	Temperature	MaxClock (MHz)	Package
AS4C128M32MD2-18BCN	128Mx32	Commercial -25°C to +85°C	533	134-ball FBGA
AS4C128M32MD2-18BIN	128Mx32	Industrial -40°C to +85°C	533	134-ball FBGA

Table 2. Speed Grade Information

Speed Grade	Clock Frequency	RL	tRCD (ns)	tRP (ns)
DDR2L-1066	533MHz	8	18	18

Pin Configurations - 11.5mmX11.5mm 134B FBGA

<Top View>

	1	2	3	4	5	6	7	8	9	10	
A	DNU	DNU	NB	NB	NB	NB	NB	NB	DNU	DNU	A
B	DNU	NC	NC	NB	VDD2	VDD1	DQ31	DQ29	DQ26	DNU	B
C	VDD1	VSS	NC	NB	VSS	VSS	VDDQ	DQ25	VSS	VDDQ	C
D	VSS	VDD2	ZQ	NB	VDDQ	DQ30	DQ27	DQS3	$\overline{DQS3}$	VSS	D
E	VSS	CA9	CA8	NB	DQ28	DQ24	DM3	DQ15	VDDQ	VSS	E
F	VDDCA	CA6	CA7	NB	VSS	DQ11	DQ13	DQ14	DQ12	VDDQ	F
G	VDD2	CA5	VREFCA	NB	$\overline{DQS1}$	DQS1	DQ10	DQ9	DQ8	VSS	G
H	VDDCA	VSS	$\overline{CK}$	NB	DM1	VDDQ	NB	NB	NB	NB	H
J	VSS	NC	CK	NB	VSS	VDDQ	VDD2	VSS	VREFDQ	NB	J
K	CKE	NC	NC	NB	DM0	VDDQ	NB	NB	NB	NB	K
L	$\overline{CS}$	NC	NC	NB	$\overline{DQS0}$	DQS0	DQ5	DQ6	DQ7	VSS	L
M	CA4	CA3	CA2	NB	VSS	DQ4	DQ2	DQ1	DQ3	VDDQ	M
N	VSS	VDDCA	CA1	NB	DQ19	DQ23	DM2	DQ0	VDDQ	VSS	N
P	VSS	VDD2	CA0	NB	VDDQ	DQ17	DQ20	DQS2	$\overline{DQS2}$	VSS	P
R	VDD1	VSS	NC	NB	VSS	VSS	VDDQ	DQ22	VSS	VDDQ	R
T	DNU	NC	NC	NB	VDD2	VDD1	DQ16	DQ18	DQ21	DNU	T
U	DNU	DNU	NB	NB	NB	NB	NB	NB	DNU	DNU	U
	1	2	3	4	5	6	7	8	9	10	

NB (No Ball)
DNU (Do Not Use)
NC (No Connect)

4Gb LPDDR2 SDRAM Signals and Addressing

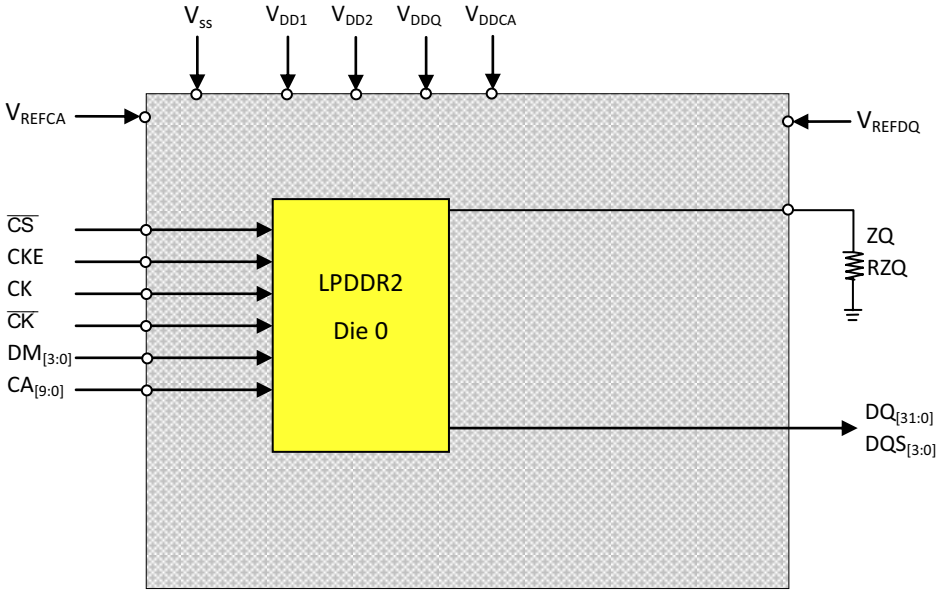
Configuration	**128Mb x 32**
DQ	[31:0]
DQS / DM	[3:0] / [3:0]
CA	[9:0]
Bank Address	BA0 ~ BA2
Row Address	R0 ~ R13
Column Address	C0 ~ C9

Signal Pin Description

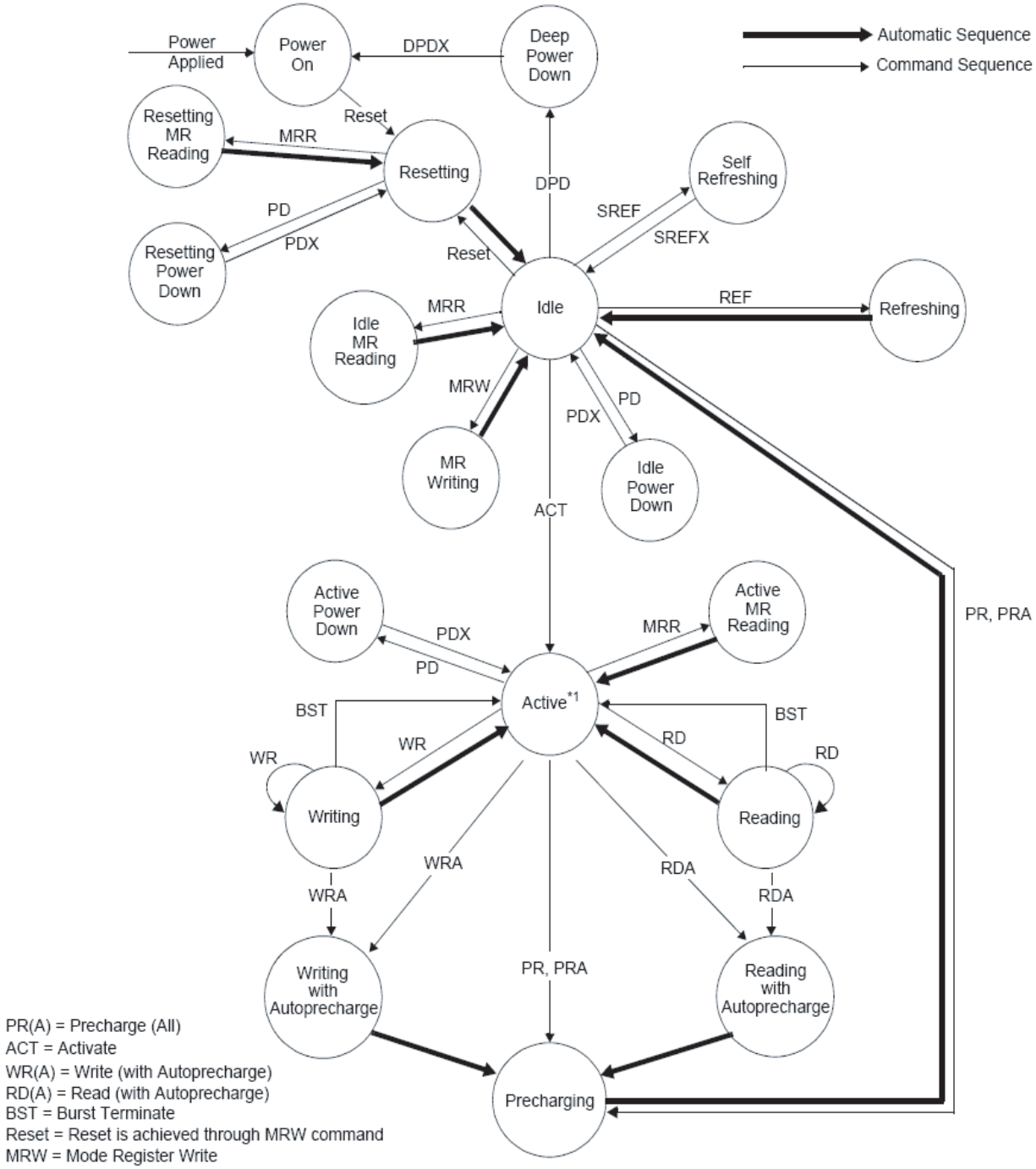
Pin	Type	Function
CK, $\overline{CK}$ (CK, CK#) (CK_t, CK_c)	Input	**Clock :** CK and $\overline{CK}$ are differential clock inputs. All CA inputs are sampled onboth rising and falling edges of CK. CS and CKE inputs are sampled at the risingedge of CK. AC timings are referenced to clock.
CKE	Input	**Clock Enable :** CKE HIGH activates and CKE LOW deactivates the internal clocksignals, input buffers, and output drivers. Power-saving modes are entered andexited via CKE transitions. CKE is considered part of the command code. CKE issampled at the rising edge of CK.
$\overline{CS}$ (CS#) (CS_n)	Input	**Chip Select :** $\overline{CS}$ is considered part of the command code and is sampled at therising edge of CK.
CA0~CA9	Input	**Command/address inputs:** Provide the command and address inputs accordingto the command truth table.
DM0~DM3	Input	**Input Data Mask :** DM is an input mask signal for write data. Although DM ballsare input-only, the DM loading is designed to match that of DQ and DQS balls.DM[3:0] is DM for each of the four data bytes, respectively.
DQ0~DQ31	Input/output	**Data input/output:** Bidirectional data bus.
DQS[3:0] (DQS_t[3:0]), $\overline{DQS}$[3:0] DQS#[3:0] (DQS_c[3:0])	Input/output	**Data strobe:** The data strobe is bidirectional (used for read and write data) andcomplementary (DQS and $\overline{DQS}$). It is edge-aligned output with read data and centered input with write data. DQS[3:0]/ $\overline{DQS}$[3:0] is DQS for each of the four data bytes, respectively.
NC		**No Connect:** No internal electrical connection is present.
ZQ	Input	**External impedance (240 ohm):** This signal is used to calibrate the device out-put impedance.
VDD1	Supply	**Core power:** Supply 1.
VDD2	Supply	**Core power:** Supply 2.
VDDQ	Supply	**DQ power supply:** Isolated on the die for improved noise immunity.
VDDCA	Supply	**Command/address power supply:** Command/address power supply.
VREFDQ, VREFCA	Supply	**Reference voltage:** VREFCA is reference for command/address input buffers,VREFDQ is reference for DQ input buffers.
VSS	Supply	**Common ground**

Functional Block Diagram

128Mb X 32 LPDDR2



Simplified State Diagram



PR(A) = Precharge (All)
ACT = Activate
WR(A) = Write (with Autoprecharge)
RD(A) = Read (with Autoprecharge)
BST = Burst Terminate
Reset = Reset is achieved through MRW command
MRW = Mode Register Write
MRR = Mode Register Read
PD = Enter Power Down
PDX = Exit Power Down
SREF = Enter Self Refresh
SREFX = Exit Self Refresh
DPD = Enter Deep Power Down
DPDX = Exit Deep Power Down
REF = Refresh

Basic Functionality

LPDDR2-S4 uses the double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank/Row Buffer information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock. Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

To achieve high-speed operation, our LPDDR2-S4 SDRAM uses the double data rate architecture and adopt 4n-prefetch interface designed to transfer two data per clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single 4n-bit wide, one clock cycle data transfer at the internal SDRAM core and four corresponding n-bit wide, one-half-clock-cycle data transfer at the I/O pins. Read and write accesses to the LPDDR2-S4 are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

For LPDDR2-S4 devices, accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Active command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access. As with standard DDR SDRAMs, the pipelined, multibank architecture of the LPDDR2-S4 SDRAMs supports concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power saving power-down mode. Deep power-down mode is offered to achieve maximum power reduction by eliminating the power of the memory array. Data will not be retained after device enters deep power-down mode. Two self refresh features, temperature-compensated self refresh (TCSR) and partial array self refresh (PASR), offer additional power saving. TCSR is controlled by the automatic on-chip temperature sensor. The PASR can be customized using the extended mode register settings. The two features may be combined to achieve even greater power saving. The DLL that is typically used on standard DDR devices is not necessary on the LPDDR2-S4 SDRAM. It has been omitted to save power.

Prior to normal operation, the LPDDR2-S4 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Power-Up, Initialization, and Power-Off

LPDDR2 devices must be powered up and initialized in a predefined manner. Power-up and initialization by means other than those specified will result in undefined operation.

Power Ramp and Device Initialization

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory and applies to devices.

Voltage Ramp:

While applying power (after Ta), CKE must be held LOW (=<0.2 x VDDCA), and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW. Following the completion of the voltage ramp (Tb), CKE must be maintained LOW. DQ, DM, DQS and DQS voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latch up. CK, CK, CS, and CA input levels must be between VSSCA and VDDCA during voltage ramp to avoid latch-up.

The following conditions apply:

Ta is the point where any power supply first reaches 300 mV.

After Ta is reached, VDD1 must be greater than VDD2 - 200 mV.

After Ta is reached, VDD1 and VDD2 must be greater than VDDCA - 200 mV.

After Ta is reached, VDD1 and VDD2 must be greater than VDDQ - 200 mV.

After Ta is reached, VREF must always be less than all other supply voltages.

The voltage difference between any of VSS, VSSQ, and VSSCA pins may not exceed 100 mV.

Tb is the point when all supply voltages are within their respective min/max operating conditions. Reference voltages shall be within their respective min/max operating conditions a minimum of 5 clocks before CKE goes high.

Power ramp duration tINIT0 (Tb - Ta) must be no greater than 20 ms.

For supply and reference voltage operating conditions, see DC power table.

Beginning at Tb, CKE must remain LOW for at least Tinit1 = 100 ns, after which CKE can be asserted HIGH. The clock must be stable at least Tinit2 = 5 x Tck prior to the first CKE LOW-to-HIGH transition (Tc). CKE, CS, and CA inputs must observe setup and hold requirements (Tis, Tih) with respect to the first rising clock edge (as well as to subsequent falling and rising edges).

If any MRRs are issued, the clock period must be within the range defined for tCKb (18ns to 100ns). MRWs can be issued at normal clock frequencies as long as all AC timings are met. Some AC parameters (for example, Tdqsck) could have relaxed timings (such as tDQSCKb) before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least Tinit3 = 200us (Td).

RESET Command:

After Tinit3 is satisfied, the MRW RESET command must be issued (Td). An optional PRECHARGE ALL command can be issued prior to the MRW RESET command. Wait at least Tinit4=1us while keeping CKE asserted and issuing NOP commands.

MRRs and Device Auto Initialization (DAI) Polling:

After Tinit4 is satisfied (Te), only MRR commands and power-down entry/exit commands are supported. After Te, CKE can go LOW in alignment with power-down entry and exit specifications. Use the MRR command to poll the DAI bit and report when device auto initialization is complete; otherwise, the controller must wait a minimum of Tinit5, or until the DAI bit is set before proceeding. As the memory output buffers are not properly configured by Te, some AC parameters must have relaxed timings before the system is appropriately configured. After the DAI bit (MR0, DAI) is set to zero by the memory device (DAI complete), the device is in the idle state (Tf). DAI status can be determined by issuing the MRR command to MR0. The device sets the DAI bit no later than Tinit5 after the RESET command. The controller must wait at least Tinit5 or until the DAI bit is set before proceeding.

ZQ Calibration:

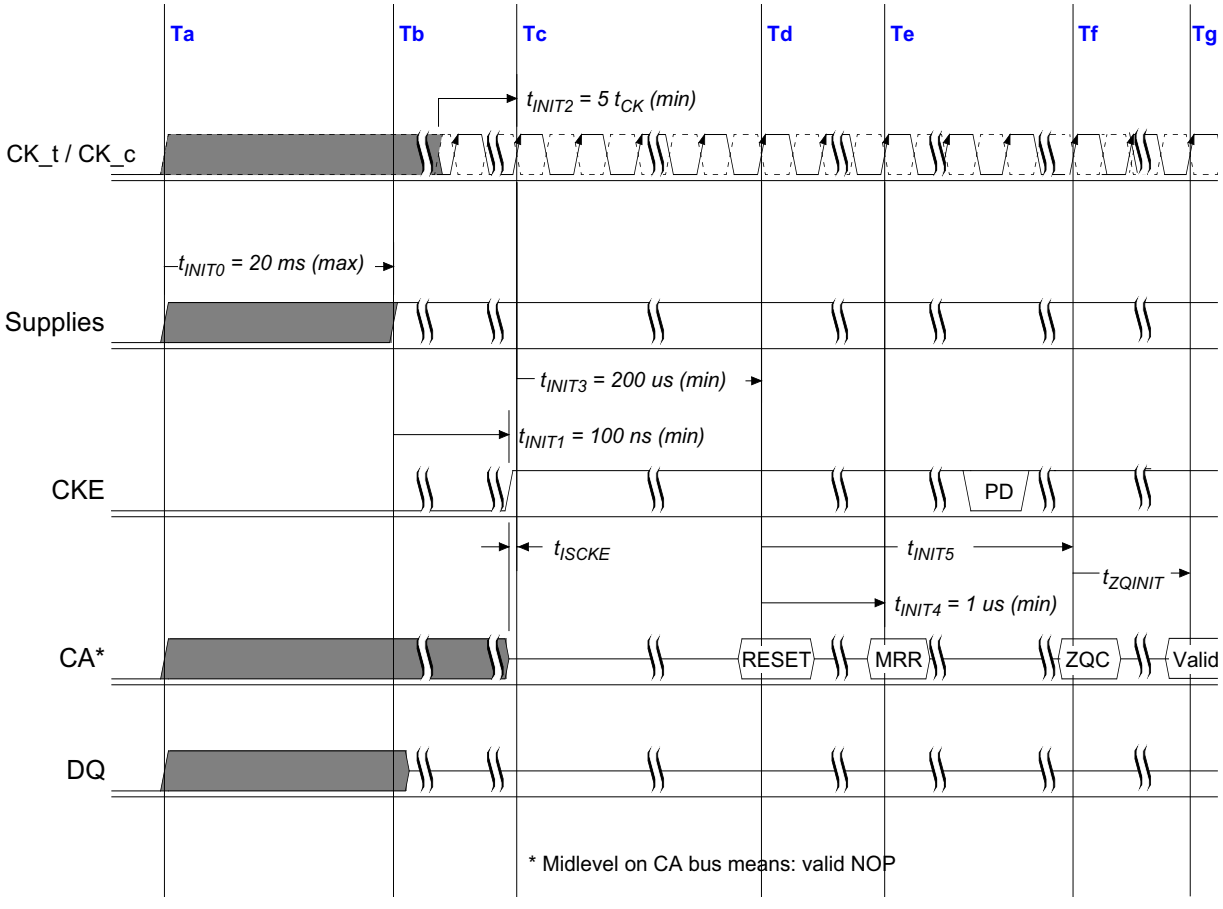
After Tinit5 (Tf), the MRW initialization calibration (ZQ_CAL) command can be issued to the memory (MR10). For LPDDR2 devices that do not support ZQ calibration, this command will be ignored. This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one LPDDR2 device exists on the same bus, the controller must not overlap MRW ZQ_CAL commands. The device is ready for normal operation after Tzqinit.

Normal Operation:

After Tzqinit (Tg), MRW commands must be used to properly configure the memory (for example the output buffer drive strength, latencies, etc.). Specifically, MR1, MR2, and MR3 must be set to configure the memory for the target frequency and memory configuration.After the initialization sequence is complete, the device is ready for any valid command. After Tg, the clock frequency can be changed using the procedure described in “Input Clock Frequency Changes and Clock Stop Events”.

Power Ramp and Initialization Sequence

Symbol	Value		Unit	Comment
	min	max		
t_{INIT0}		20	ms	Maximum Power Ramp Time
t_{INIT1}	100		ns	Minimum CKE low time after completion of power ramp
t_{INIT2}	5		tCK	Minimum stable clock before first CKE high
t_{INIT3}	200		µs	Minimum Idle time after first CKE assertion
t_{INIT4}	1		µs	Minimum Idle time after Reset command
t_{INIT5}		S: 10	µs	Maximum duration of Device Auto-Initialization
		N: vendor	µs	
t_{ZQINIT}	1		µs	ZQ Initial Calibration for LPDDR2-S4 and LPDDR2-N devices
t_{CKb}	18	100	ns	Clock cycle time during boot



Initialization after RESET (without voltage ramp)

If the RESET command is issued before or after the power-up initialization sequence, the re-initialization procedure must begin at Td.

Power-Off Sequence

Use the following sequence to power off the device. Unless specified otherwise, this procedure is mandatory and applies to devices. While powering off, CKE must be held LOW (=< 0.2 x VDDCA); all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW.

DQ, DM, DQS, and $\overline{\text{DQS}}$ voltage levels must be between VSSQ and VDDQ during the power-off sequence to avoid latch-up. CK, $\overline{\text{CK}}$, $\overline{\text{CS}}$, and CA input levels must be between VSSCA and VDDCA during the power-off sequence to avoid latch-up.

Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition table.
Tz is the point where all power supplies are below 300 mV. After Tz, the device is powered off.
The time between Tx and Tz (tPOFF) shall be less than 2s.

The following conditions apply:
Between Tx and Tz, VDD1 must be greater than VDD2 - 200 mV.
Between Tx and Tz, VDD1 and VDD2 must be greater than VDDCA - 200 mV.
Between Tx and Tz, VDD1 and VDD2 must be greater than VDDQ - 200 mV.
Between Tx and Tz, VREF must always be less than all other supply voltages.
The voltage difference between any of VSS, VSSQ, and VSSCA pins may not exceed 100 mV.

Symbol	Value		Unit	Comment
	min	max		
tPOFF	-	2	S	Maximum Power-off ramp time

Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system. After Tz (the point at which all power supplies first reach 300Mv), the device must power off. The time between Tx and Tz must not exceed 2s. During this period, the relative voltage between power supplies is uncontrolled. VDD1 and VDD2 must decrease with a slope lower than 0.5 V/us between Tx and Tz. An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Mode Register Definition

LPDDR2 devices contain a set of mode registers used for programming device operating parameters, reading device information and status, and for initiating special operations such as DQ calibration, ZQ calibration, and device reset.

Mode Register Assignment and Definition

Table below shows the mode registers for LPDDR2 SDRAM. Each register is denoted as “R”, if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written. Mode Register Read Command shall be used to read a register. Mode Register Write Command shall be used to write a register.

Mode Register Assignment

MR#	MA<0:7>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
00	00_H	Device Info.	R	(RFU)						DA	DAI
01	01_H	Device Feature1	W	nWR (for AP)			WC	BT	BL		
02	02_H	Device Feature2	W	(RFU)				RL & WL			
03	03_H	I/O Config-1	W	(RFU)				DS			
04	04_H	Refresh Rate	R	TUF	(RFU)				Refresh Rate		
05	05_H	Basic Config-1	R	LPDDR2 Manufacturer ID							
06	06_H	Basic Config-2	R	Revision ID1							
07	07_H	Basic Config-3	R	Revision ID2							
08	08_H	Basic Config-4	R	I/O width		Density				Type	
09	09_H	Test Mode	W	Vendor-Specific Test Mode							
10	$0A_H$	IO Calibration	W	Calibration Code							
11~15	$0B_H$~$0F_H$	(reserved)		(RFU)							
16	10_H	PASR_BANK	W	Bank Mask							
17	11_H	PASR_Seg	W	Segment Mask							
18~19	12_H~13_H	(Reserved)		(RFU)							
20~31	18_H~$1F_H$	Reserved for NVM									
32	20_H	DQ calibration pattern A	R	See “Data Calibration Pattern Description”							
33~39	21_H~27_H	(Do Not Use)									
40	28_H	DQ calibration pattern B	R	See “Data Calibration Pattern Description”							
41~47	29_H~$2F_H$	(Do Not Use)									
48~62	30_H~$3E_H$	(Reserved)		(RFU)							
63	$3F_H$	Reset	W	X							
64~126	40_H~$7E_H$	(Reserved)		(RFU)							
127	$7F_H$	(Do Not Use)									
128~190	80_H~BE_H	(Reserved)		(RFU)							

MR#	MA<0:7>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
191	BF_H	(Do Not Use)									
192~254	$C0_H$~FE_H	(Reserved)		(RFU)							
255	FF_H	(Do Not Use)									

Notes:
1. RFU bits shall be set to “0” during Mode Register writes.
2. RFU bits shall be read as “0” during Mode Register reads.
3. All Mode Registers from that are specified as RFU or write-only shall return undefined data when read and DQS shall be toggled.
4. All Mode Registers that are specified as RFU shall not be written.
5. Writes to read-only registers shall have no impact on the functionality of the device.

MR0_Device Information (MA<7:0> = 00H)

MR#	MA<0:7>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
00	00_H	Device Info.	R	(RFU)						DA	DAI

OP0	DI (Device Information)	Read-only	0B: DAI complete 1B: DAI still in progress
OP1	DAI (Device Auto-Initialization Status)	Read-only	0B: S2 or S4 SDRAM 1B: Do Not Use

MR1_Device Feature 1 (MA<7:0> = 01H)

MR#	MA<0:7>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
01	01_H	Device Feature1	W	nWR (for AP)			WC	BT	BL		

OP<2:0>	BL (Burst Length)	Write-only	010B: BL4 (default) 011B: BL8 100B: BL16 All others: reserved
OP3	BT*1 (Burst Type)	Write-only	0B: Sequential (default) 1B: Interleaved (allowed for SDRAM only)
OP4	WC (Wrap)	Write-only	0B: Wrap (default) 1B: No wrap (allowed for SDRAM BL4 only)
OP<7:5>	nWR*2	Write-only	001B: nWR=3 (default) 010B: nWR=4 011B: nWR=5 100B: nWR=6 101B: nWR=7 110B: nWR=8 All others: reserved

Notes:

1. BL16, interleaved is not an official combination to be supported.
2. Programmed value in Nwr register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).

Burst Sequence by BL, BT, and WC

C3	C2	C1	C0	WC	BT	BL	Burst Cycle Number and Burst Address Sequence															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
X	X	0_B	0_B	wrap	any	4	0	1	2	3												
X	X	1_B	0_B				2	3	0	1												
X	X	X	0_B	nw	any		y	y+1	y+2	y+3												
X	0_B	0_B	0_B	wrap	seq	8	0	1	2	3	4	5	6	7								
X	0_B	1_B	0_B				2	3	4	5	6	7	0	1								
X	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
X	1_B	1_B	0_B				6	7	0	1	2	3	4	5								
X	0_B	0_B	0_B		int		0	1	2	3	4	5	6	7								
X	0_B	1_B	0_B				2	3	0	1	6	7	4	5								
X	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
X	1_B	1_B	0_B				6	7	4	5	2	3	0	1								
X	X	X	0_B	nw	any		**illegal (not allowed)**															
0_B	0_B	0_B	0_B	wrap	seq	16	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0_B	0_B	1_B	0_B				2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
0_B	1_B	0_B	0_B				4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
0_B	1_B	1_B	0_B				6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
1_B	0_B	0_B	0_B				8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1_B	0_B	1_B	0_B				A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
1_B	1_B	0_B	0_B				C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
1_B	1_B	1_B	0_B				E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
X	X	X	0_B		int		**illegal (not allowed)**															
X	X	X	0_B	nw	any		**illegal (not allowed)**															

Notes:

1. C0 input is not present on CA bus. It is implied zero.
2. For BL=4, the burst address represents C1 - C0.
3. For BL=8, the burst address represents C2 - C0.
4. For BL=16, the burst address represents C3 - C0.
5. For no-wrap, BL4, the burst must not cross the page boundary or the sub-page boundary. The variable y can start at any address with C0 equal to 0, but must not start at any address shown bellow.

Non-Wrap Restrictions

	64Mb	128Mb/256Mb	512Mb/1Gb/2Gb	4Gb/6Gb/8Gb
Not across full page boundary				
x8	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001	7FE, 7FF, 000, 001	FFE, FFF, 000, 001
x16	FE, FF, 00, 01	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001	7FE, 7FF, 000, 001
x32	7E, 7F, 00, 01	FE, FF, 00, 01	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001
Not across sub page boundary				
x8	07E, 07F, 080, 081 0FE, 0FF, 100, 101 17E, 17F, 180, 181	0FE, 0FF, 100, 101 1FE, 1FF, 200, 201 2FE, 2FF, 300, 301	1FE, 1FF, 200, 201 3FE, 3FF, 400, 401 5FE, 5FF, 600, 601	3FE, 3FF, 400, 401 7FE, 7FF, 800, 801 BFE, BFF, C00, C01
x16	7E, 7F, 80, 81	0FE, 0FF, 100, 101	1FE, 1FF, 200, 201	3FE, 3FF, 400, 401
x32	None	None	None	None

Notes: Non-wrap BL= 4 data orders shown are prohibited.

MR2_Device Feature 2 (MA<7:0> = 02H)

MR#	MA<0:7>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
02	02_H	Device Feature2	W	(RFU)				RL & WL			

OP<3:0>	RL & WL (Read Latency & Write Latency)	Write-only	0001B: RL = 3 / WL = 1 (default) 0010B: RL = 4 / WL = 2 0011B: RL = 5 / WL = 2 0100B: RL = 6 / WL = 3 0101B: RL = 7 / WL = 4 0110B: RL = 8 / WL = 4 All others: reserved

MR3_I/O Configuration 1 (MA<7:0> = 03H)

MR#	MA<0:7>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
03	03_H	I/O Config-1	W	(RFU)				DS			

OP<3:0>	DS (Drive Strength)	Write-only	0000B: reserved 0001B: 34.3-ohm typical 0010B: 40-ohm typical (default) 0011B: 48-ohm typical 0100B: 60-ohm typical 0101B: reserved 0110B: 80-ohm typical 0111B: 120-ohm typical All others: reserved

MR4_Device Temperature (MA<7:0> = 04H)

MR#	MA<0:7>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
04	04_H		R	TUF	(RFU)				Refresh Rate		

OP<2:0>	Refresh Rate	Read-only	000B: SDRAM Low temperature operating limit exceeded 001B: 4x tREFI, 4x tREFIpb, 4x tREFW 010B: 2x tREFI, 2x tREFIpb, 2x tREFW 011B: 1x tREFI, 1x tREFIpb, 1x tREFW (<=85'C) 100B: Reserved 101B: 0.25x tREFI, 0.25x tREFIpb, 0.25x tREFW, do not de-rate SDRAM AC timing 110B: 0.25x tREFI, 0.25x tREFIpb, 0.25x tREFW, de-rate SDRAM AC timing 111B: SDRAM High temperature operating limit exceeded
OP7	TUF (Temperature Update Flag)	Read-only	0B: OP<2:0> value has not changed since last read of MR4. 1B: OP<2:0> value has changed since last read of MR4.

Notes:
1. A Mode Register Read from MR4 will reset OP7 to "0".
2. OP7 is reset to "0" at power-up.
3. If OP2 equals "1", the device temperature is greater than 85'C.
4. OP7 is set to "1", if OP2~OP0 has changed at any time since the last read of MR4.
5. LPDDR2 might not operate properly when OP<2:0> = 000B or 111B.
6. For specified operating temperature range and maximum operating temperature.
7. LPDDR2 devices must be derated by adding 1.875ns to the following core timing parameters: Trcd, Trc, Tras, Trp, and Trrd. The Tdqsck parameter must be derated .. Prevailing clock frequency specifications and related setup and hold timings remain unchanged.
8. The recommended frequency for reading MR4 is provided in "Temperature Sensor".

MR5_Basic Configuration 1 (MA<7:0> = 05H)

MR#	MA<0:7>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
05	05_H	Basic Config-1	R	LPDDR2 Manufacturer ID							

OP<7:0>	Manufacturer ID	Read-only	See JESD-TBD LPDDR2 Manufacturer ID encodings

MR6_Basic Configuration 2 (MA<7:0> = 06H)

MR#	MA<0:7>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
06	06_H	Basic Config-2	R	Revision ID1							

OP<7:0>	Revision ID1	Read-only	Reserved

MR7_Basic Configuration 3 (MA<7:0> = 07H)

MR#	MA<0:7>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
07	07_H	Basic Config-3	R	Revision ID2							

OP<7:0>	Revision ID1	Read-only	Reserved

MR8_Basic Configuration 4 (MA<7:0> = 08H)

MR#	MA<0:7>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
08	08_H	Basic Config-4	R	I/O width		Density				Type	

OP<1:0>	Type	Read-only	00B: S4 SDRAM 01B: S2 SDRAM 10B: N NVM 11B: Reserved
OP<5:2>	Density	Read-only	0000B: 64Mb 0001B: 128Mb 0010B: 256Mb 0011B: 512Mb 0100B: 1Gb 0101B: 2Gb 0110B: 4Gb 1110B: 6Gb 0111B: 8Gb 1000B: 16Gb 1001B: 32Gb All others: reserved
OP<7:6>	I/O width	Read-only	00B: x32 01B: x16 10B: x8 11B: not used

MR9_Test Mode (MA<7:0> = 09H)

MR#	MA<0:7>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
09	09_H	Test Mode	W	Vendor-Specific Test Mode							

OP<7:0>	Vendor-Specific Test Mode	Write-only	

MR10_Calibration (MA<7:0> = 0AH)

MR#	MA<0:7>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
10	$0A_H$	IO Calibration	W	Calibration Code							

OP<7:0>	Calibration Code	Write-only	0xFF: Calibration command after initialization 0xAB: Long calibration 0x56: Short calibration 0xC3: ZQ Reset All others: Reserved

Notes:
1. Host processor shall not write MR10 with “Reserved” values.
2. LPDDR2 devices shall ignore calibration command, when a “Reserved” values is written into MR10.
3. See AC timing table for the calibration latency.
4. If ZQ is connected to VSSCA through RZQ, either the ZQ calibration function (see “MRW ZQ Calibration Command”) or default calibration (through the ZQ RESET command) is supported. If ZQ is connected to VDDCA, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection must not change after power is supplied to the device.
5. Devices that do not support calibration ignore the ZQ calibration command.
6. Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

MR11:15_(Reserved) (MA<7:0> = 0BH- 0FH)

MR#	MA<0:7>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
11~15	$0B_H$~$0F_H$	(reserved)		(RFU)							

OP<7:0>	RFU		

MR16_PASR_Bank Mask (MA<7:0> = 010H)

MR#	MA<0:7>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
16	10_H	PASR_BANK	W	Bank Mask							

OP<7:0>	Bank Mask Code	Write-only	0B: refresh enable to the bank (=unmasked, default) 1B: refresh blocked (=masked)

OP	Bank Mask	4 Bank	8 Bank
0	XXXXXXX1	Bank 0	Bank 0
1	XXXXXX1X	Bank 1	Bank 1
2	XXXXX1XX	Bank 2	Bank 2
3	XXXX1XXX	Bank 3	Bank 3
4	XXX1XXXX	-	Bank 4
5	XX1XXXXX	-	Bank 5
6	X1XXXXXX	-	Bank 6
7	1XXXXXXX	-	Bank 7

Notes: This table indicates tha range of row addresses in each masked segment. X is don't care for a particular segment.

MR17_PASR_Segment Mask (MA<7:0> = 011H)

MR#	MA<0:7>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
17	11_H	PASR_Seg	W	Segment Mask							

OP<7:0>	Segment Mask Code	Write-only	0B: refresh enable to the segment (=unmasked, default) 1B: refresh blocked (=masked)

Segment	OP	Segment Mask	1Gb	2Gb, 4Gb	8Gb
			R12:10	R13:11	R14:12
0	0	XXXXXXX1	000B		
1	1	XXXXXX1X	001B		
2	2	XXXXX1XX	010B		
3	3	XXXX1XXX	011B		
4	4	XXX1XXXX	100B		
5	5	XX1XXXXX	101B		
6	6	X1XXXXXX	110B		
7	7	1XXXXXXX	111B		

Notes: This table indicates the range of row addresses in each masked segment. X is don't care for a particular segment.

MR18:19_(Reserved) (MA<7:0> = 012H- 013H)

MR#	MA<0:7>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
18~19	12_H~13_H	(Reserved)		(RFU)							

OP<7:0>	RFU		

MR20:31_(Do Not Use) (MA<7:0> = 014H- 01FH)

MR#	MA<0:7>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
20~31	18_H~$1F_H$	Reserved for NVM									

OP<7:0>	Reserved for NVM		

MR32_DQ Calibration Pattern A (MA<7:0> = 020H)

MR#	MA<0:7>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
32	20_H	DQ calibration pattern A	R	See “Data Calibration Pattern Description”							

OP<7:0>	Reads to MR32 return DQ calibration pattern A	Read-only	

MR40_DQ Calibration Pattern B(MA<7:0> = 028H)

MR#	MA<0:7>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
40	28_H	DQ calibration pattern B	R	See “Data Calibration Pattern Description”							

OP<7:0>	Reads to MR40 return DQ calibration pattern B	Read-only	

MR63_Reset (MA<7:0> = 03FH): MRW only

MR#	MA<0:7>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
63	$3F_H$	Reset	W	X							

OP<7:0>	Reset	Write-only	X

Notes: For additional information on MRW RESET, see “Mode Register Write Command” on Timing Spec.

Do Not Use and Reserved functions

MR#	MA<0:7>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
33~39	21_H~27_H	(Do Not Use)									
41~47	29_H~$2F_H$	(Do Not Use)									
48~62	30_H~$3E_H$	(Reserved)		(RFU)							
64~126	40_H~$7E_H$	(Reserved)		(RFU)							
127	$7F_H$	(Do Not Use)									
128~190	80_H~BE_H	(Reserved)		(RFU)							
191	BF_H	(Do Not Use)									
192~254	$C0_H$~FE_H	(Reserved)		(RFU)							
255	FF_H	(Do Not Use)									

LPDDR2-S4 SDRAM Truth Table

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR2 device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

Command Truth Table

	SDR Command Pins			DDR CA pins (10)										
SDRAM command	CKE		CS_n	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CK EDGE
	CK_t(n-1)	CK_t(n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
				MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
				MA6	MA7	x								↓
Refresh (per bank)[11]	H	H	L	L	L	H	L	x						↑
				x										↓
Refresh (all bank)	H	H	L	L	L	H	H	x						↑
				x										↓
Enter Self Refresh	H	L	L	L	L	H	x							↑
				x										↓
Activate (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	↑
				R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	↓
Write (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
				AP[3,4]	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
Read (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
				AP[3,4]	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
Precharge (bank)	H	H	L	H	H	L	H	AB	x		BA0	BA1	BA2	↑
				x										↓
BST	H	H	L	H	H	L	L	x						↑
				x										↓
Enter Deep Power Down	H	L	L	H	H	L	x							↑
				x										↓
NOP	H	H	L	H	H	H	x							↑
				x										↓
Maintain PD, SREF, DPD (NOP)	L	L	L	H	H	H	x							↑
				x										↓
NOP	H	H	H	x										↑
				x										↓
Maintain PD, SREF, DPD (NOP)	L	L	H	x										↑
				x										↓
Enter Power Down	H	L	H	x										↑
				x										↓
Exit PD, SREF, DPD	L	H	H	x										↑
				x										↓

Notes:
1. All LPDDR2 commands are defined by states of CS_n($\overline{CS}$), CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
2. For LPDDR2 SDRAM, Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon.
3. AP "high" during a READ or WRITE command indicates that an auto-precharge will occur to the bank associated with the READ or WRITE command.
4. "x" means "H or L (but a defined logic level)".
5. Self refresh exit and Deep Power Down exit are asynchronous.
6. VREF must be between 0 and VDDQ during Self Refresh and Deep Down operation.
7. CAxr refers to command/address bit "x" on the rising edge of clock.
8. CAxf refers to command/address bit "x" on the rising edge of clock.
9. CS_n($\overline{CS}$) and CKE are sampled at the rising edge of clock.
10. Per Bank Refresh is only allowed in devices with 8 banks.
11. The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.

CKE Truth Table

Device Current State*3	CKE_{n-1}*1	CKE_n*1	CS_n*2	Command n*4	Operation n*4	Device Next State	Notes
Active Power Down	L	L	X	X	Maintain Active Power Down	Active Power Down	
	L	H	H	NOP	Exit Active Power Down	Active	6, 9
Idle Power Down	L	L	X	X	Maintain Idle Power Down	Idle Power Down	
	L	H	H	NOP	Exit Idle Power Down	Idle	6, 9
Resetting Power Down	L	L	X	X	Maintain Resetting Power Down	Resetting Power Down	
	L	H	H	NOP	Exit Resetting Power Down	Idle or Resetting	6, 9, 12
Deep Power Down	L	L	X	X	Maintain Deep Power Down	Deep Power Down	
	L	H	H	NOP	Exit Deep Power Down	Power On	8
Self Refresh	L	L	X	X	Maintain Self Refresh	Self Refresh	
	L	H	H	NOP	Exit Self Refresh	Idle	7, 10
Bank(s) Active	H	L	H	NOP	Enter Active Power Down	Active Power Down	
All Banks Idle	H	L	H	NOP	Enter Idle Power Down	Idle Power Down	
	H	L	L	Enter Self-Refresh	Enter Self Refresh	Self Refresh	
	H	L	L	Deep Power Down	Enter Deep Power Down	Deep Power Down	
Resetting	H	L	H	NOP	Enter Resetting Power Down	Resetting Power Down	
	H	H	Refer to the Command Truth Table				

Notes:

1. “CKEn” is the logic state of CKE at clock rising edge n; “CKEn-1” was the state of CKE at the previous clock edge.
2. “CS_n” is the logic state of CS_n at the clock rising edge n.
3. “Current state” is the state of the LPDDR2 device immediately prior to clock edge n.
4. “Command n” is the command registered at clock edge N, and “Operation n” is a result of “Command n".
5. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
6. Power Down exit time (tXP) should elapse before a command other than NOP is issued.
7. Self-Refresh exit time (tXSR) should elapse before a command other than NOP is issued.
8. The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.
9. The clock must toggle at least once during the tXP period.
10. The clock must toggle at least twice during the tXSR time.
11. "X" means "Don't care".
12. Upon exiting Resetting Power Down, the device will return to the Idle state if tINIT5 has expired.

Current State Bank n - Command to Bank n

Current State	Command	Operation	Next State	NOTES
Any	NOP	Continue previous operation	Current State	
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (Per Bank)	Begin to refresh	Refreshing (Per Bank)	6
	Refresh (All Bank)	Begin to refresh	Refreshing(All Bank)	7
	MRW	Load value to Mode Register	MR Writing	7
	MRR	Read value from Mode Register	Idle MR Reading	
	Reset	Begin Device Auto-Initialization	Resetting	7, 8
	Precharge	Deactivate row in bank or banks	Precharging	9, 15
Row Active	Read	Select column, and start read burst	Reading	
	Write	Select column, and start write burst	Writing	
	MRR	Read value from Mode Register	Active MR Reading	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading	Read	Select column, and start new read burst	Reading	10, 11
	Write	Select column, and start write burst	Writing	10, 11, 12
	BST	Read burst terminate	Active	13
Writing	Write	Select column, and start new write burst	Writing	10, 11
	Read	Select column, and start read burst	Reading	10, 11, 14
	BST	Write burst terminate	Active	13
Power On	Reset	Begin Device Auto-Initialization	Resetting	7, 9
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Notes:

1. The table applies when both CKEn-1 and CKEn are HIGH, and after tXSR or tXP has been met if the previous state was Power Down.
2. All states and sequences not shown are illegal or reserved.
3. Current State Definitions:

Idle: The bank or banks have been precharged, and tRP has been met.
Active: A row in the bank has been activated, and tRCD has been met. No data bursts / accesses and no register accesses are in progress.

Reading: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
Writing: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

4. The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable com-mands to the other bank should be issued on any clock edge occurring during these states.

Precharging: starts with the registration of a Precharge command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
Row Activating: starts with registration of an Activate command and ends when tRCD is met. Once tRCD is met, the bank will be in the 'Active' state.
Read with AP Enabled: starts with the registration of the Read command with Auto Precharge enabled and ends when tRP has been met. Once tRP has been met, the bank will be in the idle state.
Write with AP Enabled: starts with registration of a Write command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command; NOP commands must be applied to each pos-itive clock edge during these states.

Refreshing (Per Bank): starts with registration of an Refresh (Per Bank) command and ends when tRFCpb is met. Once tRFCpb is met, the bank will be in an 'idle' state.
Refreshing (All Bank): starts with registration of an Refresh (All Bank) command and ends when tRFCab is met. Once tRFCab is met, the device will be in an 'all banks idle' state.
Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.
Resetting MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Resetting state.
Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Active state.
MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.
Precharging All: starts with the registration of a Precharge-All command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.

6. Bank-specific; requires that the bank is idle and no bursts are in progress.
7. Not bank-specific; requires that all banks are idle and no bursts are in progress.
8. Not bank-specific reset command is achieved through Mode Register Write command.
9. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for pre-charging.
10. A command other than NOP should not be issued to the same bank while a Read or Write burst with Auto Precharge is enabled.
11. The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.
12. A Write command may be applied after the completion of the Read burst; otherwise, a BST must be used to end the Read prior to asserting a Write command.
13. Not bank-specific. Burst Terminate (BST) command affects the most recent read/write burst started by the most recent Read/Write command, regardless of bank.
14. A Read command may be applied after the completion of the Write burst; otherwise, a BST must be used to end the Write prior to asserting a Read command.
15. If a Precharge command is issued to a bank in the Idle state, tRP shall still apply.

Current State Bank n - Command to Bank m

Current State of Bank n	Command for Bank m	Operation	Next State for Bank m	NOTES
Any	NOP	Continue previous operation	Current State of Bank m	
Idle	Any	Any command allowed to Bank m	-	18
Row Activating, Active, or Precharging	Activate	Select and activate row in Bank m	Active	7
	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8
	Precharge	Deactivate row in bank or banks	Precharging	9
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Reading	10, 11, 13
	BST	Read or Write burst terminate an ongoing Read/Write from/to Bank m	Active	18
Reading (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8, 14
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	8, 16
	Write	Select column, and start write burst to Bank m	Writing	8
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	8, 15
	Write	Select column, and start write burst to Bank m	Writing	8, 14, 15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	8, 15, 16
	Write	Select column, and start write burst to Bank m	Writing	8, 15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Power On	Reset	Begin Device Auto-Initialization	Resetting	12, 17
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Notes:
1. The table applies when both CKEn-1 and CKEn are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.
2. All states and sequences not shown are illegal or reserved.
3. Current State Definitions:
Idle: the bank has been precharged, and tRP has been met.
Active: a row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
Reading: a Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
Writing: a Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4. Refresh, Self-Refresh, and Mode Register Write commands may only be issued when all bank are idle.
5. A Burst Terminate (BST) command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:

Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.
Resetting MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Resetting state.
Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Active state.
MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.

7. tRRD must be met between Activate command to Bank n and a subsequent Activate command to Bank m.
8. Reads or Writes listed in the Command column include Reads and Writes with Auto Precharge enabled and Reads and Writes with Auto Precharge disabled.
9. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for pre-charging.
10. MRR is allowed during the Row Activating state (Row Activating starts with registration of an Activate command and ends when tRCD is met.)
11. MRR is allowed during the Precharging state. (Precharging starts with registration of a Precharge command and ends when tRP is met.
12. Not bank-specific; requires that all banks are idle and no bursts are in progress.
13. The next state for Bank m depends on the current state of Bank m (Idle, Row Activating, Precharging, or Active). The reader shall note that the state may be in transition when a MRR is issued. Therefore, if Bank m is in the Row Activating state and Precharging, the next state may be Active and Precharge dependent upon tRCD and tRP respectively.
14. A Write command may be applied after the completion of the Read burst, otherwise a BST must be issued to end the Read prior to asserting a Write command.
15. Read with auto precharge enabled or a Write with auto precharge enabled may be followed by any valid command to other banks provided that the timing restriction.
16. A Read command may be applied after the completion of the Write burst; otherwise, a BST must be issued to end the Write prior to asserting a Read command.
17. Reset command is achieved through Mode Register Write command.
18. BST is allowed only if a Read or Write burst is ongoing.

Data Mask Truth Table

Name (Functional)	DM	DQs	Note
Write enable	L	Valid	1
Write inhibit	H	X	1

Notes:
1. Used to mask write data, provided coincident with the corresponding data.

COMMAND Definitions and Timing Diagrams

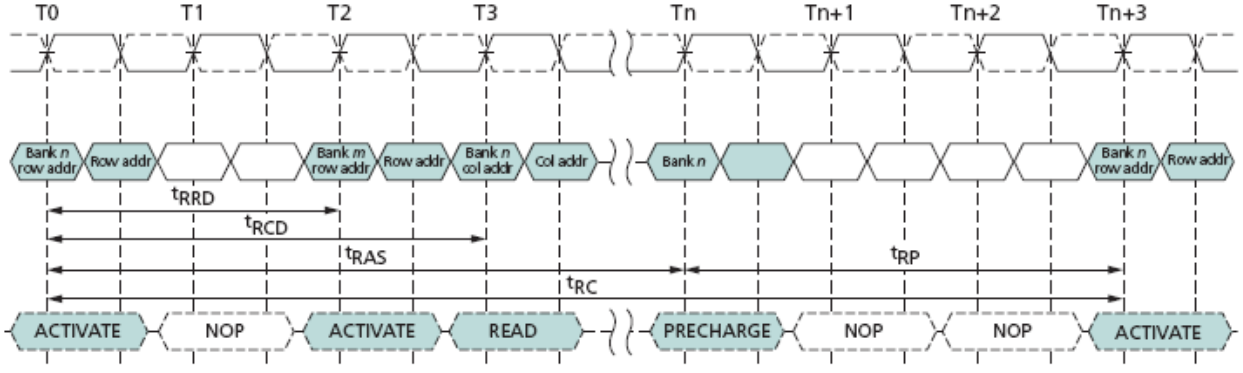
Active

The Active command is issued by holding $\overline{CS}$ LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA0-BA2 are used to select the desired bank. The row addresses R0-R14 is used to determine which row in the selected bank. The Active command must be applied before any Read or Write operation can be executed. The LPDDR2 SDRAM can accept a read or write command at time tRCD after the active command is sent. Once a bank has been active, it must be precharged before another Active command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between two successive ACTIVE commands on the same bank is determined by the RAS cycle time of the device (tRC). The minimum time interval between two successive ACTIVE commands on different banks is defined by tRRD.

Certain restriction on operation of the 8 bank devices must be observed. One for restricting the number of sequential Active commands that can be issued and another for allowing more time for RAS precharge for a Precharge All command. The rules are as follows:

8-bank device Sequential Bank Activation Restriction : No more than 4 banks may be activated (or refreshed, in the case of REFpb) in a rolling tFAW window. Converting to clocks is done by dividing tFAW[ns] by tCK[ns], and rounding up to next integer value. As an example of the rolling window, if RU{ (tFAW / tCK) } is 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued at or between clock N+1 and N+9. REFpb also counts as bank-activation for the purposes of tFAW.

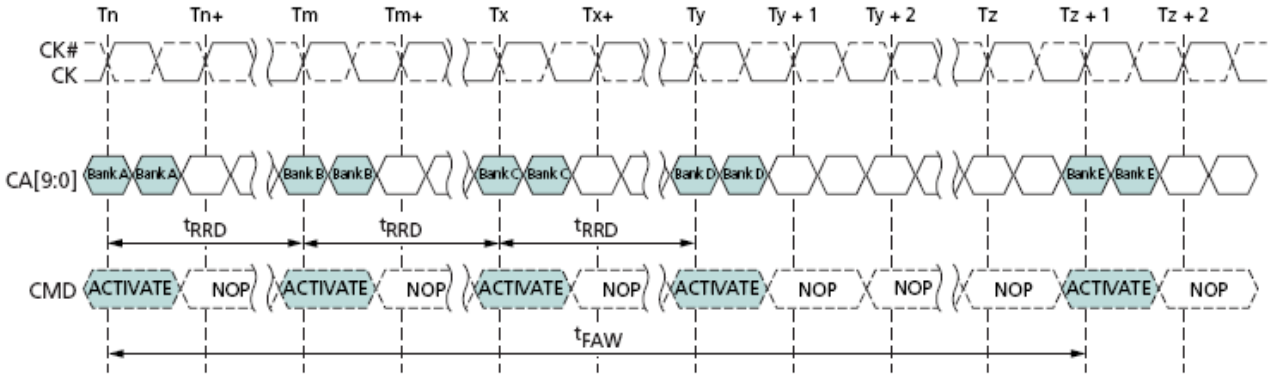
8 bank device Precharge All allowance: tRP for a Precharge All command for an 8 Bank device shall equal to tRPab, which is greater than tRPpb.



Activate command cycle: Trcd=3, Trp=3, Trrd=2

Notes:

1. A Precharge-All command uses tRPab timing, while a Single Bank Precharge command uses tRPpb timing. In this figure, Trp is used to denote either an All-bank Precharge or a Single Bank Precharge.

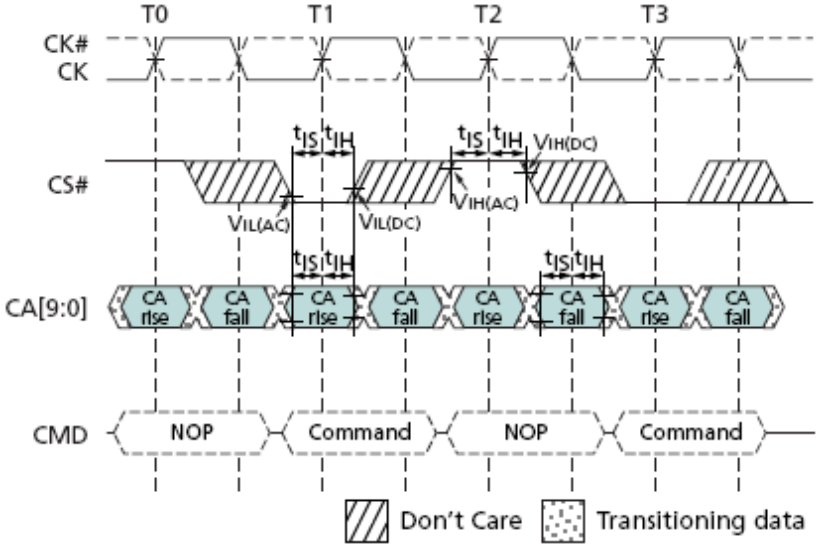


Tfaw timing

Notes:

1. Exclusively for 8-bank devices. No more than 4 banks may be activated in a rolling Tfaw window.

Command Input Signal Timing Definition



Command Input Setup and Hold Timing

Notes:

1. Setup and hold conditions also apply to the CKE pin.

Read and Write access modes

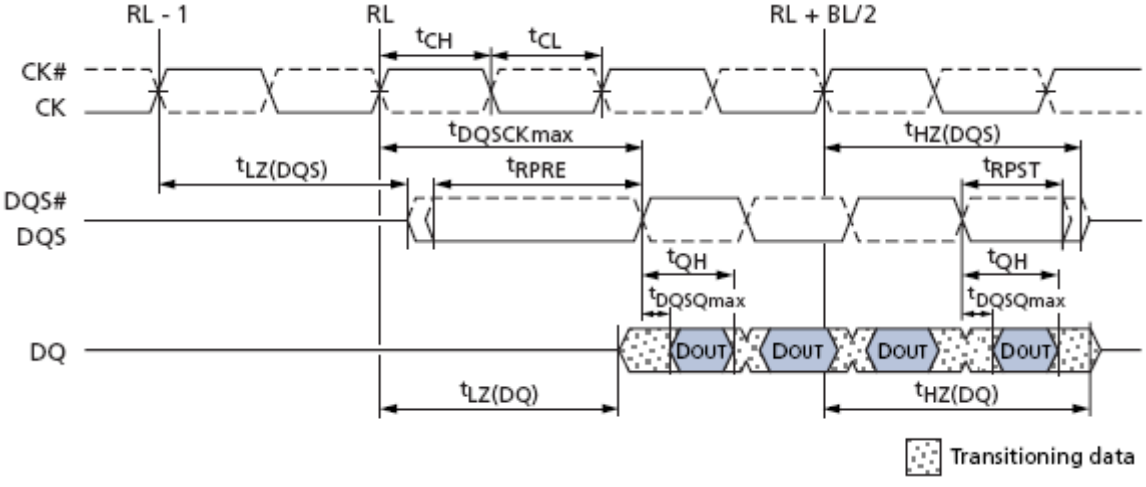
After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting $\overline{CS}$ LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a read operation (CA2 HIGH) or a write operation (CA2 LOW).

The LPDDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a burst read or write operation on successive clock cycles.

For LPDDR2-S4 devices, a new burst access must not interrupt the previous 4-bit burst operation, in case of BL=4 setting. In case of BL=8 and BL=16 settings, Reads may be interrupted by Reads, and Writes may be interrupted by Writes provided that this occurs on even clock cycles after the Read or Write command and that tCCD is met. The minimum CAS to CAS delay is defined by tCCD.

Burst Read

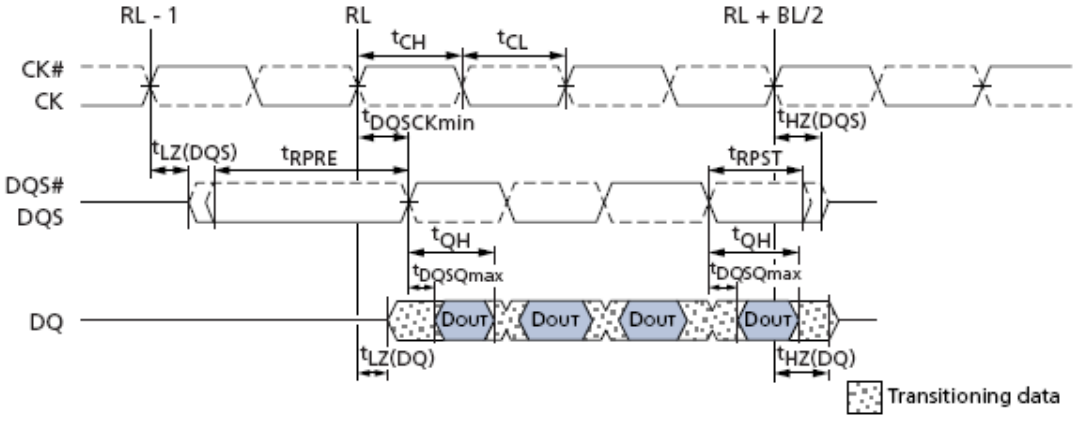
The Burst Read command is initiated by having $\overline{CS}$ LOW, CA0 HIGH, CA1 LOW and CA2 HIGH at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. The Read Latency (RL) is defined from the rising edge of the clock on which the Read Command is issued to the rising edge of the clock from which the tDQSCK delay is measured. The first valid datum is available RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Read Command is issued. The data strobe output is driven LOW tRPRE before the first rising valid strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin edge aligned with the data strobe. The RL is programmed in the mode registers. Timings for the data strobe are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$.



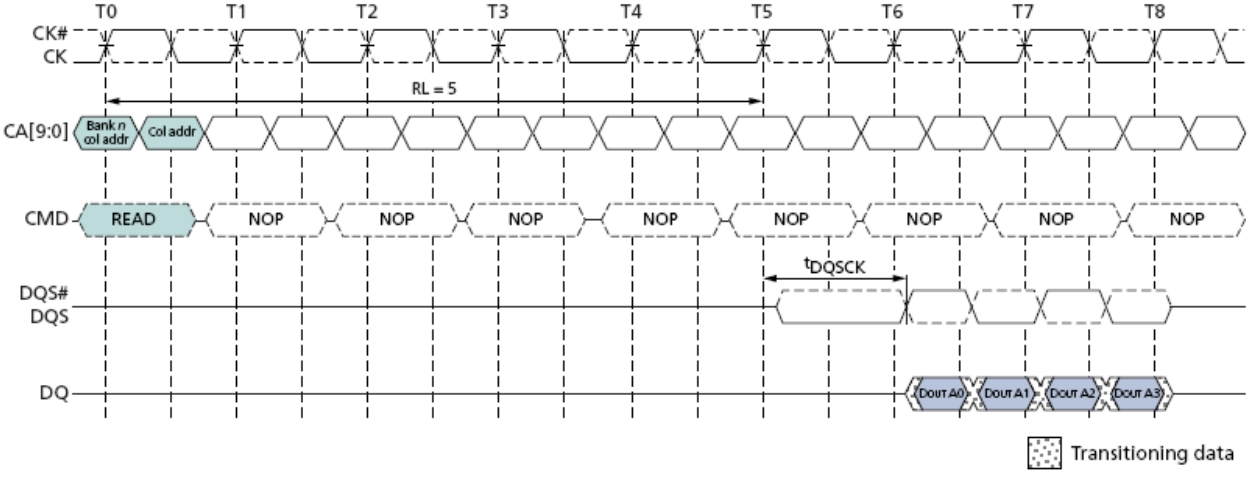
Data output (Read) timing (tDQSCKmax)

Notes:

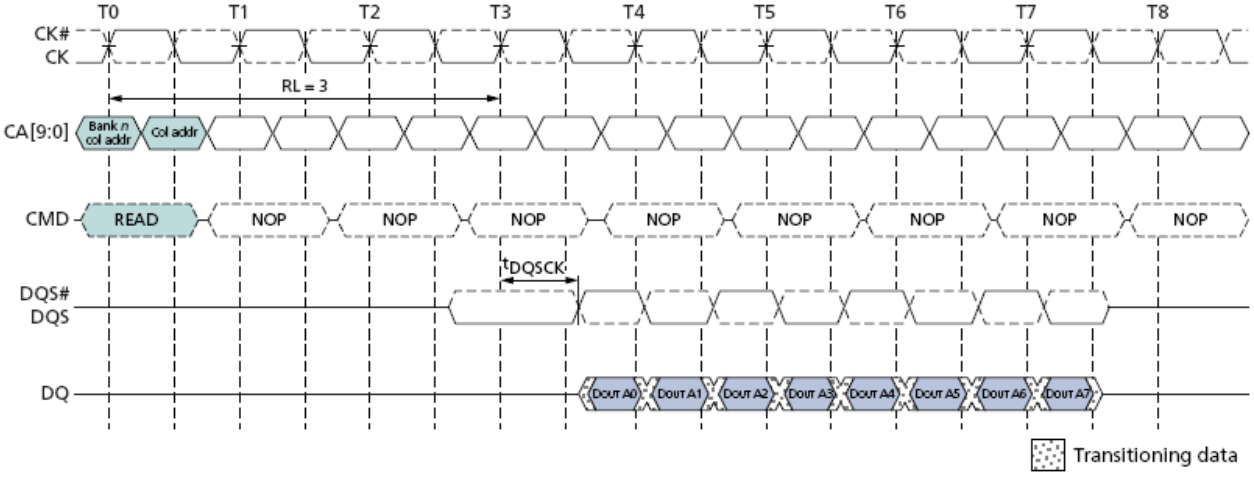
1. Tdqsck can span multiple clock periods.
2. An effective Burst Length of 4 is shown.



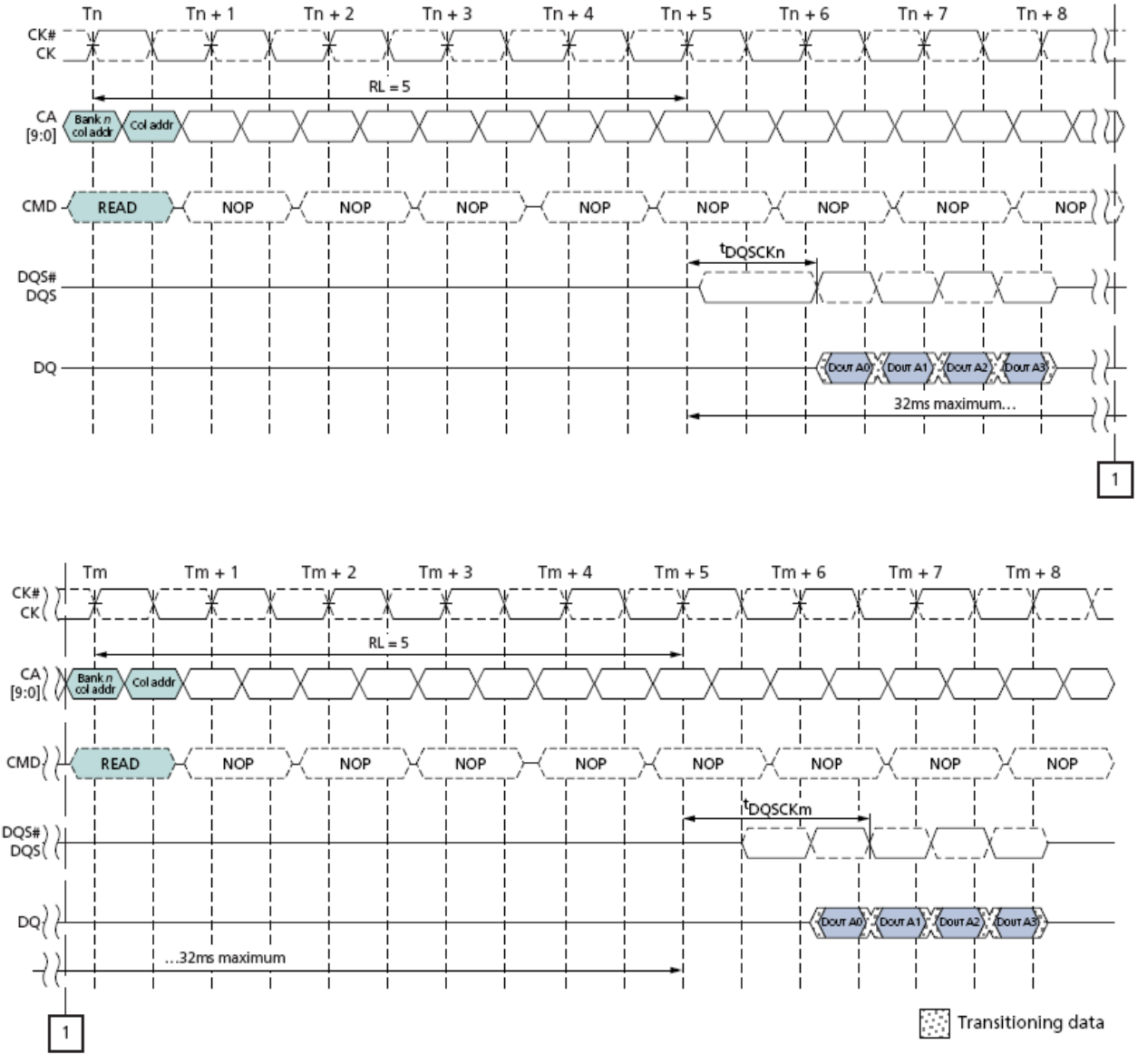
Data output (Read) timing (tDQSCKmin), BL=4



Burst Read: RL=5, BL=4, Tdqsck > Tck



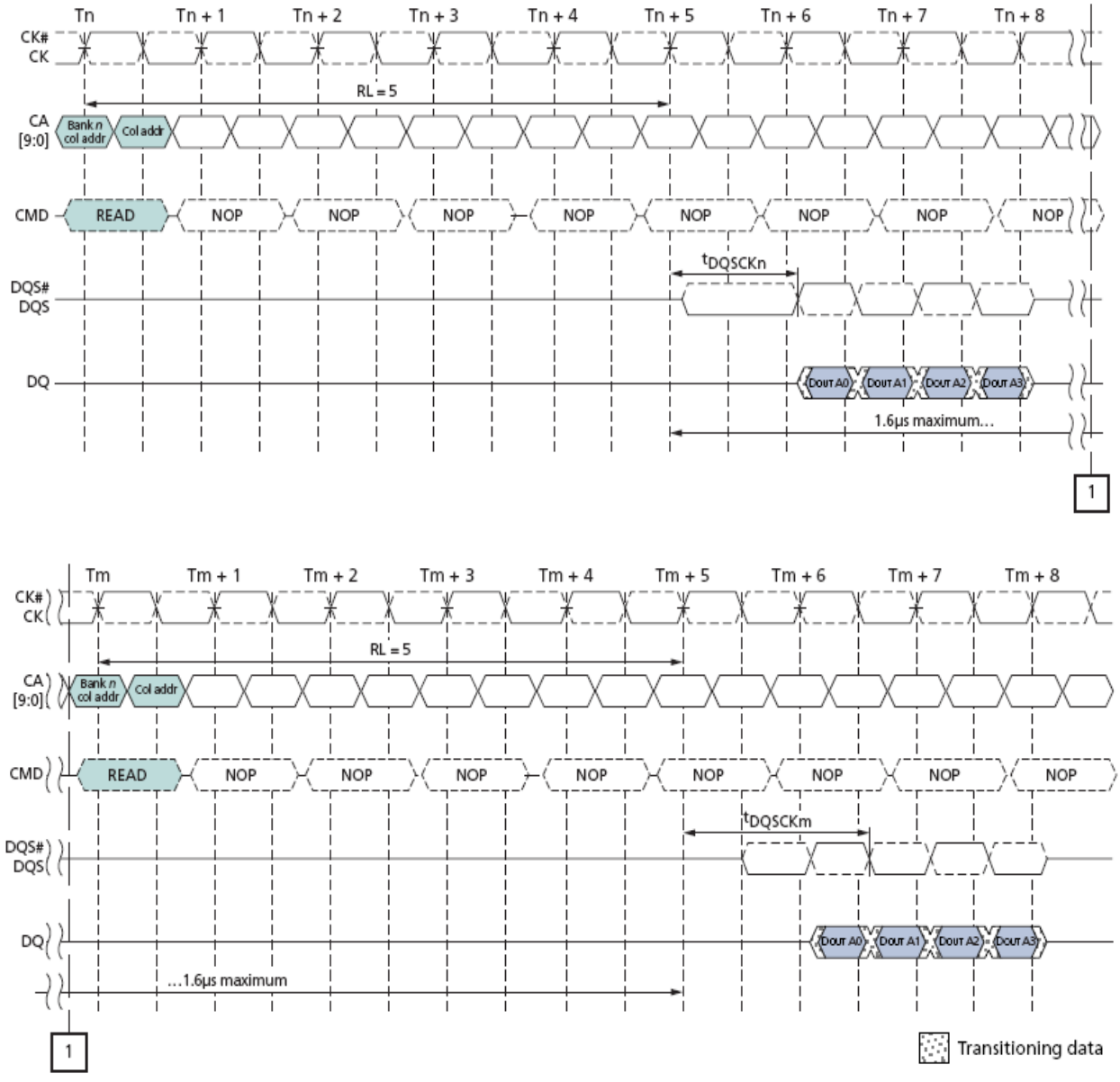
Burst Read: RL=3, BL=8, Tdqsck < Tck



Tdqsckdl timing : Tdqsckdl = |tDQSCKn – tDQSCKm| within any 32ms rolling window

Notes:

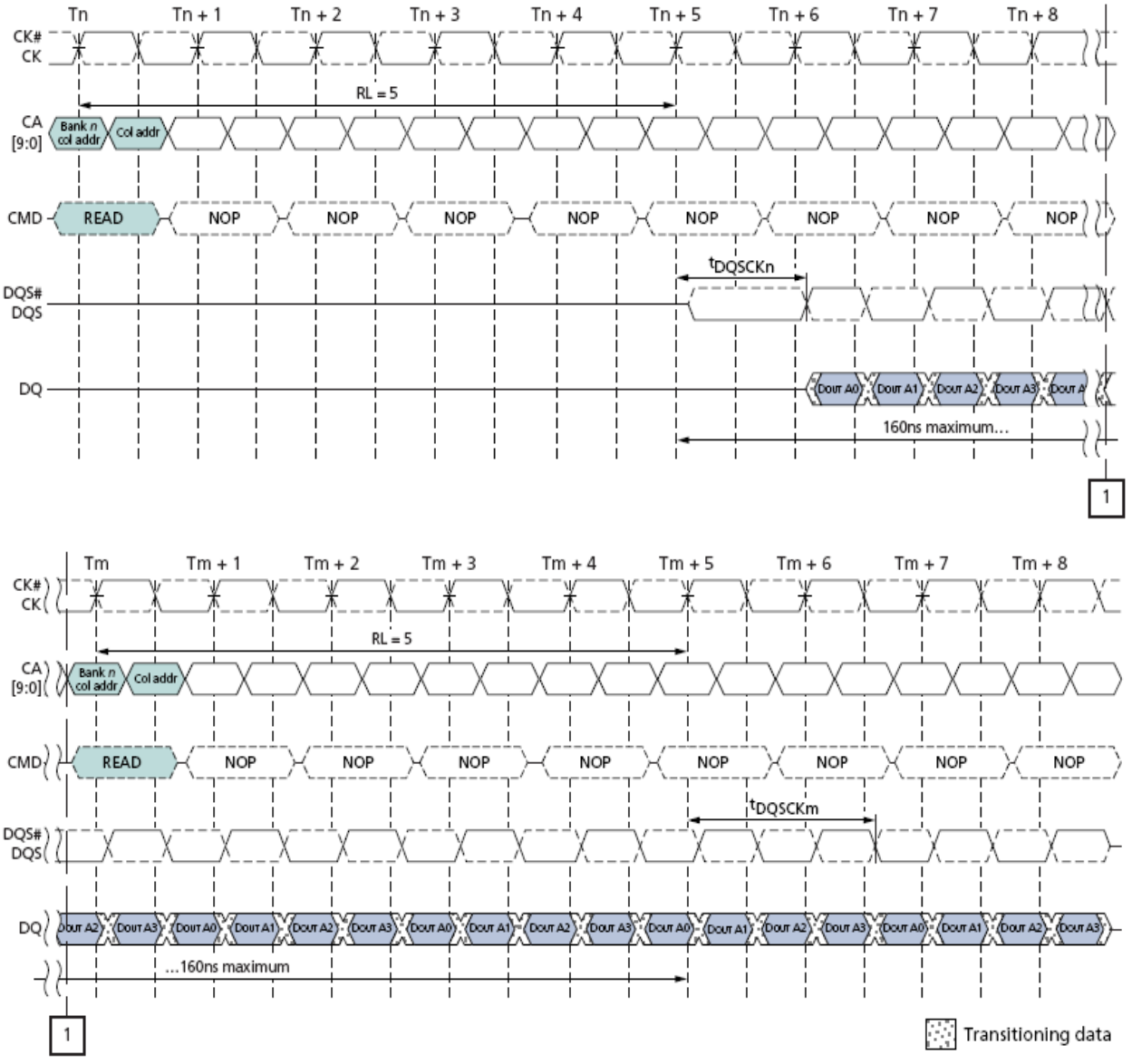
1. tDQSCKDLmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any { tDQSCKn - tDQSCKm} pair within any 32ms rolling window.



Tdqsckdm timing : Tdqsckdm= |tDQSCKn – tDQSCKm| within any 1.6us rolling window

Notes:

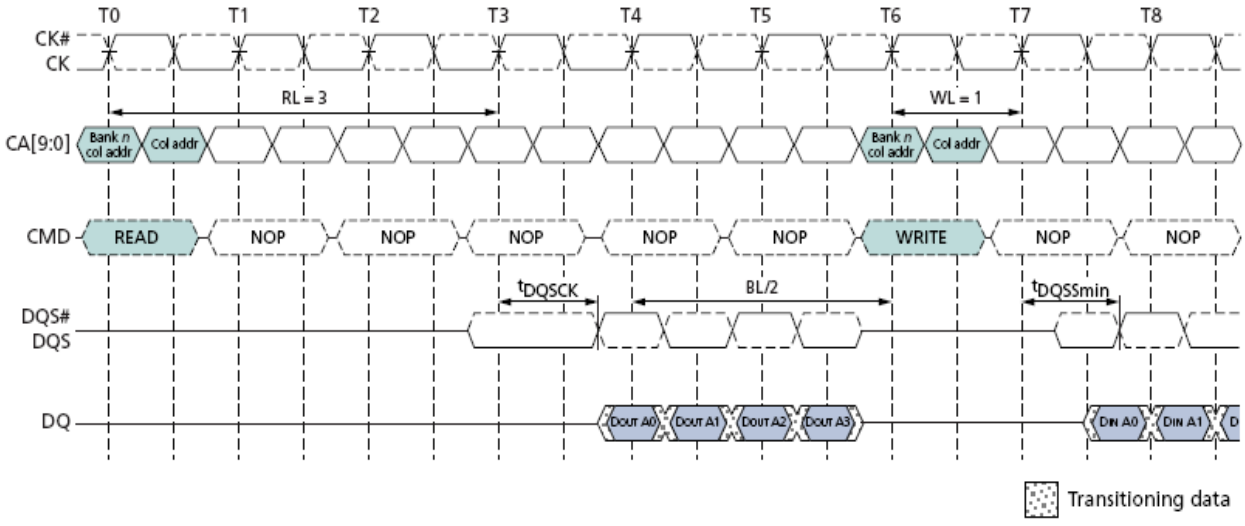
1. tDQSCKDMmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any { tDQSCKn - tDQSCKm} pair within any 1.6us rolling window.



Tdqsckds timing : Tdqsckds = |tDQSCKn – tDQSCKm| within a consecutive burst within any 160ns rolling window

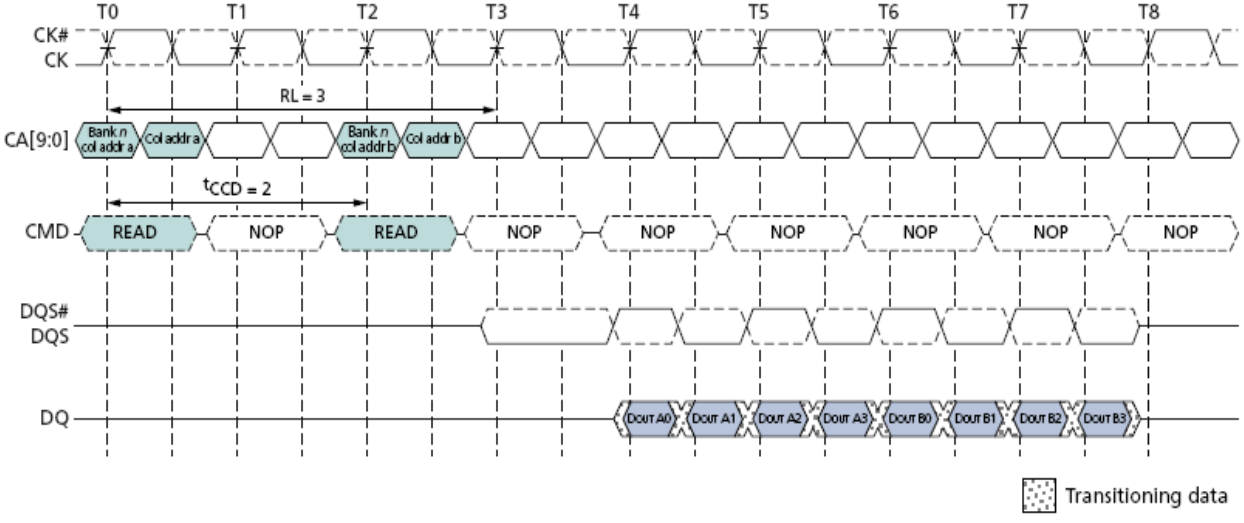
Notes:

1. tDQSCKDSmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any { tDQSCKn - tDQSCKm} pair for reads within a consecutive burst within any 160ns rolling window.



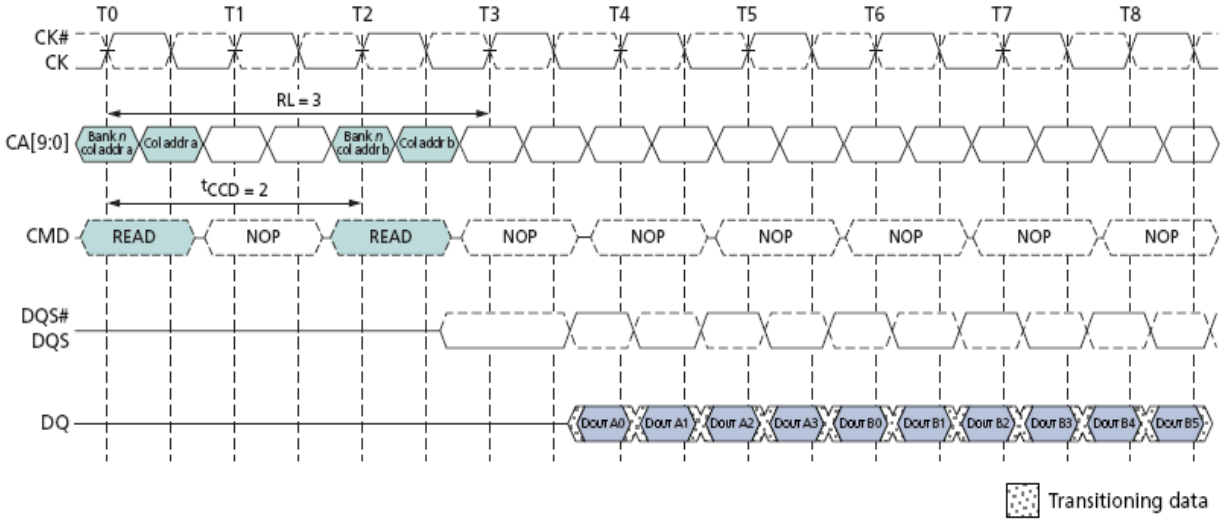
Burst Read followed by burst write: RL=3, WL=1, BL=4

The minimum time from the burst READ command to the burst WRITE command is defined by the read latency (RL) and the burst length (BL). Minimum READ-to-WRITE latency is RL + RU(Tdqsck(MAX)/Tck) + BL/2 + 1 - WL clock cycles. Note that if a READ burst is truncated with a burst TERMINATE (BST) command, the effective burst length of the truncated READ burst should be used as “BL” to calculate the minimum READ-to-WRITE delay.



Seamless Burst Read: RL=3, BL=4, Tccd=2

The seamless burst READ operation is supported by enabling a READ command at every other clock cycle for BL = 4 operation, every fourth clock cycle for BL = 8 operation, and every eighth clock cycle for BL=16 operation. This operation is supported as long as the banks are activated, whether the accesses read the same or different banks.
For LPDDR2-S4 devices, burst read can be interrupted by another read on even clock cycles after the Read command, provided that tCCD is met. For LPDDR2-S2 devices, burst reads may be interrupted by other reads on any subsequent clock, provided that tCCD is met.

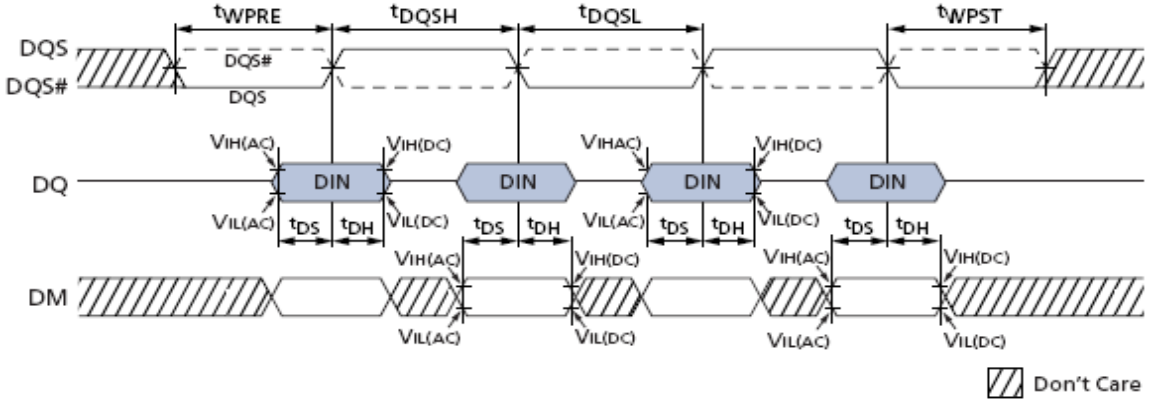


Read burst interrupt example: RL=3, BL=8, ^{t}CCD=2

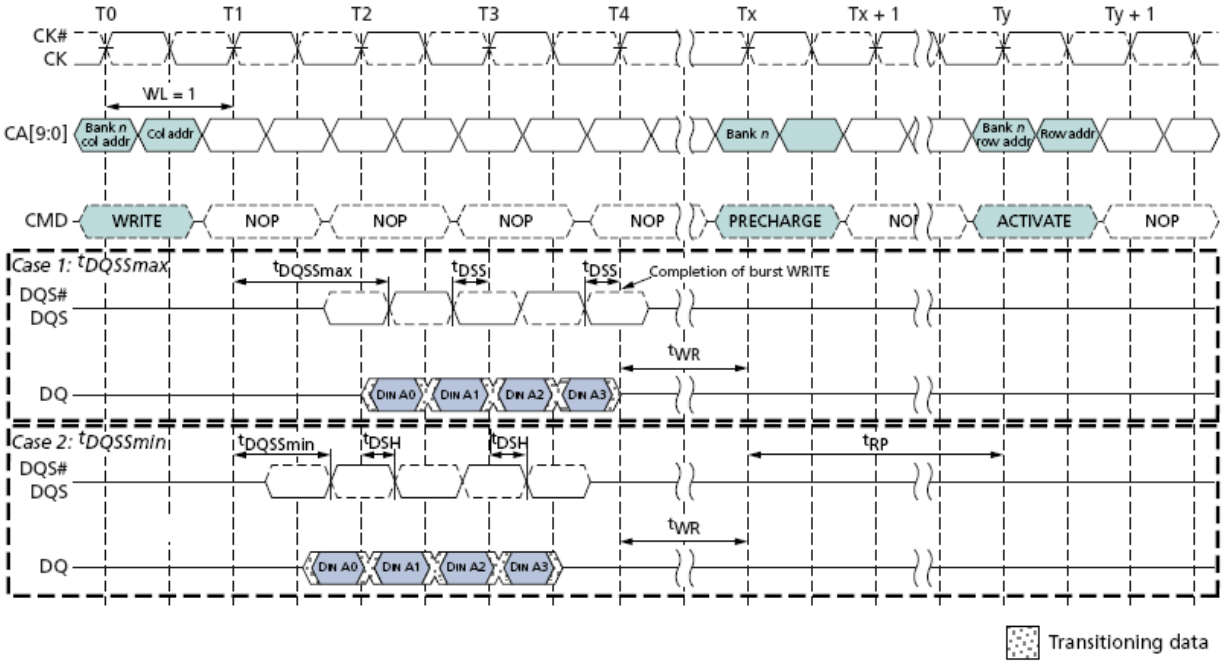
Notes:
1. Reads can only be interrupted by other reads or the BST command.
2. The effective burst length of the first read equals two times the number of clock cycles between the first read and the interrupting read.

Burst Write

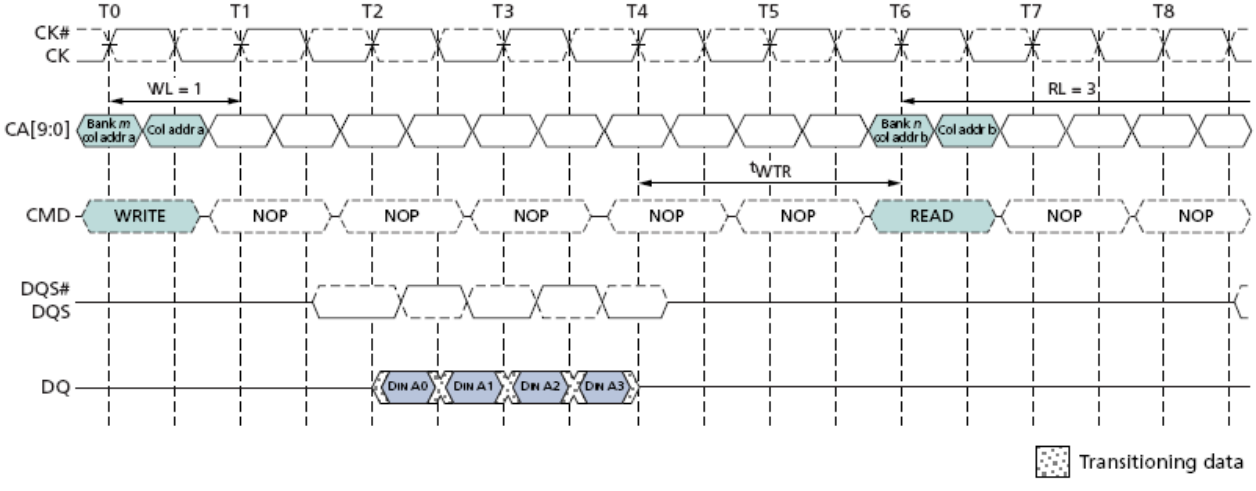
The burst WRITE command is initiated with $\overline{CS}$ LOW, CA0 HIGH, CA1 LOW, and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. Write latency (WL) is defined from the rising edge of the clock on which the WRITE command is issued to the rising edge of the clock from which the Tdqss delay is measured. The first valid data must be driven WL x Tck + Tdqss from the rising edge of the clock from which the WRITE command is issued. The data strobe signal (DQS) must be driven LOW Twpre prior to data input. The burst cycle data bits must be applied to the DQ pins Tds prior to the associated edge of the DQS and held valid until Tdh after that edge. Burst data is sampled on successive edges of the DQS until the 4-, 8-, or 16-bit burst length is completed. After a burst WRITE operation, Twr must be satisfied before a PRECHARGE command to the same bank can be issued.
Pin input timings are measured relative to the cross point of DQS and its complement, $\overline{DQS}$.



Data input (Write) timing



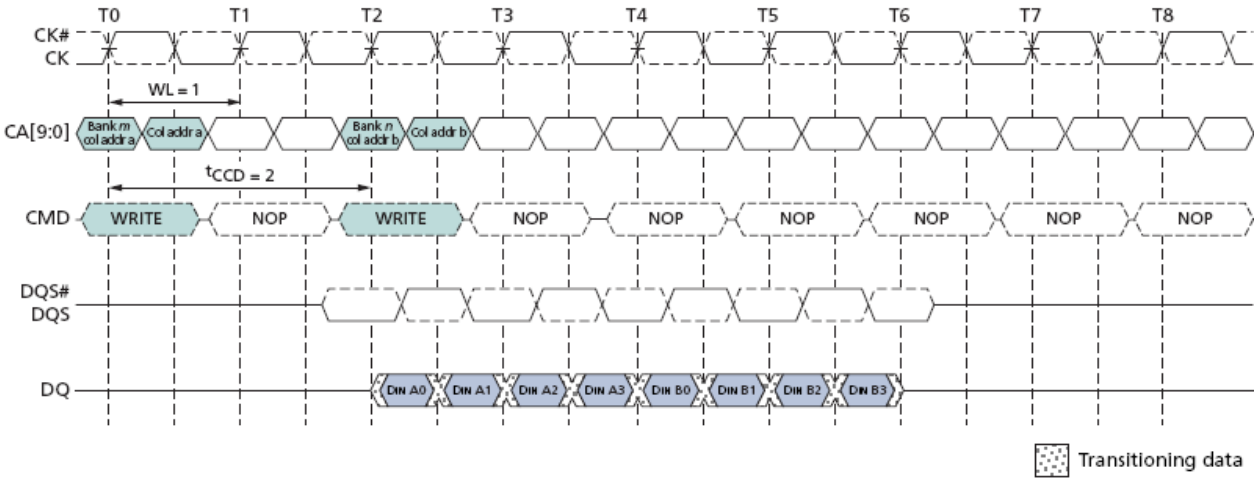
Burst write: WL=1, BL=4



Burst write followed by burst read: RL=3, WL=1, BL=4

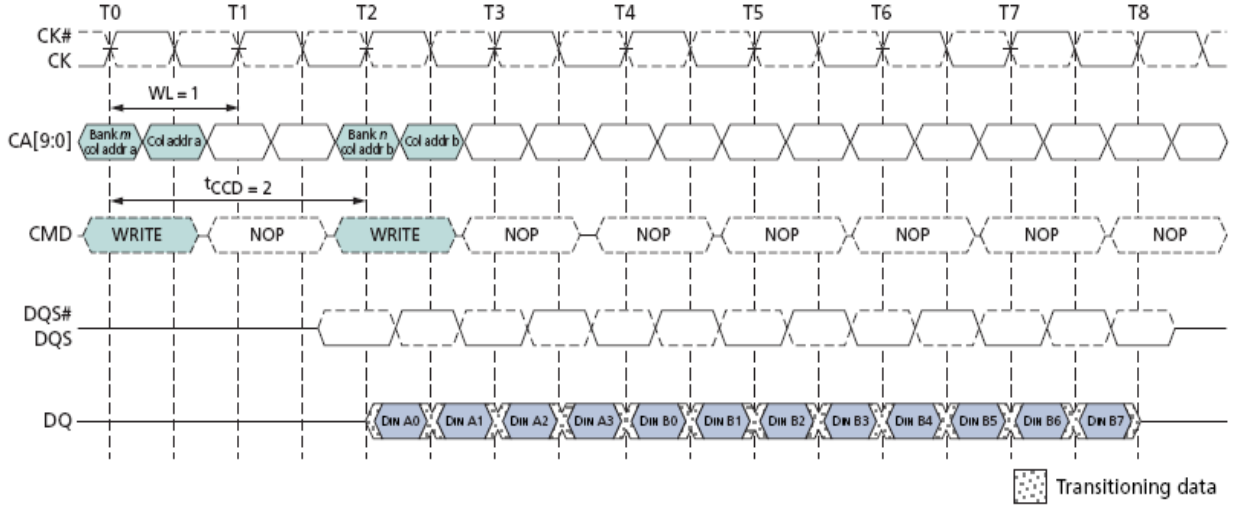
Notes:

1. The minimum number of clock cycles from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU (Twtr / Tck)].
2. Twtr starts at the rising edge of the clock after the last valid input datum.
3. If a write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated write burst should be used as “BL” to calculate the minimum write to read delay.



Seamless Burst write: WL=1, BL=4, Tccd=2

Notes:
1. The seamless burst write operation is supported by enabling a write command every other clock for BL=4 operation, every four clocks for BL=8 operation, or every eight clocks for BL=16 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.



Write burst interrupt timing: WL=1, BL=8, Tccd=2

Notes:
1. WRITEs can only be interrupted by other WRITEs or the BST command.
2. For LPDDR2-S4 devices, write burst interrupt function is only allowed on burst of 8 and burst of 16.
3. For LPDDR2-S4 devices, write burst interrupt may only occur on even clock cycles after the previous write commands, provided that Tccd(min) is met.
4. Write burst interruption is allowed to any bank inside DRAM.
5. Write burst with Auto-Precharge is not allowed to be interrupted.
6. The effective burst length of the first WRITE equals two times the number of clock cycles between the first WRITE and the interrupting WRITE.

Burst Terminate

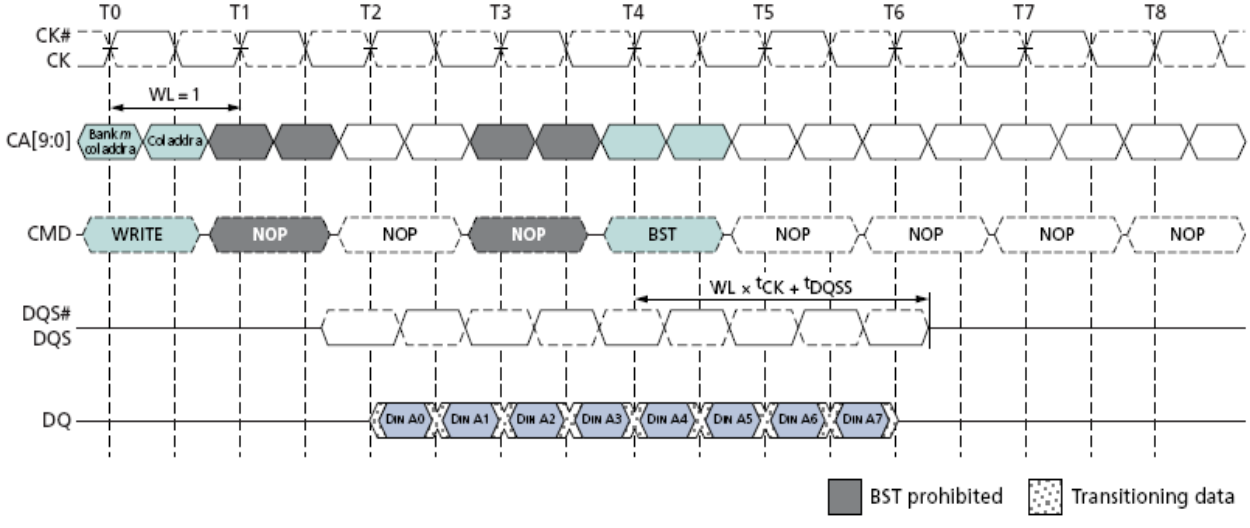
The BST command is initiated with $\overline{CS}$ LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 LOW at the rising edge of the clock. A BST command can only be issued to terminate an active READ or WRITE burst. Therefore, a BST command can only be issued up to and including BL/2 - 1 clock cycles after a READ or WRITE command. The effective burst length of a READ or WRITE command truncated by a BST command is as follows:

Effective burst length = 2 x (number of clock cycles from the READ or WRITE command to the BST command).

If a READ or WRITE burst is truncated with a BST command, to calculate the minimum READ-to-WRITE or WRITE-to-READ delay, the effective burst length of the truncated burst should be used as the value for BL.

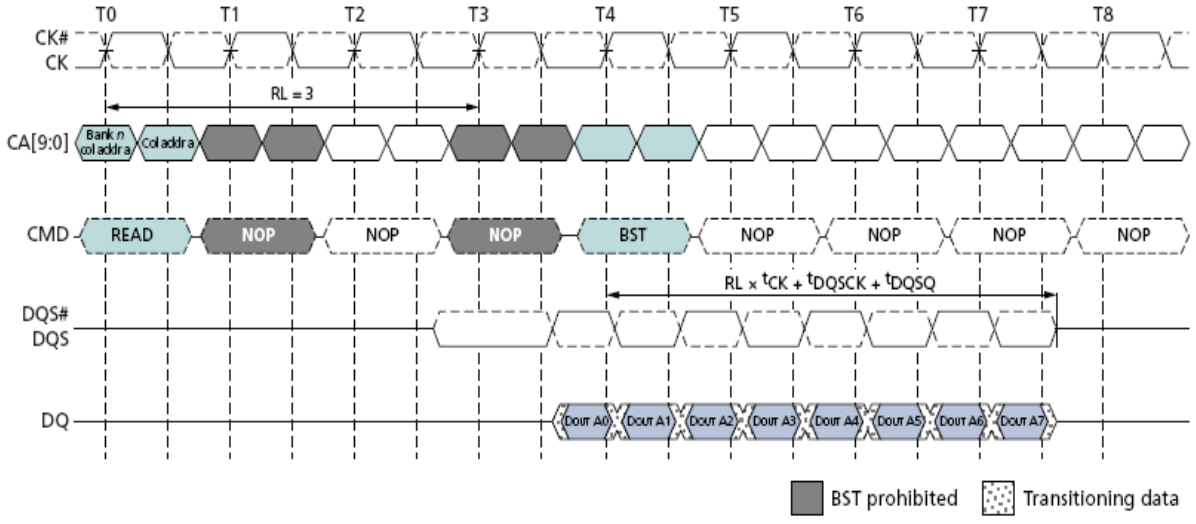
The BST command only affects the most recent READ or WRITE command. The BST command truncates an ongoing READ burst RL x Tck + Tdqsck + Tdqsq after the rising edge of the clock where the BST command is issued. The BST command truncates an on-going write burst WL x Tck + Tdqss after the rising edge of the clock where the BST command is issued.

For LPDDR2-S4 devices, the 4-bit prefetch architecture enables BST command assertion on even clock cycles following a WRITE or READ command. The effective burst length of a READ or WRITE command truncated by a BST command is thus an integer multiple of 4.



Burst Write truncated by BST: WL=1, BL=16

Notes:
1. The BST command truncates an ongoing write burst WL * tCK + tDQSS after the rising edge of the clock where the Burst Terminate command is issued.
2. For LPDDR2-S4 devices, BST can only be issued an even number of clock cycles after the Write command.
3. Additional BST commands are not allowed after T4, and may not be issued until after the next Read or Write command.

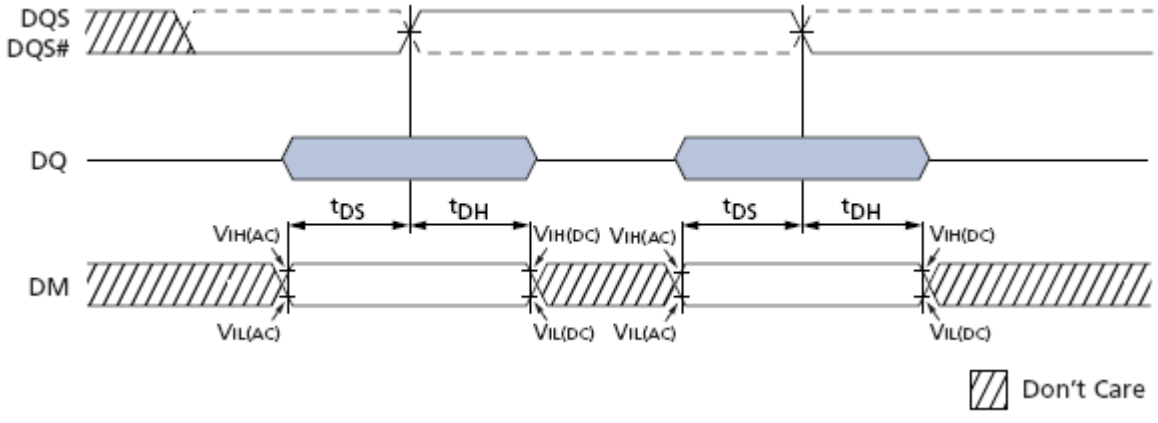


Burst Read truncated by BST: RL=3, BL=16

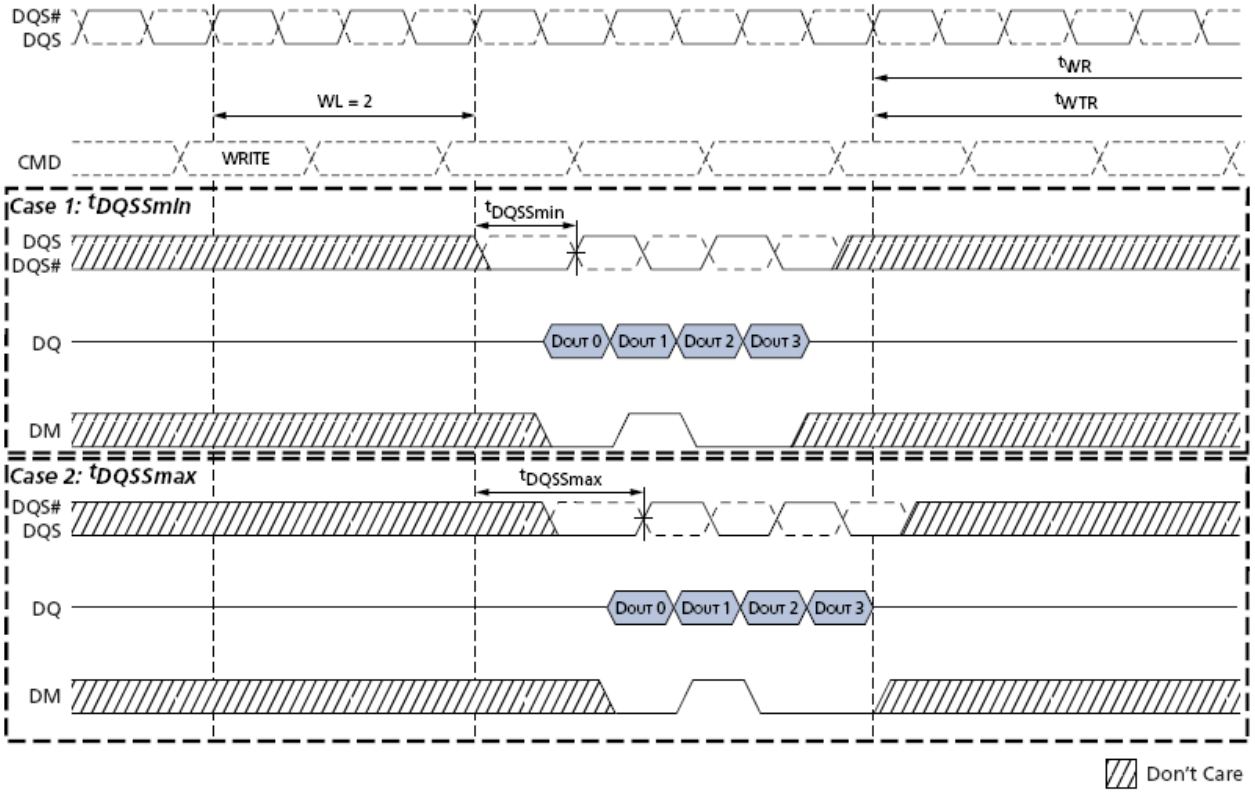
Notes:
1. The BST command truncates an ongoing read burst RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Burst Terminate command is issued.
2. For LPDDR2-S4 devices, BST can only be issued an even number of clock cycles after the Write command.
3. Additional BST commands are not allowed after T4, and may not be issued until after the next Read or Write command.

Write data Mask

One write data mask (DM) pin for each data byte (DQ) will be supported on LPDDR2 devices, consistent with the implementation on LPDDR SDRAMs. Each data mask (DM) may mask its respective data byte (DQ) for any given cycle of the burst. Data mask has identical timings on write operations as the data bits, though used as input only, is internally loaded identically to data bits to insure matched system timing.



Data Mask Timing



Write data mask: WL=2, BL=4, second DQ masked

Notes:
1. For the data mask function, WL=2, BL=4 is shown; the second data bit is masked.

Precharge

The Precharge command is used to precharge or close a bank that has been activated. The Precharge command is initiated by having $\overline{CS}$ LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. For 4-bank devices, the AB flag, and the bank address bits, BA0 and BA1, are used to determine which bank(s) to precharge. For 8-bank devices, the AB flag, and the bank address bits, BA0, BA1, and BA2, are used to determine which bank(s) to precharge. The bank(s) will be available for a subsequent row access tRPab after an All-Bank Precharge command is issued and tRPpb after a Single-Bank Precharge command is issued.

In order to ensure that 8-bank devices do not exceed the instantaneous current supplying capability of 4-bank devices, the Row Precharge time (tRP) for an All-Bank Precharge for 8-bank devices (tRPab) will be longer than the Row Precharge time for a Single-Bank Precharge (tRPpb). For 4-bank devices, the Row Precharge time (tRP) for an All-Bank Precharge (tRPab) is equal to the Row Precharge time for a Single-Bank Precharge (tRPpb).

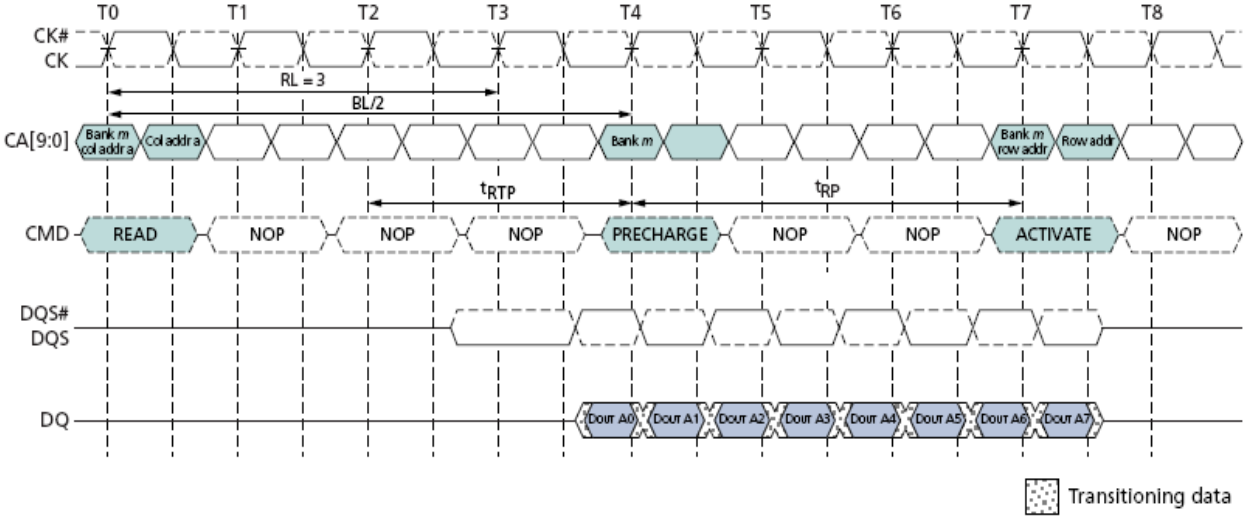
Bank selection for Precharge by address bits

AB (CA4r)	BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Precharged Bank(s) 4-bank device	Precharged Bank(s) 8-bank device
0	0	0	0	Bank 0 only	Bank 0 only
0	0	0	1	Bank 1 only	Bank 1 only
0	0	1	0	Bank 2 only	Bank 2 only
0	0	1	1	Bank 3 only	Bank 3 only
0	1	0	0	Bank 0 only	Bank 4 only
0	1	0	1	Bank 1 only	Bank 5 only
0	1	1	0	Bank 2 only	Bank 6 only
0	1	1	1	Bank 3 only	Bank 7 only
1	DON'T CARE	DON'T CARE	DON'T CARE	All Banks	All Banks

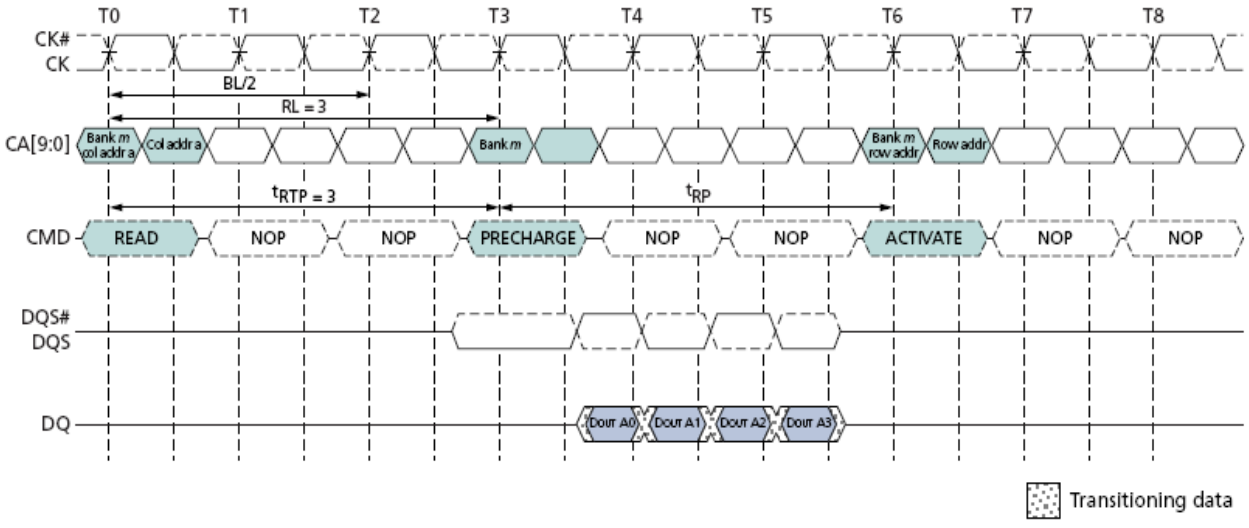
Burst Read followed by precharge

For the earliest possible precharge, the precharge command may be issued BL/2 clock cycles after a Read command. A new bank active (command) may be issued to the same bank after the Row Precharge time (tRP). A precharge command can not be issued until after tRAS is satisfied.

For LPDDR2-S4 devices, the minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising cloak edge that initiates the last 4-bit precharge of a Read command. This time is called tRTP (Read to Precharge). For LPDDR2-S4 devices, tRTP begins BL/2 - 2 clock cycles after the Read command. If the burst is truncated by a BST command, the effective "BL" ahsll be used to calculate when tRTP begins.



Burst Read followed by Precharge: RL=3, BL=8, RU(^{t}RTP(min)/^{t}CK)=2



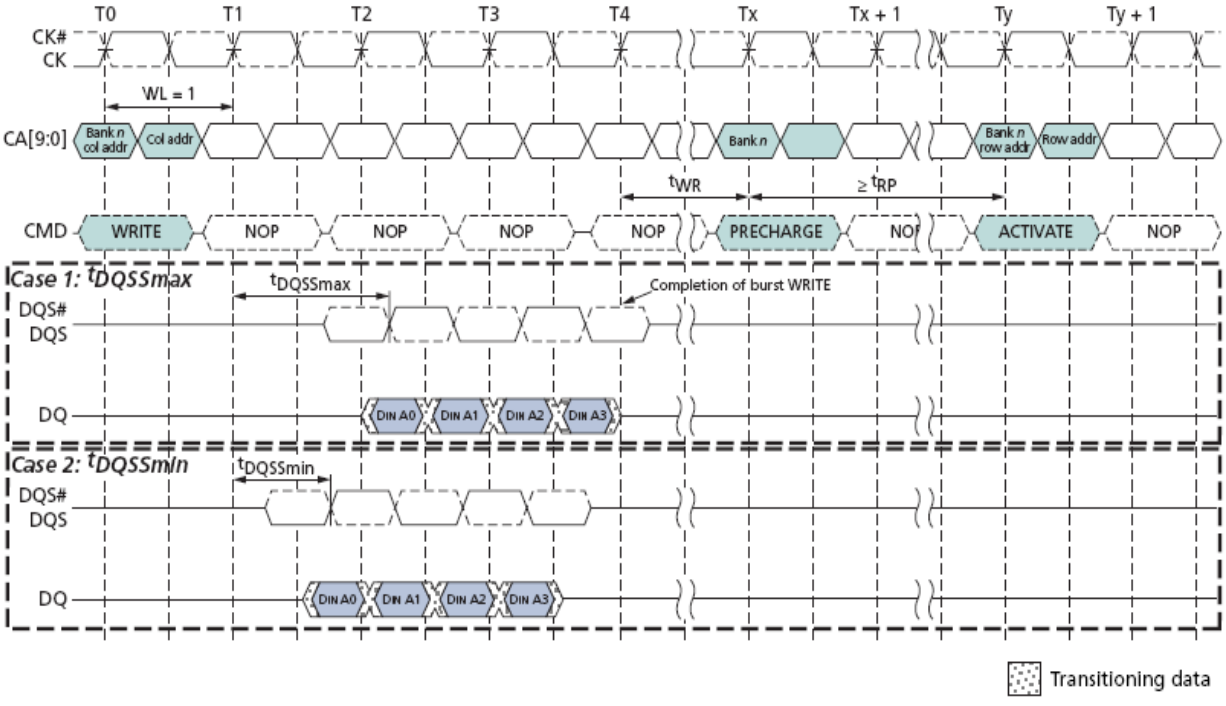
Burst Read followed by Precharge: RL=3, BL=4, RU(^{t}RTP(min)/^{t}CK) = 3

Burst Write followed by precharge

For write cycles, a delay must be satisfied from the time of the last valid burst input data until the Precharge command may be issued. This delay is known as the write recovery time (tWR) referenced from the completion of the burst write to the Precharge command. No Precharge command to the same bank should be issued prior to the tWR delay.

LPDDR2-S2 devices write data to the array in prefetch pairs (prefetch = 2) and LPDDR2-S4 devices write data to the array in prefetch quadruples (prefetch = 4). The beginning of an internal write operation may only begin after a prefetch group has been completely. Therefore, the write recovery time (tWR) starts different boundaries for LPDDR2-S2 and LPDDR2-S4 devices.

For LPDDR2-S2 devices, minimum Write to Precharge command spacing to the same bank is WL + RU(BL/2) + 1 + RU(tWR/tCK) clock cycles. For LPDDR2-S4 devices, minimum Write to Precharge command spacing to the same bank is WL + BL/2 + 1+ RU (tWR/tCK) clock cycles. For an untruncated burst, BL is the value from the Mode Register. For a truncated burst, BL is the effective burst length.



Burst Write followed by Precharge: WL=1, BL=4

Auto Precharge

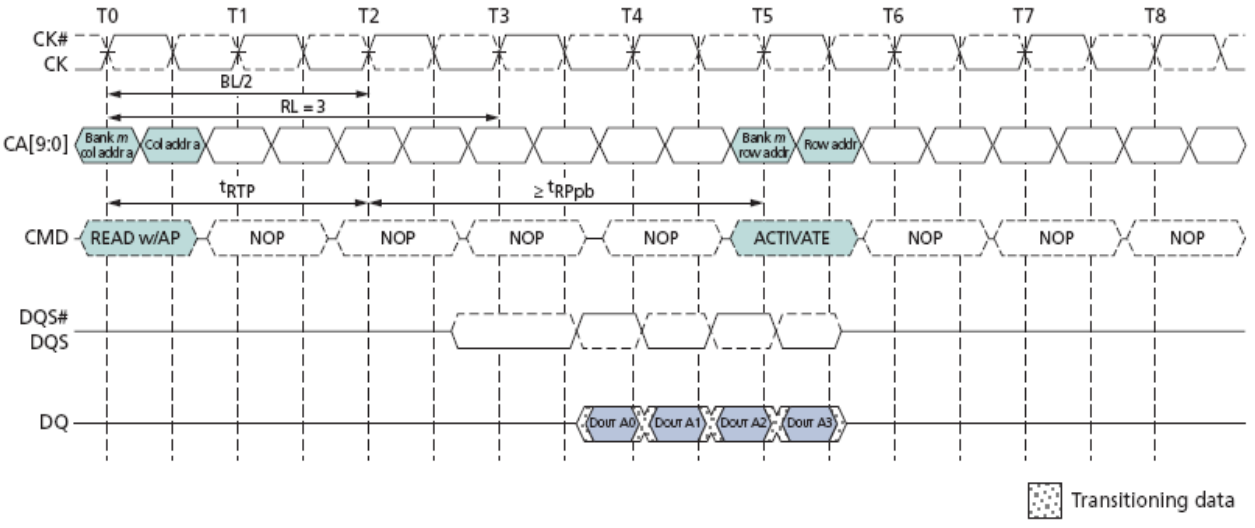
Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge command or the auto-precharge function. When a Read or a Write command is given to the LPDDR2 SDRAM, the AP bit (CA0f) may be set to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If AP is LOW when the Read or Write command is issued, the normal Read or Write burst operation is executed and the bank remains active at the completion of the burst. If AP is HIGH when the Read or Write command is issued, then the auto-precharge function is engaged. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon Read or Write latency) thus improving system performance for random data access.

Burst Read with Auto Precharge

If AP (CA0f) is HIGH when a Read Command is issued, the Read with Auto-Precharge function is engaged. LPDDR2-S4 devices start an Auto-Precharge operation on the rising edge of the clock BL/2 or BL/2 - 2 + RU(tRTP/tCK) clock cycles later than the Read with AP command, whichever is greater.

A new bank Activate command may be issued to the same bank if both of the following two conditions are satisfied simultaneously:

The RAS precharge time (tRP) has been satisfied from the clock at which the auto-precharge begins.
The RAS cycle time (tRC) from the previous bank activation has been satisfied.



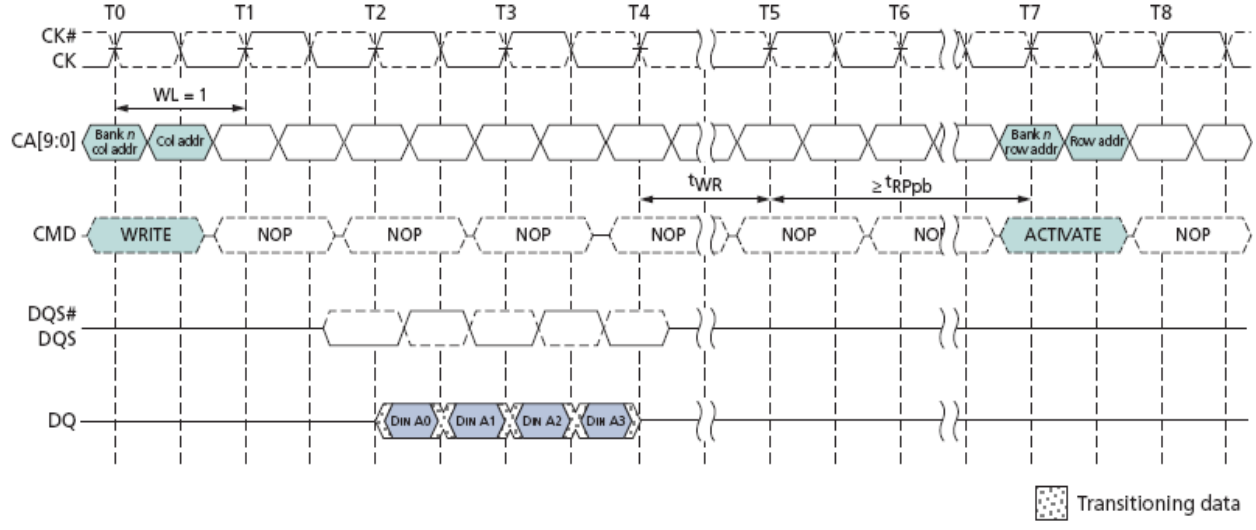
Burst Read with Auto-Precharge: RL=3, BL=4, RU(^{t}RTP(min)/^{t}CK)=2

Burst Write with Auto Precharge

If AP (CA0f) is HIGH when a Write Command is issued, the Write with Auto-Precharge function is engaged. The LPDDR2 SDRAM starts an Auto-precharge operation on the rising edge which is Twr cycles after the completion of the burst write.

A new bank Activate command may be issued to the same bank if both of the following two conditions are satisfied:

The RAS precharge time (Trp) has been satisfied from the clock at which the auto-precharge begins.
The RAS cycle time (Trc) from the previous bank activation has been satisfied.



Burst Write with Auto-Precharge: WL=1, BL=4

LPDDR2-S4: Precharge & Auto Precharge clarification

From Command	To Command	Minimum Delay between "From Command" to "To Command"	Unit	Notes
Read	Precharge (to same Bank as Read)	BL/2 + max(2, RU(tRTP/tCK)) - 2	clks	1
	Precharge All	BL/2 + max(2, RU(tRTP/tCK)) - 2	clks	1
BST (for Reads)	Precharge (to same Bank as Read)	1	clks	1
	Precharge All	1	clks	1
Read w/AP	Precharge (to same Bank as Read w/AP)	BL/2 + max(2, RU(tRTP/tCK)) - 2	clks	1,2
	Precharge All	BL/2 + max(2, RU(tRTP/tCK)) - 2	clks	1
	Activate (to same Bank as Read w/AP)	BL/2 + max(2, RU(tRTP/tCK)) - 2 + RU(tRPpb/tCK)	clks	1
	Write or Write w/AP (same bank)	Illegal	clks	3
	Write or Write w/AP (different bank)	RL + BL/2+ RU(tDQSCKmax/tCK) - WL + 1	clks	3
	Read or Read w/AP (same bank)	Illegal	clks	3
	Read or Read w/AP (different bank)	BL/2	clks	3
Write	Precharge (to same Bank as Write)	WL + BL/2 + RU(tWR/tCK) + 1	clks	1
	Precharge All	WL + BL/2 + RU(tWR/tCK) + 1	clks	1
BST (for Writes)	Precharge (to same Bank as Write)	WL + RU(tWR/tCK) + 1	clks	1
	Precharge All	WL + RU(tWR/tCK) + 1	clks	1
Write w/AP	Precharge (to same Bank as Write w/AP)	WL + BL/2 + RU(tWR/tCK) + 1	clks	1
	Precharge All	WL + BL/2 + RU(tWR/tCK) + 1	clks	1
	Activate (to same Bank as Write w/AP)	WL + BL/2 + RU(tWR/tCK) + 1 + RU(tRPpb/tCK)	clks	1
	Write or Write w/AP (same bank)	Illegal	clks	3
	Write or Write w/AP (different bank)	BL/2	clks	3
	Read or Read w/AP (same bank)	Illegal	clks	3
	Read or Read w/AP (different bank)	WL + BL/2 + RU(tWTR/tCK) + 1	clks	3
Precharge	Precharge (to same Bank as Precharge)	1	clks	1
	Precharge All	1	clks	1
Precharge All	Precharge	1	clks	1
	Precharge All	1	clks	1

Notes:
1. For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after tRP depending on the latest precharge command issued to that bank.
2. Any command issued during the minimum delay time as specified above table is illegal.
3. After Read with AP, seamless read operations to different banks are supported. After Write with AP, seamless write operations to different banks are supported. Read w/AP and Write a/AP may not be interrupted or truncated.

Refresh Command

The Refresh Command is initiated by having $\overline{CS}$ LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of clock. Per Bank Refresh is initiated by having CA3 LOW at the rising edge of the clock and All Bank Refresh is initiated by having CA3 HIGH at the rising edge of clock. Per Bank Refresh is only allowed in devices with 8 banks.
A Per Bank Refresh Command, REFpb performs a refresh operation to the bank which is scheduled by the bank counter in the memory device. The bank sequence of Per Bank Refresh is fixed to be a sequential round-robin: “0-1-2-3-4-5-6-7-0-1-...”. The bank count is synchronized between the controller and the SDRAM upon issuing a RESET command or at every exit from self refresh, by resetting bank count to zero. The bank addressing for the Per Bank Refresh count is the same as established in the single-bank Precharge command.
A bank must be idle before it can be refreshed. It is the responsibility of the controller to track the bank being refreshed by the Per Bank Refresh command. The REFpb command may not be issued to the memory until the following conditions are met:

- tRFCab has been satisfied after the prior REFab command.
- tRFCpb has been satisfied after the prior REFpb command.
- Trp has been satisfied after the prior Precharge command to that given bank.

Trrd has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than affected by the REFpb command. The target bank is inaccessible during the Per Bank Refresh cycle (tRFCpb), however other banks within the device are accessible and may be addressed during the Per Bank Refresh cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in active state or accessed by a read or a write command.
When the Per Bank Refresh cycle has completed, the affected bank will be in the idle state. As shown in the table, after issuing REFpb:

- tRFCpb must be satisfied before issuing a REFab command.
- tRFCpb must be satisfied before issuing an ACTIVE command to a same bank.
- Trrd must be satisfied before issuing an ACTIVE command to a different bank.
- tRFCpb must be satisfied before issuing another REFpb command.

An All Bank Refresh command, REFab performs a refresh operation to all banks. All banks have to be in idle state when REFab is issued (for instance, by Precharge All Bank command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. As shown in the table, the REFab command may not be issued to the memory until the following conditions have been met:

- tRFCab has been satisfied after the prior REFab command.
- tRFCpb has been satisfied after the prior REFpb command.
- Trp has been satisfied after the prior Precharge commands.

When the All Bank Refresh cycle has completed, all banks will be in the idle state. As shown in the table, after issuing REFab:

- the tRFCab latency must be satisfied before issuing an ACTIVATE command.
- the tRFCab latency must be satisfied before issuing a REFab or REFpb command.

Command Scheduling Separations related to Refresh

Symbol	minimum delay from	to	Notes
tRFCab	REFab	REFab	
		Activate cmd to any bank	
		REFpb	
tRFCpb	REFpb	REFab	
		Activate cmd to same bank as REFpb	
		REFpb	
tRRD	REFpb	Activate cmd to different bank than REFpb	
	Activate	REFpb affecting an idle bank (different bank than Activate)	1
		Activate cmd to different bank than prior Activate	

Notes:
1. A bank must be in the Idle state before it is refreshed. Therefore, after Activate, REFab is not allowed and REFpb is allowed only if it affects a bank which is in the Idle state.

Refresh Requirement

(1) Minimum number of Refresh commands:
LPDDR2 requires a minimum number, R, of REFRESH (REFab) commands within any rolling refresh window (Trefw = 32 ms @ MR4[2:0] = 011 or TC =< 85'C). For actual values per density, and the resulting average refresh interval (Trefi) is given in the table below.

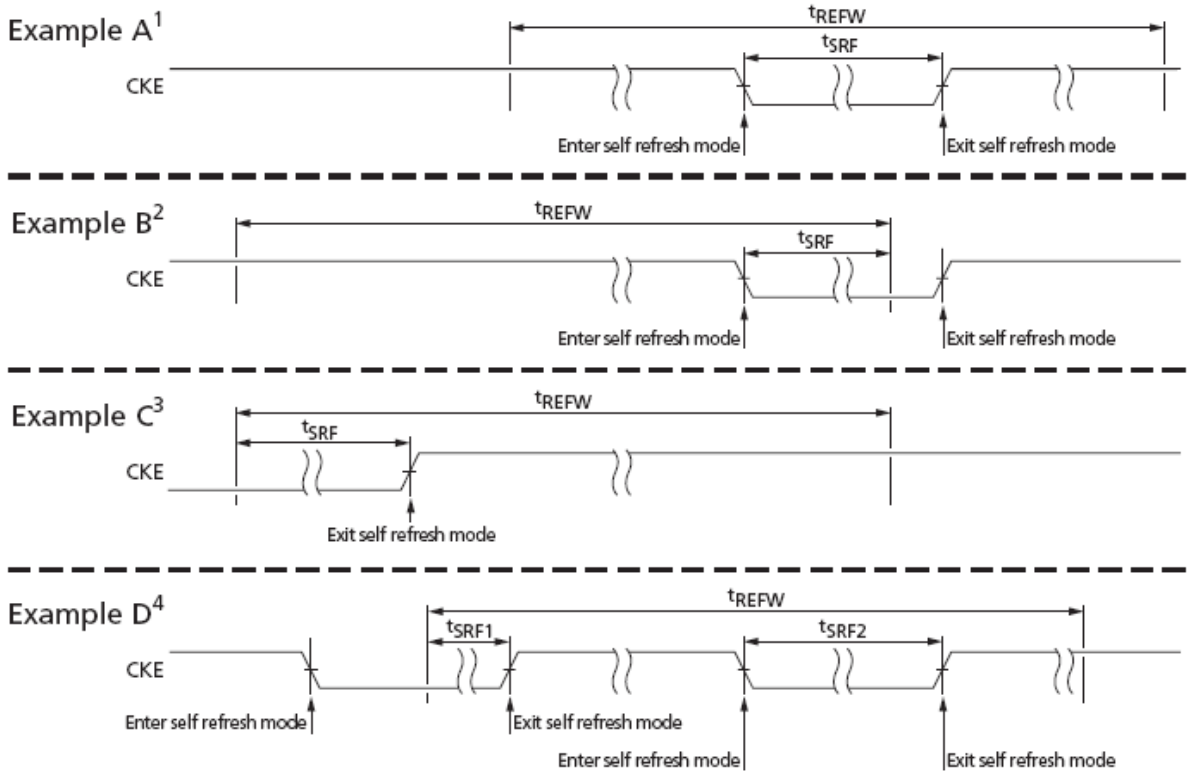
Symbol	Parameter	4Gb(Single Die)	8Gb(Dual Dies)	Unit
	Number of banks	8		
tREFW	Refresh window: TCASE =< 85'C	32		ms
tREFW	Refresh window: 85'C < TCASE =< 105'C	8		ms
R	Required number of REFRESH commands (MIN)	8192	8192	
tREFI	Average time between REFRESH commands (for reference only) TCASE <= 85'C	3.9	3.9	us
tREFIpb		0.4875	0.4875	us
tRFCab	Refresh cycle time	130	130	ns
tRFCpb	Per-bank REFRESH cycle time	60	60	ns
tREFBW	Burst REFRESH window = 4 x 8 x tRFCab	4.16	4.16	us

And see Mode Register 4 information for Trefw and Trefi refresh multipliers at different MR4 settings.
For devices supporting per-bank REFRESH, a REFab command can be replaced by a full cycle of eight REFpb commands.

(2) Burst Refresh limitation:
To limit maximum current consumption, a maximum of 8 REFab commands may be issued in any rolling Trefbw (Trefbw = 4 x 8 x tRFCab). This condition does not apply if REFpb commands are used.

(3) Refresh Requirements and Self-Refresh:
If any time within a refresh window is spent in Self-Refresh Mode, the number of required Refresh commands in this particular window is reduced to:

R*=R -RU{Tsrf/Trefi} =R-RU{R*Tsrf/Trefw }, where RU stands for the round-up function.



LPDDR2 S4: Definition of Tsrf

NOTE: Above examples are several cases on how to Tsrf is calculated
1. (Example A): Time in self refresh mode is fully enclosed in the refresh window (Trefw).
2. (Example B): At self refresh entry.
3. (Example C): At self refresh exit.
4. (Example D): Several intervals in self refresh during one Trefw interval. In this example, Tsrf = Tsrf1 + Tsrf2.

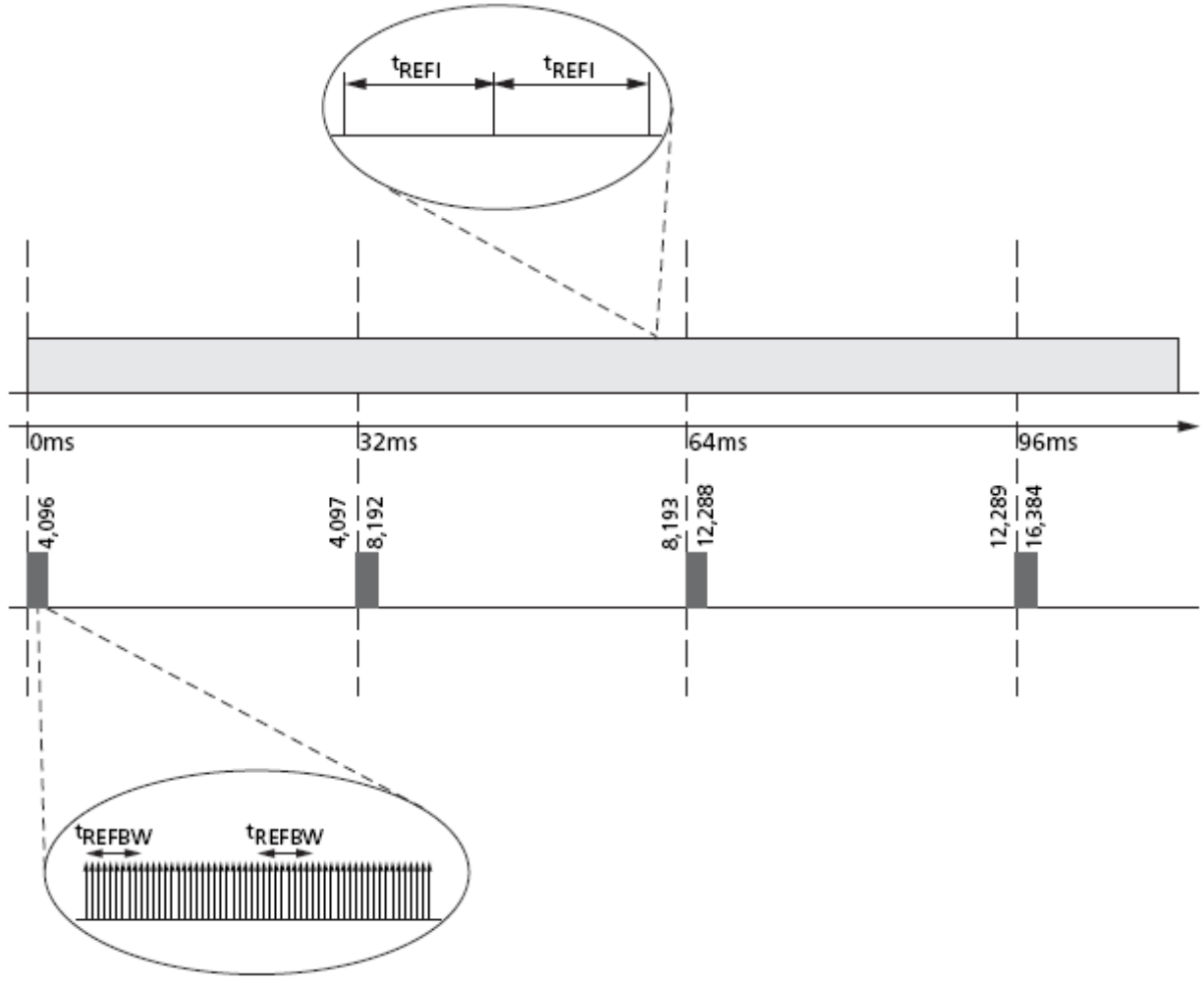
The LPDDR2 devices provide significant flexibility in scheduling REFRESH commands as long as the boundary conditions are met. In the most straightforward implementations, a REFRESH command should be scheduled every Trefi. In this case, self refresh can be entered at any time.

Users may choose to deviate from this regular refresh pattern, for example, to enable a period where no refreshes are required. In the extreme (e.g., LPDDR2-S4 1Gb), the user can choose to issue a refresh burst of 4096 REFRESH commands at the maximum supported rate (limited by Trefbw), followed by an extended period without issuing any REFRESH commands, until the refresh window is complete. The maximum supported time without REFRESH commands is calculated as follows: Trefw - (R/8) x Trefbw = Trefw - R x 4 x tRFCab.

For example, a 1Gb LPDDR2-S4 device at TC =< 85'C can be operated without REFRESH commands up to 32ms - 4096 x 4 x 130ns ~ 30 ms. Both the regular and the burst/pause patterns can satisfy refresh requirements if they are repeated in every 32ms window. It is critical to satisfy the refresh requirement in every rolling refresh window during refresh pattern transitions. The supported transition from a burst pattern to a regular distributed pattern. If this transition occurs immediately after the burst refresh phase, all rolling Trefw intervals will meet the minimum required number of refreshes.

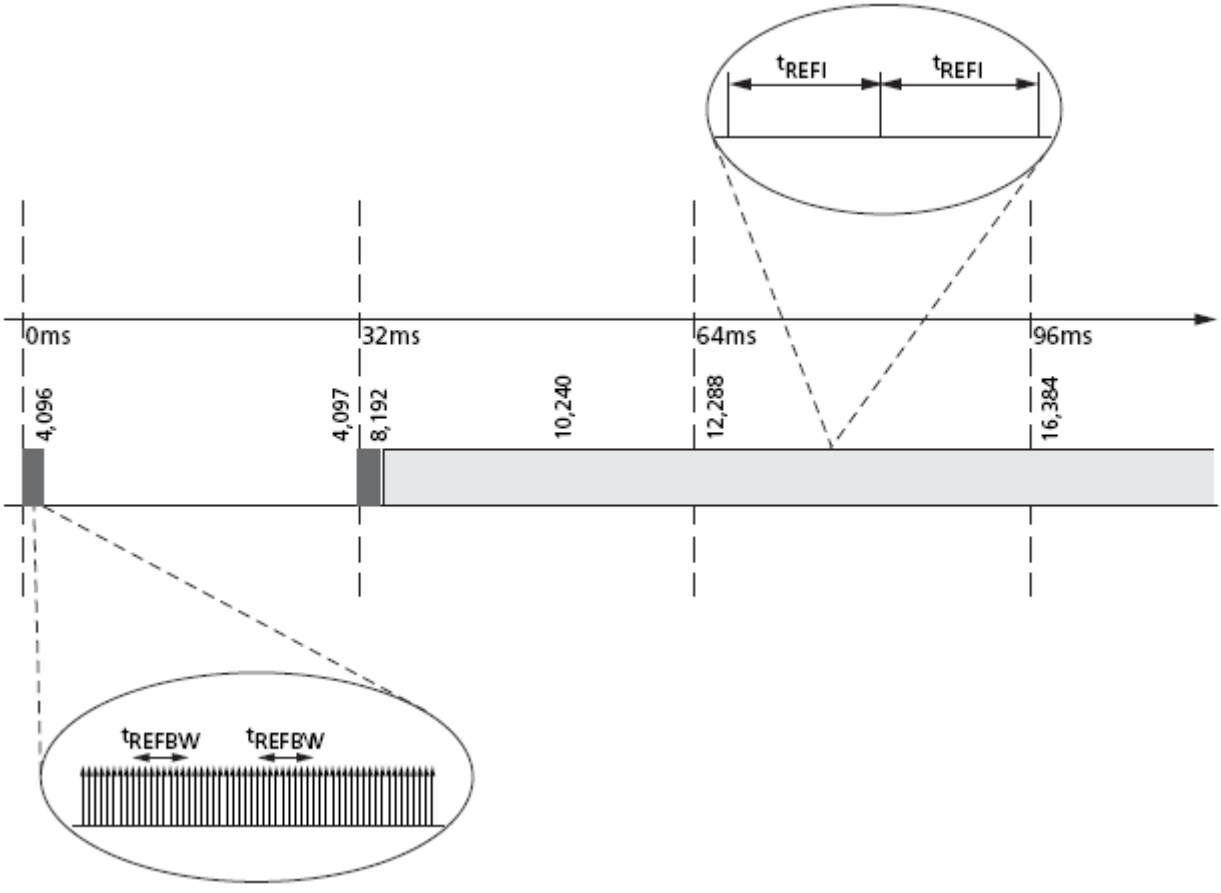
A non-supported transition - In this example, the regular refresh pattern starts after the completion of the pause phase of the burst/pause refresh pattern. For several rolling Trefw intervals, the minimum number of REFRESH commands is not satisfied.

Understanding this pattern transition is extremely important, even when only one pattern is employed. In self refresh mode, a regular distributed-refresh pattern must be assumed. It is recommended entering self refresh mode immediately following the burst phase of a burst/pause refresh pattern; upon exiting self refresh, begin with the burst phase.



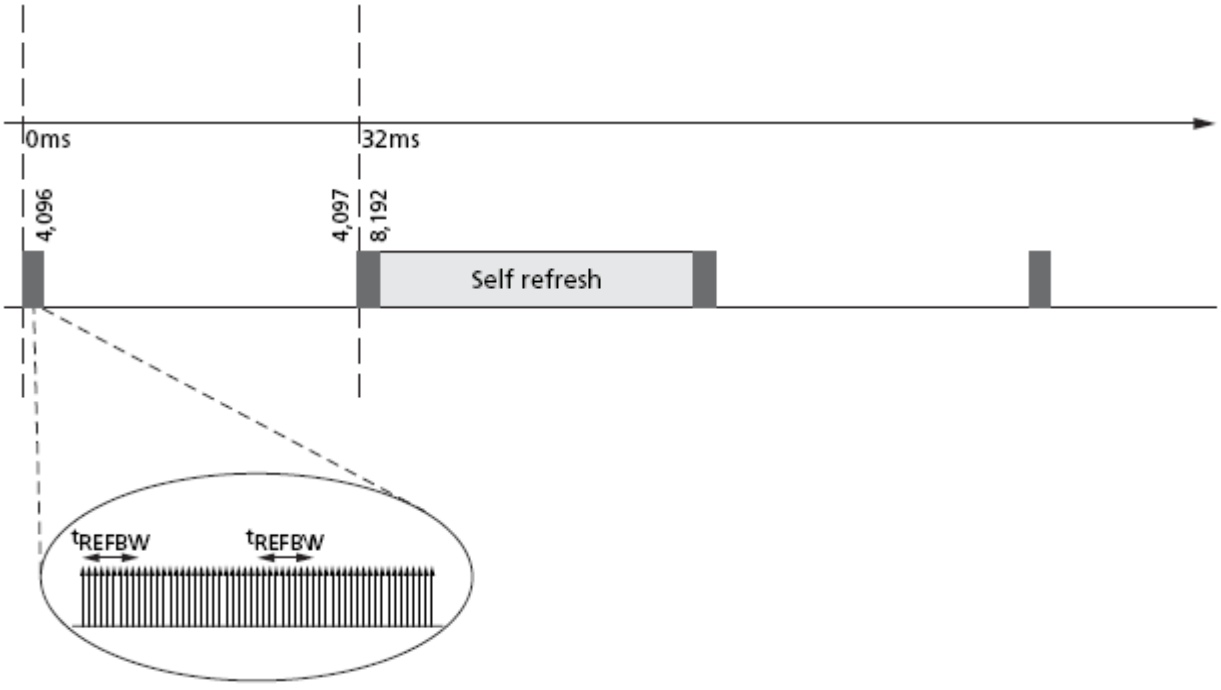
Regular, Distributed REFRESH Pattern

Notes:
1. Compared to repetitive burst REFRESH with subsequent REFRESH pause.
2. As an example, in a 1Gb LPDDR2-S4 device at TC =< 85'C, the distributed refresh pattern has one REFRESH command per 7.8us; the burst refresh pattern has one refresh command per 0.52us, followed by ~30ms without any REFRESH command.



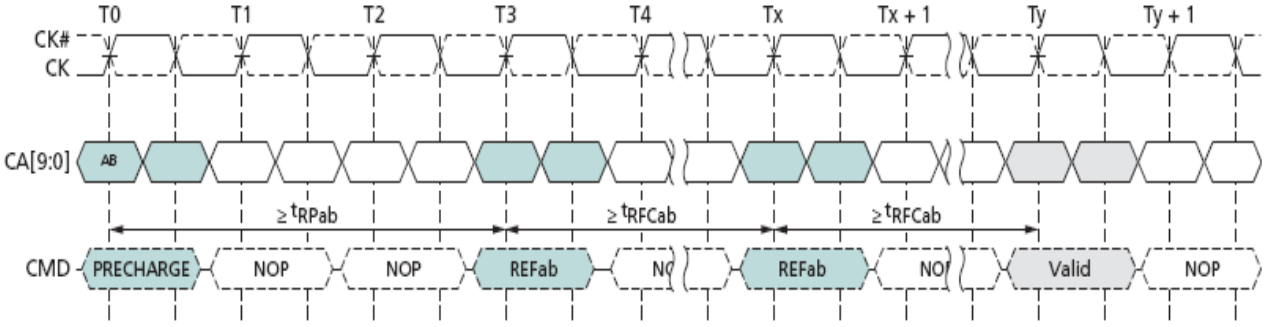
Supported Transition from Repetitive Burst REFRESH

Notes:
1. Shown with subsequent REFRESH pause to regular, distributed-refresh pattern.
2. As an example, in a 1Gb LPDDR2-S4 device at TC =< 85'C, the distributed refresh pattern has one REFRESH command per 7.8us; the burst refresh pattern has one refresh command per 0.52us, followed by ~30ms without any REFRESH command.

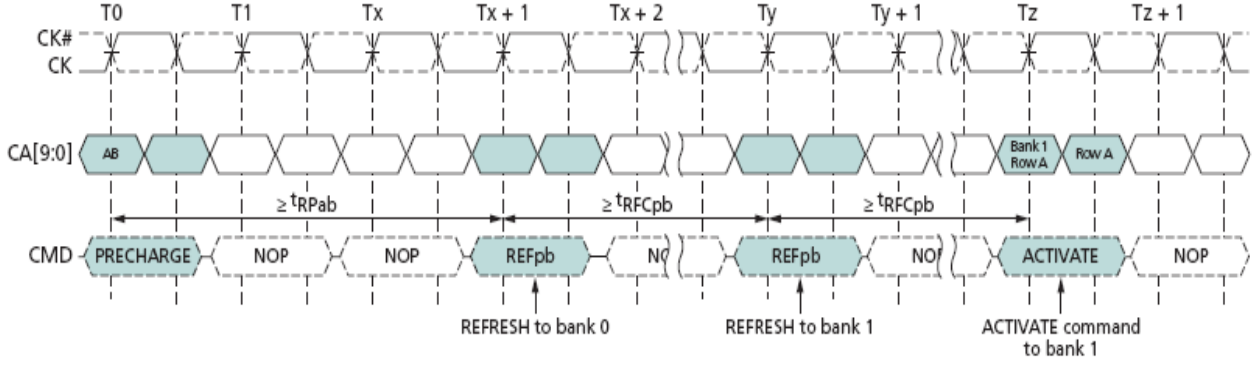


Recommended Self Refresh Entry and Exit

Notes:
1. In conjunction with a burst/pause refresh pattern.



All Bank Refresh Operation



Per-Bank Refresh Operation

Notes:
1. In the beginning of this example, the REFpb bank is pointing to Bank 0.
2. Operations to other banks than the bank being refreshed are allowed during the tREFpb period.

Self Refresh Operation

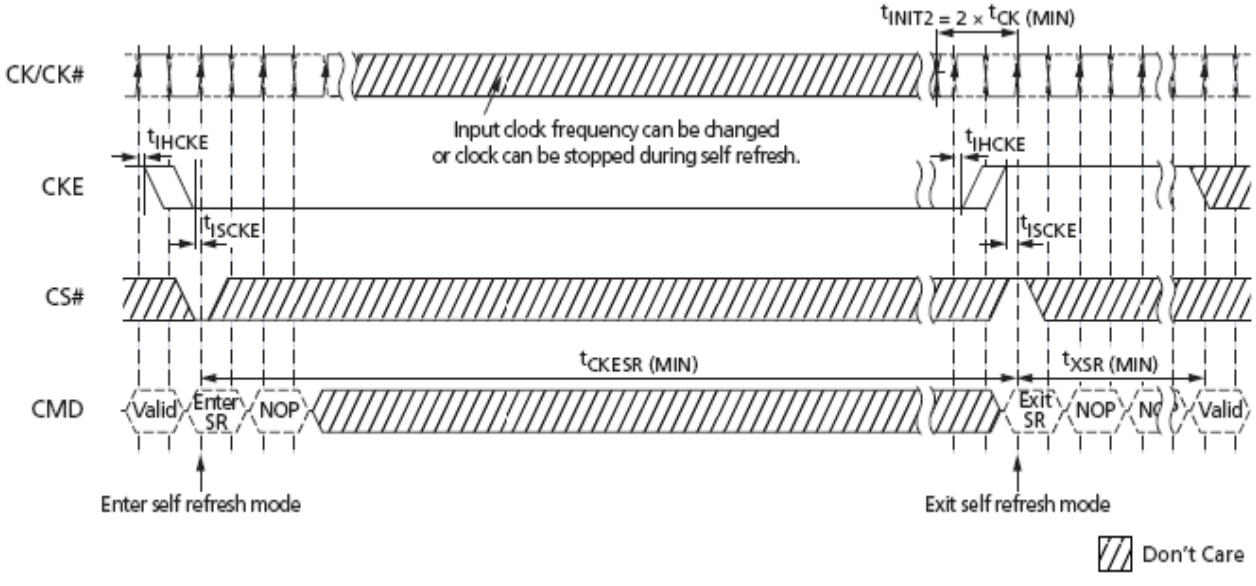
The Self Refresh command can be used to retain data in the LPDDR2 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the LPDDR2 SDRAM retains data without external clocking. The LPDDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having CKE LOW, $\overline{CS}$ LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. CKE must be HIGH during the previous clock cycle. A NOP command must be driven in the clock cycle following the power-down command. Once the command is registered, CKE must be held LOW to keep the device in Self Refresh mode.

LPDDR2-S4 devices can operate in Self Refresh in both the Standard or Extended Temperature Ranges. LPDDR2-S4 devices will also manage Self Refresh power consumption when the operating temperature changes, lower at low temperature and higher at high temperature.

Once the LPDDR2 SDRAM has entered Self Refresh mode, all of the external signals except CKE, are “don’t care”. For proper self refresh operation, power supply pins (VDD1, VDD2, and VDDCA) must be at valid levels. VDDQ may be turned off during Self-Refresh. Prior to exiting Self-Refresh, VDDQ must be within specified limits. VrefQD and VrefCA may be at any level within minimum and maximum levels. However prior to exiting Self-Refresh, VrefDQ and VrefCA must be within specified limits. The SDRAM initiates a minimum of one all-bank refresh command internally within Tckesr period, once it enters Self Refresh mode. The clock is internally disabled during Self Refresh Operation to save power. The minimum time that the LPDDR2 SDRAM must remain in Self Refresh mode is Tckesr. The user may change the external clock frequency or halt the external clock one clock after Self Refresh entry is registered; however, the clock must be restarted and stable before the device can exit Self Refresh operation.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock shall be stable and within specified limits for a minimum of 2 clock cycles prior to CKE going back HIGH. Once Self Refresh Exit is registered, a delay of at least Txsr must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period Txsr for proper operation except for self refresh re-entry. NOP commands must be registered on each positive clock edge during the Self Refresh exit interval Txsr.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, it is required that at least one Refresh command (8 per-bank or 1 all-bank) is issued before entry into a subsequent Self Refresh.



Self Refresh Operation

Notes:
1. Input clock frequency may be changed or stopped during self-refresh, provided that upon exiting self-refresh, a minimum of 2 clocks (Tinit2) of stable clock are provided and the clock frequency is between the minimum and maximum frequency for the particular speed grade.
2. Device must be in the “All banks idle” state prior to entering Self Refresh mode.
3. Txsr begins at the rising edge of the clock after CKE is driven HIGH.
4. A valid command may be issued only after Txsr is satisfied. NOPs shall be issued during Txsr.

Partial Array Self-Refresh: Bank Masking

LPDDR2-S4 SDRAM has 4 or 8 banks. For LPDDR2-S4 devices, 64Mb to 512Mb LPDDR2 SDRAM has 4 banks, while 1Gb and higher density has 8. Each bank of LPDDR2 SDRAM can be independently configured whether a self refresh operation is taking place. One mode register unit of 8 bits accessible via MRW command is assigned to program the bank masking status of each bank up to 8 banks. For bank masking bit assignments, see Mode Register 16.

The mask bit to the bank controls a refresh operation of entire memory within the bank. If a bank is masked via MRW, a refresh operation to entire bank is not blocked and data retention by a bank is not guaranteed in self refresh mode. To enable a refresh operation to a bank, a coupled mask bit has to be programmed, “unmasked”. When a bank mask bit is unmasked, the array space being refreshed within that bank is determinate by the programmed status of the segment mask bit.

Partial Array Self-Refresh: Segment Masking

Segment Programming segment mask bits is similar to programming bank mask bits. For densities 1Gb and higher, 8 segments are used for masking. Mode register 17 is used for programming segment mask bits up to 8 bits. For densities less than 1Gb, segment masking is not supported.

When the mask bit to an address range (represented as a segment) is programmed as “masked” a REFRESH operation to that segment is blocked. Conversely, when a segment mask bit to an address range is unmasked, refresh to that segment is enabled. A segment-masking scheme can be used in place of or in combination with a bank masking scheme in LPDDR2-S4 SDRAM. Each segment-mask bit setting is applied across all banks.

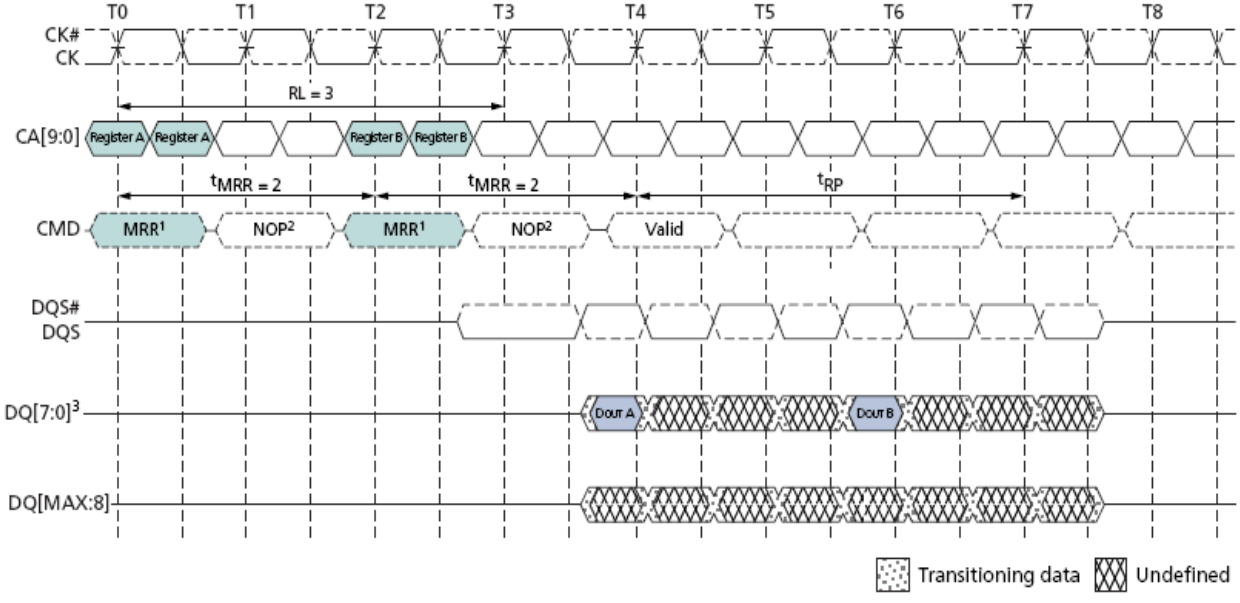
	Segment Mask (MR17)	Bnak 0	Bank 1	Bank 2	Bank 3	Bnak 4	Bank 5	Bank 6	Bank 7
Bank Mask (MR16)		0	1	0	0	0	0	0	1
Segment 0	0		M						M
Segment 1	0		M						M
Segment 2	1	M	M	M	M	M	M	M	M
Segment 3	0		M						M
Segment 4	0		M						M
Segment 5	0		M						M
Segment 6	0		M						M
Segment 7	1	M	M	M	M	M	M	M	M

Example of Bank and Segment Masking use in LPDDR2-S4 devices

Notes:
1. This table illustrates an example of an 8-bank LPDDR2-S4 device, when a refresh operation to bank 1 and bank 7, as well as segment 2 and segment 7 are masked.

Mode Register Read Command

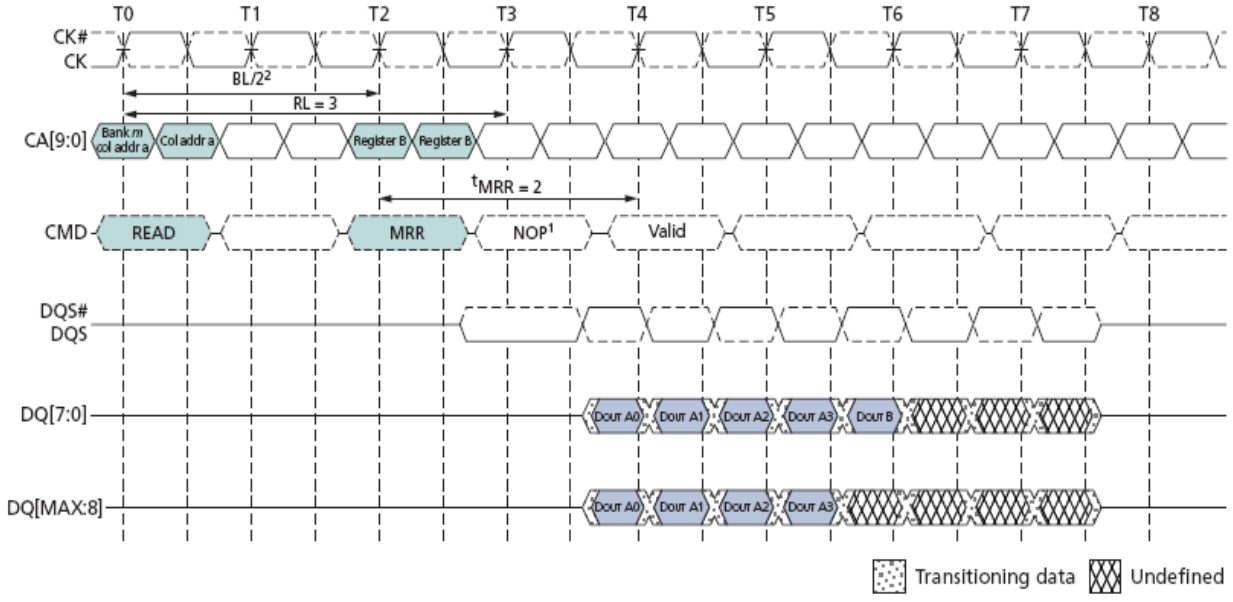
The Mode Register Read command is used to read configuration and status data from mode registers for LPDDR SDRAM. The Mode Register Read (MRR) command is initiated by having $\overline{CS}$ LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r-CA4r}. The mode register contents are available on the first data beat of DQ0-DQ7, RL * Tck + Tdqsck + Tdqsq after the rising edge of the clock where the Mode Register Read Command is issued. Subsequent data beats contain valid, but undefined content, except in the case of the DQ Calibration function DQC, where subsequent data beats contain valid content as described in “DQ Calibration”. All DQS shall be toggled for the duration of the Mode Register Read burst. The MRR command has a burst length of four. The Mode Register Read operation (consisting of the MRR command and the corresponding data traffic) shall not be interrupted. The MRR command period (Tmrr) is 2 clock cycles. Mode Register Reads to reserved and write-only registers shall return valid, but undefined content on all data beats and DQS shall be toggled.



Mode Register Read timing example: RL=3, Tmrr=2

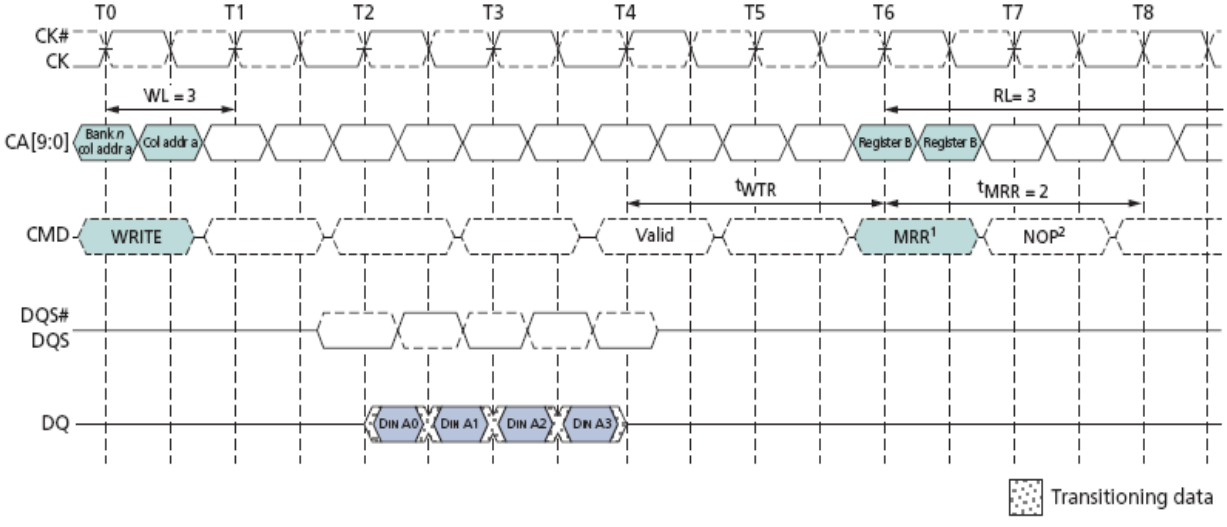
Notes:
1. Mode Register Read has a burst length of four.
2. Mode Register Read operation shall not be interrupted.
3. MRRs to DQ calibration registers MR32 and MR40 are described in “DQ Calibration”.
4. Only the NOP command is supported during Tmrr.
5. Mode register data is valid only on DQ[7:0] on the first beat. Subsequent beats contain valid but undefined data. DQ[MAX:8] contain valid but undefined data for the duration of the MRR burst.
6. Minimum Mode Register Read to write latency is RL+RU(Tdqsck,max/Tck)+4/2+1-WL clock cycles.
7. Minimum Mode Register Read to Mode Register Write Latency is RL+RU(Tdqsck,max/Tck)+4/2+1 clock cycles.

After a prior READ command, the MRR command must not be issued earlier than BL/2 clock cycles, or WL + 1 + BL/2 + RU(Twtr/Tck) clock cycles after a prior WRITE command, as READ bursts and WRITE bursts must not be truncated by MRR. Note that if a READ or WRITE burst is truncated with a BST command, the effective burst length of the truncated burst should be used for the value BL.



Read to MRR timing example: RL=3, Tmrr=2

Notes:
1. The minimum number of clocks from the burst read command to the Mode Register Read command is BL/2.
2. Only the NOP command is supported during Tmrr.



Burst Write Followed by MRR: RL=3, WL=1, BL=4

Notes:
1. The minimum number of clock cycles from the burst write command to the Mode Register Read command is [WL + 1 + BL/2 + RU(Twtr/Tck)].
2. Only the NOP command is supported during Tmrr.

Temperature Sensor

LPDDR2 devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing derating is required in the extended temperature range, and/or monitor the operating temperature. Either the temperature sensor or the device operating temperature can be used to determine if operating temperature requirements are being met.

Temperature sensor data may be read from MR4 using the Mode Register Read protocol.

When using the temperature sensor, the actual device case temperature may be higher than the operating temperature specification that applies for the standard or extended temperature ranges. For example, TCASE could be above 85'C when MR4[2:0] equals 011B.

To assure proper operation using the temperature sensor, applications must accommodate the specifications shown in bellow.

Parameter	Symbol	Max/Min	Value	Unit	Notes
System Temperature Gradient	TempGradient	Max	System Dependent	C/s	Maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2'C.
MR4 Read Interval	ReadInterval	Max	System Dependent	ms	Time period between MR4 READs from the system.
Temperature Sensor Interval	tTSI	Max	32	ms	Maximum delay between internal updates of
System Response Delay	SysRespDelay	Max	System Dependent	ms	Maximum response time from an MR4 READ to the system response.
Device Temperature Margin	TempMargin	Max	2	C	Margin above maximum temperature to support controller response.

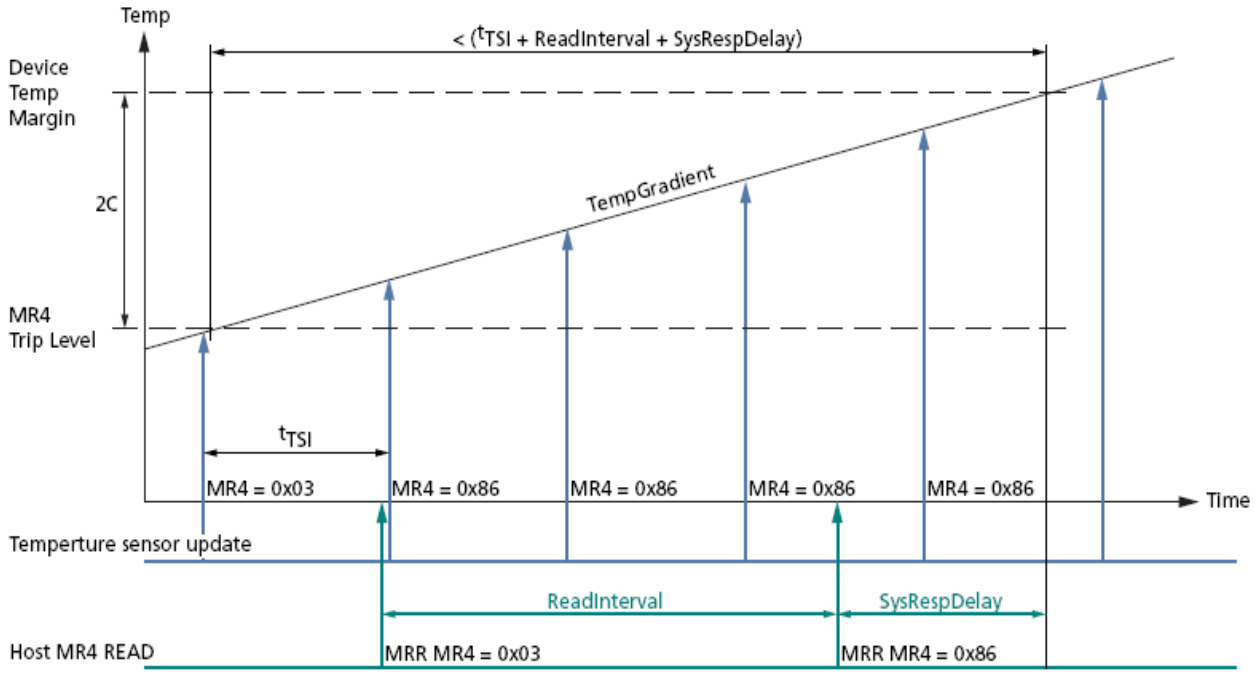
These devices accommodate the 2 degree Celsius temperature margin between the point at which the device temperature enters the extended temperature range and point at which the controller re-configures the system accordingly. To determine the required MR4 polling frequency, the system must use the maximum TempGradient and the maximum response time of the system using the following equation:

TempGradient x (ReadInterval + tTSI + SysRespDelay) =< 2'C

For example, if TempGradient is 10'C/s and the SysRespDelay is 1ms:

10'C/s x (ReadInterval + 32ms + 1ms) =< 2'C

In this case, ReadInterval shall be no greater than 167 ms.



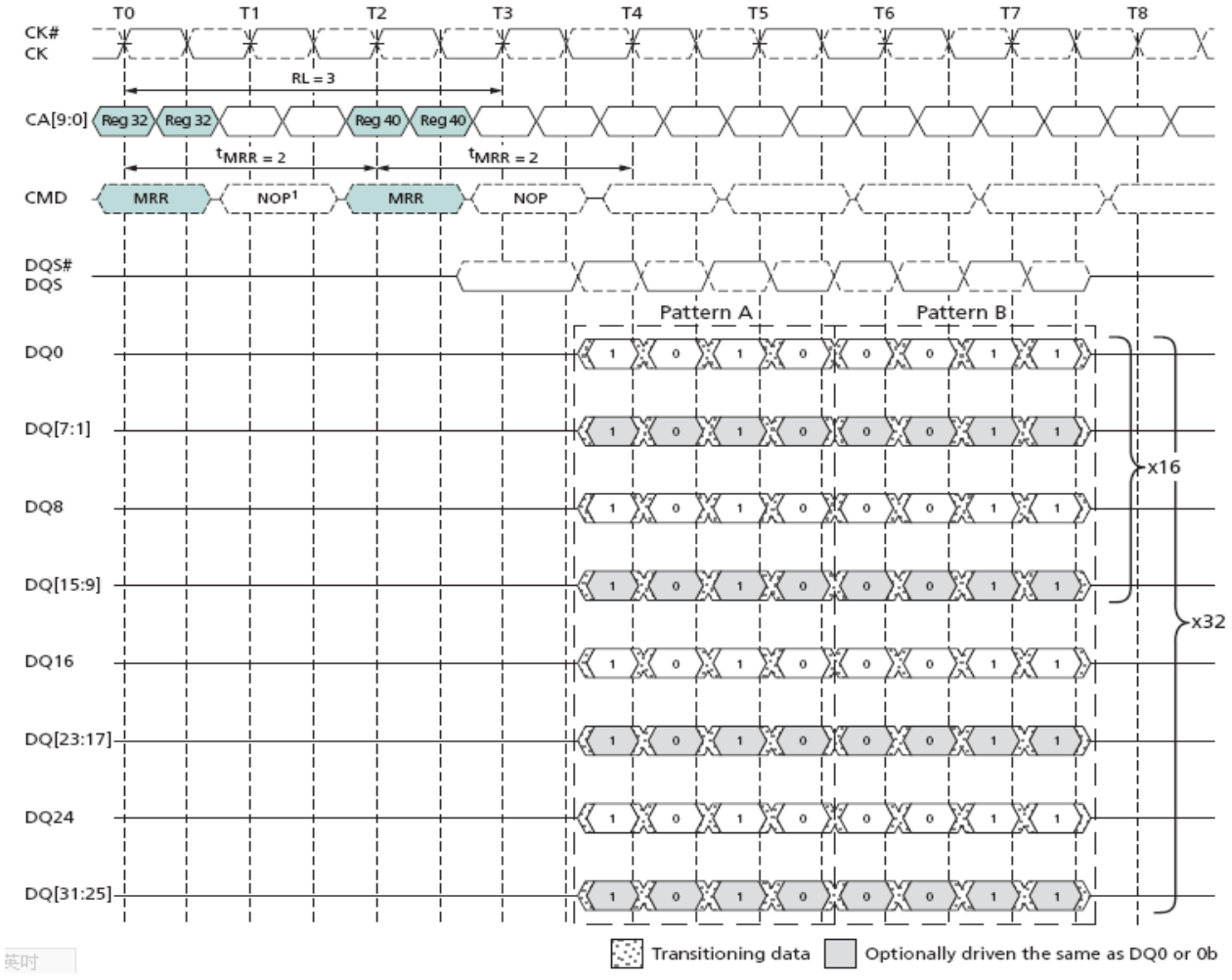
Temp Sensor Timing

DQ Calibration

LPDDR2 devices feature a DQ calibration function that outputs one of two predefined system-timing calibration patterns. MRR to MR32 (pattern A) or MRR to MR40 (pattern B) will return the specified pattern on DQ0 and DQ8 for x16 devices and DQ0, DQ8, DQ16, and DQ24 for x32 devices. For x16 devices, DQ[7:1] and DQ[15:9] drive the same information as DQ0 during the MRR burst. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] drive the same information as DQ0 during the MRR burst. MRR DQ calibration commands can occur only in the idle state.

Data Calibration Pattern Description

	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3
Pattern "A" (MR32)	1	0	1	0
Pattern "B" (MR40)	0	0	1	1

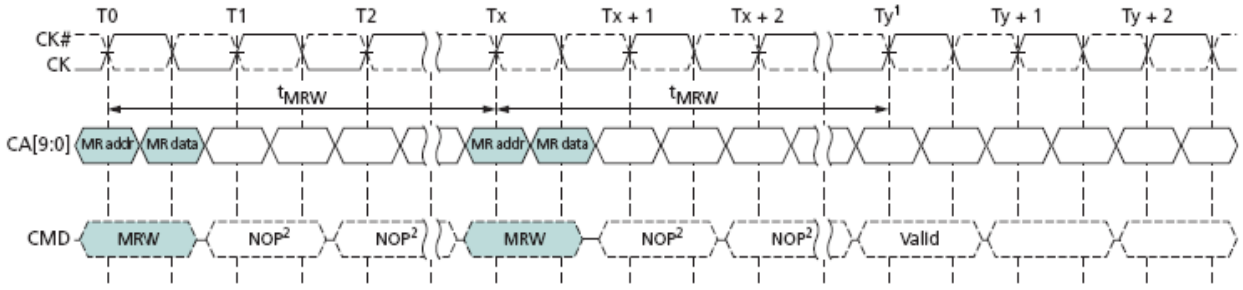


DQ MR32 and MR40 DQ Calibration timing, example: RL=3, ^{t}MRR=2

Notes: Only the NOP command is supported during Tmrr. Mode Register Read has BL4 and shall not be interrupted.

Mode Register Write Command

The MRW command is used to write configuration data to mode registers. The MRW command is initiated with $\overline{CS}$ LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by CA1f-CA0f, CA9r-CA4r. The data to be written to the mode register is contained in CA9f-CA2f. The MRW command period is defined by Tmrw. Mode register WRITEs to read-only registers have no impact on the functionality of the device.



Mode Register Write timing, example: RL=3, Tmrw=5

Notes:
1. Only the NOP command is supported during Tmrw.
2. At time Ty, the device is in the idle state.

The MRW can only be issued when all banks are in the idle precharge state. One method of ensuring that the banks are in this state is to issue a PRECHARGE-ALL command.

Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)

Current Stat	Command	Intermediate State	Next State
All Banks idle	MRR	Mode Register Reading (All Banks idle)	All Banks idle
	MRW	Mode Register Writing (All Banks idle)	All Banks idle
	MRW (Reset)	Restting (Device Auto-Init)	All Banks idle
Bank(s) Active	MRR	Mode Register Reading (Bank(s) idle)	Bank(s) Active
	MRW	Not Allowed	Not Allowed
	MRW (Reset)	Not Allowed	Not Allowed

Mode Register Write Reset (MRW Reset)

The MRW RESET command brings the device to the device auto-initialization (resetting) state in the power-on initialization sequence. The MRW RESET command can be issued from the idle state. This command resets all mode registers to their default values. Only the NOP command is supported during Tinit4. After MRW RESET, boot timings must be observed until the device initialization sequence is complete and the device is in the idle state. Array data is undefined after the MRW RESET command.

Mode Register Write ZQ Calibration command

The MRW command is used to initiate the ZQ calibration command. This command is used to calibrate the output driver impedance across process, temperature, and voltage. LPDDR2-S4 devices support ZQ calibration.

There are four ZQ calibration commands and related timings: Tzqinit, Tzqreset, Tzqcl, and Tzqcs. Tzqinit is for initialization calibration; Tzqreset is for resetting ZQ to the default output impedance; Tzqcl is for long calibration(s); and Tzqcs is for short calibration(s).

The initialization ZQ calibration (ZQINIT) must be performed for LPDDR2-S4. ZQINIT provides an output impedance accuracy of +/-15 percent. After initialization, the ZQ calibration long (ZQCL) can be used to recalibrate the system to an output impedance accuracy of +/-15 percent. A ZQ calibration short (ZQCS) can be used periodically to compensate for temperature and voltage drift in the system.

The ZQ reset command (ZQRESET) resets the output impedance calibration to a default accuracy of +/-30% across process, voltage, and temperature. This command is used to ensure output impedance accuracy to +/-30% when ZQCS and ZQCL commands are not used.

One ZQCS command can effectively correct at least 1.5% (ZQ correction) of output impedance errors within Tzqcs for all speed bins, assuming the maximum sensitivities specified are met. The appropriate interval between ZQCS commands can be determined from using these tables and system-specific parameters.

LPDDR2 devices are subject to temperature drift rate (Tdriftrate) and voltage drift rate (Vdriftrate) in various applications. To accommodate drift rates and calculate the necessary interval between ZQCS commands, apply the following formula:

$$\frac{\text{ZQcorrection}}{(\text{Tsens} \times \text{Tdriftrate}) + (\text{Vsens} \times \text{Vdriftrate})}$$

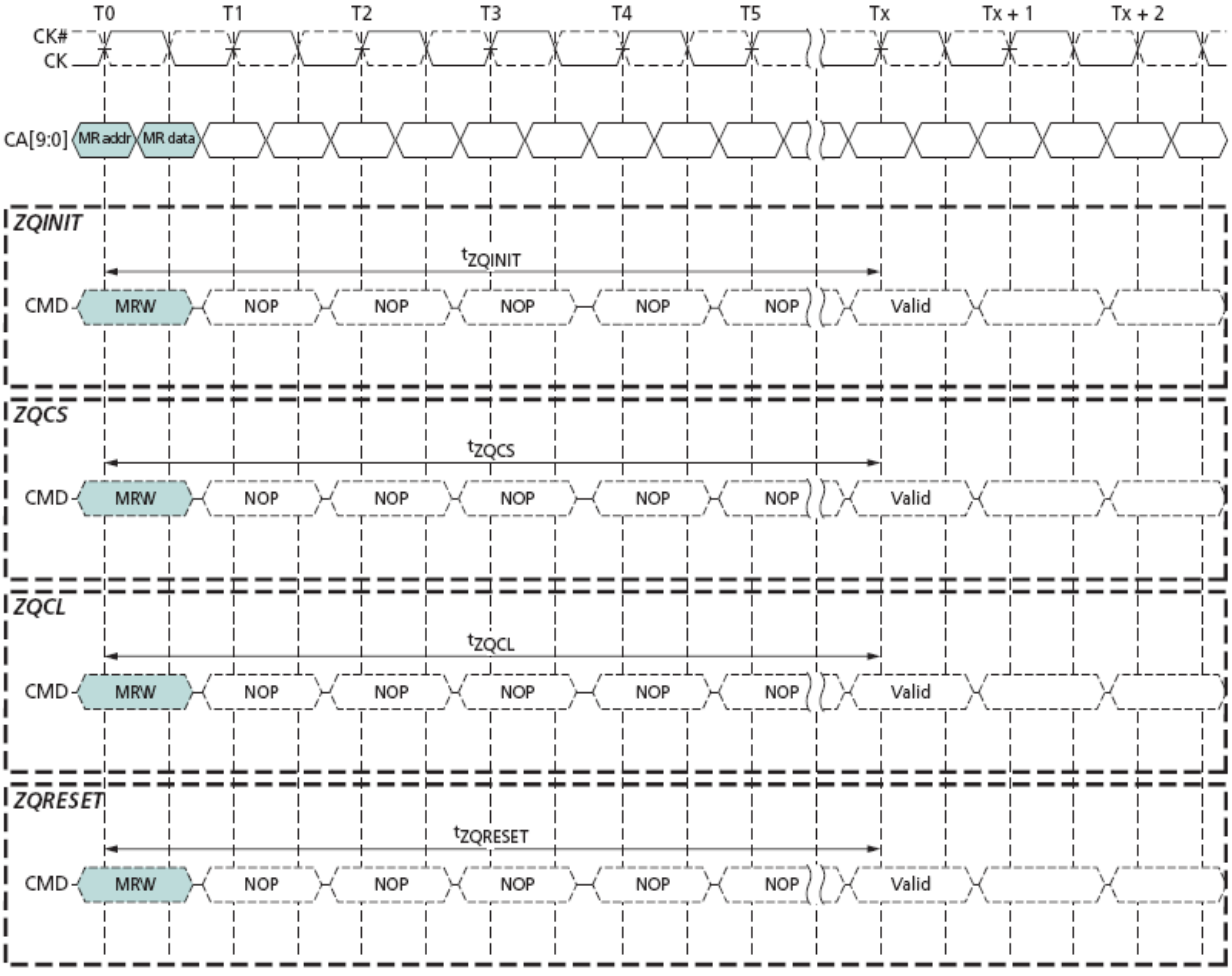
where Tsens = max(dRONdT) and Vsens = max(dRONdV), define the LPDDR2 temperature and voltage sensitivities.

For example, if Tsens = 0.75% / C, Vsens = 0.20% / Mv, Tdriftrate = 1 C / sec and Vdriftrate = 15 Mv / sec, then the interval between ZQCS commands is calculated as:

$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4\text{s}$$

For LPDDR2-S4 devices, a ZQ Calibration command may only be issued when the device is in Idle state with all banks precharged. No other activities can be performed on the LPDDR2 data bus during the calibration period (Tzqinit, Tzqcl, Tzqcs). The quiet time on the LPDDR2 data bus helps to accurately calibrate RON. There is no required quiet time after the ZQ Reset command. If multiple devices share a single ZQ Resistor, only one device may be calibrating at any given time. After calibration is achieved, the LPDDR2 device shall disable the ZQ ball's current consumption path to reduce power.

In systems that share the ZQ resistor between devices, the controller must not allow overlap of Tzqinit, Tzqcs, or Tzqcl between the devices. ZQ Reset overlap is allowed. If the ZQ resistor is absent from the system, ZQ shall be connected permanently to VDDCA. In this case, the LPDDR2 shall ignore ZQ calibration commands and the device will use the default calibration settings.



ZQ Calibration Initialization timing example

Notes:
1. Only the NOP command is supported during ZQ calibration.
2. CKE must be registered HIGH continuously during the calibration period.
3. All devices connected to the DQ bus should be High-Z during the calibration process.

ZQ External Resistor Value, Tolerance and Capacitive Loading

To use the ZQ Calibration function, a 240 Ohm +/- 1% tolerance external resistor must be connected between the ZQ pin and ground. A single resistor can be used for each LPDDR2 device or one resistor can be shared between multiple LPDDR2 devices if the ZQ calibration timings for each LPDDR2 device do not overlap. The total capacitive loading on the ZQ pin must be limited.

Power Down

Power-down is entered synchronously when CKE is registered LOW and $\overline{CS}$ is HIGH at the rising edge of clock. CKE must be registered HIGH in the previous clock cycle. A NOP command must be driven in the clock cycle following the power-down command. CKE must not go LOW while MRR, MRW, READ, or WRITE operations are in progress. CKE can go LOW while any other operations such as row activation, PRECHARGE, auto precharge, or REFRESH are in progress, but the power-down IDD specification will not be applied until such operations are complete. Power-down entry and exit are shown in below timing diagram.

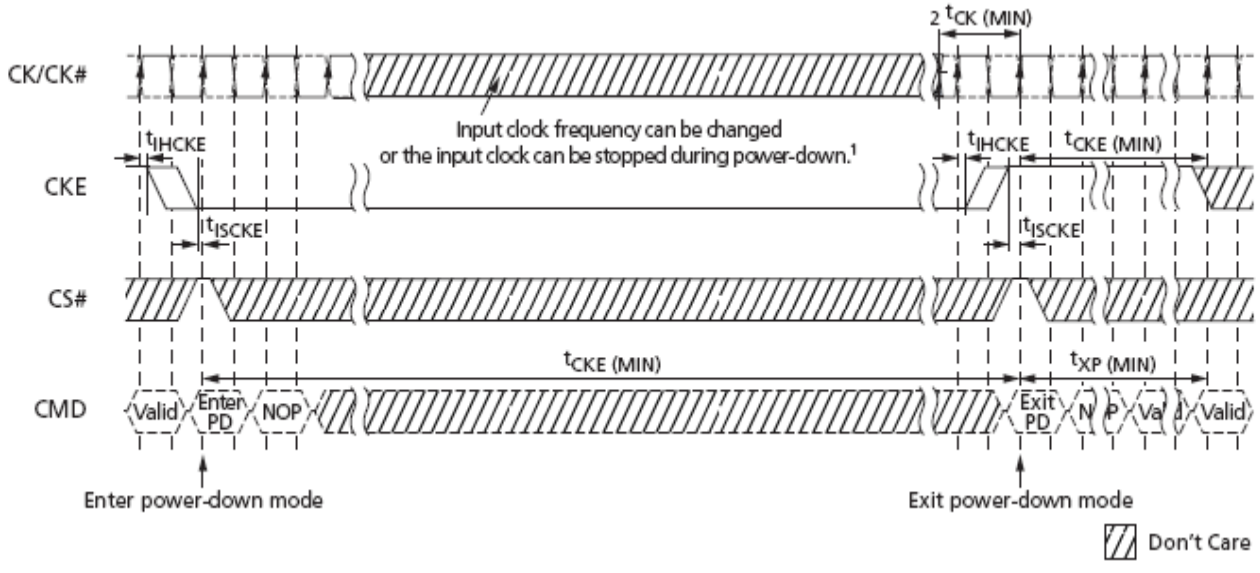
If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down.

Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$, and CKE. In power-down mode, CKE must be held LOW; all other input signals are "Don't Care." CKE LOW must be maintained until Tcke is satisfied. VREFCA must be maintained at a valid level during power-down.

VDDQ can be turned off during power-down. If VDDQ is turned off, VREFDQ must also be turned off. Prior to exiting power-down, both VDDQ and VREFDQ must be within their respective minimum/maximum operating ranges.

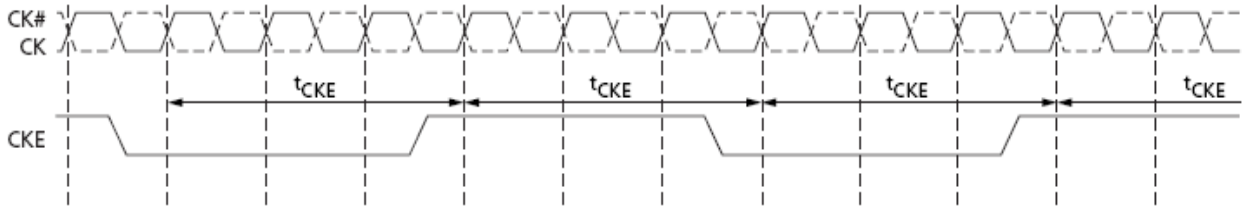
No refresh operations are performed in power-down mode. The maximum duration in power-down mode is only limited by the refresh requirements outlined in section "REFRESH Command".

The power-down state is excited when CKE is registered HIGH. The controller must drive $\overline{CS}$ HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until Tcke is satisfied. A valid, executable command can be applied with power-down exit latency Txp after CKE goes HIGH.

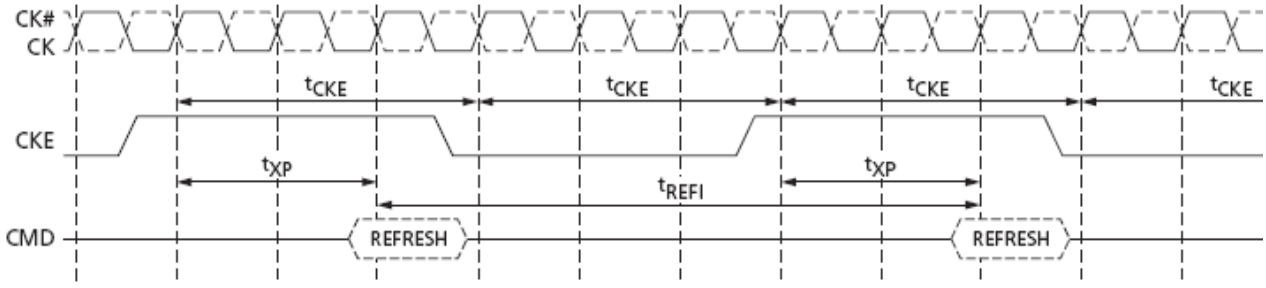


Basic Power-Down entry and exit timing

Notes: Input clock frequency can be changed or the input clock stopped during power-down, provided that the clock frequency is between the minimum and maximum specified frequencies for the speed grade in use, and that prior to power-down exit, a minimum of 2 stable clocks complete.

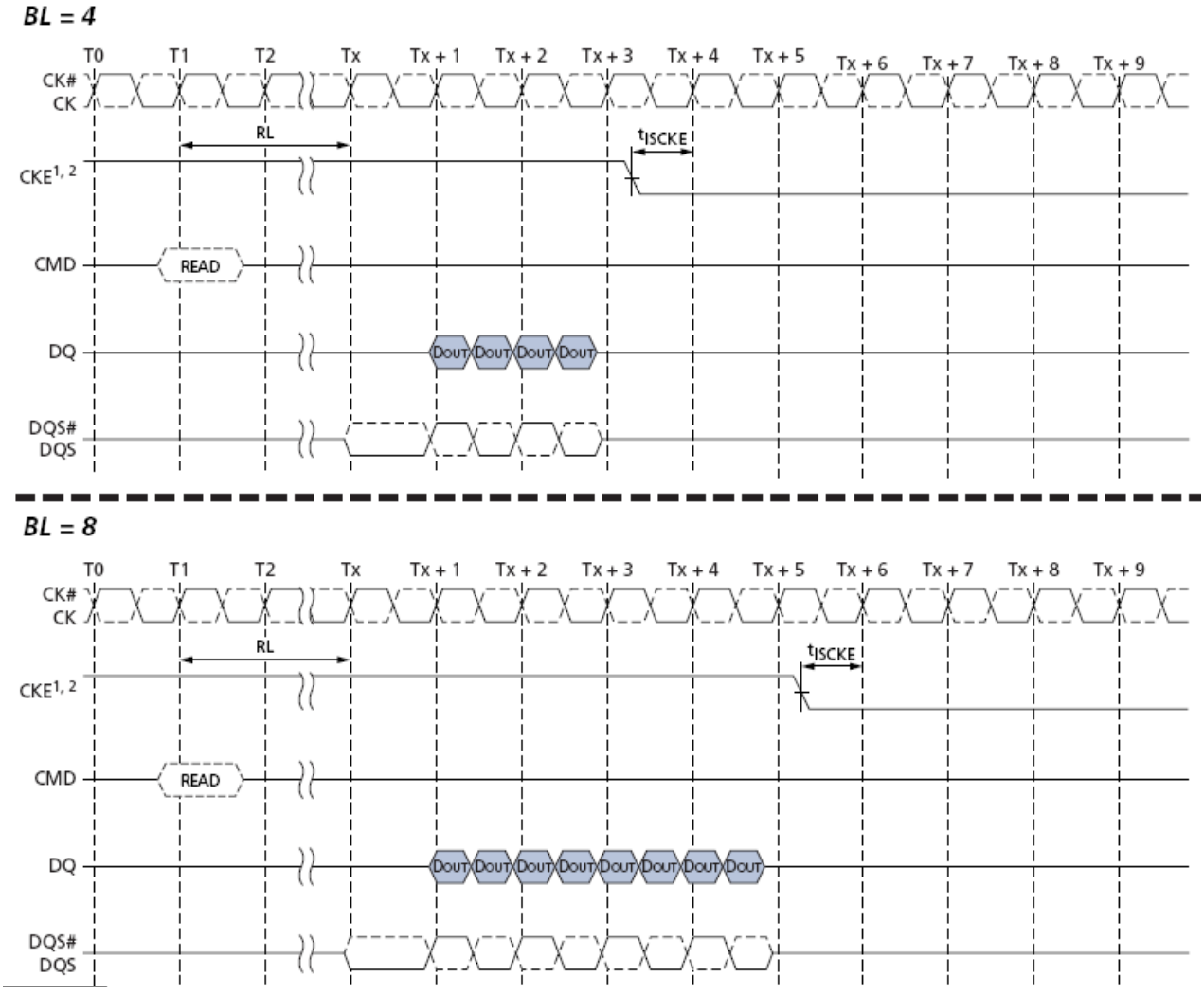


CKE intensive environment



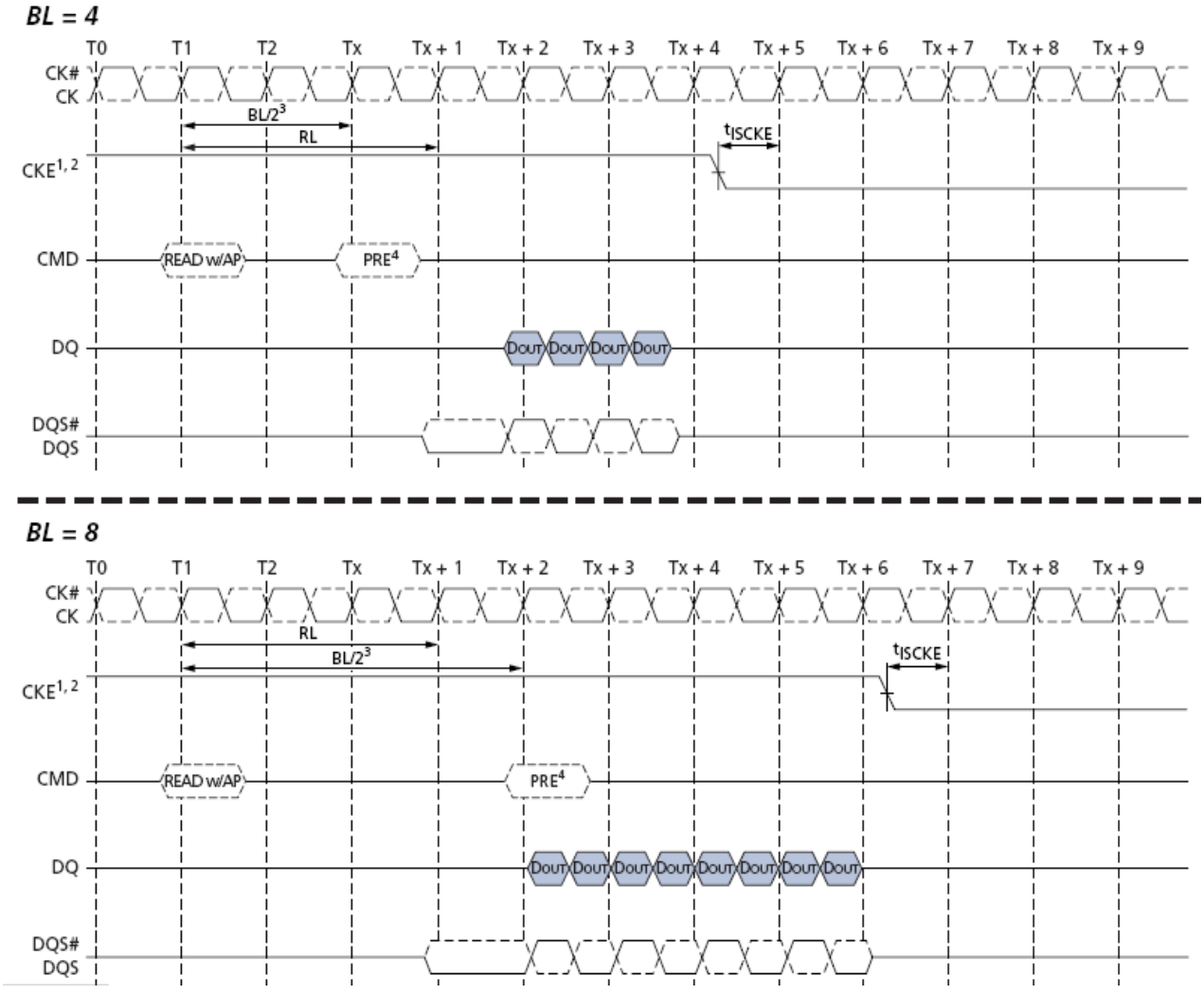
REF to REF timing in CKE intensive environment

Notes:
1. The pattern shown above can repeat over a long period of time. With this pattern, LPDDR2 SDRAM guarantees all AC and DC timing & voltage specifications with temperature and voltage drift ensured.



Read to Power-Down entry

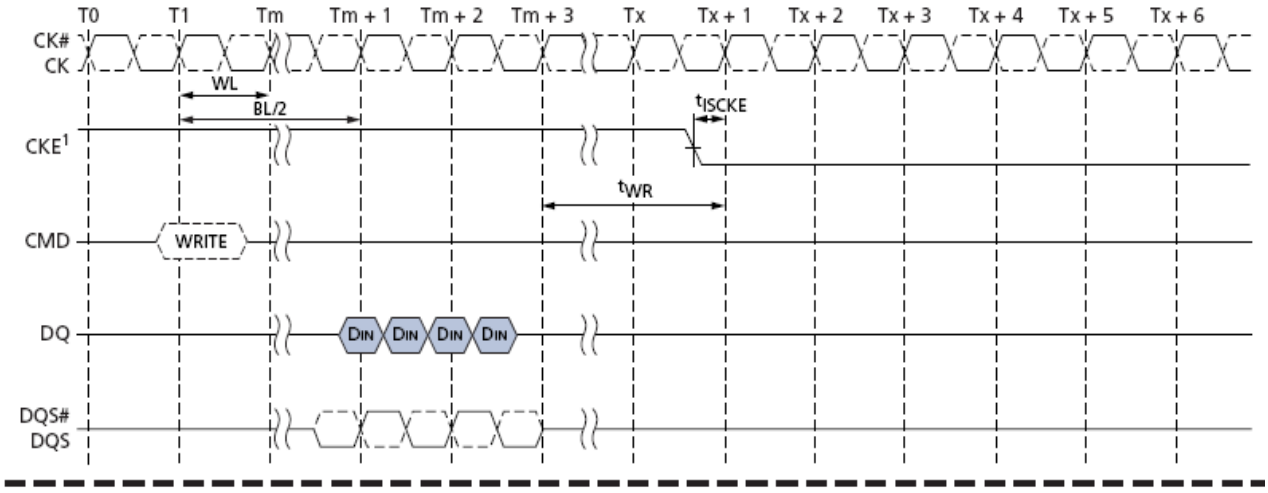
Notes:
1. CKE must be held HIGH until the end of the burst operation.
2. CKE may be registered LOW RL + RU(tDQSCK(MAX)/tCK) + BL/2 + 1 clock cycles after the clock on which the Read command is registered.



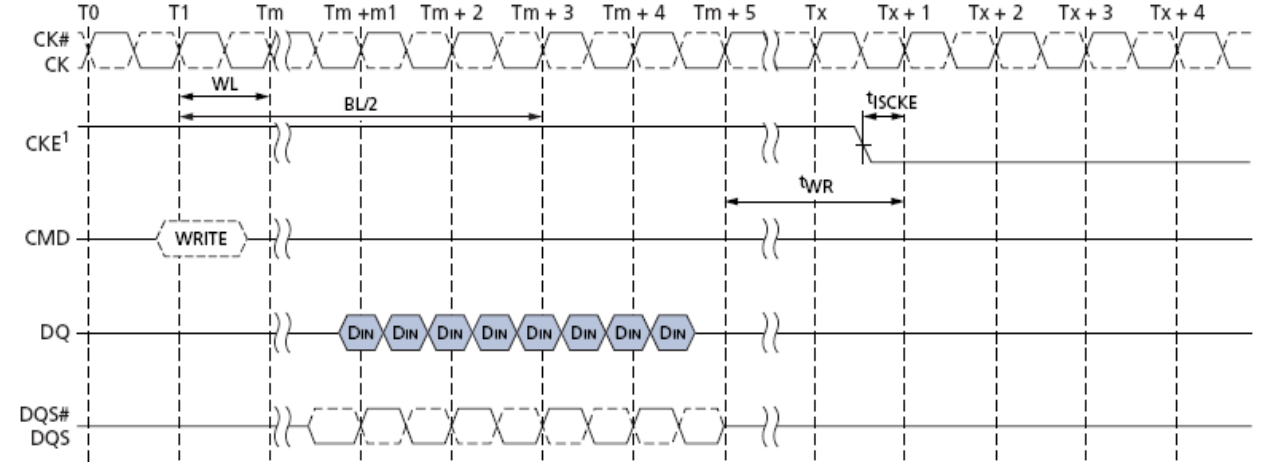
Read with Auto-precharge to Power-Down entry

Notes:
1. CKE must be held HIGH until the end of the burst operation.
2. CKE can be registered LOW at RL + RU(Tdqsck/Tck)+ BL/2 + 1 clock cycles after the clock on which the READ command is registered.
3. BL/2 with Trtp = 7.5ns and Tras (MIN) is satisfied.
4. Start internal PRECHARGE.

BL = 4



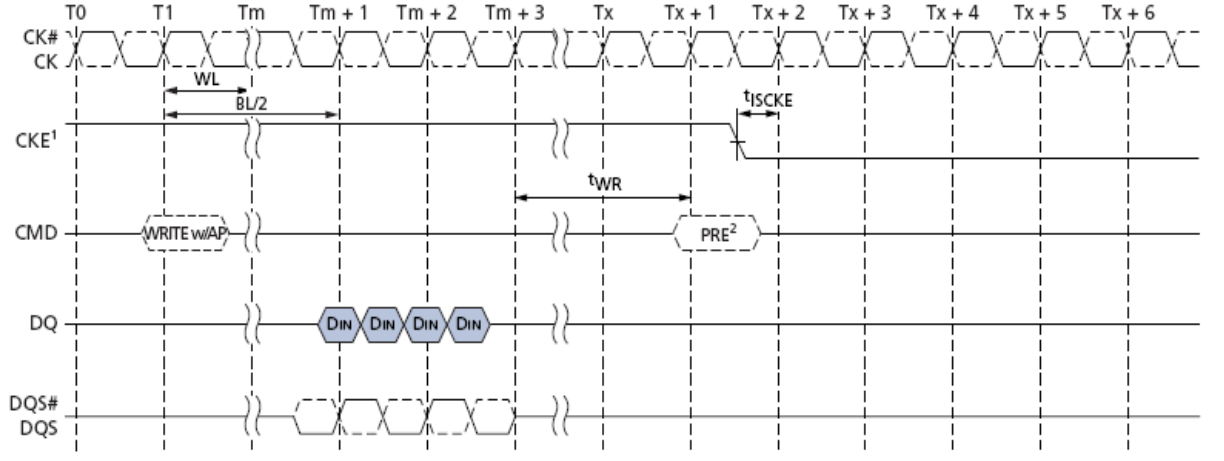
BL = 8



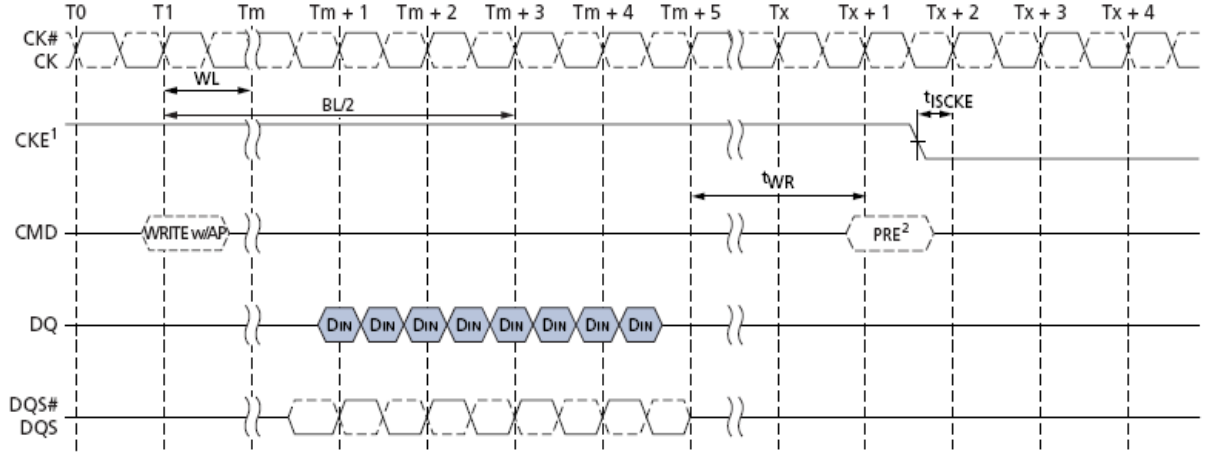
Write to Power-Down entry

Notes:
5. CKE can be registered LOW at WL + 1 + BL/2 + RU(Twr/Tck) clock cycles after the clock on which the WRITE command is registered.

BL = 4

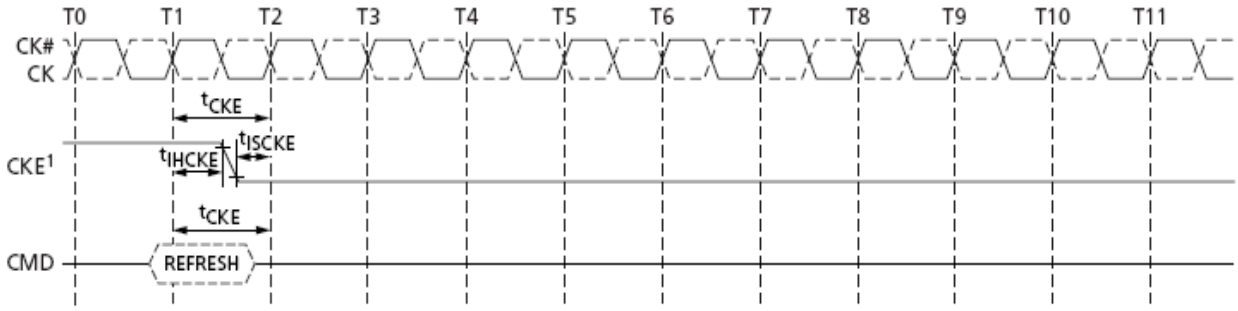


BL = 8



Write with Auto-precharge to Power-Down entry

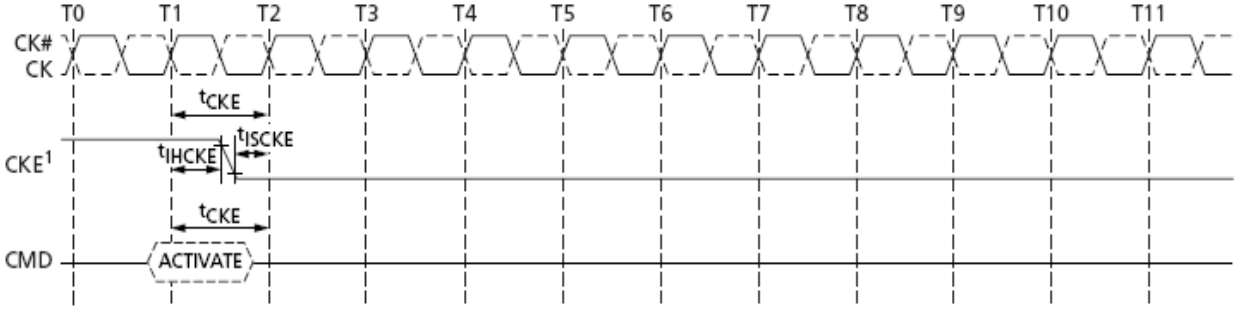
Notes:
1. CKE may be registered LOW WL + 1 + BL/2 + RU(tWR/tCK) +1 clock cycles after the Write command is registered.
2. Start internal PRECHARGE.



Refresh command to Power-Down entry

Notes:

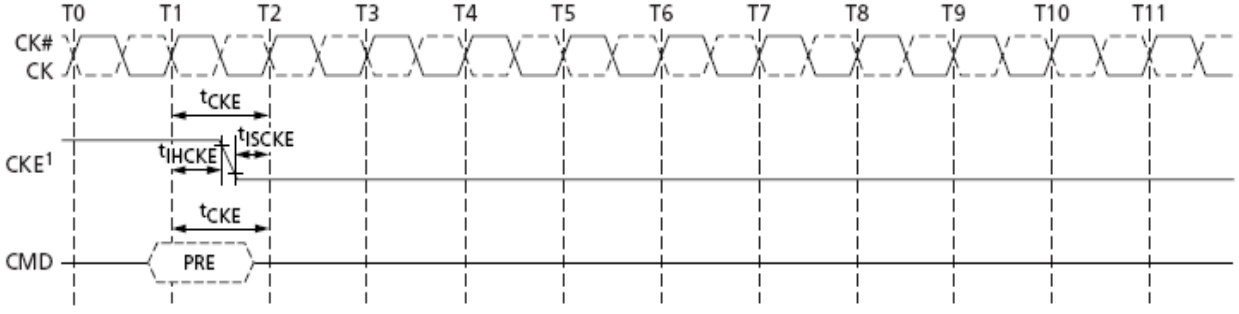
1. CKE may go LOW ^{t}IHCKE after the clock on which the Refresh command is registered.



Activate command to Power-Down entry

Notes:

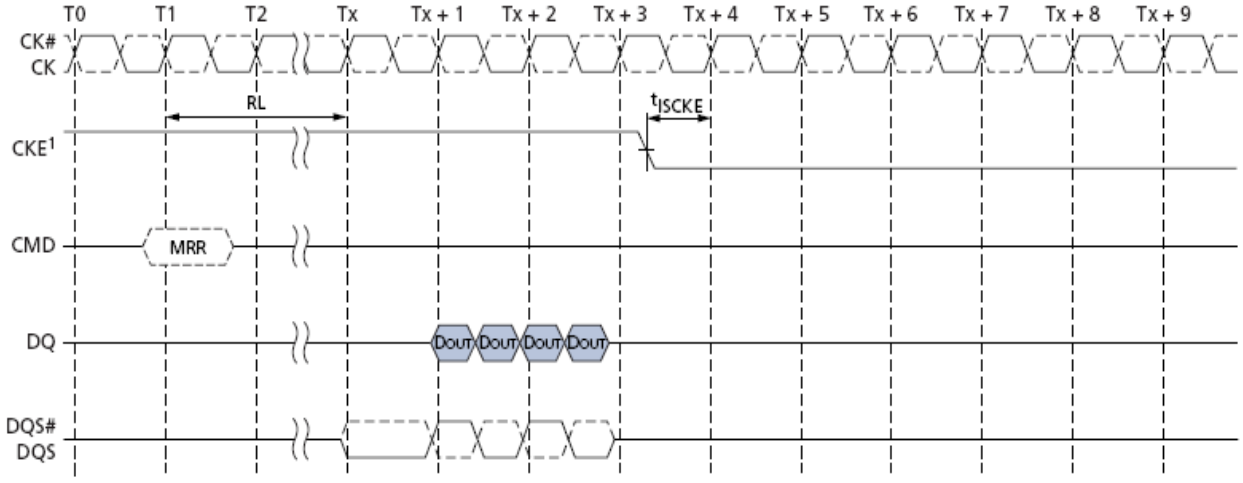
1. CKE may go LOW ^{t}IHCKE after the clock on which the Activate command is registered.



Precharge command to Power-Down entry

Notes:

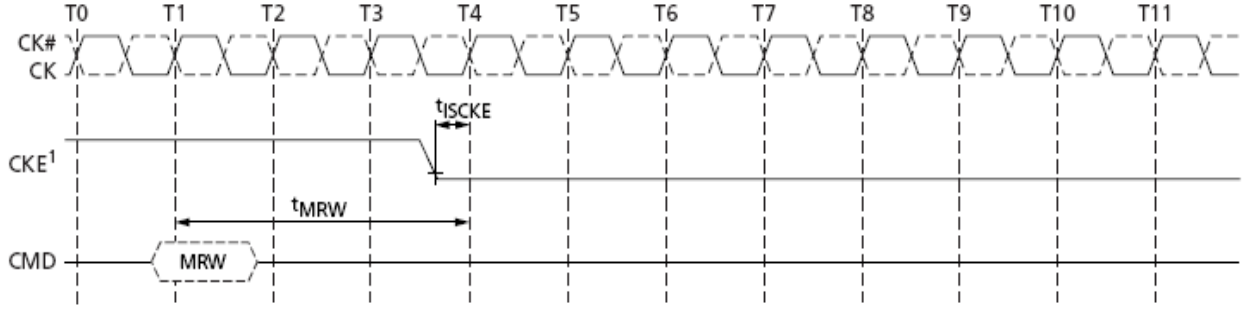
1. CKE may go LOW ^{t}IHCKE after the clock on which the Precharge command is registered.



Mode Register Read to Power-Down entry

Notes:

1. CKE may be registered LOW RL + RU(^{t}DQSCK/^{t}CK)+ BL/2 + 1 clock cycles after the clock on which the Mode Register Read command is registered.



Mode Register Write to Power-Down entry

Notes:

6. CKE may be registered LOW ^{t}MRW after the clock on which the Mode Register Write command is registered.

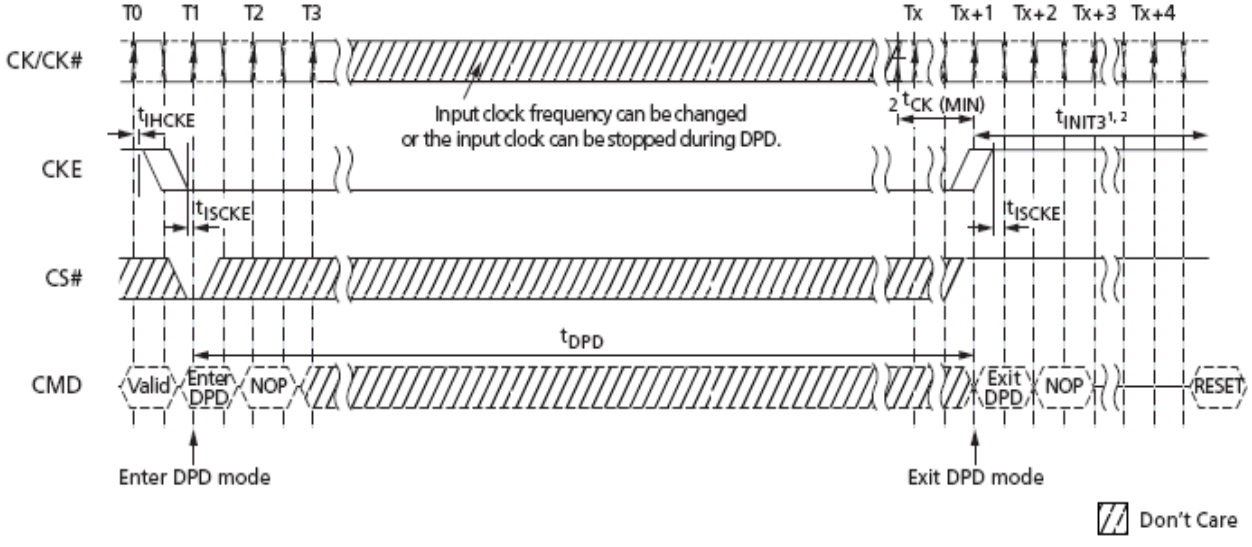
Deep Power Down

Deep Power-Down is entered when CKE is registered LOW with $\overline{CS}$ LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of clock. A NOP command must be driven in the clock cycle following the power-down command. CKE is not allowed to go LOW while mode register, read, or write operations are in progress. All banks must be in idle state with no activity on the data bus prior to entering the Deep Power Down mode. During Deep Power-Down, CKE must be held LOW.

In Deep Power-Down mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry may be disabled within the SDRAM. All power supplies must be within specified limits prior to exiting Deep Power-Down. VrefDQ and VrefCA may be at any level within minimum and maximum levels. However prior to exiting Deep Power-Down, Vref must be within specified limits.

The contents of the SDRAM may be lost upon entry into Deep Power-Down mode.

The Deep Power-Down state is exited when CKE is registered HIGH, while meeting Tiscke with a stable clock input. The SDRAM must be fully re-initialized as described in the Power up initialization Sequence. The SDRAM is ready for normal operation after the initialization sequence.



Deep Power-Down entry and exit timing diagram

Notes:
1. Initialization sequence may start at any time after Tx + 1.
2. Tinit3 and Tx + 1 and refer to timings in the initialization sequence.
3. The clock is stable and within specified limits for a minimum of 2 clock cycles prior to deep power down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

Input clock stop and frequency change

LPDDR2 devices support input clock frequency change during CKE LOW under the following conditions:

- Tck(abs)min is met for each clock cycle
- Refresh requirement apply during clock frequency change
- During clock frequency change, only REFab or REFpb commands may be executing
- Any ACTIVATE or PRECHARGE commands have completed prior to changing the frequency
- Related timing conditions,Trcd and Trp, have been met prior to changing the frequency
- The initial clock frequency must be maintained for a minimum of 2 clock cycles after CKE goes LOW
- The clock satisfies Tch(abs) and Tcl(abs) for a minimum of two clock cycles prior to CKE going HIGH.

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL, etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR2 devices support clock stop during CKE LOW under the following conditions:

- CK is held LOW and $\overline{CK}$ is held HIGH during clock stop
- Refresh requirements are met
- Only REFab or REFpb commands can be in process
- Any ACTIVATE or PRECHARGE commands have completed prior to changing the frequency
- Related timing conditions,Trcd and Trp, have been met prior to changing the frequency
- The initial clock frequency must be maintained for a minimum of 2 clock cycles after CKE goes LOW
- The clock satisfies Tch(abs) and Tcl(abs) for a minimum of two clock cycles prior to CKE going HIGH

LPDDR2 devices support input clock frequency change during CKE HIGH under the following conditions:

- Tck(abs)min is met for each clock cycle
- Refresh requirement apply during clock frequency change
- Any Activate, Read, Write, Precharge, Mode Register Write or Mode Register Read commands must have executed to completion including any associated data bursts prior to changing the frequency
- The related timing conditions (Trcd, Twr, Twra, Trp,Tmrw,Tmrr etc) have been met prior to changing the frequency
- $\overline{CS}$ shall be held HIGH during clock frequency change
- During clock frequency change, only REFab or REFpb commands may be executing
- The LPDDR2 device is ready for normal operation after the clock satisfies Tch(abs) and Tcl(abs) for a minimum of 2Tck+Txp

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL, etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR2 devices support clock stop during CKE HIGH under the following conditions:

- CK is held LOW and $\overline{CK}$ is held HIGH during clock stop
- $\overline{CS}$ shall be held HIGH during clock stop
- Refresh requirements are met
- Only REFab or REFpb commands can be in process
- Any Activate, Read, Write, Precharge, Mode Register Write or Mode Register Read commands must have executed to completion including any associated data bursts prior to stopping the clock
- The related timing conditions (Trcd, Twr, Twra, Trp,Tmrw,Tmrr etc) have been met prior to stopping the clock
- The LPDDR2 device is ready for normal operation after the clock is restarted and satisfies Tch(abs) and Tcl(abs) for a minimum of 2Tck+Txp

No Operation Command

The purpose of the No Operation command (NOP) is to prevent the LPDDR2 device from registering any unwanted command between operations. Only when the CKE level is constant for clock cycle N-1 and clock cycle N, a NOP command may be issued at clock cycle N. A NOP command has two possible encodings:

1. $\overline{CS}$ HIGH at the clock rising edge N.
2. $\overline{CS}$ LOW and CA0, CA1, CA2 HIGH at the clock rising edge N.

The No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

Absolute Maximum DC Ratings

Symbol	Parameter	Min	Max	Units	Note
V_{DD1}	Voltage on V_{DD1} pin relative to Vss	-0.4	2.3	V	2
V_{DD2}	Voltage on V_{DD2} pin relative to Vss	-0.4	1.6	V	2
V_{DDCA}	Voltage on V_{DDCA} pin relative to Vss	-0.4	1.6	V	2,4
V_{DDQ}	Voltage on V_{DDQ} pin relative to Vss	-0.4	1.6	V	2,3
Vin, Vout	Voltage on any pin relative to Vss	-0.4	1.6	V	
T_{stg}	Storage Temperature (plastic)	-55	125	°C	5

Notes :

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. See “Power-Ramp” for relationships between power supplies.
3. VREFDQ =< 0.6 x VDDQ; however, VREFDQ may be => VDDQ provided that VREFDQ =< 300mV.
4. VREFCA =< 0.6 x VDDCA; however, VREFCA may be => VDDCA provided that VREFCA =< 300mV.
5. Storage Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.

AC/DC Operating Conditions

Operating Temperature Condition

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Operating case temperature(Commercial)	-25 to +85	°C	
T_{OPER}	Operating case temperature(Industrial)	-40 to +85	°C	

Notes :

1. Operating Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.

2. Either the device case temperature rating or the temperature sensor may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the TOPER rating that applies for the Standard or Extended Temperature Ranges. For example, TCASE may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD1	Core supply voltage 1	1.70	1.80	1.95	V	
VDD2	Core supply voltage 2	1.14	1.20	1.30	V	
VDDCA	Input supply voltage	1.14	1.20	1.30	V	
VDDQ	I/O supply voltage	1.14	1.20	1.30	V	

Input Leakage Current

Symbol	parameter	Min	Max	Units	Notes
I_L	Input Leakage current For CA, CKE, $\overline{CS}$, CK, $\overline{CK}$ Any input 0V =< VIN =< VDDCA (All other pins not under test = 0V)	-2	2	uA	1
I_{VREF}	VREF supply leakage current VREFDQ = VDDQ/2 or VREFCA = VDDCA/2 (All other pins not under test = 0V)	-1	1	uA	2

Notes :

1. The minimum limit requirement is for testing purposes. The leakage current on VREFCA and VREFDQ pins should be minimal.
2. Although DM is for input only, the DM leakage shall match the DQ and DQS/$\overline{DQS}$ output leakage specification.

AC and DC Input Measurement Levels

Single-Ended AC and DC Input Levels for CA and $\overline{CS}$ Signals

Symbol	Parameter	LPDDR2 1600-466		LPDDR2 400-200		Unit	Notes
		Min	Max	Min	Max		
VIHCA(AC)	AC input logic high	VREFCA + 0.22V	-	VREFCA + 0.3V	-	V	1,2
VILCA(AC)	AC input logic Low	-	VREFCA - 0.22V	-	VREFCA + 0.3V	V	1,2
VIHCA(DC)	DC input logic high	VREFCA + 0.13V	VDDCA	VREFCA + 0.2V	VDDCA	V	1
VILCA(DC)	DC input logic Low	VSSCA	VREFCA - 0.13V	VSSCA	VREFCA + 0.2V	V	1
VREFCA(DC)	Reference Voltage for CA and $\overline{CS}$ inputs	0.49 x VDDCA	0.51 x VDDCA	0.49 x VDDCA	0.51 x VDDCA	V	3,4

Notes :
1. For CA and $\overline{CS}$ input only pins. VREF = VREFCA(DC).
2. See Overshoot and Undershoot Specifications section.
3. The ac peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than +/-1% VDDCA (for reference: approx. +/- 12 mV).
4. For reference : approx. VDD/2 ±12 mV.

Single-Ended AC and DC Input Levels for CKE

Symbol	Parameter	Min.	Max.	Units	Notes
VIHCKE	CKE input high level	0.8 x VDDCA	-	V	1
VILCKE	CKE input low level	-	0.2 x VDDCA	V	1

Notes :
1. See Overshoot and Undershoot Specifications section.

Single-Ended AC and DC Input Levels for DQ and DM Signals

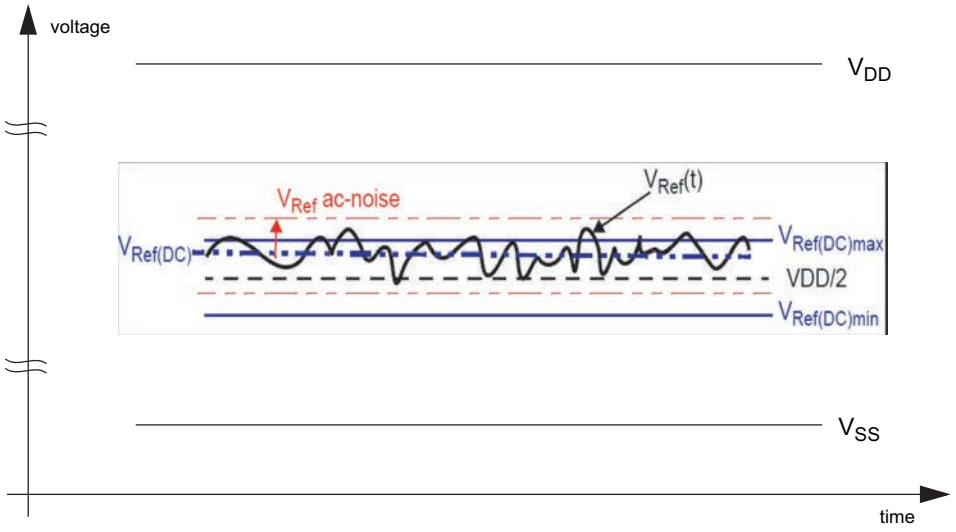
Symbol	Parameter	LPDDR2 1600-466		LPDDR2 400-200		Unit	Notes
		Min	Max	Min	Max		
VIHDQ(AC)	AC input logic high	VREFCA + 0.22V	-	VREFCA + 0.3V	-	V	1,2
VILDQ(AC)	AC input logic Low	-	VREFCA - 0.22V	-	VREFCA + 0.3V	V	1,2
VIHDQ(DC)	DC input logic high	VREFCA + 0.13V	VDDQ	VREFCA + 0.2V	VDDQ	V	1
VILDQ(DC)	DC input logic Low	VSSQ	VREFCA - 0.13V	VSSQ	VREFCA + 0.2V	V	1

VREFDQ(DC)	Reference Voltage for DQ and DM inputs	0.49 x VDDQ	0.51 x VDDQ	0.49 x VDDQ	0.51 x VDDQ	V	3,4

Notes :
1. For DQ input only pins. VREF = VREFDQ(DC).
2. See Overshoot and Undershoot Specifications section.
3. The ac peak noise on VREFDQ may not allow VREFDQ to deviate from VREFDQ(DC) by more than +/-1% VDDDQ (for reference: approx. +/- 12 mV).
4. For reference : approx. VDD/2 ±12 mV.

VREF Tolerances

The DC tolerance limits and AC noise limits for the reference voltages VREFCA and VREFDQ are illustrated bellow. This figure shows a valid reference voltage VREF(t) as a function of time. VDD is used in place of VDDCA for VREFCA, and VDDQ for VREFDQ. VREF(DC) is the linear average of VREF(t) over a very long period of time (e.g., 1 second) and is specified as a fraction of the linear average of VDDQ or VDDCA, also over a very long period of time (e.g., 1 second). This average must meet the MIN/MAX requirements. Additionally, VREF(t) can temporarily deviate from VREF(DC) by no more than +/-1% VDD. VREF(t) cannot track noise on VDDQ or VDDCA if doing so would force VREF outside these specifications.



VREF(DC) tolerance and VREF AC-Noise limits

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC), and VIL(DC) are dependent on VREF. VREF DC variations affect the absolute voltage a signal must reach to achieve a valid HIGH or LOW, as well as the time from which setup and hold times are measured. When VREF is outside the specified levels, devices will function correctly with appropriate timing deratings as long as:

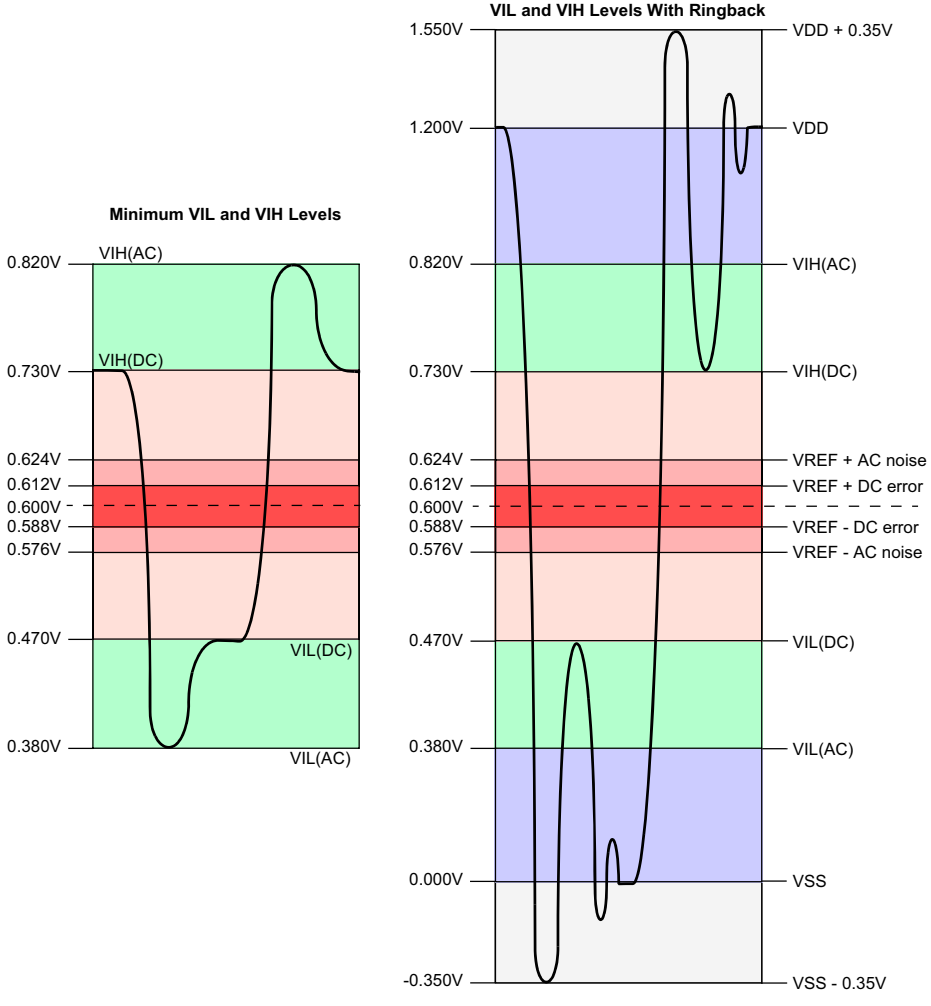
VREF is maintained between 0.44 x VDDQ (or VDDCA) and 0.56 x VDDQ (or VDDCA), and the controller achieves the required single-ended AC and DC input levels from instantaneous VREF.

System timing and voltage budgets must account for VREF deviations outside this range.

This also clarifies that the LPDDR2 setup/hold specification and derating values need to include time and voltage associated with VREF AC-noise. Timing and voltage effects due to AC-noise on VREF up to the specified limit (+/- 1% of VDD) are included in LPDDR2 timings and their associated deratings.

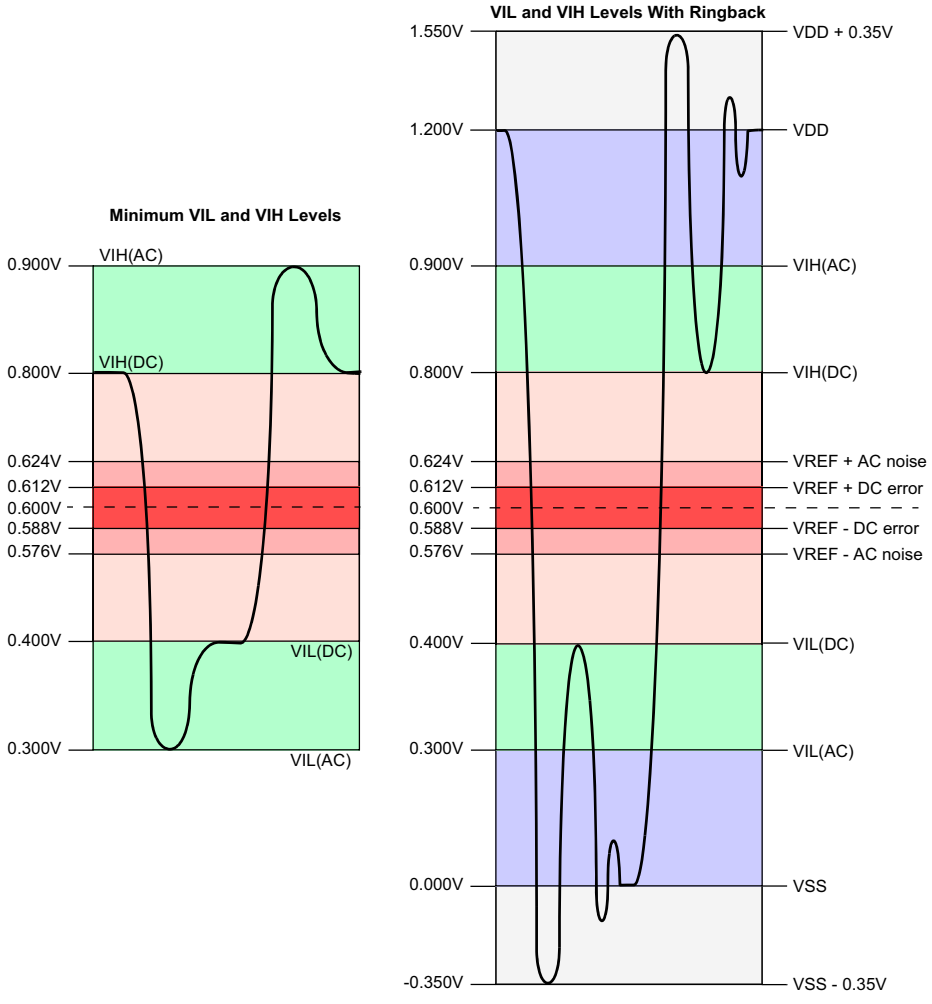
Input Signals

LPDDR2-466 to LPDDR2-1066 Input Signal



Notes:
1. Numbers reflect typical values.
2. For CA[9:0], CK, $\overline{CK}$, $\overline{CS}$, and CKE, VDD stands for VDDCA. For DQ, DM, DQS, and $\overline{DQS}$, VDD stands for VDDQ.
3. For CA[9:0], CK, $\overline{CK}$, $\overline{CS}$, and CKE, VSS stands for VSSCA. For DQ, DM, DQS, and $\overline{DQS}$, VSS stands for VSSQ.

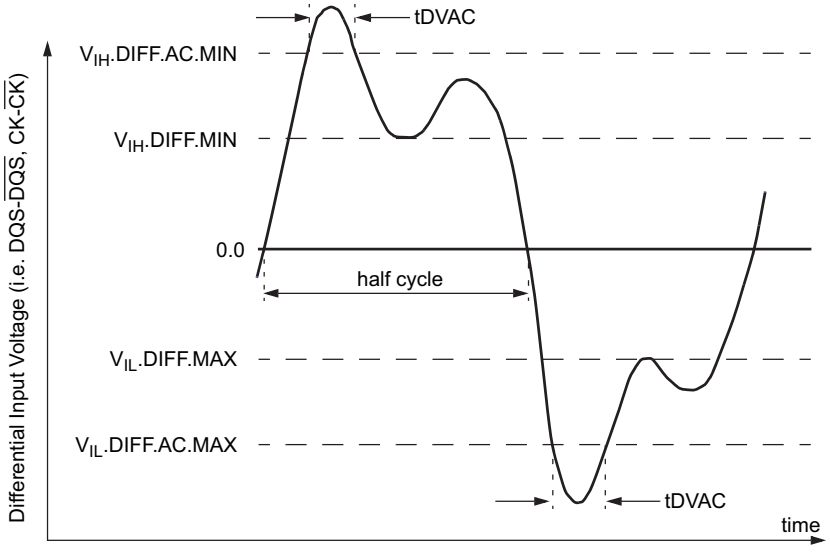
LPDDR2-200 to LPDDR2-400 Input Signal



Notes:
1. Numbers reflect typical values.
2. For CA[9:0], CK, $\overline{CK}$, $\overline{CS}$, and CKE, VDD stands for VDDCA. For DQ, DM, DQS, and $\overline{DQS}$, VDD stands for VDDQ.
3. For CA[9:0], CK, $\overline{CK}$, $\overline{CS}$, and CKE, VSS stands for VSSCA. For DQ, DM, DQS, and $\overline{DQS}$, VSS stands for VSSQ.

AC and DC Logic Input Levels for Differential Signals

Differential signals definition



Definition of differential ac-swing and "time above ac level" tDVAC

Differential swing requirement for clock (CK - $\overline{CK}$) and strobe (DQS - $\overline{DQS}$)

Differential AC and DC Input Levels

Symbol	Parameter	LPDDR2 1600-466		LPDDR2 400-200		Unit	Notes
		Min	Max	Min	Max		
VIHDIFF(AC)	Differential input high	2 x (VIH(ac) - VREF)	Note 3	2 x (VIH(ac) - VREF)	Note 3	V	2
VILDIFF(AC)	Differential input low	Note 3	2 x (VIL(ac) - Vref)	Note 3	2 x (VIL(ac) - Vref)	V	2
VIHDIFF(DC)	Differential input high	2 x (VIH(dc) - VREF)	Note 3	2 x (VIH(dc) - VREF)	Note 3	V	1
VILDIFF(DC)	Differential input low	Note 3	2 x (VIL(dc) - Vref)	Note 3	2 x (VIL(dc) - Vref)	V	1

Notes :

1. Used to define a differential signal slew-rate. For CK - $\overline{CK}$ use VIH/VIL(DC) of address/command and VREFCA; for strobes (DQS, $\overline{DQS}$) use VIH/VIL(DC) of DQs and VREFDQ; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.

2. For CK - $\overline{CK}$ use VIH/VIL(AC) of CA and VREFCA; for DQS - $\overline{DQS}$, use VIH/VIL(AC) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

3. These values are not defined, however the single-ended signals CK, $\overline{CK}$, DQS, and $\overline{DQS}$ must be within the respective limits (VIH(DC)max, VIL(DC)min) for single-ended signals and must comply with the specified limitations for overshoot and undershoot.

Allowed time before ringback (tDVAC) for CK - $\overline{CK}$ and DQS - $\overline{DQS}$

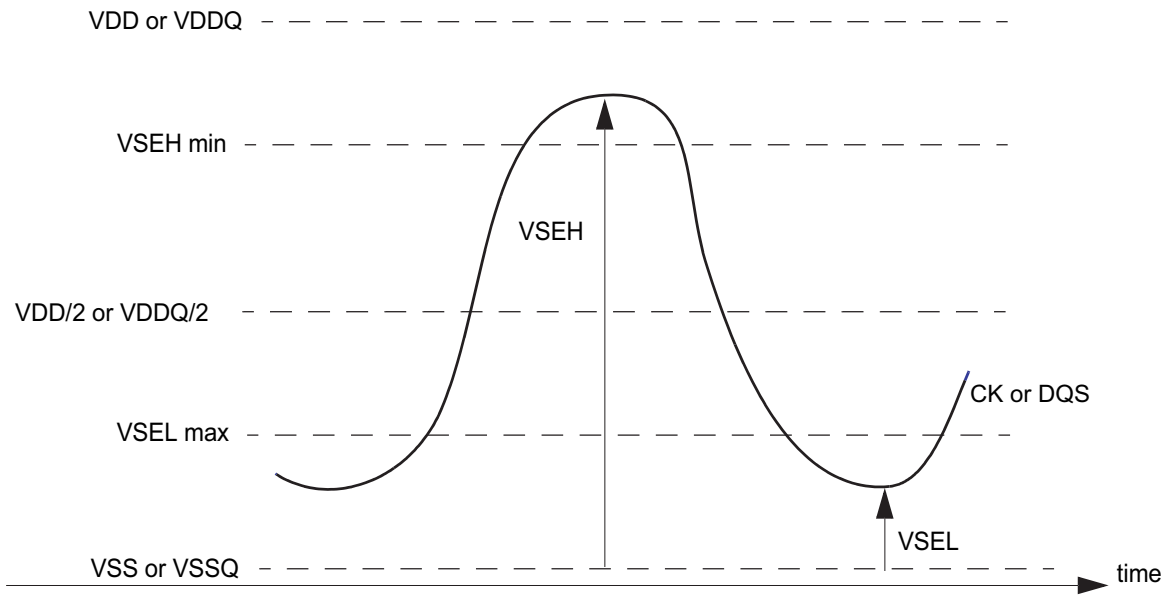
Slew Rate [V/ns]	tDVAC [ps] @ |VIH/Ldiff(AC)| = 440mV	tDVAC [ps] @ |VIH/Ldiff(AC)| = 600mV
	Min.	Min.
> 4.0	175	75
4.0	170	57
3.0	167	50
2.0	163	38
1.8	162	34
1.6	161	29
1.4	159	22
1.2	155	13
1.0	150	0
< 1.0	150	0

Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, $\overline{CK}$, $\overline{DQS}$) has also to comply with certain requirements for single-ended signals.

CK and $\overline{CK}$ shall meet VSEH(AC) min / VSEL(AC) max in every half-cycle.
DQS, $\overline{DQS}$ shall meet VSEH(AC) min / VSEL(AC) max in every half-cycle proceeding and following a valid transition.

Note that the applicable AC-levels for CA and DQ's are different per speed-bin.



Single-ended requirement for differential signals

Note that while CA and DQ signal requirements are with respect to VREF, the single-ended components of differential signals have a requirement with respect to VDDQ/2 for DQS, $\overline{DQS}$ and VDDCA/2 for CK, $\overline{CK}$; this is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSEL(AC) max, VSEH(AC) min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Single-ended levels for CK, DQS, $\overline{CK}$, $\overline{DQS}$

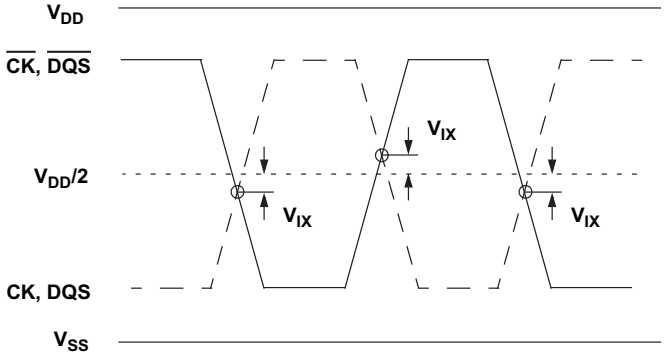
Symbol	Parameter	LPDDR21600-466		LPDDR400-200		Unit	Notes
		Min	Max	Min	Max		
VSEH(AC)	Single-ended high-level for strobes	(VDDQ/2) + 0.22	NOTE 3	(VDDQ/2) + 0.3	NOTE 3	V	2
	Single-ended high-level for CK, $\overline{CK}$	(VDDCA/2) + 0.22	NOTE 3	(VDDCA/2) + 0.3	NOTE 3	V	2
VSEL(AC)	Single-ended low-level for strobes	NOTE 3	(VDDQ/2) - 0.22	NOTE 3	(VDDQ/2) - 0.22	V	1
	Single-ended low-level for CK, $\overline{CK}$	NOTE 3	(VDDCA/2) - 0.22	NOTE 3	(VDDCA/2) - 0.22	V	1

Notes :

1. For CK, $\overline{CK}$ use VIH/VIL(AC) of CA; for strobes (DQS, $\overline{DQS}$) use VIH/VIL(AC) of DQs.
2. VIH(AC)/VIL(AC) for DQs is based on VREFDQ; VSEH(AC)/VSEL(AC) for CA is based on VREFCA; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended components of differential signals CK, $\overline{CK}$, DQS, $\overline{DQS}$ need to be within the respective limits (VIH(DC) max, VIL(DC) min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot specifications".

Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) must meet the requirements in below table. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signal to the mid level between of VDD and VSS.



VIX Definition

Cross point voltage for differential input signals (CK, DQS)

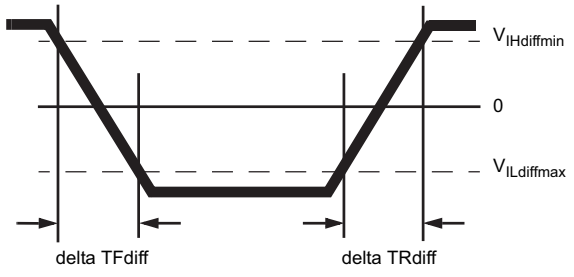
Symbol	Parameter	Min.	Max.	Units	Notes
VIXCA	Differential Input Cross Point Voltage relative to VDDCA/2 for CK, $\overline{CK}$	-120	120	mV	1,2
VIXDQ	Differential Input Cross Point Voltage relative to VDDDQ/2 for DQS, $\overline{DQS}$	-120	120	mV	1,2

Notes :
1. The typical value of VIX(AC) is expected to be about 0.5 x VDD of the transmitting device, and VIX(AC) is expected to track variations in VDD. VIX(AC) indicates the voltage at which differential input sig-nals must cross.
2. For CK and $\overline{CK}$, VREF = VREFCA(DC). For DQS and $\overline{DQS}$, VREF = VREFDQ(DC).

Differential input slew rate definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	VILdiff (max)	VIHdiff (min)	$\frac{\text{VIHdiff (min) - VILdiff (max)}}{\text{Delta TRdiff}}$
Differential input slew rate for falling edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	VIHdiff (min)	VILdiff (max)	$\frac{\text{VIHdiff (min) - VILdiff (max)}}{\text{Delta TFdiff}}$

Notes : The differential signal (i.e. CK - $\overline{CK}$ and DQS - $\overline{DQS}$) must be linear between these thresholds.



Differential Input Slew Rate definition for DQS, $\overline{DQS}$, and CK, $\overline{CK}$

AC and DC Output Measurement Levels

Single-ended AC & DC Output Levels

Symbol	Parameter	LPDDR2-1600 to LPDDR2-200	Units	Notes
VOH(DC)	DC output high measurement level (for IV curve linearity)	0.9 x VDDQ	V	1
VOL(DC)	DC output mid measurement level (for IV curve linearity)	0.1 x VDDQ	V	2
VOH(AC)	AC output high measurement level (for output SR)	VREFDQ+0.12	V	
VOL(AC)	AC output low measurement level (for output SR)	VREFDQ-0.12	V	
I_{OZ}	Output Leakage current (DQ, DM, DQS, DQS) (DQ, DQS, DQS are disabled; 0V =< VOUT =< VDDQ)	-5 (min)	uA	
		5 (max)	uA	
MM_{PUPD}	Delta RON between pull-up and pull-down for DQ/DM	-15 (min)	%	
		15 (max)	%	

Notes :
1. IOH = -0.1mA.
2. IOL = -0.1mA.

Differential AC & DC Output Levels

Symbol	Parameter	LPDDR2-1600 to LPDDR2-200	Units	Notes
VOHdiff(AC)	AC differential output high measurement level (for output SR)	+0.2 x VDDQ	V	
VOLdiff(AC)	AC differential output low measurement level (for output SR)	-0.2 x VDDQ	V	

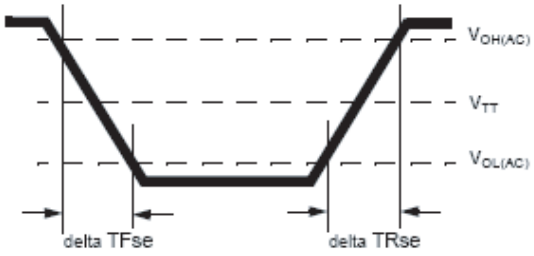
Notes :
1. IOH = -0.1mA.
2. IOL = -0.1mA.

Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals.

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	VOL(AC)	VOH(AC)	VOH(AC)-VOL(AC) / Delta TRse
Single ended output slew rate for falling edge	VOH(AC)	VOL(AC)	VOH(AC)-VOL(AC) / Delta TRse

Notes : Output slew rate is verified by design and characterization, and may not be subject to production test.



Single-ended Output Slew Rate definition

Parameter	Symbol	LPDDR2-1600 to LPDDR2-200		Units
		Min	Max	
Single ended output slew rate (RON = 40Ω +/- 30%)	SRQse	1.5	3.5	V/ns
Single ended output slew rate (RON = 60Ω +/- 30%)	SRQse	1	2.5	V/ns
Output slew-rate matching Ratio (Pull-up to Pull-down)		0.7	1.4	

Description : SR : Slew Rate
Q : Query Output (like in DQ, which stands for Data-in, Query-Output)
se : Single-ended Signals

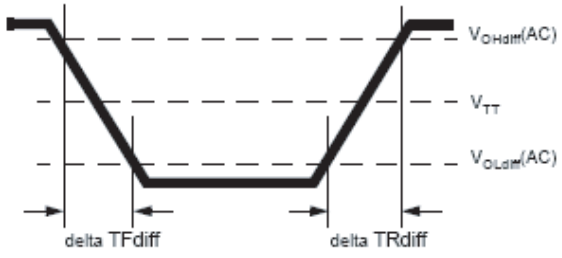
Notes :
1. Measured with output reference load.
2. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
3. The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
4. Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic-high and 1/2 of DQ signals per data byte driving logic-low.

Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOH-diff(AC) for differential signals.

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	VOLdiff(AC)	VOHdiff(AC)	VOHdiff(AC)-VOLdiff(AC) / Delta TRdiff
Differential output slew rate for falling edge	VOHdiff(AC)	VOLdiff(AC)	VOHdiff(AC)-VOLdiff(AC)) / Delta TFdiff

Notes : Output slew rate is verified by design and characterization, and may not be subject to production test.



Differential Output Slew Rate definition

Parameter	Symbol	LPDDR2-1600 to LPDDR2-200		Units
		Min	Max	
Single ended output slew rate (RON = 40Ω +/- 30%)	SRQdiff	3.0	7.0	V/ns
Single ended output slew rate (RON = 60Ω +/- 30%)	SRQdiff	2.0	5.0	V/ns

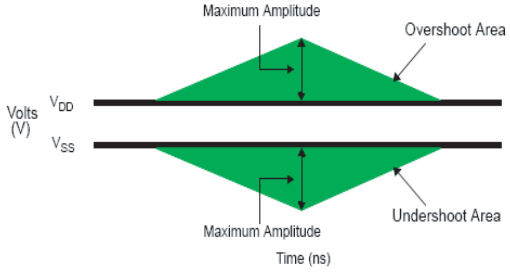
Description : SR : Slew Rate
Q : Query Output (like in DQ, which stands for Data-in, Query-Output)
diff : Differential Signals

Notes :
1. Measured with output reference load.
2. he output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
3. Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic-high and 1/2 of DQ signals per data byte driving logic-low.

Overshoot and Undershoot Specification

AC Overshoot/Undershoot specifications

Parameter	Specification										Unit
	1066	933	800	667	533	466	400	333	266	200	
Maximum peak amplitude allowed for overshoot area	0.35										V
Maximum peak amplitude allowed for undershoot area	0.35										V
Maximum overshoot area above VDD	0.15	0.17	0.20	0.24	0.30	0.35	0.40	0.48	0.60	0.80	V-ns
Maximum undershoot area below VSS	0.15	0.17	0.20	0.24	0.30	0.35	0.40	0.48	0.60	0.80	V-ns



Address and Control Overshoot and Undershoot Definition

Notes:
1. For CA0-9, CK, $\overline{CK}$, $\overline{CS}$, and CKE, VDD stands for VDDCA. For DQ, DM, DQS, and $\overline{DQS}$, VDD stands for VDDQ.
2. For CA0-9, CK, $\overline{CK}$, $\overline{CS}$, and CKE, VSS stands for VSSCA. For DQ, DM, DQS, and $\overline{DQS}$, VSS stands for VSSQ.
3. Maximum peak amplitude values are referenced from actual VDD and VSS values.
4. Maximum area values are referenced from maximum operating VDD and VSS values.

Input/Output Capacitance

Parameter	Symbol	LPDDR2 1066-466		LPDDR2 400-200		Units	NOTE
		Min	Max	Min	Max		
Input capacitance (CK and $\overline{CK}$)	CCK	1	2	1	2	pF	1,2
Input capacitance delta (CK and $\overline{CK}$)	CDCK	0	0.2	0	0.25	pF	1,2,3
Input capacitance (All other input-only pins)	CI	1	2	1	2	pF	1,2,4
Input capacitance delta (All other input-only pins)	CDI	-0.4	0.4	-0.5	0.5	pF	1,2,5
Input/output capacitance (DQ, DQS, $\overline{DQS}$, DM)	CIO	1.25	2.5	1.25	2.5	pF	1,2,6,7
Input/output capacitance delta (DQS and $\overline{DQS}$)	CDDQS	0	0.25	0	0.3	pF	1,2,7,8
Input/output capacitance delta (DQ, DM)	CDIO	-0.5	0.5	-0.6	0.6	pF	1,2,7,9
Input/output capacitance: ZQ	CZQ	0	2.5	0	2.5	pF	1,2

Notes :
1. This parameter applies to die device only (does not include package capacitance).
2. 2This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer) with VDD1, VDD2, VDDQ, VSS, $\overline{VSS}$CA, VSSQ applied and all other pins floating.
3. Absolute value of CCK-C$\overline{CK}$
4. CI applies to $\overline{CS}$, CKE, CA0-C$\overline{A9}$.
5. CDI = CI - 0.5 * (CCK + C$\overline{CK}$)
6. DM loading matches DQ and DQS.
7. MR3 I/O configuration DS OP3-$\overline{OP0}$ = 0001B (34.3 Ohm typical).
8. Absolute value of CDQS and C$\overline{DQS}$.
9. CDIO = CIO - 0.5 * (CDQS + C$\overline{DQS}$) in byte-lane.
10. Maximum external load capacitance on ZQ pin, including packaging, board, pin, resistor, and other LPDDR2 devices: 5 pF.

IDD Specification

(VDD2, VDDQ,VDDCA = 1.14~1.30V, VDD1 = 1.70~1.95V)

Conditions	Symbol	Power Supply	1066	Unit
Operating One Bank Active-Precharge Current: tCK = tCK(avg)min; tRC = tRCmin; CKE is HIGH; $\overline{CS}$ is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD0_1$ $IDD0_2$ $IDD0_{IN}$	VDD1 VDD2 VDDCA,VDDQ	15 70 10	mA
Idle power-down standby current: tCK = tCK(avg)min; CKE is LOW; $\overline{CS}$ is HIGH; All banks/RBs idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD2P_1$ $IDD2P_2$ $IDD2P_{IN}$	VDD1 VDD2 VDDCA,VDDQ	600 800 120	uA
Idle power-down standby current with clock stop: CK =LOW, $\overline{CK}$ =HIGH; CKE is LOW; $\overline{CS}$ is HIGH; All banks/RBs idle; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD2PS_1$ $IDD2PS_2$ $IDD2PS_{IN}$	VDD1 VDD2 VDDCA,VDDQ	600 800 120	uA
Idle non power-down standby current: tCK = tCK(avg)min; CKE is HIGH; $\overline{CS}$ is HIGH; All banks/RBs idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD2N_1$ $IDD2N_2$ $IDD2N_{IN}$	VDD1 VDD2 VDDCA,VDDQ	2 20 10	mA
Idle non power-down standby current with clock stop: CK_t =LOW, CK_c =HIGH; CKE is HIGH; $\overline{CS}$ is HIGH; All banks/RBs idle; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD2NS_1$ $IDD2NS_2$ $IDD2NS_{IN}$	VDD1 VDD2 VDDCA,VDDQ	1.7 10 6	mA
Active power-down standby current: tCK = tCK(avg)min; CKE is LOW; $\overline{CS}$ is HIGH; One bank/RB active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD3P_1$ $IDD3P_2$ $IDD3P_{IN}$	VDD1 VDD2 VDDCA,VDDQ	1000 7.5 150	uA mA uA

Conditions	Symbol	Power Supply	1066	Unit
Active power-down standby current with clock stop: CK=LOW, $\overline{CK}$=HIGH; CKE is LOW; $\overline{CS}$ is HIGH; One bank/RB active; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD3PS_1$ $IDD3PS_2$ $IDD3PS_{IN}$	VDD1 VDD2 VDDCA,VDDQ	1200 7.5 150	uA mA uA
Active non power-down standby current: tCK = tCK(avg)min; CKE is HIGH; $\overline{CS}$ is HIGH; One bank/RB active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD3N_1$ $IDD3N_2$ $IDD3N_{IN}$	VDD1 VDD2 VDDCA,VDDQ	2 25 10	mA
Active non power-down standby current with clock stop: CK=LOW, $\overline{CK}$=HIGH; CKE is HIGH; $\overline{CS}$ is HIGH; One bank/RB active; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD3NS_1$ $IDD3NS_2$ $IDD3NS_{IN}$	VDD1 VDD2 VDDCA,VDDQ	2 20 6	mA
Operating burst read current: tCK = tCK(avg)min; $\overline{CS}$ is HIGH between valid commands; One bank/RB active; BL = 4; RL = RLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer	$IDD4R_1$ $IDD4R_2$ $IDD4R_{IN}$ $IDD4R_Q$	VDD1 VDD2 VDDCA VDDQ	3 250 10	mA
Operating burst write current: tCK = tCK(avg)min; $\overline{CS}$ is HIGH between valid commands; One bank/RB active; BL = 4; WL = WLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer	$IDD4W_1$ $IDD4W_2$ $IDD4W_{IN}$	VDD1 VDD2 VDDCA,VDDQ	3 250 35	mA

All Bank Refresh Burst current:
tCK = tCK(avg)min;
CKE is HIGH between valid commands;
tRC = tRFCabmin;
Burst refresh;
CA bus inputs are SWITCHING;
Data bus inputs are STABLE
	$IDD5_1$
	$IDD5_2$
	$IDD5_{IN}$
		VDD1
		VDD2
		VDDCA,VDDQ
			20
			150
			10
				mA

All Bank Refresh Average current:
tCK = tCK(avg)min;
CKE is HIGH between valid commands;
tRC = tREFI;
CA bus inputs are SWITCHING;
Data bus inputs are STABLE
	$IDD5AB_1$
	$IDD5AB_2$
	$IDD5AB_{IN}$
		VDD1
		VDD2
		VDDCA,VDDQ
			5
			25
			10
				mA

Conditions	Symbol	Power Supply	1066	Unit

Per Bank Refresh Average current:
tCK = tCK(avg)min;
CKE is HIGH between valid commands;
tRC = tREFI/8;
CA bus inputs are SWITCHING;
Data bus inputs are STABLE
	$IDD5PB_1$
	$IDD5PB_2$
	$IDD5PB_{IN}$
		VDD1
		VDD2
		VDDCA,VDDQ
			5
			25
			10
				mA

Self refresh current (Standard Temperature Range): CK=LOW, $\overline{CK}$=HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE; Maximum 1x Self-Refresh Rate	$IDD6_1$ $IDD6_2$ $IDD6_{IN}$	VDD1 VDD2 VDDCA,VDDQ	1000 4000 120	uA
Self refresh current (+85'C to +105'C): CK=LOW, $\overline{CK}$=HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE;	$IDD6ET_1$ $IDD6ET_2$ $IDD6ET_{IN}$	VDD1 VDD2 VDDCA,VDDQ	TBD TBD TBD	mA

Notes :
1. Published IDD values are the maximum of the distribution of the arithmetic mean.
2. IDD current specifications are tested after the device is properly initialized.
3. The 1x self refresh rate is the rate at which the device is refreshed internally during self refresh, before going into the extended temperature range.
4. Measured currents are the summation of VDDQ and VDDCA.
5. Guaranteed by design with output load of 5PF and RON = 40Ohm.
6. Per Bank Refresh only applicable for LPDDR2-S4 devices of 1Gb or higher densities
7. This is the general definition that applies to full-array SELF REFRESH).
8. IDD6ET is typical values

IDD6 Partial Array Self-Refresh Current

PASR	Supply	1066	Unit
Full Array	VDD1 VDD2 VDDCA,VDDQ	1000 4000 120	uA
1/2 Array	VDD1 VDD2 VDDCA,VDDQ	950 2300 120	uA
1/4 Array	VDD1 VDD2 VDDCA,VDDQ	900 1500 120	uA
1/8 Array	VDD1 VDD2 VDDCA,VDDQ	850 1060 120	uA

REFRESH Requirements by Device Density

LPDDR2-S4 Refresh Requirement Parameters (per density)

Symbol	Parameter	4Gb(Single Die)	8Gb(Dual Dies)	Unit
	Number of banks	8		
tREFW	Refresh window: TCASE =< 85'C	32		ms
tREFW	Refresh window: 85'C < TCASE =< 105'C	8		ms
R	Required number of REFRESH commands (MIN)	8192	8192	
tREFI	Average time between REFRESH commands (for reference only) TCASE <= 85'C	3.9	3.9	us
tREFIpb		0.4875	0.4875	us
tRFCab	Refresh cycle time	130	130	ns
tRFCpb	Per-bank REFRESH cycle time	60	60	ns
tREFBW	Burst REFRESH window = 4 x 8 x tRFCab	4.16	4.16	us

AC Characteristics

(VDD2, VDDQ,VDDCA = 1.14~1.30V, VDD1 = 1.70~1.95V)

Parameter	Symbol	min/max	min tCK	Speed Grade		Unit
				1066	800	
Clock Timing						
Max. Frequency		~		533	400	MHz
Average Clock Period	tCK(avg)	min		1.875	2.5	ns
		max		100		
Average HIGH pulse width	tCH(avg)	min		0.45		tCK(avg)
		max		0.55		
Average LOW pulse width	tCL(avg)	min		0.45		tCK(avg)
		max		0.55		
Absolute Clock Period	tCK(abs)	min		tCK(avg)min + tJIT(per),min		ps
Absolute clock HIGH pulse width (with allowed jitter)	tCH(abs), allowed	min		0.43		tCK(avg)
		max		0.57		
Absolute clock LOW pulse width (with allowed jitter)	tCL(abs), allowed	min		0.43		tCK(avg)
		max		0.57		
Clock Period Jitter (with allowed jitter)	tJIT(per), allowed	min		-90	-100	ps
		max		90	100	
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	tJIT(cc), allowed	max		180	200	ps
Duty cycle Jitter (with allowed jitter)	tJIT(duty), allowed	min		min((tCH(abs),min - tCH(avg),min), (tCL(abs),min - tCL(avg),min)) * tCK(avg)		ps
		max		max((tCH(abs),max - tCH(avg),max), (tCL(abs),max - tCL(avg),max)) * tCK(avg)		
Cumulative error across 2 cycles	tERR(2per), allowed	min		-132	-147	ps
		max		132	147	
Cumulative error across 3 cycles	tERR(3per), allowed	min		-157	-175	ps
		max		157	175	
Cumulative error across 4 cycles	tERR(4per), allowed	min		-175	-194	ps
		max		175	194	
Cumulative error across 5 cycles	tERR(5per), allowed	min		-188	-209	ps
		max		188	209	
Cumulative error across 6 cycles	tERR(6per), allowed	min		-200	-222	ps
		max		200	222	
Cumulative error across 7 cycles	tERR(7per), allowed	min		-209	-232	ps
		max		209	232	

Parameter	Symbol	min/max	min tCK	Speed Grade		Unit
				1066	800	
Cumulative error across 8 cycles	tERR(8per), allowed	min		-217	-241	ps
		max		217	241	
Cumulative error across 9 cycles	tERR(9per), allowed	min		-224	-249	ps
		max		224	249	
Cumulative error across 10 cycles	tERR(10per), allowed	min		-231	-257	ps
		max		231	257	
Cumulative error across 11 cycles	tERR(11per), allowed	min		-237	-263	ps
		max		237	263	
Cumulative error across 12 cycles	tERR(12per), allowed	min		-242	-269	ps
		max		242	269	
Cumulative error across n = 13, 14 . . . 49, 50cycles	tERR(nper), allowed	min		tERR(nper),allowed,min = (1 + 0.68ln(n)) * tJIT(per),allowed,min		ps
		max		tERR(nper),allowed,max = (1 + 0.68ln(n)) * tJIT(per),allowed,max		
ZQ Calibration Parameters						
Initialization Calibration Time	tZQINIT	min		1		us
Long Calibration Time	tZQCL	min	6	360		ns
Short Calibration Time	tZQCS	min	6	90		ns
Calibration Reset Time	tZQRESET	min	3	50		ns
Read Parameters						
DQS output access time from CK/$\overline{CK}$	tDQSCK	min		2500		ps
		max		5500		
DQSCK Delta Short	tDQSCKDS	max		330	450	ps
DQSCK Delta Medium	tDQSCKDM	max		680	900	ps
DQSCK Delta Long	tDQSCKDL	max		920	1200	ps
DQS - DQ skew	tDQSQ	max		200	240	ps
Data hold skew factor	tQHS	max		230	280	ps
DQS Output High Pulse Width	tQSH	min		tCH(abs) - 0.05		tCK(avg)
DQS Output Low Pulse Width	tQSL	min		tCL(abs) - 0.05		tCK(avg)
Data Half Period	tQHP	min		min(tQSH, tQSL)		tCK(avg)
DQ / DQS output hold time from DQS	tQH	min		tQHP - tQHS		ps
Read preamble	tRPRE	min		0.9		tCK(avg)
Read postamble	tRPST	min		tCL(abs) - 0.05		tCK(avg)
DQS low-Z from clock	tLZ(DQS)	min		tDQSCK(MIN) - 300		ps
DQ low-Z from clock	tLZ(DQ)	min		tDQSCK(MIN) - (1.4 * tQHS(MAX))		ps

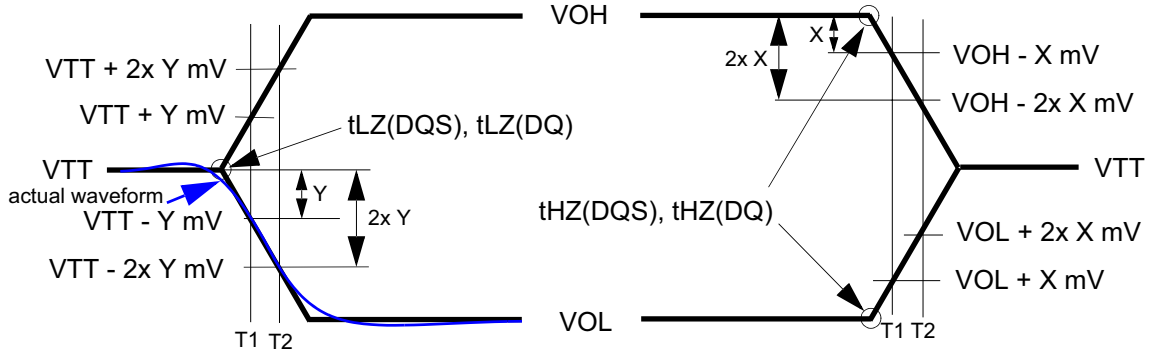
Parameter	Symbol	min/max	min tCK	Speed Grade		Unit
				1066	800	
DQS high-Z from clock	tHZ(DQS)	max		tDQSCK(MAX) - 100		ps
DQ high-Z from clock	tHZ(DQ)	max		tDQSCK(MAX) + (1.4 * tDQSQ(MAX))		ps
Write Parameters						
DQ and DM input hold time (Vref based)	tDH	min		210	270	ps
DQ and DM input setup time (Vref based)	tDS	min		210	270	ps
DQ and DM input pulse width	tDIPW	min		0.35		tCK(avg)
Write command to 1st DQS latching transition	tDQSS	min		0.75		tCK(avg)
		max		1.25		
DQS input high-level width	tDQSH	min		0.4		tCK(avg)
DQS input low-level width	tDQSL	min		0.4		tCK(avg)
DQS falling edge to CK setup time	tDSS	min		0.2		tCK(avg)
DQS falling edge hold time from CK	tDSH	min		0.2		tCK(avg)
Write postamble	tWPST	min		0.4		tCK(avg)
Write preamble	tWPRE	min		0.35		tCK(avg)
CKE Input Parameters						
CKE min. pulse width (high and low pulse width)	tCKE	min	3	3		tCK(avg)
CKE input setup time	tISCKE	min		0.25		tCK(avg)
CKE input hold time	tIHCKE	min		0.25		tCK(avg)
Command Address Input Parameters						
Address and control input setup time (Vref based)	tIS	min		220	290	ps
Address and control input hold time (Vref based)	tIH	min		220	290	ps
Address and control input pulse width	tIPW	min		0.4		tCK(avg)
Mode Register Parameters						
MODE REGISTER Write command period	tMRW	min	5	5		tCK(avg)
Mode Register Read command period	tMRR	min	2	2		tCK(avg)
LPDDR2 SDRAM Core Parameters						
Read Latency	RL	min	3	8	6	tCK(avg)
Write Latency	WL	min	1	4	3	tCK(avg)
ACTIVE to ACTIVE command period	tRC	min		tRAS + tRPab (with all-bank Precharge) tRAS + tRPpb (with per-bank Precharge)		ns
CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	tCKESR	min	3	15		ns
Self refresh exit to next valid command delay	tXSR	min	2	tRFCab + 10		ns

Parameter	Symbol	min/max	min tCK	Speed Grade		Unit
				1066	800	
Exit power down to next valid command delay	tXP	min	2	7.5		ns
CAS to CAS delay	tCCD	min	2	2		tCK(avg)
Internal Read to Precharge command delay	tRTP	min	2	7.5		ns
RAS to CAS Delay	tRCD	min	3	18		ns
Row Precharge Time(single bank)	tRPpb	min	3	18		ns
Row Precharge Time(all banks)	tRPab 8-bank	min	3	21		ns
Row Active Time	tRAS	min	3	42		ns
		max	-	70		us
Write Recovery Time	tWR	min	3	15		ns
Internal Write to Read Command Delay	tWTR	min	2	7.5		ns
Active bank A to Active bank B	tRRD	min	2	10		ns
Four Bank Activate Window	tFAW	min	8	50		ns
Minimum Deep Power Down Time	tDPD	min		500		us
LPDDR2 Temperature De-Rating						
tDQSCK De-Rating	tDQSCK (Derated)	max		5620	6000	ps
Core Timings Temperature De-Rating	tRCD (Derated)	min		tRCD + 1.875		ns
	tRC (Derated)	min		tRC + 1.875		ns
	tRAS (Derated)	min		tRAS + 1.875		ns
	tRP (Derated)	min		tRP + 1.875		ns
	tRRD (Derated)	min		tRRD + 1.875		ns
Boot Parameters (10 MHz - 55 MHz)						
Clock Cycle Time	tCKb	min		18		ns
		max		100		
CKE Input Setup Time	tISCKEb	min		2.5		ns
CKE Input Hold Time	tIHCKEb	min		2.5		ns
Address & Control Input Setup Time	tISb	min		1150		ps
Address & Control Input Hold Time	tIHb	min		1150		ps
DQS Output Data Access Time from CK/$\overline{CK}$	tDQSCKb	min		2		ns
		max		10		
DQS - DQ skew	tDQSQb	max		1.2		ns

Parameter	Symbol	min/max	min tCK	Speed Grade		Unit
				1066	800	
Data Hold Skew Factor	tQHSb	max		1.2		ns

Notes for AC Electrical Characteristics

1. Frequency values are for reference only. Clock cycle time (tCK) is used to determine device capabilities.
2. All AC timings assume an input slew rate of 1 V/ns.
3. READ, WRITE, and input setup and hold values are referenced to VREF.
4. tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a contiguous sequence of bursts in a 160ns rolling window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is < 10 'C/s. Values do not include clock jitter. .
5. tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 1.6us rolling window. tDQSCKdm is not tested and is guaranteed by design. Temperature drift in the system is < 10 'C/s. Values do not include clock jitter.
6. tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 32ms rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is < 10 'C/s. Values do not include clock jitter.
7. For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the transition threshold (VTT). tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Figure shows a method to calculate the point when device is no longer driving tHZ (DQS) and tHZ (DQ), or begins driving tLZ (DQS), tLZ (DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.



begin driving point = 2 x T1 - T2 stop driving point = 2 x T1 - T2

HSUL_12 Driver Output Reference Load for Timing and Skew Rate

The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS-$\overline{DQS}$.

8. Measured from the point when DQS, $\overline{DQS}$ begins driving the signal to the point when DQS, $\overline{DQS}$ begins driving the first rising strobe edge.
9. Measured from the last falling strobe edge of DQS, $\overline{DQS}$ to the point when DQS, $\overline{DQS}$ finishes driving the signal.
10. CKE input setup time is measured from CKE reaching a HIGH/LOW voltage level to CK, $\overline{CK}$ crossing.
11. CKE input hold time is measured from CK, $\overline{CK}$ crossing to CKE reaching a HIGH/LOW voltage level.
12. Input set-up/hold time for signal (CA[9:0], $\overline{CS}$).
13. To ensure device operation before the device is configured, a number of AC boot-timing parameters are defined in this table. Boot parameter symbols have the letter b appended (for example, tCK during boot is tCKb).

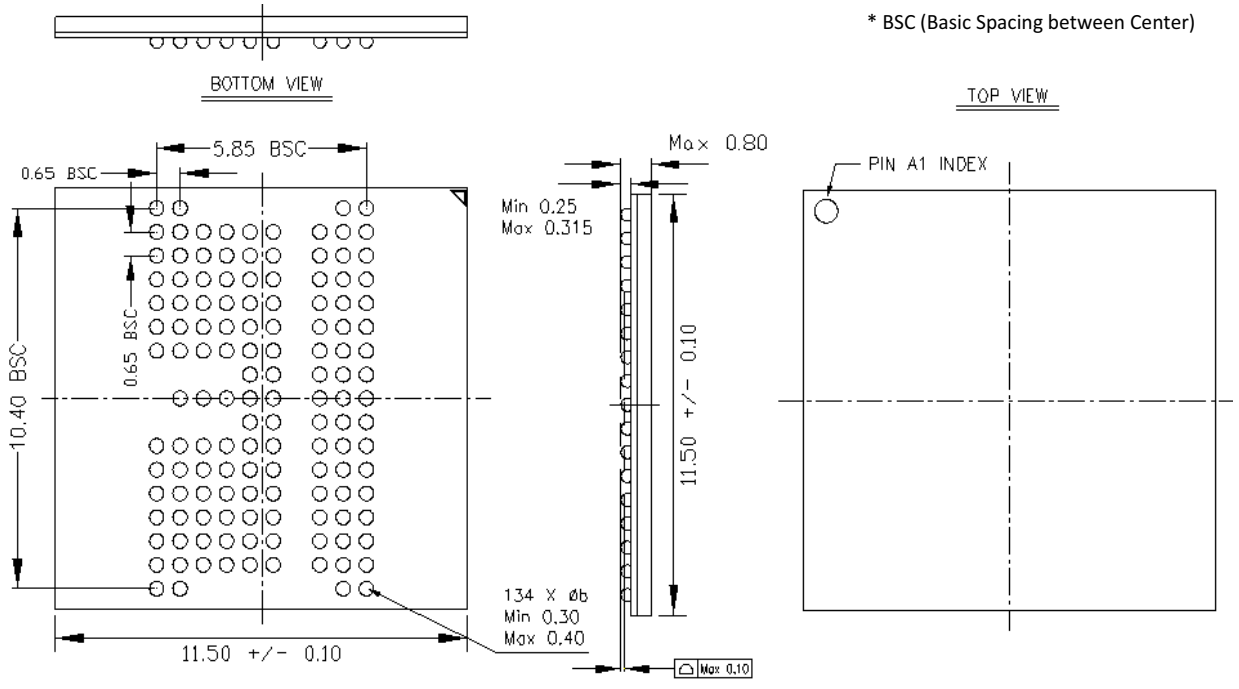
14. The LPDDR device will set some mode register default values upon receiving a RESET command as specified in Mode Register Definition.
15. The output skew parameters are measured with default output impedance settings using the reference load.
16. The minimum tCK column applies only when tCK is greater than 6ns.

Package Diagram

134-Ball FBGA - 11.5mm x 11.5mm 0.65mm pitch

Unit: mm

* BSC (Basic Spacing between Center)



PART NUMBERING SYSTEM

AS4C	128M32MD2	18	B	C / I	N
DRAM	128M32=128Mx32 MD2=LPDDR2	18=533MHz	B = FBGA	C=Commercial (-25° C~+85° C) I = Industrial (-40° C~+85° C)	Indicates Pb and Halogen Free

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