Revision History
AS7C34098B

Revision	Details	Date
Rev 1.0	Initial Issue	Aug. 2016
Rev 2.0	Add TFBGA package	June. 2017

AS7C34098B

256K X 16 BIT HIGH SPEED CMOS SRAM

FEATURES

- Fast access time : 10ns ■
- **Low power consumption:**
  Operating current:
  40mA (TYP.)
  Standby current:
  2mA (TYP.)
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)
  UB# (DQ8 ~ DQ15)
- Data retention voltage : 1.5V (MIN.)
- **ROHS compliant**
- Package : 44-pin 400mil TSOP II
  48-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

The AS7C34098B is a 4,194,304-bit high speed CMOS static random access memory organized as 262,144 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS7C34098B operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

Table 1. Ordering Information

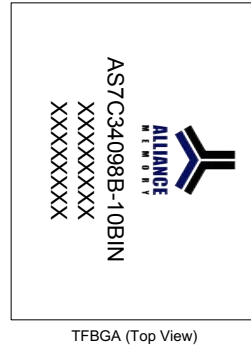| Part Number	Speed	Temperature	Vcc Range	Package
AS7C34098B-10TIN*	10ns	Industrial -40°C to +85°C	2.7 ~ 3.6V	44pin TSOPII
AS7C34098B-10BIN*	10ns	Industrial -40°C to +85°C	2.7 ~ 3.6V	48-ball TFBGA

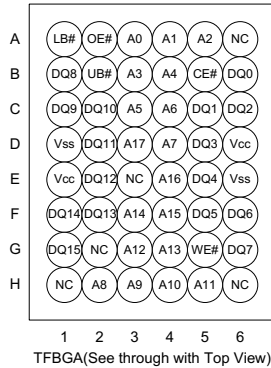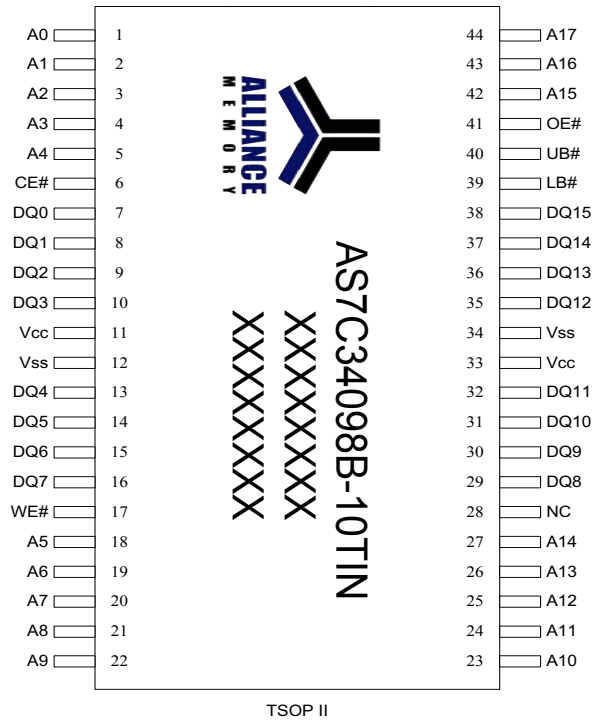* : indicates Tray and add TR =Tape Reel packing type

FUNCTIONAL BLOCK DIAGRAM
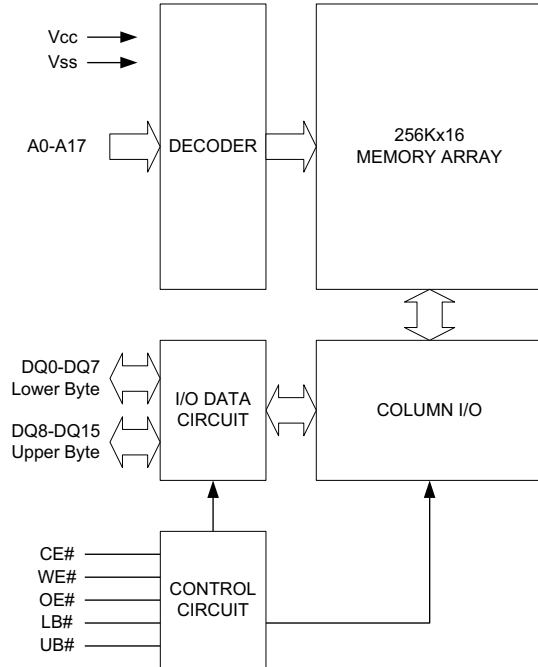
SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
DQ0 - DQ15	Data Inputs/Outputs
CE#	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

PIN DESCRIPTION

PIN CONFIGURATION

A0	1		44	A17
A1	2		43	A16
A2	3		42	A15
A3	4		41	OE#
A4	5		40	UB#
CE#	6		39	LB#
DQ0	7		38	DQ15
DQ1	8		37	DQ14
DQ2	9	AS7C34098B-10TIN	36	DQ13
DQ3	10		35	DQ12
Vcc	11		34	Vss
Vss	12		33	Vcc
DQ4	13		32	DQ11
DQ5	14		31	DQ10
DQ6	15		30	DQ9
DQ7	16		29	DQ8
WE#	17		28	NC
A5	18		27	A14
A6	19		26	A13
A7	20		25	A12
A8	21		24	A11
A9	22		23	A10

TSOP II

	1	2	3	4	5	6
A	LB#	OE#	A0	A1	A2	NC
B	DQ8	UB#	A3	A4	CE#	DQ0
C	DQ9	DQ10	A5	A6	DQ1	DQ2
D	Vss	DQ11	A17	A7	DQ3	Vcc
E	Vcc	DQ12	NC	A16	DQ4	Vss
F	DQ14	DQ13	A14	A15	DQ5	DQ6
G	DQ15	NC	A12	A13	WE#	DQ7
H	NC	A8	A9	A10	A11	NC

TFBGA(See through with Top View)

AS7C34098B-10BIN

TFBGA (Top View)

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{CC} relative to V_{SS}	V_{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to V_{SS}	V_{T2}	-0.5 to V_{CC}+0.5	V
Operating Temperature	T_A	-40 to 85	℃
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
						DQ0 - DQ7	DQ8 - DQ15	
Standby	H	X	X	X	X	High-Z	High-Z	I_{SB}, I_{SB1}
Output Disable	L	H	H	X	X	High-Z	High-Z	I_{CC}, I_{CC1}
	L	X	X	H	H	High-Z	High-Z	
Read	L	L	H	L	H	D_{OUT}	High-Z	I_{CC}, I_{CC1}
	L	L	H	H	L	High-Z	D_{OUT}	
	L	L	H	L	L	D_{OUT}	D_{OUT}	
Write	L	X	L	L	H	D_{IN}	High-Z	I_{CC}, I_{CC1}
	L	X	L	H	L	High-Z	D_{IN}	
	L	X	L	L	L	D_{IN}	D_{IN}	

Note: H = V_{IH}, L = V_{IL}, X = Don't care

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. [4]	MAX.	UNIT
Supply Voltage	V_{CC}		2.7	3.3	3.6	V
Input High Voltage	V_{IH} [1]		2.2	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL} [2]		- 0.3	-	0.8	V
Input Leakage Current	I_{LI}	$V_{CC} \geqq V_{IN} \geqq V_{SS}$	- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{CC} \geqq V_{OUT} \geqq V_{SS}$, Output Disabled	- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = -4mA	2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA	-	-	0.4	V
Average Operating Power supply Current	I_{CC}	Cycle time = MIN. CE# = V_{IL}, $I_{I/O}$ = 0mA, Others at V_{IL} or V_{IH}	-	50	70	mA
Average Operating Power supply Current	I_{CC1}	CE# $\leqq$ 0.2, Others at 0.2V or V_{CC}-0.2V $I_{I/O}$ = 0mA; f=MAX.	-	40	55	mA
Standby Power Supply Current	I_{SB}	CE# = V_{IH}, Others at V_{IL} or V_{IH}	-	-	30	mA
Standby Power Supply Current	I_{SB1}	CE# $\geqq V_{CC}$ - 0.2V, Others at 0.2V or V_{CC} - 0.2V	-	2	10	mA

Notes:
1. V_{IH}(max) = V_{CC} + 2.0V for pulse width less than 6ns.
2. V_{IL}(min) = V_{SS} - 2.0V for pulse width less than 6ns.
3. Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
4. Typical values are included for reference only and are not guaranteed or tested.
   Typical valued are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25℃

CAPACITANCE (T_A = 25℃, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Speed	10ns
Input Pulse Levels	0.2V to V_{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -4mA/8mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	AS7C34098B-10		UNIT
		MIN.	MAX.	
Read Cycle Time	t_{RC}	10	-	ns
Address Access Time	t_{AA}	-	10	ns
Chip Enable Access Time	t_{ACE}	-	10	ns
Output Enable Access Time	t_{OE}	-	4.5	ns
Chip Enable to Output in Low-Z	t_{CLZ}*	2	-	ns
Output Enable to Output in Low-Z	t_{OLZ}*	0	-	ns
Chip Disable to Output in High-Z	t_{CHZ}*	-	4	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	4	ns
Output Hold from Address Change	t_{OH}	2	-	ns
LB#, UB# Access Time	t_{BA}	-	4.5	ns
LB#, UB# to High-Z Output	t_{BHZ}*	-	4	ns
LB#, UB# to Low-Z Output	t_{BLZ}*	0	-	ns

(2) WRITE CYCLE

PARAMETER	SYM.	AS7C34098B-10		UNIT
		MIN.	MAX.	
Write Cycle Time	t_{WC}	10	-	ns
Address Valid to End of Write	t_{AW}	8	-	ns
Chip Enable to End of Write	t_{CW}	8	-	ns
Address Set-up Time	t_{AS}	0	-	ns
Write Pulse Width	t_{WP}	8	-	ns
Write Recovery Time	t_{WR}	0	-	ns
Data to Write Time Overlap	t_{DW}	6	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	ns
Output Active from End of Write	t_{OW}*	2	-	ns
Write to Output in High-Z	t_{WHZ}*	-	4	ns
LB#, UB# Valid to End of Write	t_{BW}	8	-	ns

*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

Address

t_{RC}

t_{AA}

t_{OH}

Dout   Previous Data Valid   Data Valid
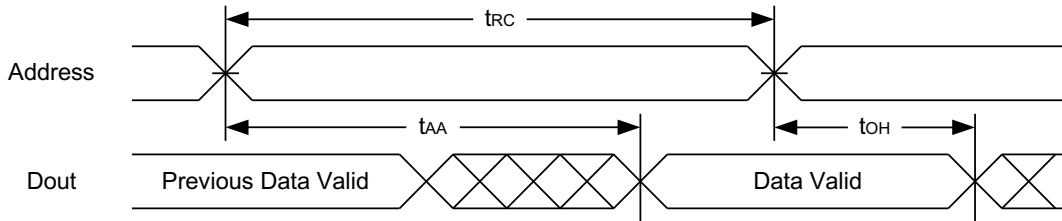
READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)

Address

t_{RC}

t_{AA}

CE#

t_{ACE}

LB#,UB#

t_{BA}

OE#

t_{OE}

t_{OLZ}

t_{OH}

t_{OHZ}

t_{BLZ}

t_{BHZ}

t_{CLZ}

t_{CHZ}

Dout   High-Z   Data Valid   High-Z
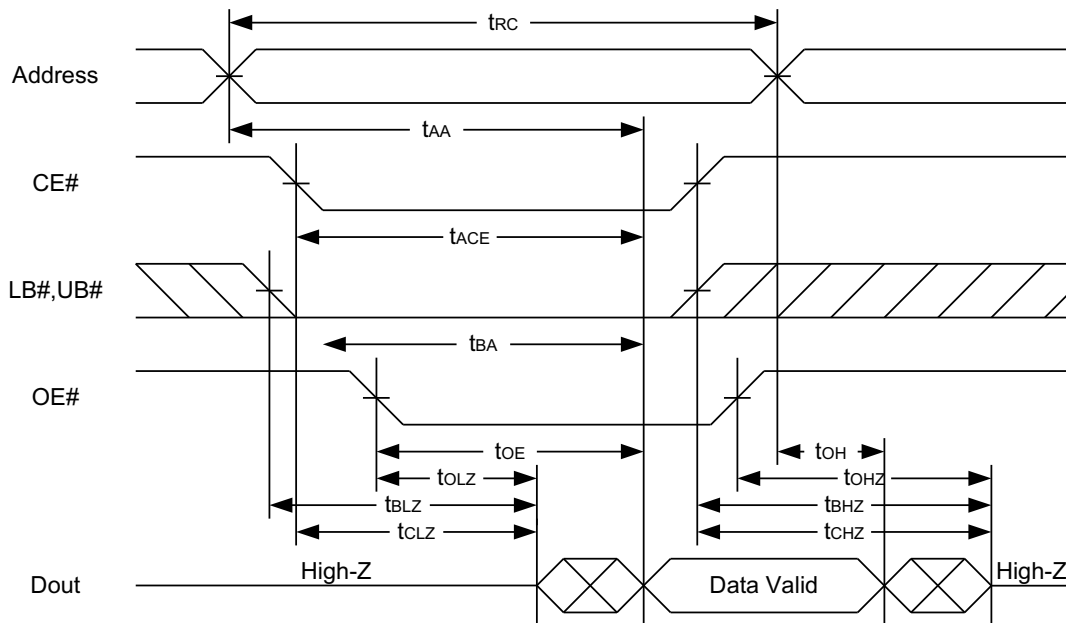
Notes :
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, LB# or UB# = low transition; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ}, t_{BLZ}, t_{OLZ}, t_{CHZ}, t_{BHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ}, t_{OHZ} is less than t_{OLZ}

WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)
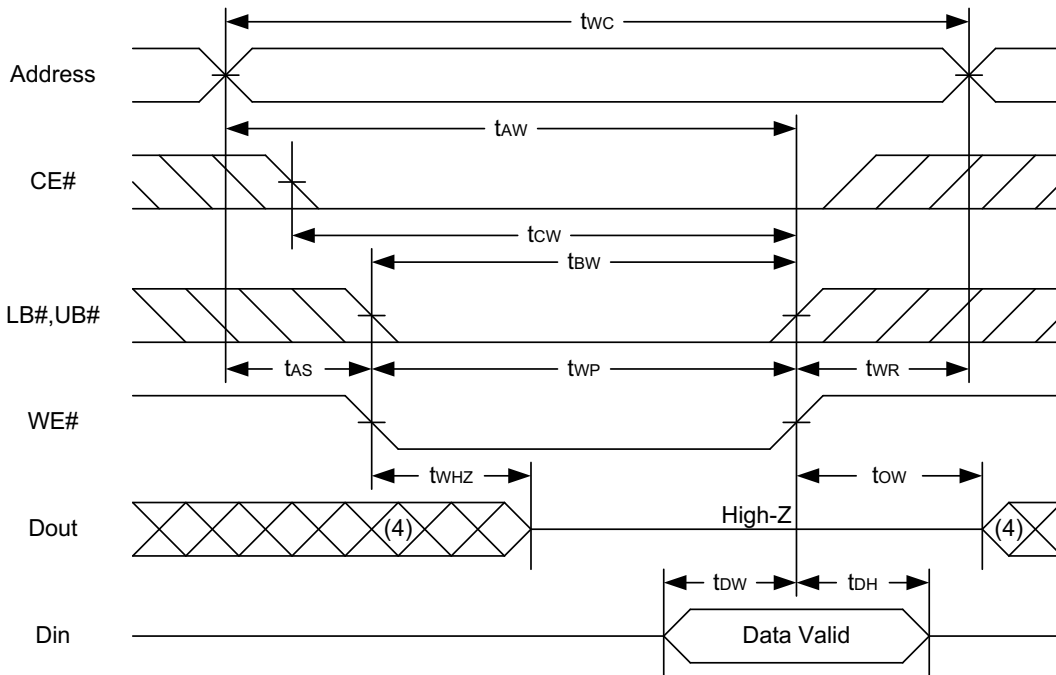
WRITE CYCLE 2 (CE# Controlled) (1,4,5)
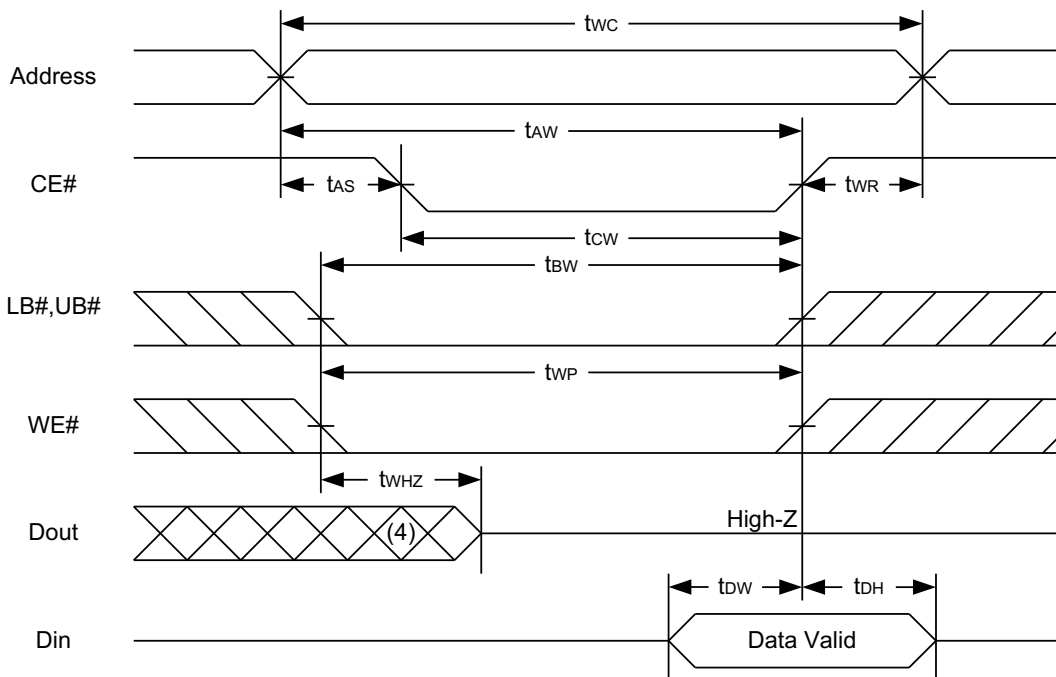
WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)
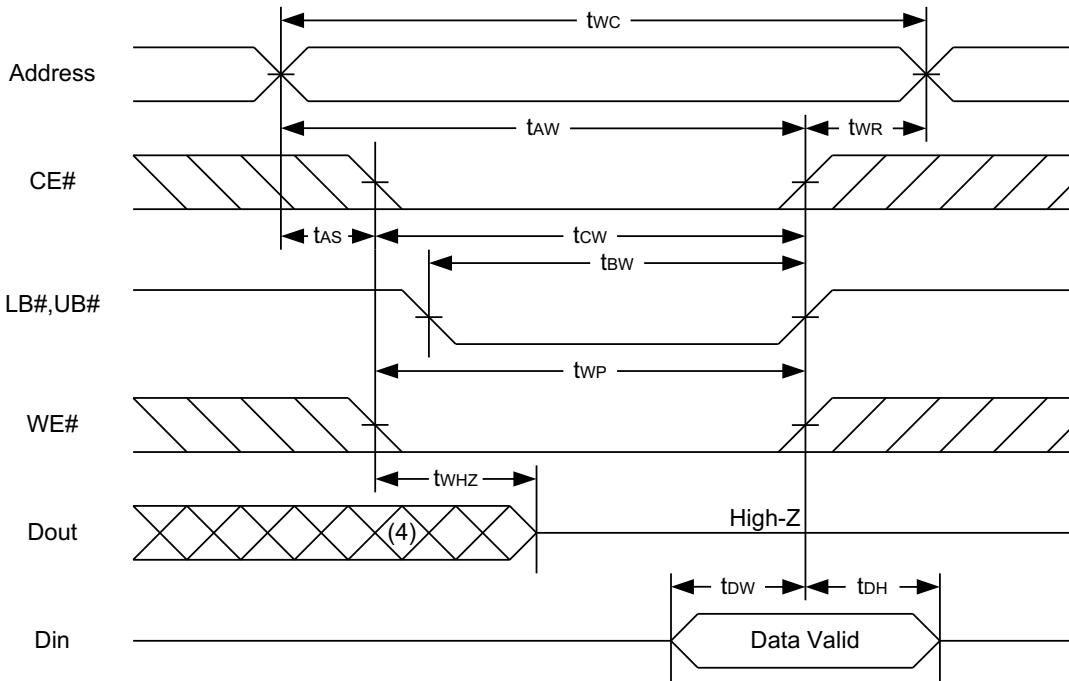
Notes :

1. A write occurs during the overlap of a low CE#, low WE#, LB# or UB# = low.

2. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than t_{WHZ} + t_{DW} to allow the drivers to turn off and data to be placed on the bus.

3. During this period, I/O pins are in the output state, and input signals must not be applied.

4. If the CE#, LB#, UB# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.

5. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V_{CC} for Data Retention	V_{DR}	CE# $\geq V_{CC}$ - 0.2V	1.5	-	3.6	V
Data Retention Current	I_{DR}	V_{CC} = 1.5V, CE# $\geq V_{CC}$ - 0.2V Others at 0.2V or V_{CC} – 0.2V	-	2	10	mA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t_R		t_{RC*}	-	-	ns

t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM
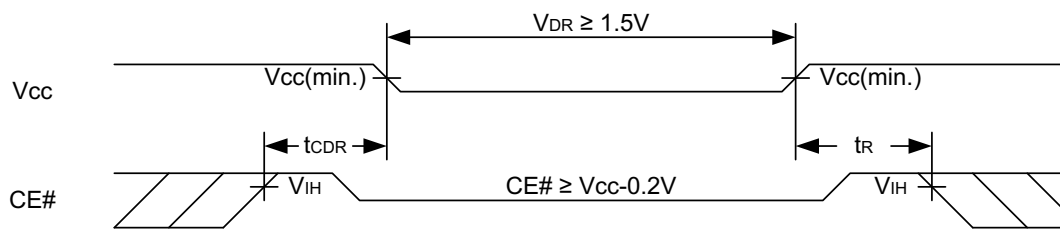
PACKAGE OUTLINE DIMENSION

44-pin 400 mil TSOP Ⅱ Package Outline Dimension
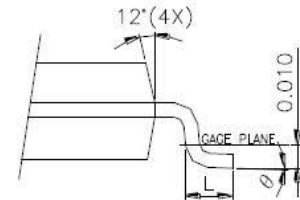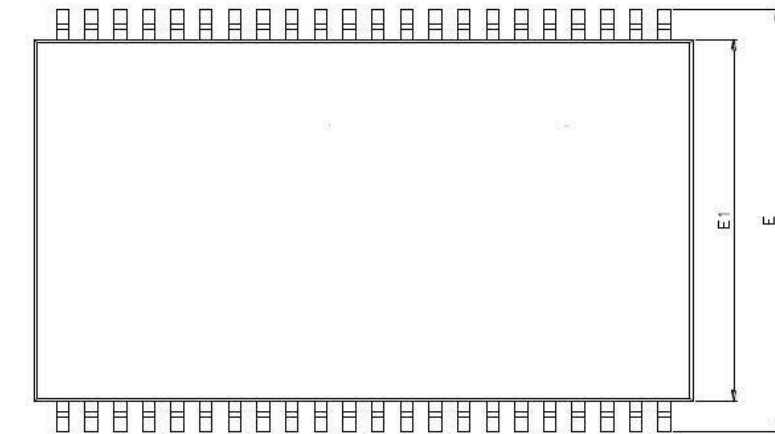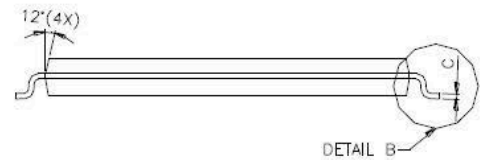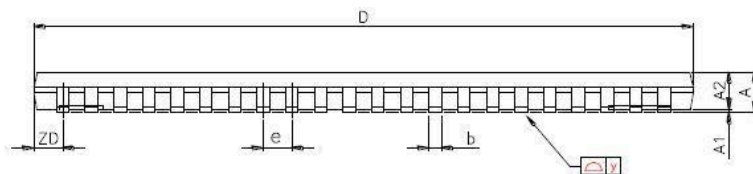
SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
Θ	0°	3°	6°	0°	3°	6°

48-ball 6mm × 8mm TFBGA Package Outline Dimension

TOP VIEW

BOTTOM VIEW

DETAIL A

SIDE VIEW

DETAIL A

SOLDER BALL

Øb(48x PLACES)

DETAIL B
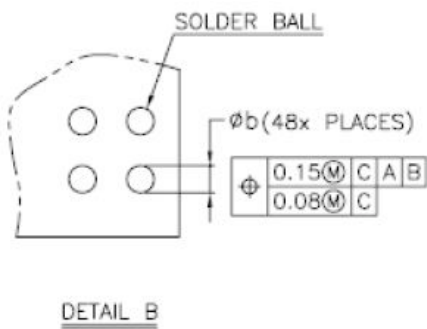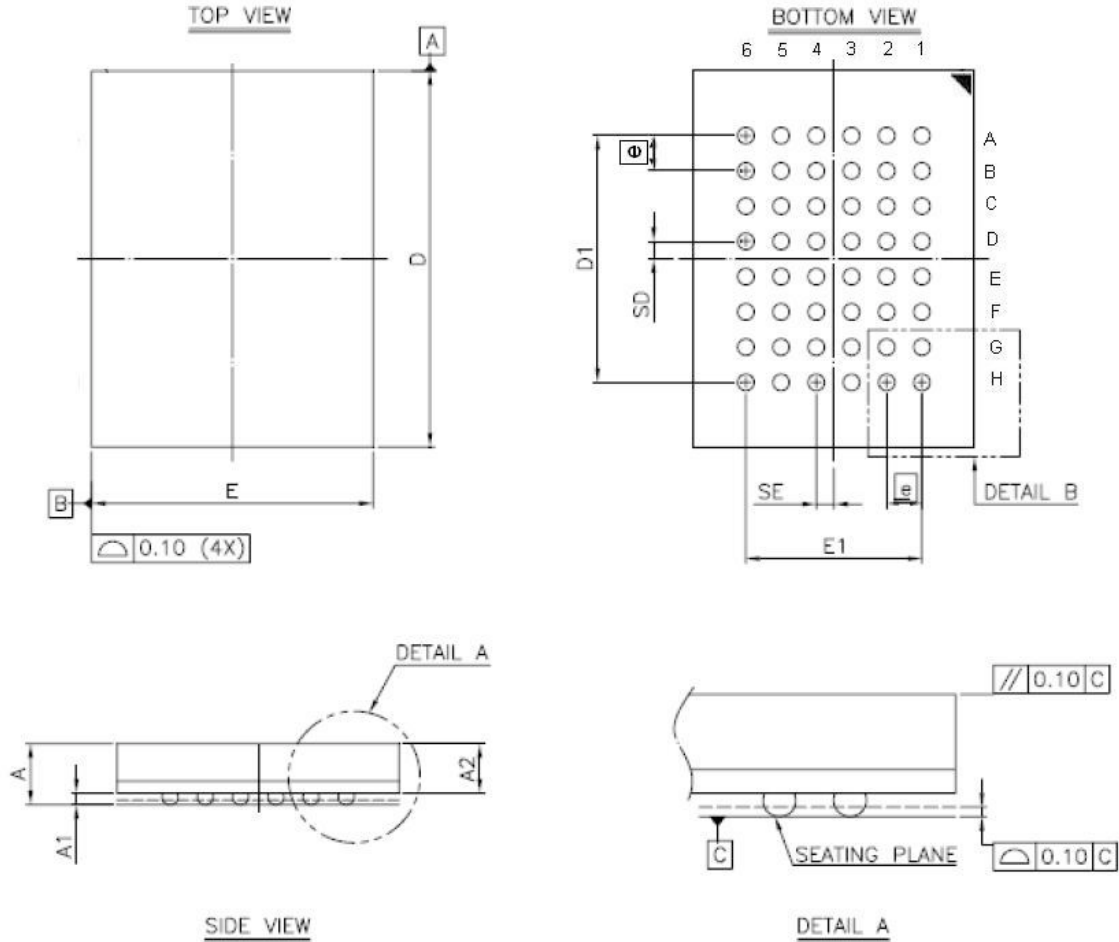
SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.40	—	—	0.055
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	—	—	1.05	—	—	0.041
b	0.30	0.35	0.40	0.012	0.014	0.016
D	7.95	8.00	8.05	0.313	0.315	0.317
D1	5.25 BSC			0.207 BSC		
E	5.95	6.00	6.05	0.234	0.236	0.238
E1	3.75 BSC			0.148 BSC		
SE	0.375 TYP			0.015 TYP		
SD	0.375 TYP			0.015 TYP		
e	0.75 BSC			0.030 BSC		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.

ORDERING INFORMATION

Package Type	Access Time (Speed/ns)	Temperature Range(℃)	Packing Type	Alliance Memory Part Number
44-pin (400mil) TSOP II	10	-40℃~85℃	Tray	AS7C34098B-10TIN
			Tape Reel	AS7C34098B-10TINTR
48-ball (6mm x 8mm) TFBGA	10	-40℃~85℃	Tray	AS7C34098B-10BIN
			Tape Reel	AS7C34098B-10BINTR

Alliance Memory, Inc.
511 Taylor Way,
San Carlos, CA 94070
Tel: 650-610-6800
Fax: 650-620-9211
www.alliancememory.com

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for SRAM *category:*

Click to view products by Alliance Memory *manufacturer:*

Other Similar products are found below :

CY6116A-35DMB CY7C1049GN-10VXI CY7C128A-45DMB GS8161Z36DD-200I GS88237CB-200I RMLV0408EGSB-4S2#AA0 IDT70V5388S166BG IS64WV3216BLL-15CTLA3 IS66WVE4M16ECLL-70BLI PCF8570P K6F2008V2E-LF70000 K6T4008C1B-GB70 CY7C1353S-100AXC AS6C8016-55BIN AS7C164A-15PCN 515712X IDT71V67603S133BG IS62WV51216EBLL-45BLI IS63WV1288DBLL-10HLI IS66WVE2M16ECLL-70BLI 70V639S10BCG IS66WVE4M16EALL-70BLI IS62WV6416DBLL-45BLI IS61WV102416DBLL-10TLI CY7C1381KV33-100AXC CY7C1381KVE33-133AXI 8602501XA 5962-3829425MUA 5962-3829430MUA 5962-8855206YA 5962-8866201YA 5962-8866204TA 5962-8866206MA 5962-8866208UA 5962-8872502XA 5962-9062007MXA 5962-9161705MXA 70V3579S6BFI GS882Z18CD-150I M38510/28902BVA 8413202RA 5962-9161708MYA 5962-8971203XA 5962-8971202ZA 5962-8872501LA 5962-8866208YA 5962-8866205YA 5962-8866205UA 5962-8866203YA 5962-8855202YA