Features

- Dual-core ARM Cortex™-A53 CPU@1512 MHz
- Dual-core HiFi4@400 MHz
- ARM China Zhouyi Z1 AIPU, up to 0.25TOPS@600 MHz (only for R329-N4 and R329-N3)
- Memories
  - Embedded with 256 MB or 128 MB DDR3, clock frequency up to 774 MHz
  - 8-bit NAND Flash with 80-bit ECC per 1024 bytes
  - Two SD/MMC host controller (SMHC) interfaces
- Analog Audio Codec
  - 2 DAC channels and 5 ADC channels
  - Two differential speaker outputs: SPKLP/N, SPKRP/N
  - Five differential microphone inputs: MICIN1P/1N, MICIN2P/2N, MICIN3P/3N, MICIN4P/4N, MICIN5P/5N
- Three I2S/PCM external interfaces (I2S0, I2S1, S-I2S0)
- Maximum 8 digital PDM microphones
- One OWA TX, compliance with S/PDIF interface
- Security Engine
  - Symmetrical algorithm: AES, DES, TDES
  - Hash algorithm: MD5, SHA, HMAC
  - Asymmetrical algorithm: RSA
  - Hardware PRNG and TRNG
  - 1 Kbit eFuse
- External Peripherals
  - One USB 2.0 DRD (USB0) and one USB 1.1 HOST (USB1)
  - 10/100/1000 Mbps Ethernet port with RGMII and RMII interfaces
  - Up to 5 UART controllers (UART0, UART1, UART2, UART3, S-UART0)
  - Up to 2 SPI controllers (SPI0, SPI1)
  - Up to 3 TWI controllers (TWI0, TWI1, S-TWI0)
  - Two CIR RX interfaces and one CIR TX interface
  - Up to 15 PWM channels (PWM[8:0], S-PWM[5:0])
  - One LRADC input channel
  - Up to 4 GPADC input channels
  - One Smart Card Reader (SCR)
  - One LEDC for using to control the external intelligent control LED lamp
- Package
  - LFBGA231 balls, 0.65 mm ball pitch, 0.35 mm ball size, 12 mm x 12 mm body (only for R329-N3 and R329-S3)
  - LFBGA228 balls, 0.65 mm ball pitch, 0.35 mm ball size, 12 mm x 14.5 mm body (only for R329-N4)

Revision History

Revision	Date	Author	Description
1.0	December 30, 2020	AWA0330	Initial release version.
1.1	February 17, 2022	AWA1890	Update the specification of OWA.
1.2	March 29, 2022	AWA1890	Update CIR RX specification in the cover page

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About This Documentation

Purpose

The documentation describes features of each module, pin/signal characteristics, current consumption, interface timing, thermal and package, and part reliability of the R329 processor. For details about register descriptions of each module, see the *R329_User_Manual*.

Intended Audience

The document is intended for:

- Hardware designers and maintenance personnel for electronics
- Sales personnel for electronic parts and components

Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
 **WARNING**	Indicates potential risk of injury or death exists if the instructions are not obeyed.
 **CAUTION**	Indicates potential risk of equipment damage, data loss, performance degradation, or unexpected results exists if the instructions are not obeyed.
 **NOTE**	Provides additional information to emphasize or supplement important points of the main text.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Numerical Conventions

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity	1K	1024
	1M	1,048,576
	1G	1,073,741,824
Frequency, data rate	1k	1000
	1M	1,000,000
	1G	1,000,000,000

1. Overview

Allwinner's R329 is a highly integrated dual-core SoC targeted for audio application markets. The R329 integrates a dual-core ARM Cortex™-A53 operating up to 1512 MHz, a dual-core HiFi4 DSP operating up to 400 MHz, and ARM Zhouyi Z1 AIPU 0.25T, which provides powerful and energy-efficient computing power for audio applications. An extensive set of audio interfaces such as audio codec (5 ADCs, 2 DACs), I2S/PCM, DMIC, one wire audio (OWA) are included for voice wake-up/recognition/record/playback applications on connected audio products. The outstanding audio subsystem supports all major high-resolution audio formats and works seamlessly with the CPU to accelerate multimedia algorithms and improve the user experience.

To reduce the BOM cost, a 256 MB or 128 MB DDR3 die is embedded for the R329. The R329 comes with extensive connectivity and interfaces, such as USB, SDIO, SPI, UART, TWI, EMAC, CIR, etc. Besides the R329 can connect with other different peripherals like WIFI and BT via SDIO and UART. Security functions are enabled and accelerated by hardware crypto engine, secure boot, and secure eFuse, etc.

1.1. Device Difference

The R329 is configured with different sets of features in different devices. Table 1-1 shows the feature differences across different devices.

Table 1-1 Device Feature Differences

Contents	R329-N4	R329-N3	R329-S3
SDRAM	SIP 256 MB DDR3	SIP 128 MB DDR3	SIP 128 MB DDR3
AIPU	Support	Support	No support
Package	LFBGA228 balls (G9, J7, K13: No ball), 12 mm x 14.5 mm body	LFBGA231 balls (G9, J7, K13: GND ball), 12 mm x 12 mm body	LFBGA231 balls (G9, J7, K13: GND ball), 12 mm x 12 mm body
PCB Footprint	LFBGA231 12 mm x 14.5 mm for PCB pin-to-pin design		

2. Features

2.1. CPU Architecture

- Dual-core ARM Cortex™-A53 Processor, frequency up to 1512 MHz
- Power-efficient ARM v8 architecture
- 64 and 32bit execution states for scalable high performance
- Trustzone technology supported
- Supports NEON Advanced Single Instruction Multiple Data (SIMD) instruction for acceleration of media and signal processing functions
- VFPv4 Floating Point Unit
- 32 KB L1 I-cache and 32 KB L1 D-cache for per core
- 256 KB L2 cache shared

2.2. DSP Architecture

- Dual-core HiFi4
- Up to 400 MHz
- 32 KB L1 I-cache and 32 KB L1 D-cache for per core
- 2 MB SRAM

2.3. AIPU

- ARM China Zhouyi Z1 AIPU, 1TEC+128mac FF
- Up to 0.25TOPS@600MHz

NOTE

R329-S3 does not support AIPU. Only R329-N3 and R329-N4 support.

2.4. Memory Subsystem

2.4.1. Boot ROM (BROM)

- On-chip memory
- Supports system boot from the following devices:
  - SD card
  - eMMC
  - NAND Flash
  - SPI NOR Flash
  - SPI NAND Flash
- Supports mandatory upgrade process through USB
- Supports mandatory upgrade process through SD card (This requires that the flash on the device has no valid firmware)
- Supports the GPIO pin to select the boot media type
- Supports eFuse to select the boot media type
- Supports normal booting and secure booting
- Secure BROM loads only certified firmware
- Secure BROM ensures that the secure boot is a trusted environment

2.4.2. SDRAM

- Embedded with 256 MB DDR3 (only for R329-N4)
- Embedded with 128 MB DDR3 (only for R329-N3 and R329-S3)
- Supports clock frequency up to 774 MHz for DDR3

2.4.3. NAND Flash

- Compliant with ONFI 2.0 and Toggle 2.0
- Up to 80-bit ECC per 1024 bytes
- Supports 1K/2K/4K/8K/16K/32K bytes page size
- Up to 8-bit data bus width
- Supports SLC/MLC/TLC flash and EF-NAND
- Supports SDR/Toggle DDR/ONFI DDR NAND interface

2.4.4. SMHC

- Two SD/MMC host controller (SMHC) interfaces
- The SMHC0 controls the devices that comply with the following protocols:
  - Secure Digital Memory (SD mem-version 3.0)
  - Multimedia Card (eMMC-version 5.1)
- The SMHC1 controls the device that complies with the protocol Secure Digital I/O (SDIO-version 3.0)
- Maximum performance:
  - SDR mode 150 MHz@1.8 V IO pad
  - DDR mode 50 MHz@1.8 V IO pad
  - DDR mode 50 MHz@3.3 V IO pad
- Supports 1-bit or 4-bit data width
- Supports hardware CRC generation and error detection
- Supports block size of 1 to 65535 bytes

2.5. System Peripherals

2.5.1. Timer

- The timer module implements the timing and counting functions, which includes timer0, timer1, watchdog, and audio video synchronization (AVS)
- The timer0/timer1 is a 32-bit down counter. The timer0 and timer1 are completely consistent
- The watchdog is used to transmit a reset signal to reset the entire system when an exception occurs in the system
- The AVS is used to synchronize the audio and video. The AVS sub-block includes AVS0 and AVS1, which are completely consistent

2.5.2. High Speed Timer (HSTimer)

- The HSTimer module consists of HSTimer0 and HSTimer1. HSTimer0 and HSTimer1 are down counters that implement timing and counting functions. They are completely consistent.
- Configurable 56-bit down timer
- Supports 5 prescale factors
- The clock source is synchronized with AHB1 clock, much more accurate than other timers
- Supports 2 working modes: periodic mode and single counting mode
- Generates an interrupt when the count is decreased to 0

2.5.3. GIC

- Supports 16 Software Generated Interrupts (SGIs), 16 Private Peripheral Interrupts (PPIs), and 160 Shared Peripheral Interrupts (SPIs)
- Enabling, disabling, and generating processor interrupts from hardware interrupt
- Interrupt masking and prioritization
- Uniprocessor and multiprocessor environments
- ARM architecture security extensions
- ARM architecture virtualization extensions
- Wakeup events in power-management environments

2.5.4. DMAC

- Up to 8-ch DMA in CPUX domain and 8-ch DMA in CPUS domain
- Interrupt generated for each DMA channel
- Flexible data width of 8/16/32/64-bit
- Supports linear and IO address modes
- Supports data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory, peripheral-to-peripheral
- Supports transfer with linked list
- DRQ response includes waiting mode and handshake mode
- DMA channel supports pause function

2.5.5. Clock Controller Unit (CCU)

- 4 PLLs
- One on-chip RC oscillator
- Supports one external 24 MHz DCXO and one external 32.768 kHz oscillator
- Supports clock configuration and clock generation for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules

2.5.6. Thermal Sensor Controller (THS)

- One thermal sensor located in CPU
- Temperature accuracy: ±3°C from 0°C to +100°C, ±5°C from -25°C to +125°C
- Supports over-temperature protection interrupt and over-temperature alarm interrupt
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt

2.5.7. CPU Configuration

- CPU reset system: core reset, debug circuit reset, and other functional modules reset
- CPU related control: interface control, CP15 control, and power-on/off control
- CPU status check: idle status, SMP status, interrupt status, and so on
- Including CPU debug control and status register

2.5.8. LDO Power

- Integrated 2 LDOs (LDOA, LDOB)
- LDOA: 1.8 V power output, LDOB: 1.35 V/1.5 V/1.8 V power output
- LDOA for IO and analog module, LDOB for SDRAM
- Input voltage is 2.4 V to 3.6 V

2.5.9. RTC

- Implements time counter and timing wakeup
- Provides a 16-bit counter for counting day, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- External connect a 32.768 kHz low-frequency oscillator for count clock
- Timer frequency is 1 kHz
- Configurable initial value by software anytime
- Supports timing alarm, and generates interrupt and wakeup the external devices
- Supports fanout function of internal 32K clock
- 8 general purpose registers for storing power-off information

2.5.10. Reset

- Integrated internal reset
- Reset R329 or other IC

2.6. Audio Subsystem

2.6.1. Audio Codec

- Two audio digital-to-analog (DAC) channels
  - Supports 16-bit and 20-bit sample resolution
  - 8 kHz to 192 kHz DAC sample rate
  - 100 ± 2dB SNR@A-weight, -85 ± 3dB THD+N
- Two audio outputs:
  - Two differential speaker outputs: SPKLP/N, SPKRP/N
- Five audio analog-to-digital (ADC) channels
  - Supports 16-bit and 20-bit sample resolution
  - 8 kHz to 48 kHz ADC sample rate
  - 95 ± 3dB SNR@A-weight, -80 ± 3dB THD+N
- Five audio inputs:
  - Five differential microphone inputs: MICIN1P/1N, MICIN2P/2N, MICIN3P/3N, MICIN4P/4N, MICIN5P/5N
- One low-noise analog microphone bias output
- Supports Dynamic Range Controller adjusting the DAC playback and ADC recording
- One 128x20-bits FIFO for DAC data transmit, one 256x20-bits FIFO for ADC data receive
- Programmable FIFO thresholds
- Supports interrupts and DMA

2.6.2. I2S/PCM

- Three I2S/PCM external interfaces (I2S0, I2S1, S-I2S0) for connecting external power amplifier and MIC ADC
- I2S0 supports 4 data channels; I2S1 and S-I2S0 support 2 data channels
- S-I2S0 supports asynchronous sample rate conversion (ASRC)
- Compliant with standard Philips Inter-IC sound (I2S) bus specification
- Compliant with Left-justified, Right-justified, PCM mode, and Time Division Multiplexing (TDM) format
- TDM mode supports maximum 16 channels output and 16 channels input
- Supports full-duplex synchronous work mode
- Supports Master/Slave mode
- Clock up to 49.152 MHz data output of I2S/PCM in Master mode when the IO PAD and peripheral I2S/PCM satisfy timing parameters
- Clock up to 12.288 MHz data input of I2S/PCM in Master mode when the IO PAD and peripheral I2S/PCM satisfy timing parameters

- Supports adjustable audio sample resolution from 8-bit to 32-bit
- Sample rate from 8 kHz to 384 kHz (channels=2)
- Supports 8-bit u-law and 8-bit A-law companded sample
- One 128 depth x 32-bit width TXFIFO for data transmit, one 64 depth x 32-bit width RXFIFO for data receive
- Supports programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Programmable FIFO thresholds

2.6.3. DMIC

- Supports maximum 8 digital PDM microphones
- Supports sample rate from 8 kHz to 48 kHz

2.6.4. One Wire Audio (OWA)

- One OWA TX
- Compliance with S/PDIF Interface
- IEC-60958 transmitter and receiver functionality
- Supports 16-bit, 20-bit and 24-bit data formats
- Supports channel status insertion for the transmitter
- Hardware parity generation on the transmitter
- One 128×24 bits TXFIFO for audio data transfer
- Supports interrupts and DMA
- Function clock includes 24.576MHz and 22.5792MHz frequency

2.7. Security Engine

2.7.1. Crypto Engine (CE)

- Supports Symmetrical algorithm for encryption and decryption: AES, DES, TDES
  - Supports ECB, CBC, CTS, CTR, CFB, OFB mode for AES
  - Supports 128/192/256-bit key for AES
  - Supports ECB, CBC, CTR mode for DES/TDES
- Supports Hash algorithm for tamper proofing: MD5, SHA, HMAC
  - Supports SHA1, SHA224, SHA256, SHA384, SHA512 for SHA
  - Supports HMAC-SHA1, HMAC-SHA256 for HMAC
  - Supports multi-package mode for MD5/SHA1/SHA224/SHA256/SHA384/SHA512
- Supports Asymmetrical algorithm for signature verification: RSA
  - RSA supports 512/1024/2048-bit width
- Supports 160-bit hardware PRNG with 175-bit seed
- Supports 256-bit hardware TRNG
- Internal DMA controller for data transfer with memory
- Supports secure and non-secure interfaces respectively

2.7.2. Security ID (SID)

- Supports 1 Kbit eFuse for chip ID and security application
- The eFuse has secure zone and non-secure zone
- Backup eFuse information by using SID_SRAM
- Burning the key to the SID
- Reading the key use status in the SID
- Loading the key to the CE

2.7.3. Secure Memory Control (SMC)

- The SMC is always secure, only secure CPU can access the SMC
- Sets secure area of DRAM
- Sets secure property that Master accesses to DRAM

2.7.4. Secure Peripherals Control (SPC)

- The SPC is always secure, only secure CPU can access the SPC
- Sets secure property of peripherals

2.8. External Peripherals

2.8.1. USB

- One USB 2.0 DRD (USB0), with integrated USB 2.0 analog PHY
  - Compatible with USB 2.0 Specification
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s), and Low-Speed (LS, 1.5 Mbit/s) in host mode
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) in device mode
  - Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a for host mode
  - Supports bi-directional endpoint0 (EP0) for Control transfer
  - Up to 8 user-configurable endpoints (EP1 +, EP1 -, EP2 +, EP2 -, EP3 +, EP3 -, EP4 +, EP4 -) for Bulk, Isochronous and Interrupt bi-directional transfers
  - Supports (4 KB + 64 Bytes) FIFO for EPs (including EP0)
  - Supports point-to-point and point-to-multipoint transfer in both host and peripheral modes
- One USB 1.1 HOST (USB1), with integrated USB 1.1 analog PHY
  - Compatible with USB 1.1 Specification and Open Host Controller Interface (OHCI) Specification, Version 1.0a.
  - Supports Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) device

2.8.2. EMAC

- One EMAC interface for connecting external Ethernet PHY
- 10/100/1000 Mbps Ethernet port with RGMII and RMII interfaces
- Compliant with IEEE 802.3-2002 standard
- Supports both full-duplex and half-duplex operation
- Provides the management data input/output (MDIO) interface for PHY device configuration and management with configurable clock frequencies
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
- Supports linked-list descriptor list structure
- Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4 KB of data
- Comprehensive status reporting for normal operation and transfers with errors
- 4 KB TXFIFO for transmission packets and 16 KB RXFIFO for reception packets
- Programmable interrupt options for different operational conditions

2.8.3. UART

- Up to 5 UART controllers (UART0, UART1, UART2, UART3, S-UART0)

- UART0, S-UART0: 2-wire; UART1, UART2, UART3: 4-wire
- Compatible with industry-standard 16450/16550 UARTs
- Supports IrDA-compatible slow infrared (SIR) format
- Supports RS-485/9-bit mode
- Capable of speed up to 4 Mbit/s
- Supports 5 to 8 data bits and 1/1.5/2 stop bits
- Programmable parity (even, odd, or no parity)
- Supports DMA controller interface
- Supports software/hardware flow control
- Two separate FIFOs: one is RX FIFO, and the other is TX FIFO
  - Each of them is 64 bytes (For UART0 and S-UART0)
  - Each of them is 256 bytes (For UART1, UART2 and UART3)

2.8.4. SPI and SPI_DBI

- Up to 2 SPI controllers (SPI0, SPI1)
- The SPI0 only supports SPI mode; The SPI1 supports SPI mode and display bus interface (DBI) mode
- SPI mode:
  - Full-duplex synchronous serial interface
  - Master/slave configurable
  - Mode0 to Mode3 are supported for both transmit and receive operations
  - 8-bit wide by 64-entry FIFO for both transmit and receive data
  - Polarity and phase of the Chip Select (SPI-CS) and SPI Clock (SPI-CLK) are configurable
  - Supports 3-wire/4-wire SPI
  - Supports programmable serial data frame length: 1-bit to 32-bit
  - Supports Standard SPI, Dual-Output/Dual-Input SPI, Dual IO SPI, Quad-Output/Quad-Input SPI
- DBI mode:
  - Supports DBI Type C 3 Line/4 Line Interface Mode
  - Supports 2 Data Lane Interface Mode
  - Supports RGB111/444/565/666/888 video format
  - Maximum resolution of RGB666 240 x 320@30Hz with single data lane
  - Maximum resolution of RGB888 240 x 320@60Hz or 320 x 480@30Hz with dual data lane
  - Supports Tearing effect
  - Supports software flexible control video frame rate

2.8.5. Two Wire Interface (TWI)

- Up to 3 TWI controllers (TWI0, TWI1, S-TWI0)
- Software-programmable for slave or master
- Supports Standard mode (up to 100 kbit/s) and Fast mode (up to 400 kbit/s)
- Supports 7-bit and 10-bit device addressing modes
- Supports repeated START signal
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Byte-by-byte data transfer
- Allows operation from a wide range of input clock frequency
- The TWI controller includes one TWI engine and one TWI driver. And the TWI driver supports packet transmission and DMA mode when TWI works in master mode

2.8.6. CIR Receiver (CIR_RX)

- Up to 2 CIR_RX interfaces (IR-RX, S-IR-RX)
- Full physical layer implementation

- Supports NEC format infra data
- Supports CIR for remote control or wireless keyboard
- 64x8 bits FIFO for data buffer
- Sample clock up to 1 MHz

2.8.7. CIR Transmitter (CIR_TX)

- 1 CIR_TX interface (IR-TX)
- Supports arbitrary wave generator
- Configurable carrier frequency
- Supports handshake mode and waiting mode of DMA
- 128 bytes FIFO for data buffer

2.8.8. PWM

- 15 PWM channels (PWM[8:0], S-PWM[5:0])
- Supports pulse, cycle and complementary pair output
- Supports capture input
- Programming deadzone output
- Build-in the programmable dead-time generator and the controllable dead-time
- Three kinds of output waveform: continuous waveform, pulse waveform and complementary pair
- Output frequency range: 0 to 24 MHz or 100 MHz
- Various duty-cycle: 0% to 100%
- Minimum resolution: 1/65536
- Interrupt generation of PWM output and capture input

2.8.9. Low Rate ADC (LRADC)

- One LRADC input channel
- 6-bit sampling resolution and 5-bit precision
- Sample rate up to 2 kHz
- Supports hold Key and general Key
- Supports normal, continuous and single working mode
- Power supply voltage: AVCC, power reference voltage: 0.75*AVCC, analog input and detected voltage range: 0 to 1.266 V

2.8.10. General Purpose ADC (GPADC)

- 4-ch successive approximation register (SAR) analog-to-digital converter (ADC)
- 12-bit sampling resolution and 8-bit precision
- 64 FIFO depth of data register
- Power reference voltage: AVCC, analog input voltage range: 0 to AVCC
- Maximum sampling frequency up to 1 MHz
- Supports three operation modes: single conversion mode, continuous conversion mode, burst conversion mode

2.8.11. Smart Card Reader (SCR)

- Supports the ISO/IEC 7816-3:1997(E) and EMV2000 (4.0) Specifications
- Performs functions needed for complete smart card sessions, including:
  - Card activation and deactivation
  - Cold/warm reset
  - Answer to Reset (ATR) response reception

  - Data transfers to and from the card
- Supports adjustable clock rate and bit rate
- Configurable automatic byte repetition
- Supports commonly used communication protocols:
  - T=0 for asynchronous half-duplex character transmission
  - T=1 for asynchronous half-duplex block transmission
- Supports FIFOs for receive and transmit buffers (up to 128 characters) with threshold
- Supports configurable timing functions:
  - Smart card activation time
  - Smart card reset time
  - Guard time
  - Timeout timers
- Supports synchronous and any other non-ISO 7816 and non-EMV cards

2.8.12. LEDC

- LEDC is used to control the external intelligent control LED lamp
- Configurable LED output high/low level width
- Configurable LED reset time
- LEDC data supports DMA configuration mode and CPU configuration mode
- Maximum 1024 LEDs serial connect
- LED data transfer rate up to 800 kbit/s

2.9. Package

- LFBGA231 balls, 0.65 mm ball pitch, 0.35 mm ball size, 12 mm x 12 mm body (only for R329-N3 and R329-S3)
- LFBGA228 balls, 0.65 mm ball pitch, 0.35 mm ball size, 12 mm x 14.5 mm body (only for R329-N4)

3. Block Diagram

Figure 3-1 shows the system block diagram of the R329.

Figure 3-1 R329 System Block Diagram

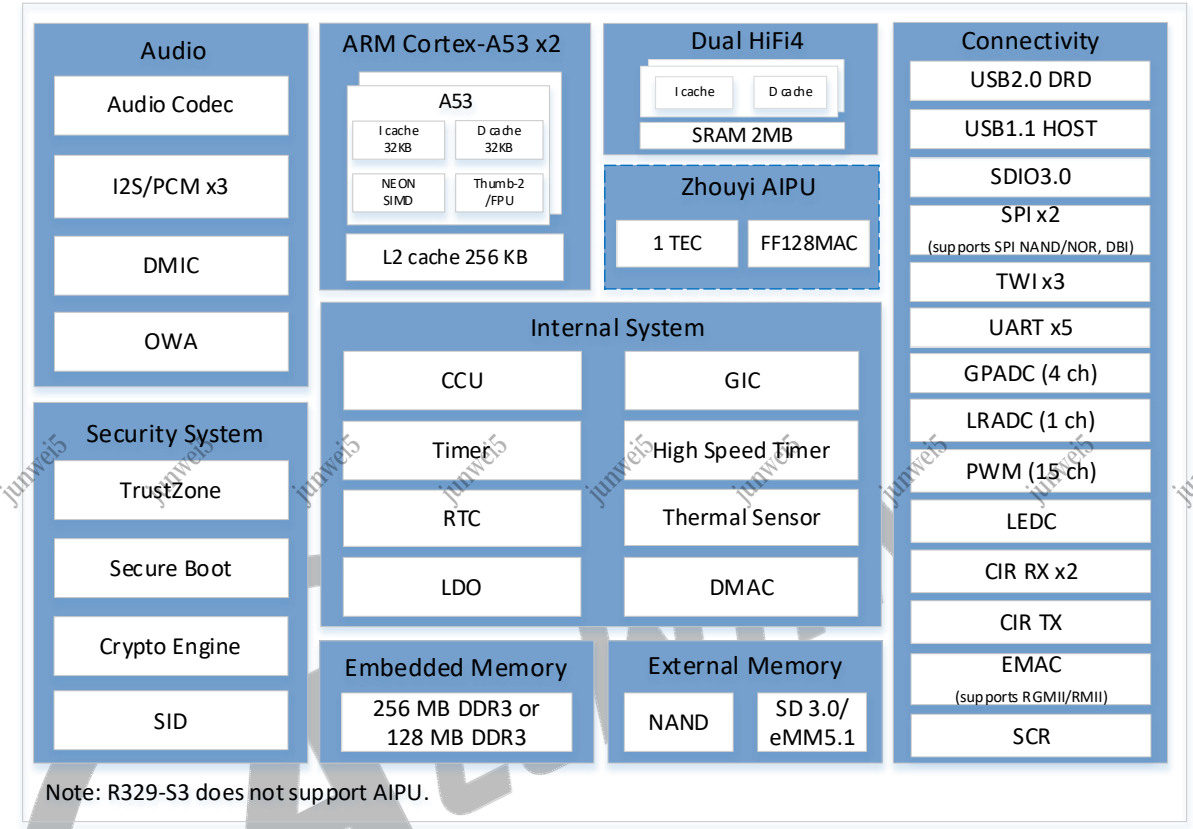
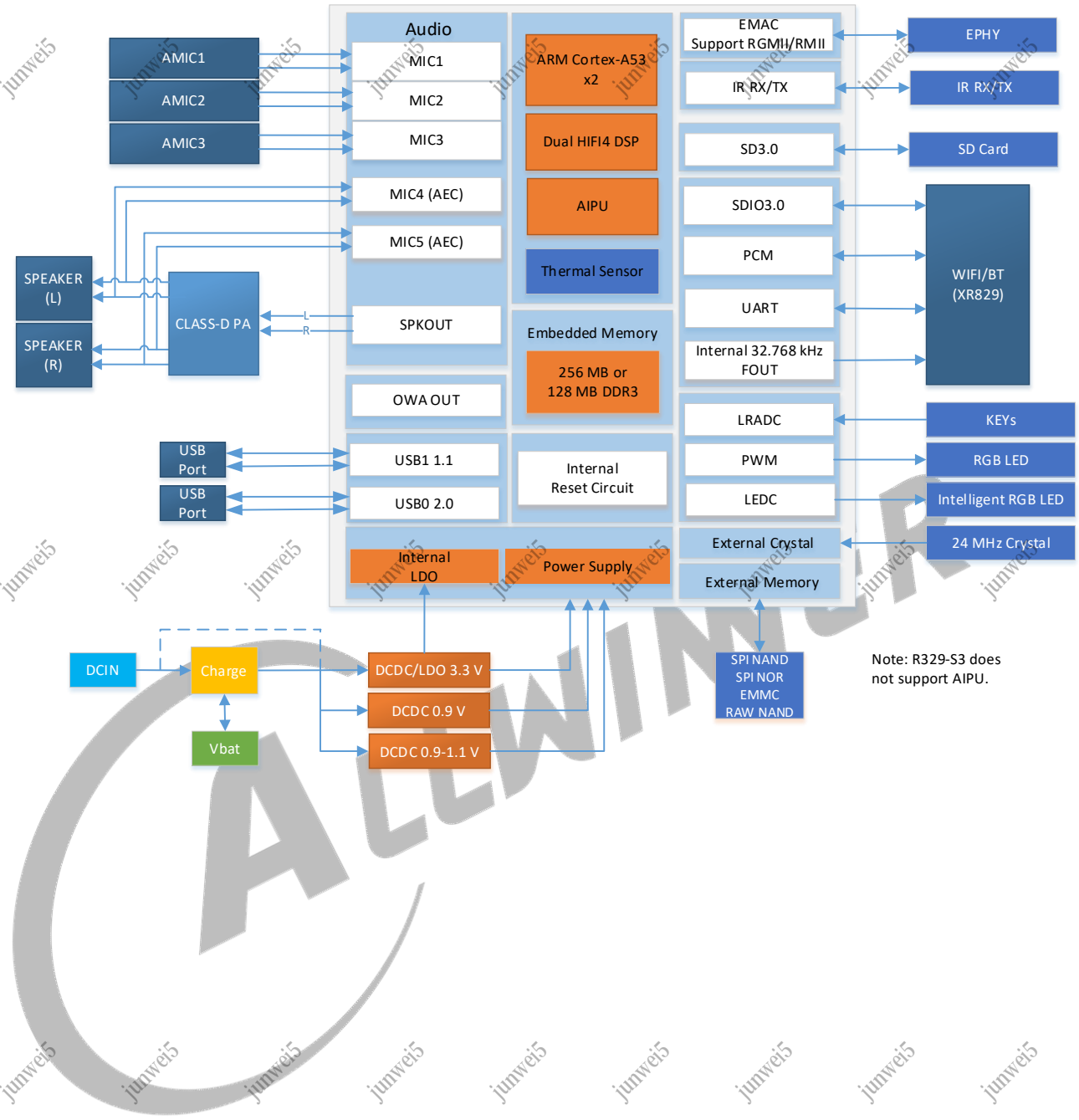


Figure 3-2 shows the intelligent speaker solution of the R329.

Figure 3-2 R329 Intelligent Speaker Solution



4. Pin Description

4.1. Pin Quantity

4.1.1. R329-N3/R329-S3

Table 4-1 lists the pin quantity of the R329-N3 and R329-S3.

Table 4-1 R329-N3/R329-S3 Pin Quantity

Pin Type	Quantity
I/O	128
Power	23
Ground	73
DDR Power	7
Total	231

4.1.2. R329-N4

Table 4-2 lists the pin quantity of the R329-N4.

Table 4-2 R329-N4 Pin Quantity

Pin Type	Quantity
I/O	128
Power	23
Ground	70
DDR Power	7
Total	228

4.2. Pin Characteristics

Table 4-3 lists the characteristics of the R329 pins from the following seven aspects.

[1].Ball#: Package ball numbers associated with each signal.

[2].Pin Name: The name of the package pin.

[3].Type: Denotes the signal direction
I (Input),
O (Output),
I/O (Input/Output),
OD (Open-Drain),
A (Analog),
AI (Analog Input),
AO (Analog Output),
P (Power),
G (Ground)

[4].Ball Reset State: The state of the terminal at reset. PU: pull up; PD: pull down; Z: high impedance.

[5].Pull Up/Down: Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled via software.

[6].Default Buffer Strength: Defines the default drive strength of the associated output buffer. The maximum drive strength of each GPIO is 6 mA.

[7].Power Supply: The voltage supply for the IO buffers of the terminal.

Table 4-3 Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
SDRAM						
K11,L12,M12, P12,K12,N12, P11	VCC-DRAM	P	NA	NA	NA	NA
GPIOB						
V11	PB0	I/O	Z	PU/PD	4	VCC-IO
U11	PB1	I/O	Z	PU/PD	4	VCC-IO
T11	PB2	I/O	Z	PU/PD	4	VCC-IO
U10	PB3	I/O	Z	PU/PD	4	VCC-IO
T10	PB4	I/O	Z	PU/PD	4	VCC-IO
V9	PB5	I/O	Z	PU/PD	4	VCC-IO
U9	PB6	I/O	Z	PU/PD	4	VCC-IO
T9	PB7	I/O	Z	PU/PD	4	VCC-IO
U8	PB8	I/O	Z	PU/PD	4	VCC-IO
GPIOC						
V3	PC0	I/O	PU	PU/PD	4	VCC-PC
U3	PC1	I/O	Z	PU/PD	4	VCC-PC
V2	PC2	I/O	PU	PU/PD	4	VCC-PC
T3	PC3	I/O	Z	PU/PD	4	VCC-PC
U2	PC4	I/O	Z	PU/PD	4	VCC-PC
U1	PC5	I/O	PU	PU/PD	4	VCC-PC
T2	PC6	I/O	Z	PU/PD	4	VCC-PC
T1	PC7	I/O	PU	PU/PD	4	VCC-PC
J6	VCC-PC	P	NA	NA	NA	NA
GPIOF						
N2	PF0	I/O	Z	PU/PD	4	VCC-PF
N3	PF1	I/O	Z	PU/PD	4	VCC-PF
P1	PF2	I/O	Z	PU/PD	4	VCC-PF
P2	PF3	I/O	Z	PU/PD	4	VCC-PF
P3	PF4	I/O	Z	PU/PD	4	VCC-PF
R2	PF5	I/O	Z	PU/PD	4	VCC-PF
R3	PF6	I/O	Z	PU/PD	4	VCC-PF
L5	VCC-PF	P	NA	NA	NA	NA
GPIOG						
H1	PG0	I/O	Z	PU/PD	4	VCC-PG
H3	PG1	I/O	Z	PU/PD	4	VCC-PG
J2	PG2	I/O	Z	PU/PD	4	VCC-PG
J3	PG3	I/O	Z	PU/PD	4	VCC-PG
K1	PG4	I/O	Z	PU/PD	4	VCC-PG
K2	PG5	I/O	Z	PU/PD	4	VCC-PG
L3	PG6	I/O	Z	PU/PD	4	VCC-PG
L2	PG7	I/O	Z	PU/PD	4	VCC-PG
M1	PG8	I/O	Z	PU/PD	4	VCC-PG

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
M2	PG9	I/O	Z	PU/PD	4	VCC-PG
F1	PG10	I/O	Z	PU/PD	4	VCC-PG
F2	PG11	I/O	Z	PU/PD	4	VCC-PG
G3	PG12	I/O	Z	PU/PD	4	VCC-PG
F3	PG13	I/O	Z	PU/PD	4	VCC-PG
G2	PG14	I/O	Z	PU/PD	4	VCC-PG
K5	VCC-PG	P	NA	NA	NA	NA
GPIOH						
T4	PH0	I/O	Z	PU/PD	4	VCC-IO
U4	PH1	I/O	Z	PU/PD	4	VCC-IO
T5	PH2	I/O	Z	PU/PD	4	VCC-IO
U5	PH3	I/O	Z	PU/PD	4	VCC-IO
V5	PH4	I/O	Z	PU/PD	4	VCC-IO
T6	PH5	I/O	Z	PU/PD	4	VCC-IO
U6	PH6	I/O	Z	PU/PD	4	VCC-IO
T7	PH7	I/O	Z	PU/PD	4	VCC-IO
U7	PH8	I/O	Z	PU/PD	4	VCC-IO
V7	PH9	I/O	Z	PU/PD	4	VCC-IO
GPIOL						
J18	PL0	I/O	Z	PU/PD	4	VCC-PL
H17	PL1	I/O	Z	PU/PD	4	VCC-PL
H16	PL2	I/O	Z	PU/PD	4	VCC-PL
G18	PL3	I/O	Z	PU/PD	4	VCC-PL
G17	PL4	I/O	Z	PU/PD	4	VCC-PL
G16	PL5	I/O	Z	PU/PD	4	VCC-PL
F17	PL6	I/O	Z	PU/PD	4	VCC-PL
F16	PL7	I/O	Z	PU/PD	4	VCC-PL
E18	PL8	I/O	Z	PU/PD	4	VCC-PL
E17	PL9	I/O	Z	PU/PD	4	VCC-PL
E16	PL10	I/O	Z	PU/PD	4	VCC-PL
E11	VCC-PL	P	NA	NA	NA	NA
GPIOM						
E2	PM0	I/O	Z	PU/PD	4	VCC-PM
D3	PM1	I/O	Z	PU/PD	4	VCC-PM
D2	PM2	I/O	Z	PU/PD	4	VCC-PM
D1	PM3	I/O	Z	PU/PD	4	VCC-PM
C2	PM4	I/O	Z	PU/PD	4	VCC-PM
E3	PM5	I/O	Z	PU/PD	4	VCC-PM
A4	PM6	I/O, OD	NA	NA	NA	VCC-RTC
C1	PM7	I/O	Z	PU/PD	4	VCC-PM
B1	PM8	I/O	Z	PU/PD	4	VCC-PM
J5	VCC-PM	P	NA	NA	NA	NA
GPION						

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
B10	PN0	I/O	Z	PU/PD	4	VCC-PN
C11	PN1	I/O	Z	PU/PD	4	VCC-PN
C12	PN2	I/O	Z	PU/PD	4	VCC-PN
C13	PN3	I/O	Z	PU/PD	4	VCC-PN
A15	PN4	I/O	Z	PU/PD	4	VCC-PN
B16	PN5	I/O	Z	PU/PD	4	VCC-PN
B17	PN6	I/O	Z	PU/PD	4	VCC-PN
C17	PN7	I/O	Z	PU/PD	4	VCC-PN
C10	PN8	I/O	Z	PU/PD	4	VCC-PN
B11	PN9	I/O	Z	PU/PD	4	VCC-PN
A11	PN10	I/O	Z	PU/PD	4	VCC-PN
B12	PN11	I/O	Z	PU/PD	4	VCC-PN
C15	PN12	I/O	Z	PU/PD	4	VCC-PN
C16	PN13	I/O	Z	PU/PD	4	VCC-PN
A17	PN14	I/O	Z	PU/PD	4	VCC-PN
B18	PN15	I/O	Z	PU/PD	4	VCC-PN
A13	PN16	I/O	Z	PU/PD	4	VCC-PN
C14	PN17	I/O	Z	PU/PD	4	VCC-PN
B14	PN18	I/O	Z	PU/PD	4	VCC-PN
D17	PN19	I/O	Z	PU/PD	4	VCC-PN
C18	PN20	I/O	Z	PU/PD	4	VCC-PN
A9	PN21	I/O	Z	PU/PD	4	VCC-PN
C9	PN22	I/O	Z	PU/PD	4	VCC-PN
B9	PN23	I/O	Z	PU/PD	4	VCC-PN
E10	VCC-PN	P	NA	NA	NA	NA
System						
T8	FEL	I	PU	PU	NA	VCC-IO
B8	RESETN	I/O, OD	PD	NA	NA	VCC-RTC
GPADC						
L18	GPADC0	AI	NA	NA	NA	AVCC
L17	GPADC1	AI	NA	NA	NA	AVCC
L16	GPADC2	AI	NA	NA	NA	AVCC
K17	GPADC3	AI	NA	NA	NA	AVCC
LRADC						
K16	LRADC	AI	NA	NA	NA	AVCC
USB						
U13	USB0-DM	A I/O	NA	NA	NA	VCC-IO
T13	USB0-DP	A I/O	NA	NA	NA	VCC-IO
V12	USB1-DM	A I/O	NA	NA	NA	VCC-IO
U12	USB1-DP	A I/O	NA	NA	NA	VCC-IO
Audio Codec						
M16	MICIN1P	AI	NA	NA	NA	AVCC
M17	MICIN1N	AI	NA	NA	NA	AVCC

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
N17	MICIN2P	AI	NA	NA	NA	AVCC
N18	MICIN2N	AI	NA	NA	NA	AVCC
P16	MICIN3P	AI	NA	NA	NA	AVCC
P17	MICIN3N	AI	NA	NA	NA	AVCC
U17	MICIN4P	AI	NA	NA	NA	AVCC
V17	MICIN4N	AI	NA	NA	NA	AVCC
U16	MICIN5P	AI	NA	NA	NA	AVCC
V16	MICIN5N	AI	NA	NA	NA	AVCC
T15	SPKLP	AO	NA	NA	NA	AVCC
U15	SPKLN	AO	NA	NA	NA	AVCC
U14	SPKRP	AO	NA	NA	NA	AVCC
V14	SPKRN	AO	NA	NA	NA	AVCC
R17	MBIAS	AO	NA	NA	NA	VCC-IO
U18	VRA1	AO	NA	NA	NA	AVCC
T18	VRA2	AO	NA	NA	NA	AVCC
T17	VRP	AO	NA	NA	NA	AVCC
R16	AVCC	P	NA	NA	NA	NA
R18	AGND	G	NA	NA	NA	NA
RTC & PLL						
B7	X32KIN	AI	NA	NA	NA	VCC-RTC
A7	X32KOUT	AO	NA	NA	NA	VCC-RTC
E13	VCC-RTC	P	NA	NA	NA	NA
B4	PLLTEST	AO, OD	NA	NA	NA	VCC-PLL
E14	VCC-PLL	P	NA	NA	NA	NA
DCXO						
C6	DXIN	AI	NA	NA	NA	VCC-PLL
B6	DXOUT	AO	NA	NA	NA	VCC-PLL
A5	REFCLK-OUT	AO	NA	NA	NA	VCC-PLL
Power						
G13	LDO-IN	P	NA	NA	NA	NA
H14	LDOA-OUT	P	NA	NA	NA	NA
J13	LDOB-OUT	P	NA	NA	NA	NA
A2	VDD-CPUFB	P	NA	NA	NA	NA
H6	VCC-IO	P	NA	NA	NA	NA
A3,B3,C3,C4, D4	VDD-CPU	P	NA	NA	NA	NA
E6,E7,E8	VDD-SYS	P	NA	NA	NA	NA
Ground(1)						
A1,A18,B13, B15,B2,B5,C5, C7,C8,D16,E12, E9,F11,F12,F13 ,F14,F5,F6,F7, F8,F9,G11,G12,	GND	G	NA	NA	NA	NA

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
G5,G6,G7,G8, G9,H2,J11,J16, J17,J7,J8,K13, K14,K3,L10,L11 ,L14,L9,M10, M11,M13,M14 ,M3,M5,M7, M8,M9,N10, N11,N13,N14, N16,N5,N6,N7, N8,N9,P13,P14 ,P5,P6,P7,P8, P9,T12,T14, T16,V1,V18						

(1) For R329-N3/R329-S3, the G9, J7, K13 are GND ball; but for R329-N4, the G9, J7, K13 are empty.

4.3. GPIO Multiplex Function

The following table provides a description of the R329 GPIO multiplex function.

NOTE

For each GPIO, Function0 is input function; Function1 is output function.

Table 4-4 GPIO Multiplex Function

Pin Name	GPIO Group	IO Type	Function2	Function3	Function4	Function5	Function6
PB0	GPIOB	I/O	UART2-TX	PWM0	JTAG-MS	LEDC-DO	PB-EINT0
PB1		I/O	UART2-RX	PWM1	JTAG-CK	I2S0-MCLK	PB-EINT1
PB2		I/O	UART2-RTS	PWM2	JTAG-DO	I2S0-LRCK	PB-EINT2
PB3		I/O	UART2-CTS	PWM3	JTAG-DI	I2S0-BCLK	PB-EINT3
PB4		I/O	UART0-TX	PWM4	I2S0-DOUT0	I2S0-DIN1	PB-EINT4
PB5		I/O	UART0-RX	PWM5	I2S0-DOUT1	I2S0-DIN0	PB-EINT5
PB6		I/O	IR-RX	PWM6	I2S0-DOUT2	TWI0-SCK	PB-EINT6
PB7		I/O	IR-TX	PWM7	I2S0-DOUT3	TWI0-SDA	PB-EINT7
PB8		I/O	IR-TX	PWM8	IR-RX	LEDC-DO	PB-EINT8
PC0	GPIOC	I/O	NAND-RB0	SDC0-CLK	SPI0-CS0		
PC1		I/O	NAND-RE	SDC0-CMD	SPI0-MISO		
PC2		I/O	NAND-CE0	SDC0-D2	SPI0-WP		
PC3		I/O	NAND-CLE	SDC0-D1	SPI0-MOSI		
PC4		I/O	NAND-ALE	SDC0-D0	SPI0-CLK		
PC5		I/O	NAND-WE	SDC0-D3	SPI0-HOLD		
PC6		I/O	NAND-DQ0	SDC0-RST			
PC7		I/O	NAND-DQ1			BOOT-SEL	
PF0	GPIOF	I/O	NAND-DQ7	SIM0-VPPEN	JTAG-MS	SDC0-D1	PF-EINT0
PF1		I/O	NAND-DQ6	SIM0-VPPPP	JTAG-DI	SDC0-D0	PF-EINT1
PF2		I/O	NAND-DQ5	SIM0-PWREN	UART0-TX	SDC0-CLK	PF-EINT2
PF3		I/O	NAND-DQ4	SIM0-CLK	JTAG-DO	SDC0-CMD	PF-EINT3
PF4		I/O	NAND-DQS	SIM0-DATA	UART0-RX	SDC0-D3	PF-EINT4
PF5		I/O	NAND-DQ3	SIM0-RST	JTAG-CK	SDC0-D2	PF-EINT5

Pin Name	GPIO Group	IO Type	Function2	Function3	Function4	Function5	Function6
PF6		I/O	NAND-DQ2	SIM0-DET		OWA-OUT	PF-EINT6
PG0	GPIOG	I/O	SDC1-CLK	SDC1-D2	SDC1-D2		PG-EINT0
PG1		I/O	SDC1-CMD	SDC1-D3	SDC1-CLK		PG-EINT1
PG2		I/O	SDC1-D0	SDC1-CMD	SDC1-D3	PLL-LOCK-DBG	PG-EINT2
PG3		I/O	SDC1-D1	SDC1-CLK	SDC1-D1		PG-EINT3
PG4		I/O	SDC1-D2	SDC1-D0	SDC1-D0		PG-EINT4
PG5		I/O	SDC1-D3	SDC1-D1	SDC1-CMD		PG-EINT5
PG6		I/O	UART1-TX	TWI0-SCK			PG-EINT6
PG7		I/O	UART1-RX	TWI0-SDA			PG-EINT7
PG8		I/O	UART1-RTS	TWI1-SCK		SPI1-HOLD/ DBI-DCX/ DBI-WRX	PG-EINT8
PG9		I/O	UART1-CTS	TWI1-SDA		SPI1-WP/DBI-TE	PG-EINT9
PG10		I/O		I2S1-MCLK	LEDC-DO		PG-EINT10
PG11		I/O	UART3-TX	I2S1-LRCK		SPI1-CS/DBI-CSX	PG-EINT11
PG12		I/O	UART3-RX	I2S1-BCLK		SPI1-CLK/ DBI-SCLK	PG-EINT12
PG13		I/O	UART3-RTS	I2S1-DOUT0	I2S1-DIN1	SPI1-MOSI/ DBI-SDO	PG-EINT13
PG14		I/O	UART3-CTS	I2S1-DOUT1	I2S1-DIN0	SPI1-MISO/ DBI-SDI/ DBI-TE/ DBI-DCX	PG-EINT14
PH0	GPIOH	I/O	TWI0-SCK	UART0-TX	SPI1-CS/DBI-CSX	PWM0	PH-EINT0
PH1		I/O	TWI0-SDA	UART0-RX	SPI1-CLK/ DBI-SCLK	PWM1	PH-EINT1
PH2		I/O	TWI1-SCK	LEDC-DO	SPI1-MOSI/ DBI-SDO	IR-RX	PH-EINT2
PH3		I/O	TWI1-SDA	OWA-OUT	SPI1-MISO/ DBI-SDI/ DBI-TE/ DBI-DCX	IR-TX	PH-EINT3
PH4		I/O	UART3-TX	SPI1-CS/ DBI-CSX	SPI1-HOLD/ DBI-DCX/ DBI-WRX	PWM2	PH-EINT4
PH5		I/O	UART3-RX	SPI1-CLK/ DBI-SCLK	SPI1-WP/DBI-TE	PWM3	PH-EINT5
PH6		I/O	UART3-RTS	SPI1-MOSI/ DBI-SDO	TWI0-SCK	PWM4	PH-EINT6
PH7		I/O	UART3-CTS	SPI1-MISO/ DBI-SDI/ DBI-TE/DBI-DCX	TWI0-SDA	PWM5	PH-EINT7
PH8		I/O	TWI1-SCK	SPI1-HOLD/ DBI-DCX/ DBI-WRX		IR-RX	PH-EINT8
PH9		I/O	TWI1-SDA	SPI1-WP/DBI-TE	LEDC-DO	IR-TX	PH-EINT9
PL0	GPIOL	I/O	S-I2S0-LRCK		S-DMIC-DATA3	S-PWM0	PL-EINT0
PL1		I/O	S-I2S0-BCLK		S-DMIC-DATA2	S-PWM1	PL-EINT1
PL2		I/O	S-I2S0-DOUT0	S-I2S0-DIN1	S-DMIC-DATA1	S-PWM2	PL-EINT2
PL3		I/O	S-I2S0-DOUT1	S-I2S0-DIN0	S-DMIC-DATA0	S-TWI0-SDA	PL-EINT3
PL4		I/O	S-I2S0-MCLK	S-IR-RX	S-DMIC-CLK	S-TWI0-SCK	PL-EINT4
PL5		I/O	S-TWI0-SDA			S-PWM3	PL-EINT5
PL6		I/O	S-TWI0-SCK			S-PWM4	PL-EINT6
PL7		I/O	S-IR-RX		X32KFOUT	S-PWM5	PL-EINT7

Pin Name	GPIO Group	IO Type	Function2	Function3	Function4	Function5	Function6
PL8		I/O	S-UART0-TX	S-TWI0-SDA	S-IR-RX		PL-EINT8
PL9		I/O	S-UART0-RX	S-TWI0-SCK	X32KFOUT		PL-EINT9
PL10		I/O					PL-EINT10
PM0	GPIOM	I/O	S-UART0-TX	S-JTAG-MS			PM-EINT0
PM1		I/O	S-UART0-RX	S-JTAG-CK			PM-EINT1
PM2		I/O		S-JTAG-DO	S-TWI0-SDA	S-IR-RX	PM-EINT2
PM3		I/O	S-TWI0-SDA	S-IR-RX			PM-EINT3
PM4		I/O	S-TWI0-SCK				PM-EINT4
PM5		I/O	X32KFOUT	S-JTAG-DI	S-TWI0-SCK		PM-EINT5
PM6		I/O, OD	NMI	S-IR-RX	X32KFOUT		PM-EINT6
PM7		I/O	S-IR-RX	X32KFOUT			PM-EINT7
PM8		I/O					PM-EINT8
PN0	GPION	I/O					PN-EINT0
PN1		I/O		MDC			PN-EINT1
PN2		I/O		MDIO			PN-EINT2
PN3		I/O		RGMII-TXD3			PN-EINT3
PN4		I/O		RGMII-TXCK/ RMII-TXCK			PN-EINT4
PN5		I/O		RGMII-RXD2			PN-EINT5
PN6		I/O		RGMII-RXD0/ RMII-RXD0			PN-EINT6
PN7		I/O		RGMII-RXCK			PN-EINT7
PN8		I/O		RMII-RXER			PN-EINT8
PN9		I/O		RGMII-TXCTL/ RMII-TXEN			PN-EINT9
PN10		I/O		RGMII-RXD3			PN-EINT10
PN11		I/O		RGMII-RXD1/ RMII-RXD1			PN-EINT11
PN12		I/O		RGMII-RXCTL/ RMII-CRS-DV			PN-EINT12
PN13		I/O		RGMII-TXD2			PN-EINT13
PN14		I/O		RGMII-TXD1/ RMII-TXD1			PN-EINT14
PN15		I/O		RGMII-TXD0/ RMII-TXD0			PN-EINT15
PN16		I/O		EPHY-25M			PN-EINT16
PN17		I/O		RGMII-CLKIN			PN-EINT17
PN18		I/O					PN-EINT18
PN19		I/O					PN-EINT19
PN20		I/O					PN-EINT20
PN21		I/O					PN-EINT21
PN22		I/O					PN-EINT22
PN23		I/O					PN-EINT23

4.4. Detailed Signal Description

Table 4-5 shows the detailed function description of every signal based on the different interface.

[1].**Signal Name**: The name of every signal.

[2].**Description**: The detailed function description of every signal.

[3].**Type**: Denotes the signal direction:

I (Input),

O (Output),

I/O (Input/Output),
OD (Open-Drain),
A (Analog),
AI (Analog Input),
AO (Analog Output),
A I/O (Analog Input/Output),
P (Power),
G (Ground)

Table 4-5 Detailed Signal Description

Signal Name[1]	Description[2]	Type[3]
DRAM		
VCC-DRAM	DRAM Power Supply	P
System Control		
NMI	Non-maskable Interrupt	I/O, OD
FEL	Boot Select 0: Mandatory upgrade process 1: Try media boot process	I
BOOT-SEL	Boot Media Select	I
RESETN	Reset Signal (low active)	I/O, OD
Clock		
X32KIN	Clock Input of 32.768 kHz Crystal	AI
X32KOUT	Clock Output of 32.768 kHz Crystal	AO
X32KFOUT	32.768 kHz Clock Fanout Provides low frequency clock for external devices	AO
VCC-RTC	RTC Power	P
PLLTEST	PLL Test	AO, OD
VCC-PLL	PLL Power Supply	P
DCXO		
REFCLK-OUT	Digital Compensated Crystal Oscillator Clock Fanout	AO
DXIN	Digital Compensated Crystal Oscillator Input	AI
DXOUT	Digital Compensated Crystal Oscillator Output	AO
USB		
USB0-DM	USB DRD Data Signal DM	A I/O
USB0-DP	USB DRD Data Signal DP	A I/O
USB1-DM	USB HOST Data Signal DM	A I/O
USB1-DP	USB HOST Data Signal DP	A I/O
GPADC		
GPADC0	General Purpose ADC Input Channel 0	AI
GPADC1	General Purpose ADC Input Channel 1	AI
GPADC2	General Purpose ADC Input Channel 2	AI
GPADC3	General Purpose ADC Input Channel 3	AI
LRADC		
LRADC	Low Rate ADC Input Channel	AI
AUDIO CODEC		
SPKLP	Left Speaker Positive Output	AO
SPKLN	Left Speaker Negative Output	AO

Signal Name[1]	Description[2]	Type[3]
SPKRP	Right Speaker Positive Output	AO
SPKRN	Right Speaker Negative Output	AO
MBIAS	Master Analog Microphone Bias Voltage Output	AO
MICIN1P	Microphone Positive Input 1	AI
MICIN1N	Microphone Negative Input 1	AI
MICIN2P	Microphone Positive Input 2	AI
MICIN2N	Microphone Negative Input 2	AI
MICIN3P	Microphone Positive Input 3	AI
MICIN3N	Microphone Negative Input 3	AI
MICIN4P	Microphone Positive Input 4	AI
MICIN4N	Microphone Negative Input 4	AI
MICIN5P	Microphone Positive Input 5	AI
MICIN5N	Microphone Negative Input 5	AI
VRA1	Reference Voltage	AO
VRA2	Reference Voltage	AO
VRP	Reference Voltage	AO
AVCC	Power Supply for Analog Part	P
AGND	Analog Ground	G
SMHC		
SDC0-CMD	Command Signal for SD Card or eMMC	I/O, OD
SDC0-CLK	Clock for SD Card or eMMC	O
SDC0-D[3:0]	Data Input and Output for SD Card or eMMC	I/O
SDC0-RST	Reset for SD Card or eMMC	O
SDC1-CMD	Command Signal for SDIO WIFI	I/O, OD
SDC1-CLK	Clock for SDIO WIFI	O
SDC1-D[3:0]	Data Input and Output for SDIO WIFI	I/O
NAND Flash		
NAND-WE	Write Enable	O
NAND-RE	Read Enable	O
NAND-ALE	Address Latch Enable (high active)	O
NAND-CLE	Command Latch Enable (high active)	O
NAND-CE0	Chip Enable (low active)	O
NAND-RB0	Ready/busy (low active)	I
NAND-DQS	Data Strobe	I/O
NAND-DQ[7:0]	Data Input/Output	I/O
I2S/PCM		
I2S0-MCLK	I2S0 Master Clock	O
I2S0-LRCK	I2S0/PCM0 Sample Rate Clock/Sync	I/O
I2S0-BCLK	I2S0/PCM0 Sample Rate Clock	I/O
I2S0-DOUT[3:0]	I2S0/PCM0 Serial Data Output Channel [3:0]	O
I2S0-DIN[1:0]	I2S0/PCM0 Serial Data Input Channel [1:0]	I
I2S1-MCLK	I2S1 Master Clock	O
I2S1-LRCK	I2S1/PCM1 Sample Rate Clock/Sync	I/O
I2S1-BCLK	I2S1/PCM1 Sample Rate Clock	I/O

Signal Name[1]	Description[2]	Type[3]
I2S1-DOUT[1:0]	I2S1/PCM1 Serial Data Output Channel [1:0]	O
I2S1-DIN[1:0]	I2S1/PCM1 Serial Data Input Channel [1:0]	I
S-I2S0-MCLK	S-I2S0 Master Clock	O
S-I2S0-LRCK	S-I2S0/PCM0 Sample Rate Clock/Sync	I/O
S-I2S0-BCLK	S-I2S0/PCM0 Sample Rate Clock	I/O
S-I2S0-DOUT[1:0]	S-I2S0/PCM0 Serial Data Output Channel [1:0]	O
S-I2S0-DIN[1:0]	S-I2S0/PCM0 Serial Data Input Channel [1:0]	I
DMIC		
S-DMIC-CLK	Digital Microphone Clock Output	O
S-DMIC-DATA[3:0]	Digital Microphone Data Input	I
EMAC		
RGMII-RXD3	RGMII Receive Data3	I
RGMII-RXD2	RGMII Receive Data2	I
RGMII-RXD1/RMII-RXD1	RGMII/RMII Receive Data1	I
RGMII-RXD0/RMII-RXD0	RGMII/RMII Receive Data0	I
RGMII-RXCK	RGMII Receive Clock	I
RGMII-RXCTL/RMII-CRS-DV	RGMII Receive Control/RMII Carrier Sense Receive Data Valid	I
RMII-RXER	RMII Receive Error	I
RGMII-TXD3	RGMII Transmit Data3	O
RGMII-TXD2	RGMII Transmit Data2	O
RGMII-TXD1/RMII-TXD1	RGMII/RMII Transmit Data1	O
RGMII-TXD0/RMII-TXD0	RGMII/RMII Transmit Data0	O
RGMII-TXCK/RMII-TXCK	RGMII/RMII Transmit Clock For RGMII, IO type is output; For RMII, IO type is input	I/O
RGMII-TXCTL/RMII-TXEN	RGMII Transmit Control/RMII Transmit Enable	O
RGMII-CLKIN	RGMII Transmit Clock from External	I
MDC	RGMII/RMII Management Data Clock	O
MDIO	RGMII/RMII Management Data Input/Output	I/O
EPHY-25M	25MHz Output for EMAC PHY	O
OWA		
OWA-OUT	One Wire Audio Output	O
LEDC		
LEDC-DO	Intelligent Control LED Signal Output	O
Interrupt		
PB-EINT[8:0]	GPIO B Interrupt	I
PF-EINT[6:0]	GPIO F Interrupt	I
PG-EINT[14:0]	GPIO G Interrupt	I
PH-EINT[8:0]	GPIO H Interrupt	I
PL-EINT[10:0]	GPIO L Interrupt	I
PM-EINT[9:0]	GPIO M Interrupt	I
PN-EINT[23:0]	GPIO N Interrupt	I
CIR Receiver		
IR-RX	Consumer Infrared Receiver	I

Signal Name[1]	Description[2]	Type[3]
S-IR-RX	Consumer Infrared Receiver	I
CIR Transmitter		
IR-TX	Consumer Infrared Transmitter	O
PWM		
PWM[8:0]	Pulse Width Modulation Output Channel [8:0]	I/O
S-PWM[5:0]	Pulse Width Modulation Output Channel [5:0]	I/O
Smart Card		
SIM-PWREN	Smart Card Power Enable	O
SIM-VPPEN	Smart Card Program Voltage Enable	O
SIM-VPPPP	Smart Card Program Control	O
SIM-CLK	Smart Card Clock	O
SIM-DATA	Smart Card Data	I/O
SIM-RST	Smart Card Reset	O
SIM-DET	Smart Card Detect	I
SPI&SPI_DBI		
SPI0-CS	SPI0 Chip Select Signal, Low Active	I/O
SPI0-CLK	SPI0 Clock Signal Provides serial interface timing.	I/O
SPI0-MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0-MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI0-WP	SPI0 Write Protect, Low Active Protects the memory area against all program or erase instructions. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode.	I/O
SPI0-HOLD	SPI0 Hold Signal Pauses any serial communication with the device without deselecting or resetting it. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode.	I/O
SPI1-CS	SPI1 Chip Select Signal, Low Active	I/O
SPI1-CLK	SPI1 Clock Signal Provides serial interface timing.	I/O
SPI1-MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1-MISO	SPI1 Master Data In, Slave Data Out	I/O
SPI1-WP	SPI1 Write Protect, Low Active Protects the memory area against all program or erase instructions. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode.	I/O
SPI1-HOLD	SPI1 Hold Signal Pauses any serial communication with the device without resetting it. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode.	I/O
DBI-CSX	Chip Select Signal, Low Active	I/O
DBI-SCLK	Serial Clock Signal	I/O
DBI-SDO	Data Output Signal	I/O
DBI-SDI	Data Input Signal	I/O

Signal Name[1]	Description[2]	Type[3]
	The data is sampled on the rising edge and the falling edge	
DBI-TE	Tearing Effect Input It is used to capture the external TE signal edge. The rising and falling edge is configurable.	I/O
DBI-DCX	DCX pin is the select output signal of data and command. DCX = 0: register command; DCX = 1: data or parameter.	I/O
DBI-WRX	When DBI operates in dual data lane format, the RGB666 format 2 can use WRX to transfer data	I/O
UART		
UART0-TX	UART0 Data Transmit	O
UART0-RX	UART0 Data Receive	I
UART1-TX	UART1 Data Transmit	O
UART1-RX	UART1 Data Receive	I
UART1-CTS	UART1 Data Clear to Send	I
UART1-RTS	UART1 Data Request to Send	O
UART2-TX	UART2 Data Transmit	O
UART2-RX	UART2 Data Receive	I
UART2-CTS	UART2 Data Clear to Send	I
UART2-RTS	UART2 Data Request to Send	O
UART3-TX	UART3 Data Transmit	O
UART3-RX	UART3 Data Receive	I
UART3-CTS	UART3 Data Clear to Send	I
UART3-RTS	UART3 Data Request to Send	O
S-UART0-TX	S-UART0 Data Transmit	O
S-UART0-RX	S-UART0 Data Receive	I
TWI		
TWI0-SCK	TWI0 Serial Clock Signal	I/O
TWI0-SDA	TWI0 Serial Data Signal	I/O
TWI1-SCK	TWI1 Serial Clock Signal	I/O
TWI1-SDA	TWI1 Serial Data Signal	I/O
S-TWI0-SCK	S-TWI0 Serial Clock Signal	I/O
S-TWI0-SDA	S-TWI0 Serial Data Signal	I/O
JTAG		
JTAG-MS	JTAG Mode Select	I
JTAG-CK	JTAG Clock Signal	I
JTAG-DO	JTAG Data Output	O
JTAG-DI	JTAG Data Input	I
S-JTAG-MS	S-JTAG Mode Select	I
S-JTAG-CK	S-JTAG Clock Signal	I
S-JTAG-DO	S-JTAG Data Output	O
S-JTAG-DI	S-JTAG Data Input	I

5. Electrical Characteristics

5.1. Parameter Conditions

5.1.1. Minimum and Maximum Values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage, and frequencies by tests in production on 100% of the devices with ambient temperature at Ta = 25 °C and Ta = Ta max.

Data based on characterization results, design simulation, and/or technology characteristics are indicated in the table footnotes and are not tested in production.

5.1.2. Typical Values

Unless otherwise specified, the typical data are based on Ta = 25 °C. They are given only as design guidelines.

5.1.3. Temperature Definitions

- Ambient Temperature— the temperature of the surrounding environment.
- Junction Temperature— the hottest temperature of the silicon chip inside the package.
- Absolute Maximum Junction Temperature— the temperature beyond which damage occurs to the device. The device may not function or meet expected performance at this temperature.
- Recommended Operating Temperature— the junction temperature at which the device operates continuously at the designated performance over the designed lifetime. The reliability of the device may be degraded if the device operates above this temperature. Some devices will not function electrically above this temperature.

5.2. Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Table 5-1 specifies the absolute maximum ratings.

CAUTION

Stresses beyond those listed under Table 5-1 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Section 5.3, *Recommended Operating Conditions*, is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 5-1 Absolute Maximum Ratings

Symbol	Parameter	Min(1)	Max(1)	Unit
AVCC	Power Supply for Analog Part	-0.3	2.16	V
VCC-PC	Digital GPIO C Power	-0.3	3.96	V
VCC-PF	Digital GPIO F Power	-0.3	3.96	V
VCC-PG	Digital GPIO G Power	-0.3	3.96	V
VCC-PL	Digital GPIO L Power	-0.3	3.96	V
VCC-PM	Digital GPIO M Power	-0.3	3.96	V
VCC-PN	Digital GPIO N Power	-0.3	3.96	V
VCC-IO	Power Supply for 3.3 V Digital Part	-0.3	3.96	V

Symbol	Parameter		Min(1)	Max(1)	Unit
VCC-RTC	Power Supply for RTC		-0.3	2.16	V
VCC-PLL	Power Supply for System PLL		-0.3	2.16	V
VCC-DRAM	Power Supply for DRAM		-0.3	1.8	V
VDD-CPU	Power Supply for CPU		-0.3	1.3	V
VDD-SYS	Power Supply for System		-0.3	1.3	V
LDO-IN	Internal LDOA/B Input Voltage		-0.3	3.96	V
LDOA-OUT	Internal LDOA Output Voltage for Analog Device and IO		-0.3	2.16	V
LDOB-OUT	Internal LDOB Output Voltage for VCC-DRAM		-0.3	2.16	V
T_{STG}	Storage Temperature		-40	150	°C
Tj	Working Junction Temperature		-40	125	°C
V_{ESD}	Electrostatic Discharge(2)	Human Body Model(HBM)(3)	-2000	2000	V
		Charged Device Model(CDM)(4)	-500	500	V
$I_{Latch-up}$	Latch-up I-test performance current-pulse injection on each IO pin(5)		Pass		
	Latch-up over-voltage performance voltage injection on each IO pin(6)		Pass		

(1) The min/max voltages of power rails are guaranteed by design, not tested in production.
(2) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the devices.
(3) Level listed above is the passing level per ESDA/JEDEC JS-001-2017.
(4) Level listed above is the passing level per ESDA/JEDEC JS-002-2018.
(5) Based on JESD78E; each device is tested with IO pin injection of ±200 mA at room temperature.
(6) Based on JESD78E; each device is tested with a stress voltage of 1.5 x Vddmax at room temperature.

5.3. Recommended Operating Conditions

Table 5-2 describes operating conditions of the R329.

NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 5-2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature (when VCC-DRAM uses external power)	-20	-	85	°C
	Ambient Operating Temperature (when VCC-DRAM uses internal LDO)	-20	-	70	°C
Tj	Working Junction Temperature Range	-20	-	110(1)	°C
AVCC	Power Supply for Analog Part	1.764	1.8	1.836	V
VCC-PC	Digital GPIO C Power 1.8 V voltage 3.3 V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PF	Digital GPIO F Power 1.8 V voltage 3.3 V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PG	Digital GPIO G Power 1.8 V voltage 3.3 V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V

Symbol	Parameter	Min	Typ	Max	Unit
VCC-PL	Digital GPIO L Power 3.3 V voltage	2.97	3.3	3.63	V
VCC-PM	Digital GPIO M Power 1.8 V voltage 3.3 V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PN	Digital GPIO N Power 1.8 V voltage 3.3 V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-IO	Power Supply for Digital Part 3.3 V voltage	3.135	3.3	3.465	V
VCC-RTC	Power Supply for RTC	1.71	1.8	1.89	V
VCC-PLL	Power Supply for System PLL	1.62	1.8	1.98	V
VCC-DRAM	Power Supply for DRAM IO and DDR3	1.425	1.5	1.575	V
VDD-CPU	Power Supply for CPU(2)	0.9	1.0	1.1	V
VDD-SYS	Power Supply for System(3)	0.81	0.9	1.0	V
LDO-IN	Internal LDOA/B Input Voltage	2.4	3.3	3.6	V
LDOA-OUT	Internal LDOA Output Voltage for Analog Device and IO	1.746	1.8	1.854	V
LDOB-OUT	Internal LDOB Output Voltage for VCC-DRAM	1.31 1.455 1.746	1.35(4) 1.5 1.8	1.39 1.545 1.854	V

(1). The chip junction temperature in normal working condition should be less than or equal to the maximum junction temperature in Table 5-2.

(2). The voltage of the CPU is the lowest voltage of the corresponding frequency, and the highest voltage does not exceed 1.2 V.

(3). To ensure the performance of DSP/AIPU/DRAM, the VDD-SYS cannot be less than 0.87 V. When the frequency of the DSP is less than 100 MHz, the AIPU/DRAM enters the standby mode, the VDD-SYS can be down to 0.81 V to reduce the power consumption.

(4). The default voltage of LDOB-OUT is 1.35 V.

5.4. Power Consumption Parameters

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in the following table.

NOTE

Since the data presented in the following table is based on empirical measurements on small sample size, the results presented are not guaranteed.

Table 5-3 Power Consumption Parameters

Parameter	Sub Parameter	Power Supply	Condition	Typ	Max	Unit
Internal Core Power	CPU	VDD-CPU	1.1 V, 1512 MHz	-	800	mA
	SYS	VDD-SYS	0.9 V	-	500	mA
GPIO Power		VCC-IO	For GPIO, voltage 3.3 V, N=19	-	114	mA
		VCC-PC	For GPIO, voltage 3.3 V, N=8	-	48	mA

Parameter	Sub Parameter	Power Supply	Condition	Typ	Max	Unit
		VCC-PF	For GPIO, voltage 3.3 V, N=7	-	42	mA
		VCC-PG	For GPIO, voltage 3.3 V, N=15	-	90	mA
		VCC-PL	For GPIO, voltage 3.3 V, N=11	-	66	mA
		VCC-PM	For GPIO, voltage 3.3 V, N=9	-	54	mA
		VCC-PN	For GPIO, voltage 3.3 V, N=24	-	144	mA
Memory I/O Power		VCC-DRAM	1.5 V, 774 MHz, disable ODT, 2500 MB/s data width	-	250	mA
24 MHz Crystal Oscillator		VCC-PLL	1.8 V	-	3	mA
RTC Power		VCC-RTC	1.8 V	-	1	mA
ADC Analog Power		AVCC	1.8 V, 48 kHz sample rate, 5-chs are enabled	-	15	mA
DAC Analog Power		AVCC	1.8 V, 48 kHz sample rate, 2-chs are enabled	-	3	mA
USB Power		VCC-IO	2 x USB, 3.3 V	-	50	mA

General equation for estimated, maximum power consumption of an group IO power supply:
Imax = N x 6 mA
Where:
N—Number of IO pins supplied by the power line.
The maximum power consumption for each IO is 6 mA.

5.5. DC Electrical Characteristics

Table 5-4 summarizes the DC electrical characteristics of the R329. For the interfaces of GPIO function port, refer to the DC parameters in Table 5-4 unless otherwise stated.

Table 5-4 DC Electrical Characteristics

(VCC-IO/VCC-PC/VCC-PF/VCC-PG/VCC-PL/VCC-PM/VCC-PN)

Symbol	Parameter		Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage		0.7 * VCC-IO	-	VCC-IO + 0.3	V
V_{IL}	Low-Level Input Voltage		-0.3	-	0.3 * VCC-IO	V
R_{PU}	Input Pull-up Resistance	PC0 to PC7, PF3, PF6	12	15	18	kΩ
		PG0 to PG5	26	33	40	kΩ
		Other GPIOs (except PM6)	80	100	120	kΩ
R_{PD}	Input Pull-down Resistance	PC0 to PC7, PF3, PF6	12	15	18	kΩ
		PG0 to PG5	26	33	40	kΩ
		Other GPIOs (except PM6)	80	100	120	kΩ
I_{IH}	High-Level Input Current		-	-	10	uA
I_{IL}	Low-Level Input Current		-	-	10	uA
V_{OH}	High-Level Output Voltage		VCC-IO – 0.3	-	VCC-IO	V
V_{OL}	Low-Level Output Voltage		0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current		-10	-	10	uA
C_{IN}	Input Capacitance		-	-	5	pF
C_{OUT}	Output Capacitance		-	-	5	pF

5.6. SDIO Electrical Characteristics

The SDIO electrical parameters are related to different supply voltage.

Figure 5-1 SDIO Voltage Waveform

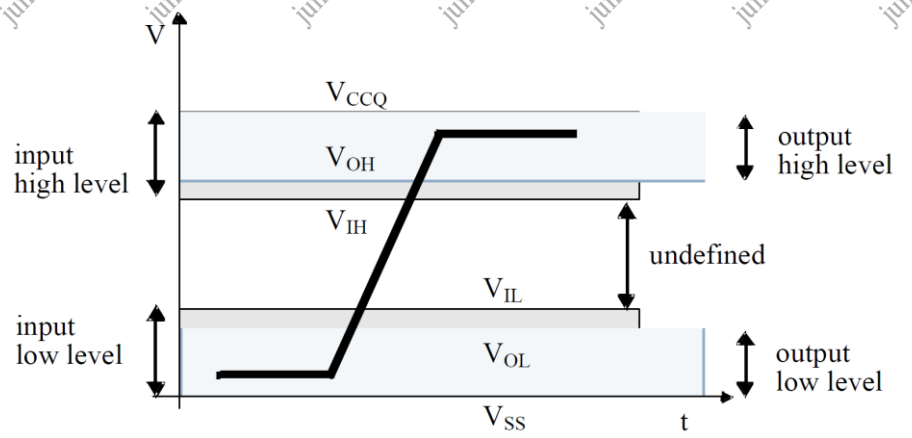


Table 5-5 shows 3.3 V SDIO electrical parameters.

Table 5-5 3.3 V SDIO Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	2.7		3.6	V
V_{OH}	Output high-level voltage	0.75 * V_{CCQ}	-	-	V
V_{OL}	Output low-level voltage	-	-	0.125 * V_{CCQ}	V
V_{IH}	Input high-level voltage	0.625 * V_{CCQ}	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} – 0.3	-	0.25 * V_{CCQ}	V

Table 5-6 shows 1.8 V SDIO electrical parameters.

Table 5-6 1.8 V SDIO Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	1.7		1.95	V
V_{OH}	Output high-level voltage	V_{CCQ} – 0.45	-	-	V
V_{OL}	Output low-level voltage	-	-	0.45	V
V_{IH}	Input high-level voltage	0.625 * V_{CCQ} (1)	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} – 0.3	-	0.35 * V_{CCQ} (2)	V
(1).0.7 * V_{CCQ} for MMC4.3 or lower. (2).0.3 * V_{CCQ} for MMC4.3 or lower.					

5.7. GPADC Electrical Characteristics

The GPADC contains a 4-ch analog-to-digital (ADC) converter. The GPADC is a type of successive approximation register (SAR) converter. Table 5-7 lists GPADC electrical characteristics.

Table 5-7 GPADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	12	-	bits
Full-scale Input Range	0	-	AVCC	V

Parameter	Min	Typ	Max	Unit
Quantizing Error	-	8	-	LSB
Clock Frequency	-	-	1	MHz
Conversion Time	-	14	-	ADC Clock Cycles

5.8. LRADC Electrical Characteristics

The LRADC is a 6-bit resolution ADC for key applications. The LRADC can work up to 2 kHz conversion rate. Table 5-8 lists LRADC electrical characteristics.

Table 5-8 LRADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	6	-	bits
Full-scale Input Range	0	-	LEVELB(1)	V
Quantizing Error	-	2	-	LSB
Clock Frequency	-	-	2	kHz
Conversion Time	-	6	-	ADC Clock Cycles
(1) The maximum value of LEVELB is 1.266 V. For details, see the register description of LRADC in *R329_User_Manual*.				

5.9. Audio Codec Electrical Characteristics

Test Conditions

VDD-SYS = 0.9 V, AVCC = 1.8 V, Ta = 25 °C, 1 kHz sinusoid signal, DAC fs = 48 kHz, ADC fs = 16 kHz, Input gain = 0 dB, 16-bit audio data unless otherwise stated.

Table 5-9 Audio Codec Typical Performance Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DAC Path	**DAC to SPKOUTLP/N or SPKOUTRP/N**					
	Full-scale	0dBFS 1 kHz	-	1.1	-	Vrms
	SNR(A-weighted)	0data	-	100	-	dB
	THD+N	0dBFS 1 kHz	-	-84	-	dB
	Crosstalk	R_0dB_L_0data 1 kHz L_0dB_R_0data 1 kHz	-	-105	-	dB
ADC Path	**MIC1 via ADC1 or MIC2 via ADC2**					
	Output Level	MICP=3.3Vpp/2, MICN=3.3Vpp/2, 1 kHz, 0 dB Gain	-	883	-	mFFS
	SNR(A-weighted)		-	94	-	dB
	THD+N		-	-89	-	dB
	Output Level	MICP=3.3Vpp/2, MICN=3.3Vpp/2, 1 kHz, 6 dB Gain	-	883	-	mFFS
	SNR(A-weighted)		-	94	-	dB
	THD+N		-	-89	-	dB
	Output Level	MICP=3.3Vpp/2, MICN=3.3Vpp/2, 1 kHz, 12 dB Gain	-	883	-	mFFS
	SNR(A-weighted)		-	93	-	dB
	THD+N		-	-88	-	dB
	Output Level	MICP=3.3Vpp/2, MICN=3.3Vpp/2, 1 kHz, 18 dB Gain	-	883	-	mFFS
	SNR(A-weighted)		-	92	-	dB
	THD+N		-	-85	-	dB
	Output Level	MICP=3.3Vpp/2, MICN=3.3Vpp/2, 1 kHz, 24 dB Gain	-	883	-	mFFS
	SNR(A-weighted)		-	88	-	dB
	THD+N		-	-81	-	dB
	Output Level	MICP=3.3Vpp/2, MICN=3.3Vpp/2, 1 kHz, 30 dB Gain	-	883	-	mFFS
	SNR(A-weighted)		-	84	-	dB

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	THD+N		-	-75	-	dB
	Output Level	MICP=3.3Vpp/2, MICN=3.3Vpp/2, 1 kHz, 36 dB Gain	-	883	-	mFFS
	SNR(A-weighted)		-	75	-	dB
	THD+N		-	-70	-	dB
MBIAS	Current	-	-	2.0	-	mA
	Voltage	-	1.8	2.0	2.55	V
	Noise	20 Hz to 20 kHz	-	7	-	uV

5.10. External Clock Source Characteristics

5.10.1. High-speed Crystal Resonator Characteristics

The high-speed external clock can be supplied with a 24 MHz crystal resonator (oscillation mode). The 24 MHz crystal resonator provides 24 MHz reference clock which is connected to the DXIN and DXOUT terminals.

Table 5-10 High-speed 24 MHz Crystal Circuit Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{X24M_IN}	Crystal parallel resonance frequency	-	24	-	MHz
	Crystal frequency stability and tolerance at 25 °C (1)	-50	-	+50	ppm
	Oscillation mode	Fundamental			-
C_{shunt}	Shunt capacitance (2)	-	6.5	-	pF

1. The 50 ppm frequency stability and tolerance can meet the requirement of R329. We recommend selecting 20 ppm crystal devices. If the REFCLK-OUT (24 MHz fanout) is used for Wi-Fi chip, the crystal uses the recommended specification or the specified model for Wi-Fi chip.
2. The 6.5 pF is only a simulation value. The crystal shunt capacitance (C_0) is given by the crystal manufacturer.

Table 5-11 Crystal Circuit Parameters

Symbol	Parameter
C_1	C_1 capacitance
C_2	C_2 capacitance
C_L	Equivalent load capacitance, specified by the crystal manufacturer
C_0	Crystal shunt capacitance, specified by the crystal manufacturer
C_{shunt}	Total shunt capacitance

Frequency stability mainly requires that the total load capacitance (C_L) be constant. The crystal manufacturer typically specifies a total load capacitance which is the series combination of C_1, C_2, and C_{shunt}.

The total load capacitance is $C_L = [(C_1 * C_2)/(C_1 + C_2)] + C_{shunt}$.

- C_1 and C_2 represent the total capacitance of the respective PCB trace, load capacitor, and other components (excluding the crystal) connected to each crystal terminal. C_1 and C_2 are usually the same size.
- C_{shunt} is the crystal shunt capacitance (C_0) plus any mutual capacitance (C_{pkg} + C_{PCB}) seen across the DXIN and DXOUT signals.

In the application, the crystal resonator and the load capacitors must be placed close to the oscillator pins in order to minimize output distortion and the startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics.

NOTE

For the above capacitances of 24 MHz crystal circuit, refer to the capacitance recommended in the *R329_Schematic_Diagram*.

5.10.2. Low-speed Crystal Resonator Characteristics

The R329 contains an RC oscillation circuit that generates a 32.768 kHz clock, meanwhile, the DCXO module can calibrate the RC oscillation circuit regularly. If the product does not have a high requirement for the accuracy of the system clock, the external 32.768 kHz crystal circuit can be omitted and the internal RC oscillation circuit can be adopted, meanwhile, the relevant clock configuration needs to be turned on by the software.

The R329 also can connect to a 32.768 kHz crystal resonator (oscillation mode). The 32.768 kHz crystal resonator provides 32.768 kHz reference clock which is connected to the X32KIN and X32KOUT terminals. In the application, the crystal resonator and the load capacitors must be placed close to the oscillator pins to minimize output distortion and the startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics.

Table 5-12 Low-speed 32.768 kHz Crystal Circuit Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{X32K_IN}	Crystal parallel resonance frequency	-	32.768	-	kHz
	Crystal frequency stability and tolerance at 25 °C (1)	-	-	-	ppm
	Oscillation mode	Fundamental			-
C_{shunt}	Shunt capacitance (2)	-	1.1	-	pF

1. The R329 has no requirement for the frequency stability and tolerance of 32.768 kHz crystal. If the actual product has requirement for the accuracy of timing function, the 20 ppm stability and tolerance is recommended.
2. The 1.1 pF is only a simulation value. The crystal shunt capacitance (C_0) is given by the crystal manufacturer.

NOTE

For capacitances of 32.768 kHz crystal circuit, refer to the capacitance recommended in the *R329_Schematic_Diagram*.

5.11. Output Clock Characteristics

The X32KFOUT signal can output 32.768 kHz clock. Table 5-13 lists the output clock characteristics.

Table 5-13 X32KFOUT Output Clock Characteristics

Parameter	Specification	Unit
Input Source	24 MHz crystal or 32.768 kHz crystal	-
Nominal Output Frequency	32.768	kHz
Frequency Accuracy	The output frequency accuracy is related to the accuracy of external crystal.	ppm
Duty Cycle	50	%
Signal Type	Square-wave	-

5.12. Internal Reset Electrical Characteristics

Table 5-14 Internal Reset Electrical Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
Power-on threshold voltage of VDD-SYS on which the reset signal is excited	Ta= -20°C to 85°C	-	0.4	-	V
Reset active timeout period	Ta= -20°C to 85°C	-	64	-	ms
Reset open-drain output voltage	Ta= -20°C to 85°C, pull up 3.3 V	-0.3	-	0.3*VCC	V
Power-off threshold voltage of VCC-PL on which the reset signal is excited	The voltage can be enabled by software, and it can be configured as 3.0 V, 2.9 V, 2.8 V, 2.7 V, 2.6 V, or 2.5 V.				

5.13. External Memory Electrical Characteristics

5.13.1. NAND AC Electrical Characteristics

Figure 5-2 Conventional Serial Access Cycle Timing (SAM0)

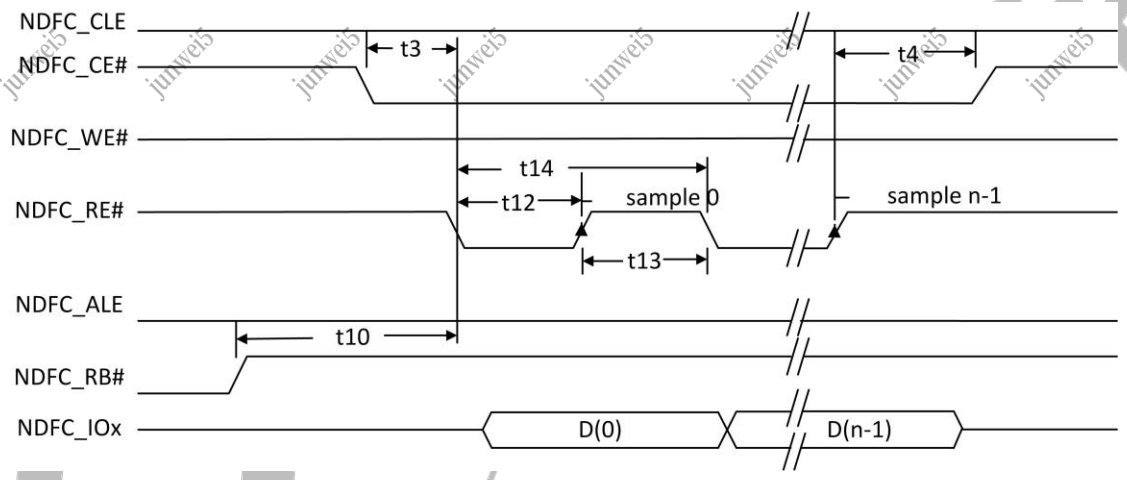


Figure 5-3 EDO Type Serial Access after Read Cycle Timing (SAM1)

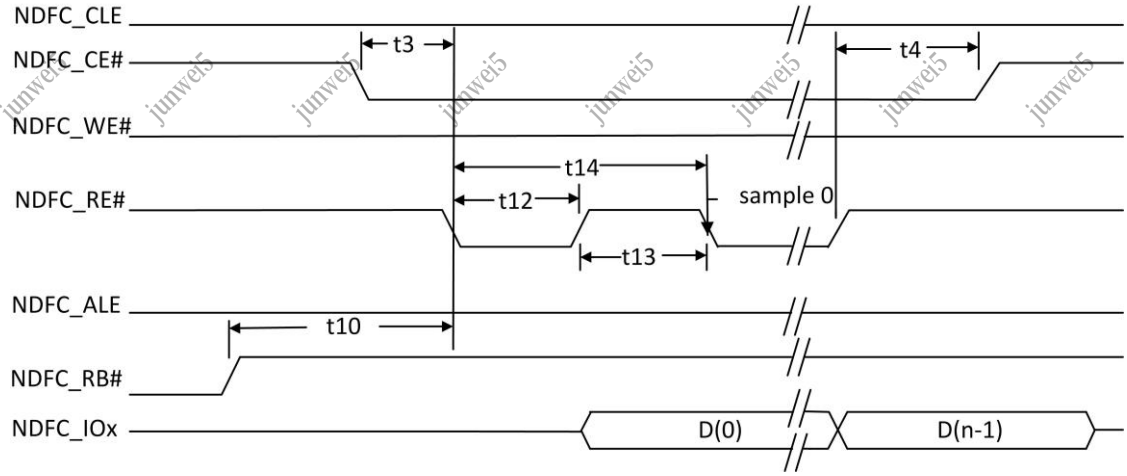


Figure 5-4 Extending EDO Type Serial Access Mode Timing (SAM2)

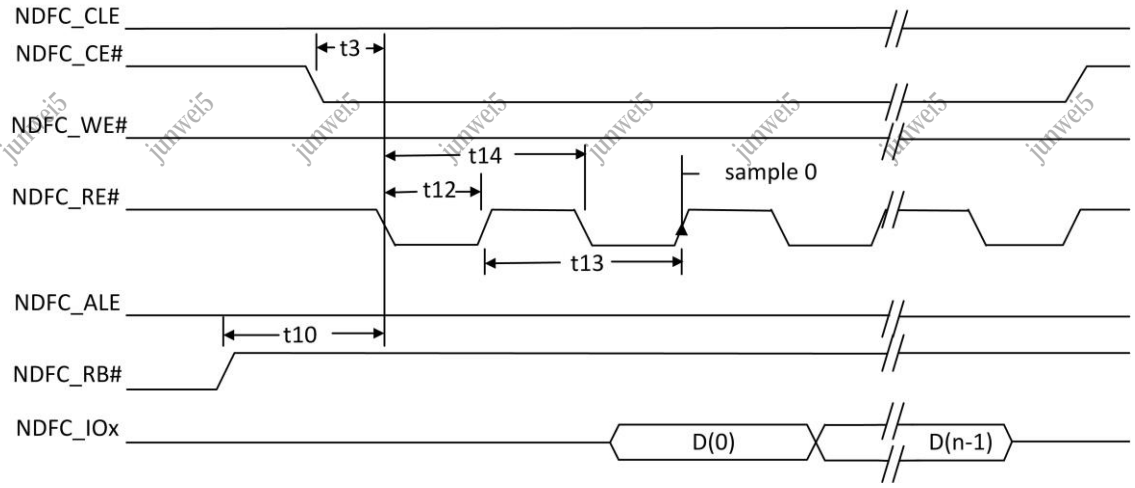


Figure 5-5 Command Latch Cycle Timing

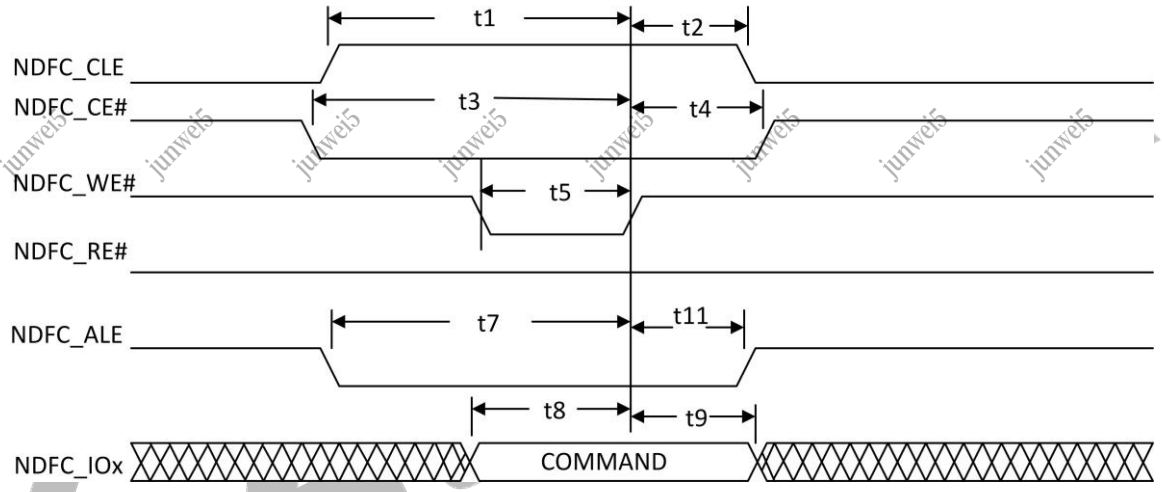


Figure 5-6 Address Latch Cycle Timing

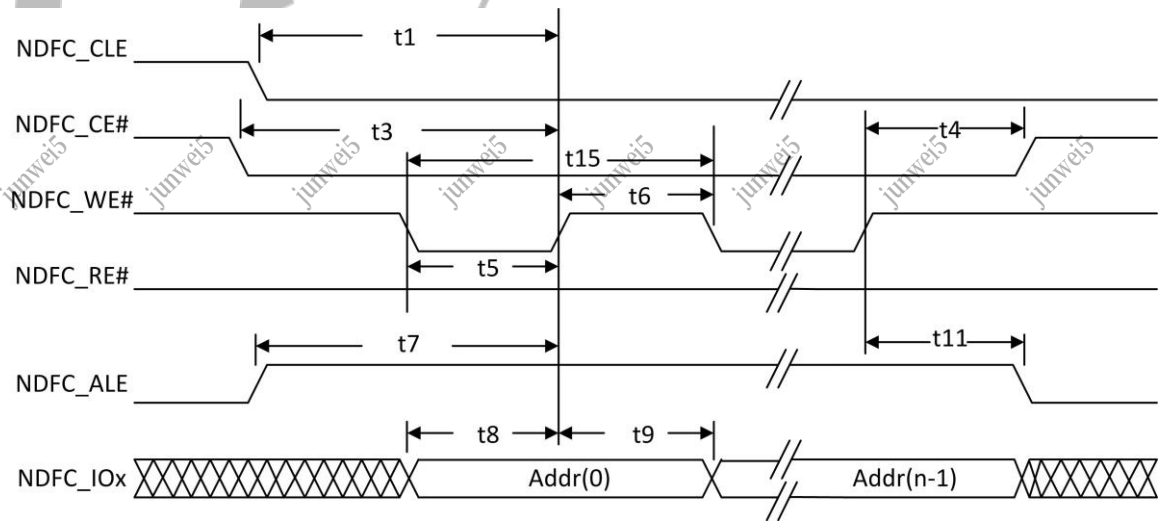


Figure 5-7 Write Data to Flash Cycle Timing

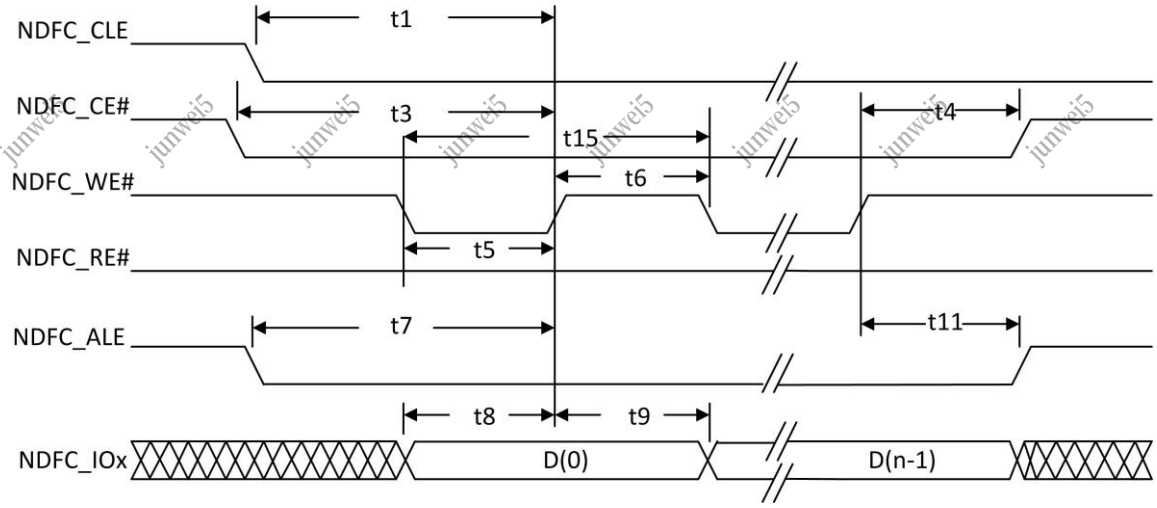


Figure 5-8 Waiting R/B# Ready Timing

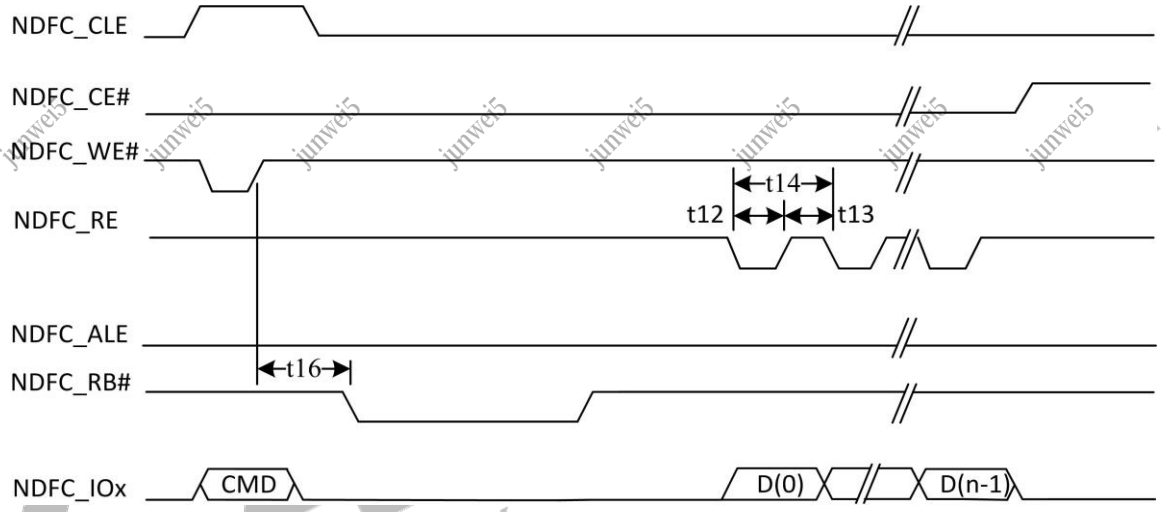


Figure 5-9 WE# High to RE# Low Timing

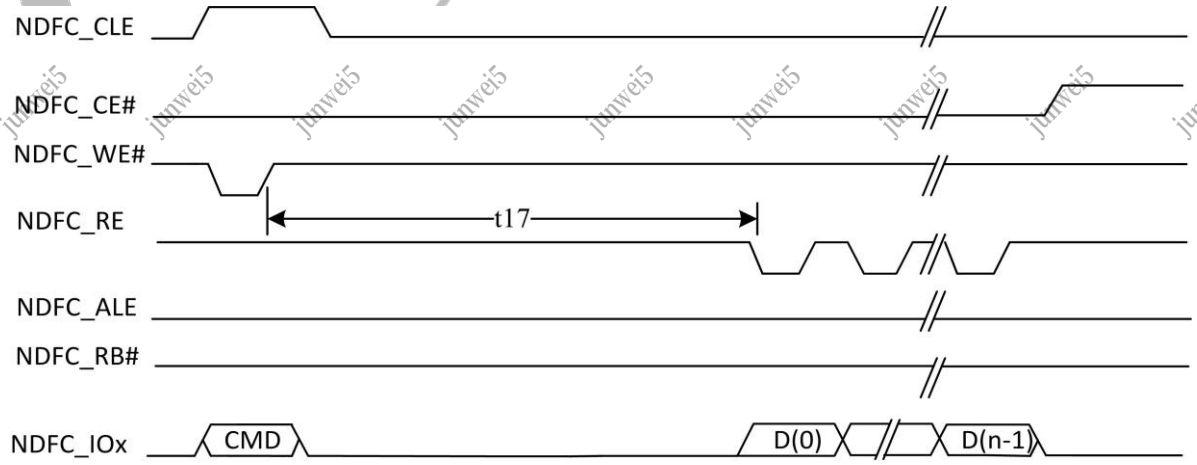


Figure 5-10 RE# High to WE# Low Timing

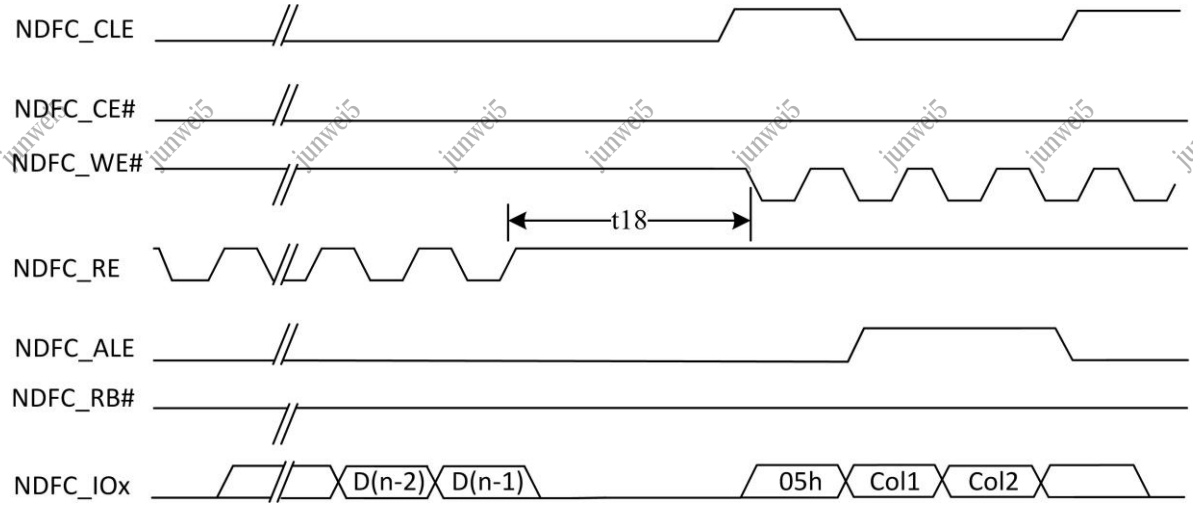


Figure 5-11 Address to Data Loading Timing

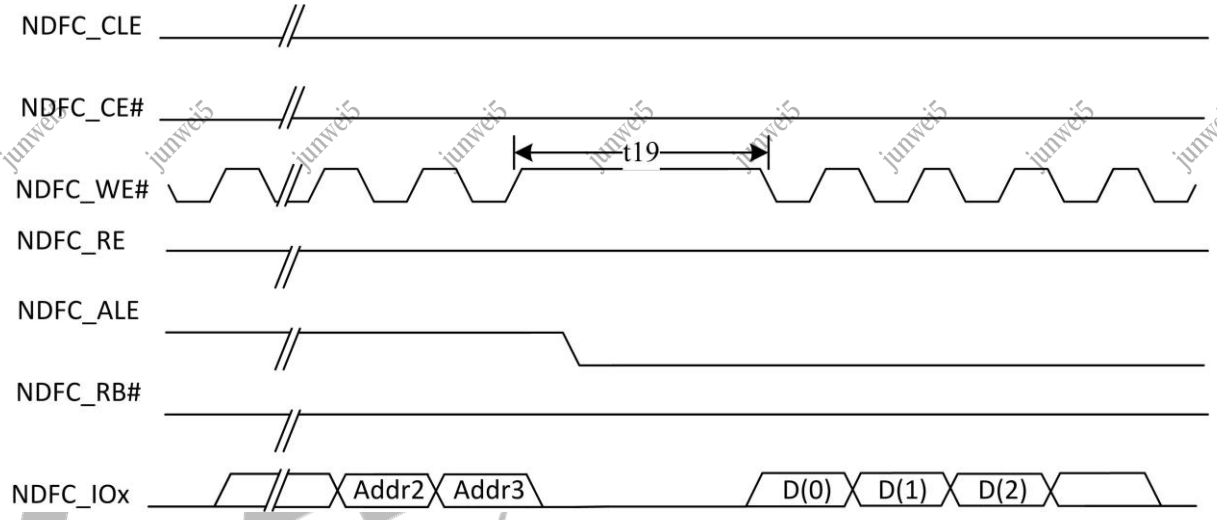


Table 5-15 NAND Timing Constants

Parameter	Symbol	Timing	Unit
NDFC_CLE setup time	t1	2T	ns
NDFC_CLE hold time	t2	2T	ns
NDFC_CE setup time	t3	2T	ns
NDFC_CE hold time	t4	2T	ns
NDFC_WE# pulse width	t5	T(1)	ns
NDFC_WE# hold time	t6	T	ns
NDFC_ALE setup time	t7	2T	ns
Data setup time	t8	T	ns
Data hold time	t9	T	ns
Ready to NDFC_RE# low	t10	3T	ns
NDFC_ALE hold time	t11	2T	ns
NDFC_RE# pulse width	t12	T	ns
NDFC_RE# hold time	t13	T	ns
Read cycle time	t14	2T	ns
Write cycle time	t15	2T	ns
NDFC_WE# high to R/B# busy	t16	T_WB(2)	ns
NDFC_WE# high to NDFC_RE# low	t17	T_WHR(3)	ns
NDFC_RE# high to NDFC_WE# low	t18	T_RHW(4)	ns
Address to Data Loading time	t19	T_ADL(5)	ns

Parameter	Symbol	Timing	Unit
(1): T is the cycle of internal clock. (2),(3),(4),(5): These values are configurable in NAND flash controller. The value of T_WB could be 14*2T/22*2T/30*2T/38*2T, the value of T_WHR could be 0*2T/6*2T/14*2T/22*2T, the value of T_RHW could be 4*2T/12*2T/20*2T/28*2T, the value of T_ADL could be 0*2T/6*2T/14*2T/22*2T.			

5.13.2. SMHC AC Electrical Characteristics

(1) HS-SDR Mode

NOTE

IO voltage is 1.8 V or 3.3 V.

Figure 5-12 SMHC HS-SDR Mode Output Timing Diagram

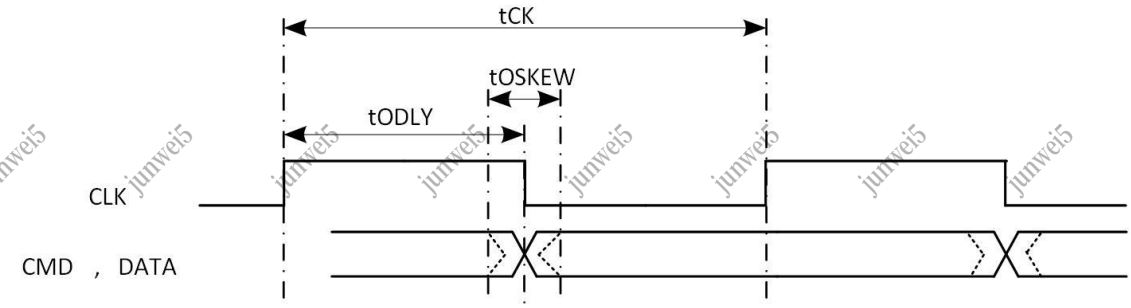


Table 5-16 SMHC HS-SDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA (referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	0.5	-	0.8	ns
(1). The Unit Interval (UI) is 1-bit nominal time. For example, UI=20 ns at 50 MHz. **(2). The driver strength level of GPIO is 2 for test.**					

Figure 5-13 SMHC HS-SDR Mode Input Timing Diagram

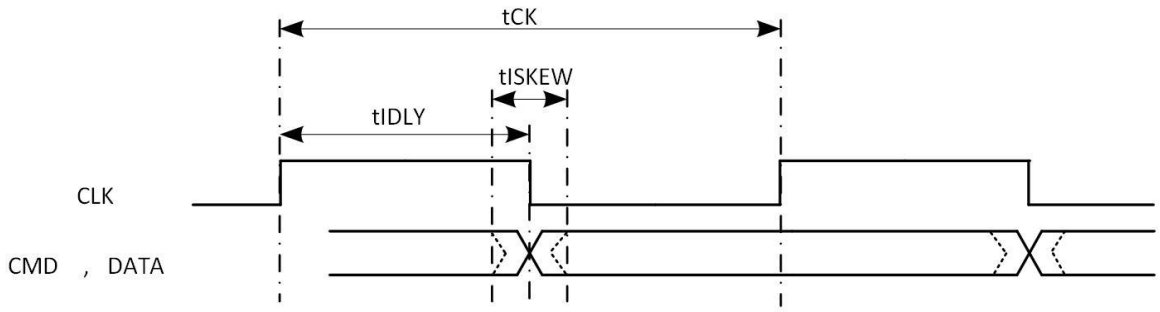


Table 5-17 SMHC HS-SDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Input CMD, DATA (referenced to CLK 50 MHz)					
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY	-	-	-	ns
Data input skew time in SDR mode	tISKEW	0.5	-	0.8	ns
(1). The driver strength level of GPIO is 2 for test.					

(2) HS-DDR Mode

Figure 5-14 SMHC HS-DDR Mode Output Timing Diagram

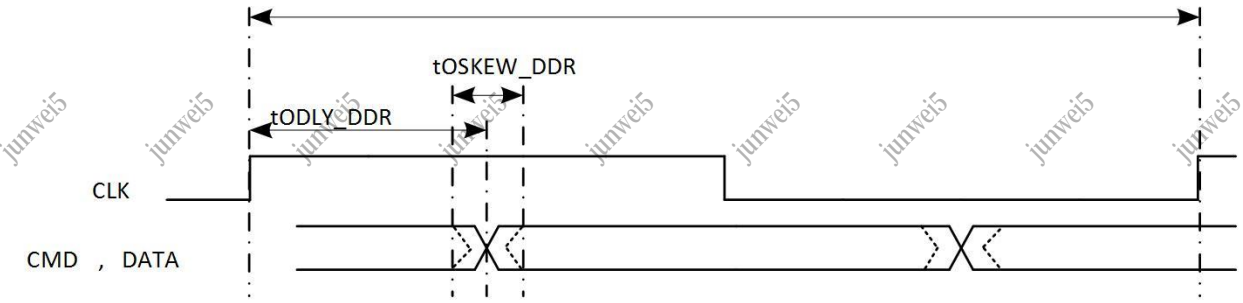


Table 5-18 SMHC HS-DDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA (referenced to CLK)					
CMD, Data output delay time in DDR mode	tODLY_DDR	-	0.25	0.25	UI
Data output delay skew time	tOSKEW_DDR	0.5	-	0.8	ns
(1). The Unit Interval (UI) is 1-bit nominal time. For example, UI=20 ns at 50 MHz.					
(2). The driver strength level of GPIO is 2 for test.					

Figure 5-15 SMHC HS-DDR Mode Input Timing Diagram

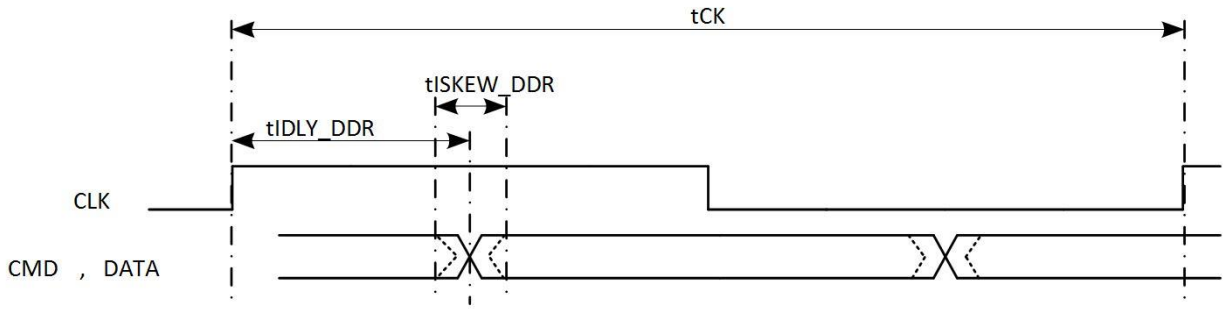


Table 5-19 SMHC HS-DDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Input CMD, DATA (referenced to CLK 50 MHz)					
Data input delay in DDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY_DDR	-	-	-	ns
Data input skew time in DDR mode	tISKEW_DDR	0.5	-	0.8	ns
(1). The driver strength level of GPIO is 2 for test.					

(3) HS200 Mode

Figure 5-16 SMHC HS200 Mode Output Timing Diagram

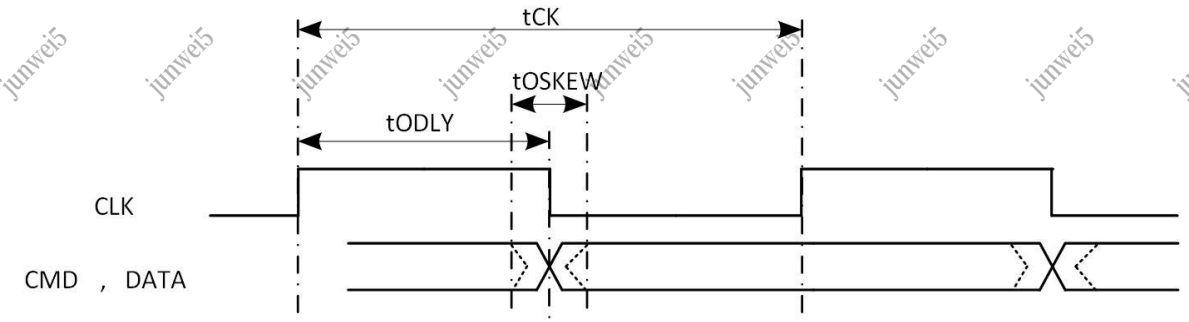


Table 5-20 SMHC HS200 Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	-	150	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA (referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	0.5	-	0.8	ns
(1). The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz. **(2). The driver strength level of GPIO is 3 for test.**					

Figure 5-17 SMHC HS200 Mode Input Timing Diagram

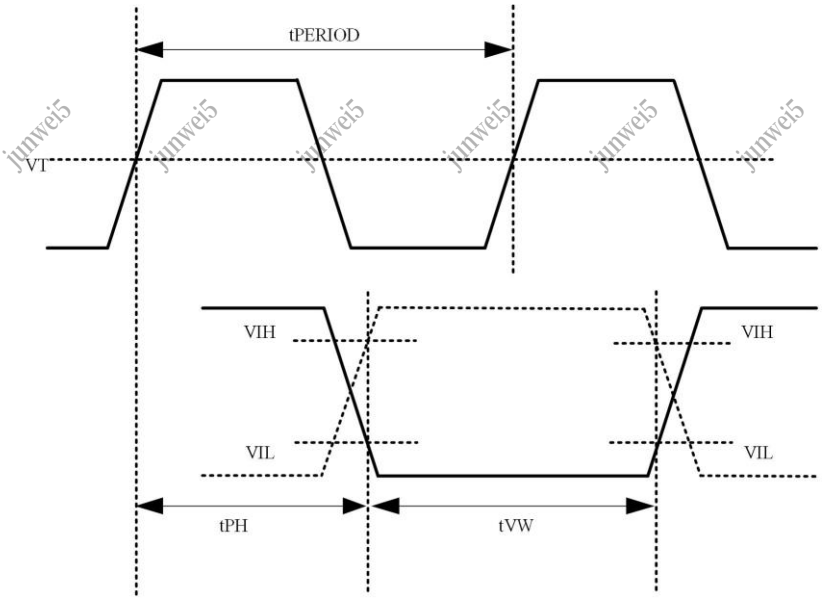


Table 5-21 SMHC HS200 Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	6.66	-	-	ns	Max: 150 MHz
Duty cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Input CMD, DATA (referenced to CLK)						
Input delay	tPH	0	-	2	UI	
Input delay variation due to temperature change after tuning	dPH	-350[3]	-	1550[4]	ps	
CMD, Data valid window	tVW	0.575	-	-	UI	
(1). The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz. **(2). The driver strength level of GPIO is 3 for test.** **(3). Temperature variation: -20°C.** **(4). Temperature variation: 90°C.**						

5.14. External Peripheral Electrical Characteristics

5.14.1. EMAC AC Electrical Characteristics

5.14.1.1. RGMII

Figure 5-18 RGMII Interface Transmit Timing

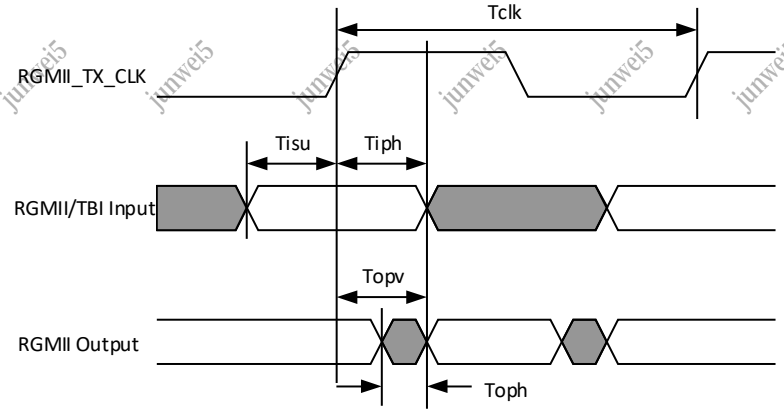


Table 5-22 RGMII Transmit Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RGMII_TX_CLK clock period	Tclk	8	-	DC	ns
RGMII/TBI input setup prior to RGMII_TX_CLK	Tisu	2.8	-	-	ns
RGMII/TBI input data hold after RGMII_TX_CLK	Tiph	0.1	-	-	ns
RGMII output data valid after RGMII_TX_CLK	Topv	-	-	0.85	ns
RGMII output data hold after RGMII_TX_CLK	Toph	0	-	-	ns

Figure 5-19 RGMII Interface Receive Timing

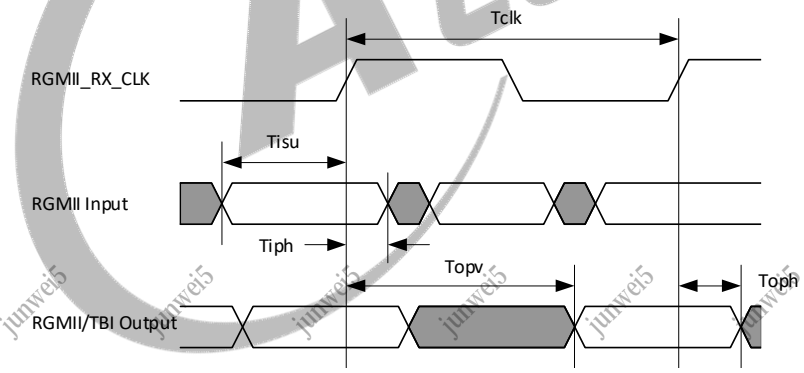


Table 5-23 RGMII Receive Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RGMII_RX_CLK clock period	Tclk	8	-	DC	ns
RGMII input setup prior to RGMII_RX_CLK	Tisu	2.6	-	-	ns
RGMII input data hold after RGMII_RX_CLK	Tiph	0.8	-	-	ns
RGMII/TBI input data valid after RGMII_RX_CLK	Topv	-	-	5.2	ns
RGMII output data hold after RGMII_RX_CLK TBI output data hold after RGMII_RX_CLK	Toph	0.1 0.5	-	-	ns

5.14.1.2. RMII

Figure 5-20 RMII Interface Transmit Timing

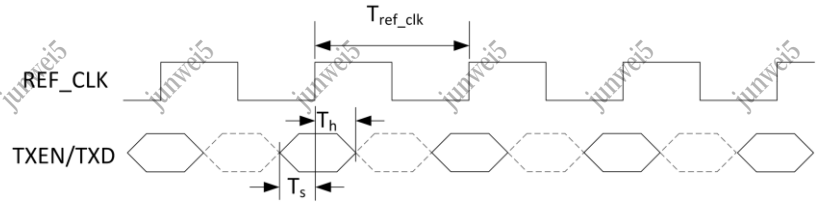


Table 5-24 RMII Transmit Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Reference clock period	T_{ref_clk}	-	20	-	ns
TXD/TXEN to REF_CLK setup time	Ts	4	-	-	ns
TXD/TXEN to REF_CLK hold time	Th	2	-	-	ns

Figure 5-21 RMII Interface Receive Timing

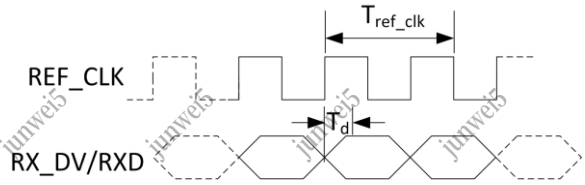


Table 5-25 RMII Receive Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Reference clock period	T_{ref_clk}	-	20	-	ns
REF_CLK rising edge to RX_DV/RXD	Td	-	10	12	ns

5.14.2. SPI AC Electrical Characteristics

Figure 5-22 SPI Writing Timing

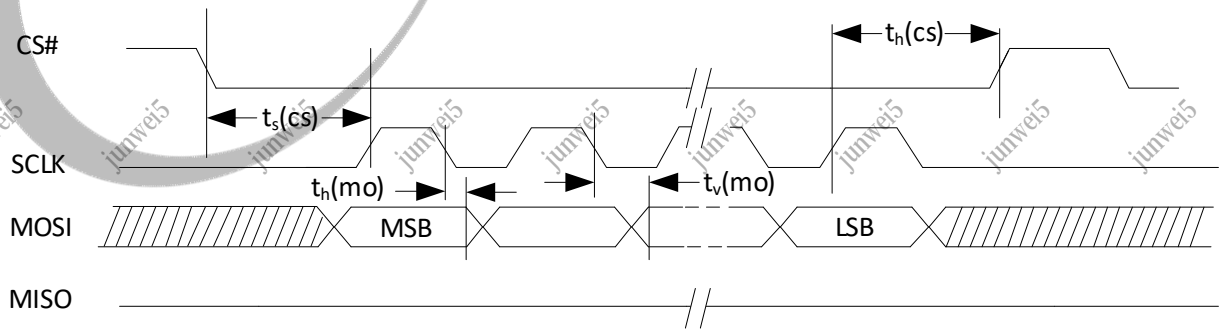


Figure 5-23 SPI Reading Timing

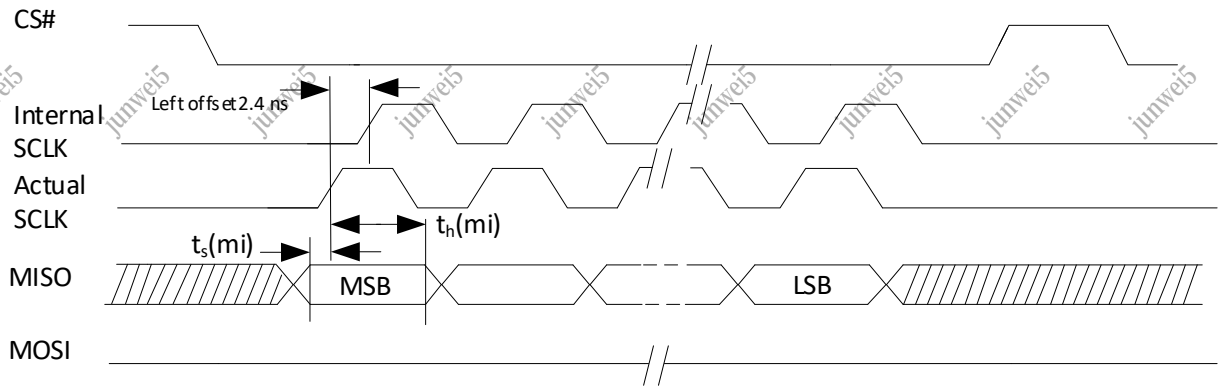


Table 5-26 SPI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CS# active setup time	t_s(cs)	-	$2T^{(1)}$	-	ns
CS# active hold time	t_h(cs)	-	$2T^{(1)}$	-	ns
Data output valid time	t_v(mo)	-	$T^{(1)}/2-3$	-	ns
Data output hold time	t_h(mo)	-	$T^{(1)}/2-3$	-	ns
Data input setup time	t_s(mi)	0.2	-	-	ns
Data input hold time	t_h(mi)	0.2	-	-	ns
(1).T is the cycle of clock.					

5.14.3. UART AC Electrical Characteristics

Figure 5-24 UART RX Timing

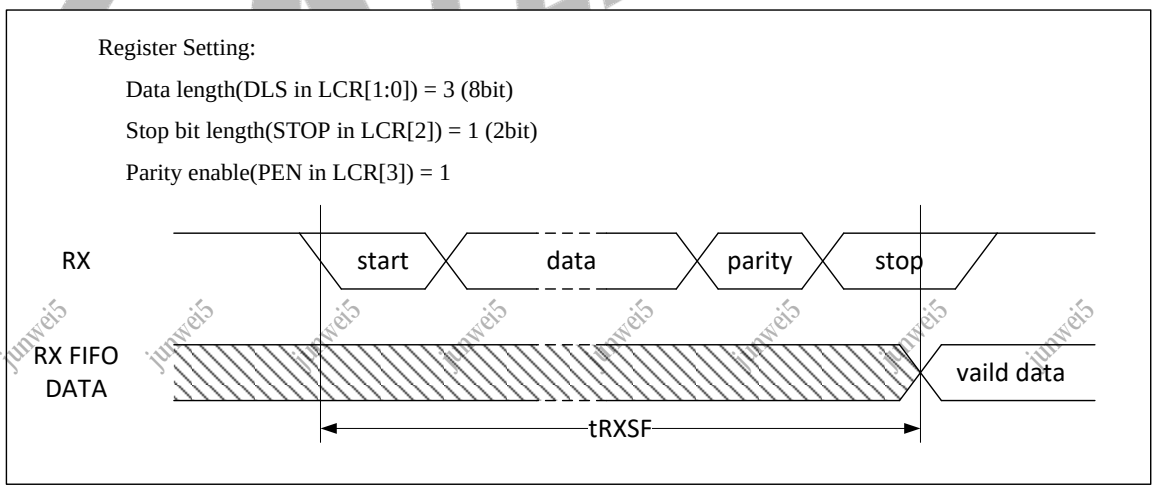


Figure 5-25 UART nCTS Timing

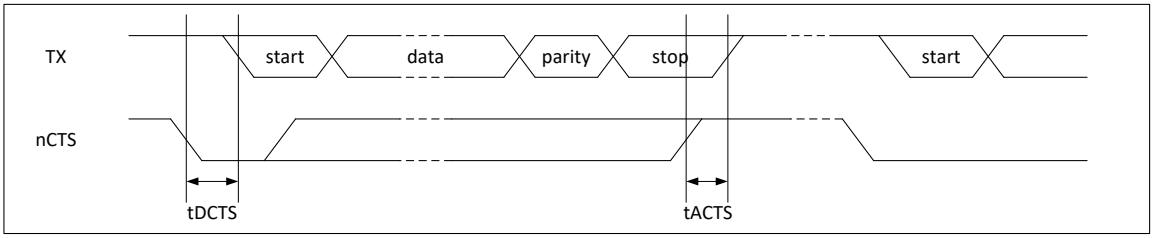


Figure 5-26 UART nRTS Timing

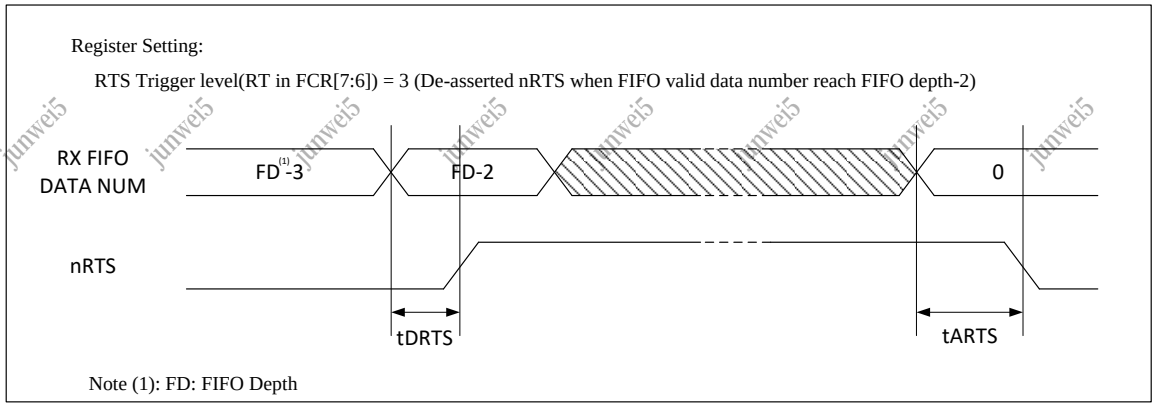


Table 5-27 UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	10.5 * BRP(1)	-	11 * BRP(1)	ns
Delay time of de-asserted nCTS to TX start	tDCTS	-	-	BRP(1)	ns
Step time of asserted nCTS to stop next transmission	tACTS	BRP(1)/4	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	BRP(1)	ns
Delay time of asserted nRTS	tARTS	-	-	BRP(1)	ns
(1). BRP: Baud-Rate Period.					

5.14.4. TWI AC Electrical Characteristics

Figure 5-27 TWI Timing

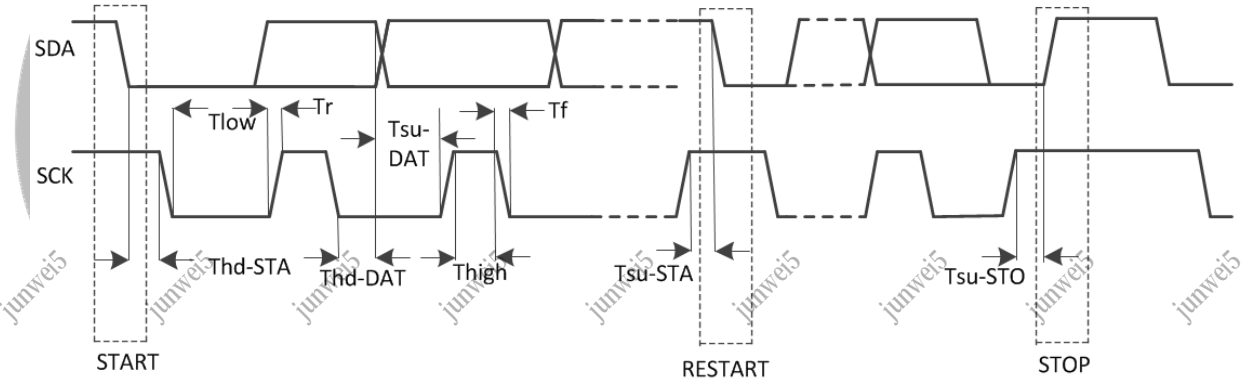


Table 5-28 TWI Timing Parameters

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK clock frequency	Fsck	0	100	0	400	kHz
Setup time in Start	Tsu-STA	4.7	-	0.6	-	us
Hold time in Start	Thd-STA	4.0	-	0.6	-	us
Setup time in Data	Tsu-DAT	250	-	100	-	ns
Hold time in Data	Thd-DAT	5.0	-	-	-	ns
Setup time in Stop	Tsu-STO	4.0	-	6.0	-	us
SCK low level time	Tlow	4.7	-	1.3	-	us
SCK high level time	Thigh	4.0	-	0.6	-	ns
SCK/SDA falling time	Tf	-	300	20	300	ns

Parameter	Symbol	Standard mode		Fast mode		Unit
SCK/SDA rising time	Tr	-	1000	20	300	ns

5.14.5. I2S/PCM AC Electrical Characteristics

Figure 5-28 I2S/PCM Timing in Master Mode

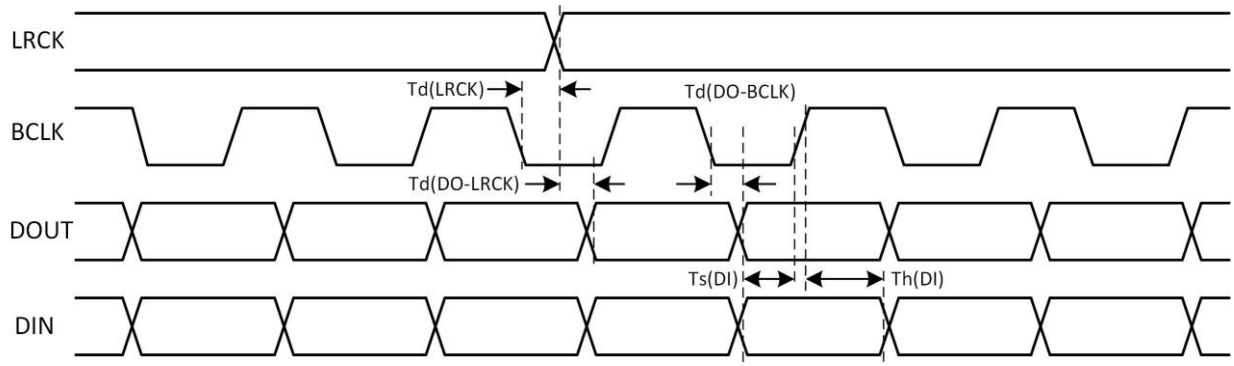


Table 5-29 I2S/PCM Timing Constants in Master Mode

Parameter	Symbol	Min	Typ	Max	Unit
LRCK delay	T_d(LRCK)	-	-	10	ns
LRCK to DOUT delay (For LJF)	T_d(DO-LRCK)	-	-	10	ns
BCLK to DOUT delay	T_d(DO-BCLK)	-	-	10	ns
DIN setup	T_s(DI)	4	-	-	ns
DIN hold	T_h(DI)	4	-	-	ns
BCLK rise time	T_r	-	-	8	ns
BCLK fall time	T_f	-	-	8	ns

Figure 5-29 I2S/PCM Timing in Slave Mode

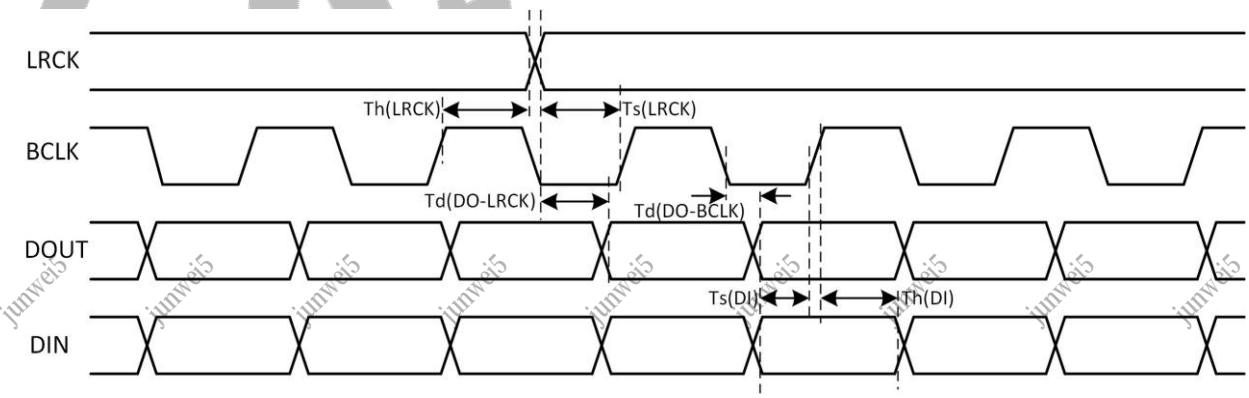


Table 5-30 I2S/PCM Timing Constants in Slave Mode

Parameter	Symbol	Min	Typ	Max	Unit
LRCK setup	T_s(LRCK)	4	-	-	ns
LRCK hold	T_h(LRCK)	4	-	-	ns
LRCK to DOUT delay (For LJF)	T_d(DO-LRCK)	-	-	10	ns
BCLK to DOUT delay	T_d(DO-BCLK)	-	-	10	ns
DIN setup	T_s(DI)	4	-	-	ns
DIN hold	T_h(DI)	4	-	-	ns
BCLK rise time	T_r	-	-	4	ns
BCLK fall time	T_f	-	-	4	ns

5.14.6. DMIC AC Electrical Characteristics

Figure 5-30 DMIC Timing

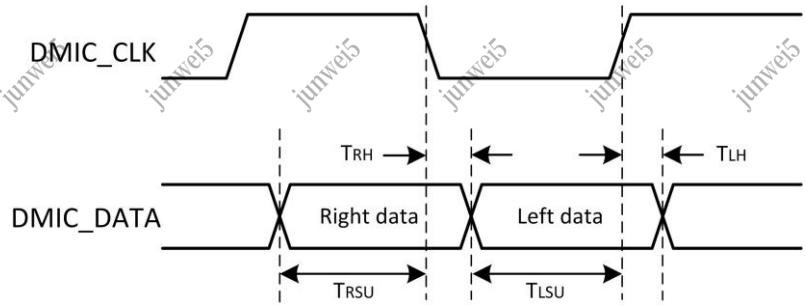


Table 5-31 DMIC Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DMIC_DATA (Right) setup time to falling edge of DMIC_CLK	TRSU	15	-	-	ns
DMIC_DATA (Right) hold time from falling edge of DMIC_CLK	TRH	0	-	-	ns
DMIC_DATA (Left) setup time to rising edge of DMIC_CLK	TLSU	15	-	-	ns
DMIC_DATA (Left) hold time from rising edge of DMIC_CLK	TLH	0	-	-	ns

5.14.7. OWA AC Electrical Characteristics

Figure 5-31 OWA Timing

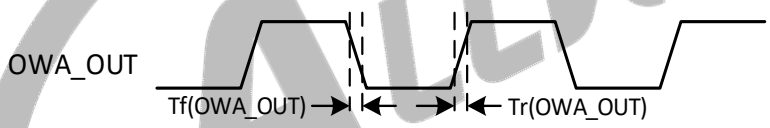


Table 5-32 OWA Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
OWA_OUT rise time	Tr(OWA_OUT)	-	-	8	ns
OWA_OUT fall time	Tf(OWA_OUT)	-	-	8	ns

5.14.8. CIR_RX AC Electrical Characteristics

Figure 5-32 CIR_RX Timing

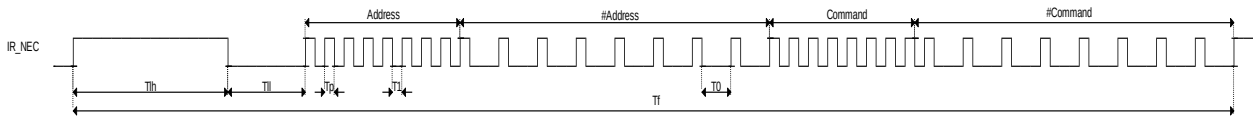


Table 5-33 CIR_RX Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Frame period	Tf	-	67.5	-	ms
Lead code high time	Tlh	-	9	-	ms
Lead code low time	Tll	-	4.5	-	ms
Pulse time	Tp	-	560	-	us

Parameter	Symbol	Min	Typ	Max	Unit
Logical 1 low time	T1	-	1680	-	us
Logical 0 low time	T0	-	560	-	us

5.14.9. SCR AC Electrical Characteristics

Figure 5-33 SCR Activation and Cold Reset Timing

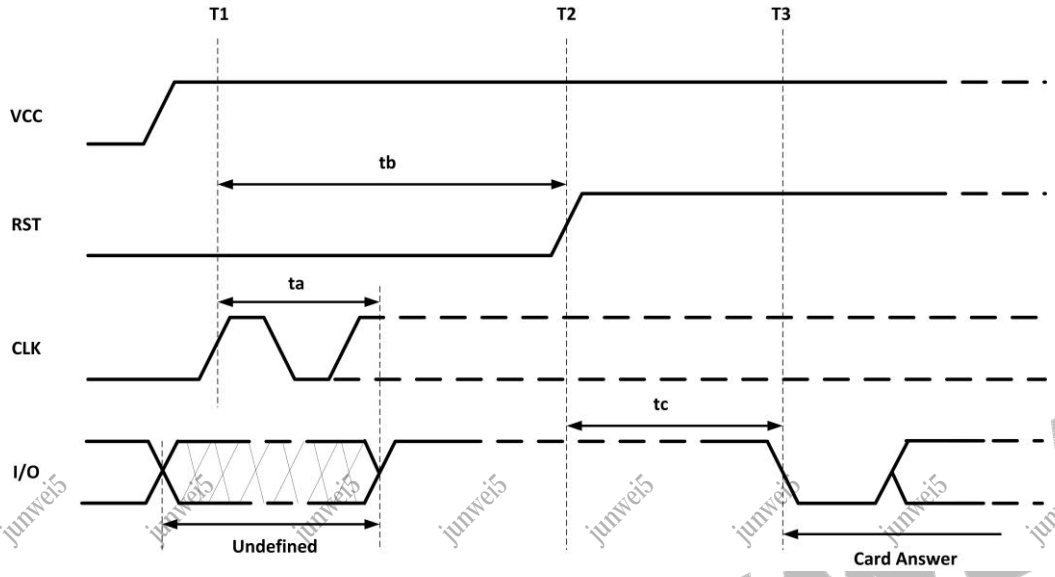


Figure 5-34 SCR Warm Reset Timing

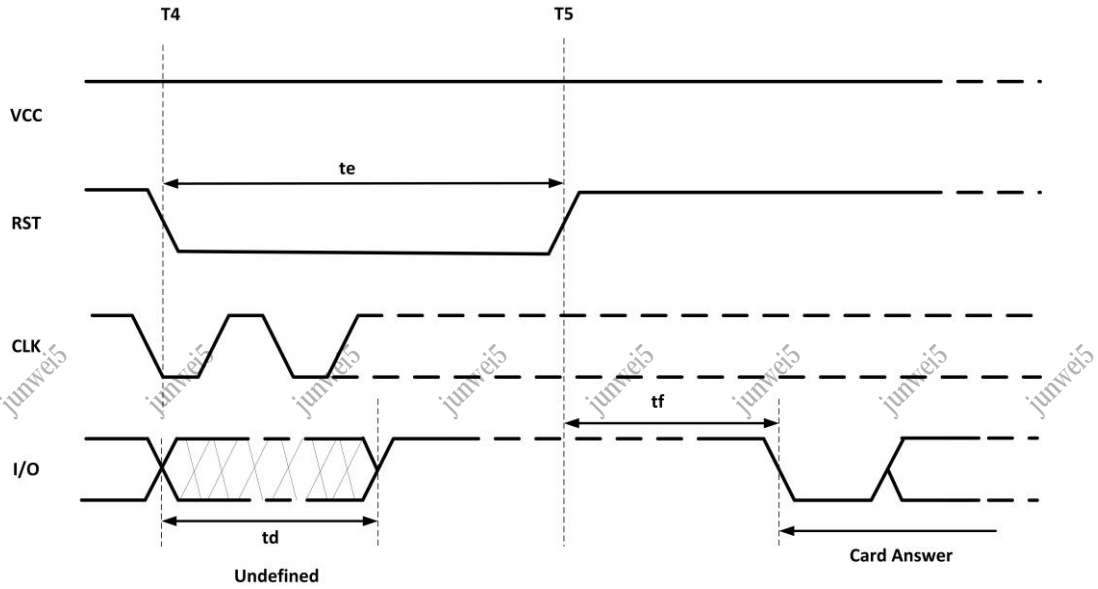


Table 5-34 SCR Timing Constants

Symbol	Min	Typ	Max	Unit
ta	-	-	200/f	us
tb	400/f	-	-	us
tc	400/f	-	40000/f	us
td	-	-	200/f	us
te	400/f	-	-	us
tf	400/f	-	40000/f	us
(1) Activation: Before time T1				

Symbol	Min	Typ	Max	Unit
(2) Cold Reset: After time T1 (3) T1: The clock signal applies to CLK at time T1. (4) T2: The RST is put to state H. (5) T3: The card begins to answer at time T3. (6) ta: The card shall set I/O to state H within 200 clock cycles (delay ta) after the clock signal is applied to CLK (at time T1+ta). (7) tb: The cold reset results from maintaining RST at state L for at least 400 clock cycles (delay tb) after the clock signal is applied to CLK (at time T1+tb). (8) tc: The answer on I/O shall begin between 400 and 40000 clock cycles (delay tc) after the rising edge of the signal on RST (at time T2+tc). (9) td: The card shall set I/O to state H within 200 clock cycles (delay td) after state L is applied to RST (at time T4+td). (10) te: The controller initiates a warm reset (at time T4) by putting RST to state L for at least 400 clock cycles (delay te) while VCC remains powered and CLK provided with a suitable and stabled clock signal. (11) tf: The card answer on I/O shall begin between 400 and 40000 clock cycles (delay tf) after the rising edge of the signal on RST (at time T5+tf). (12) f is the frequency of clock.				

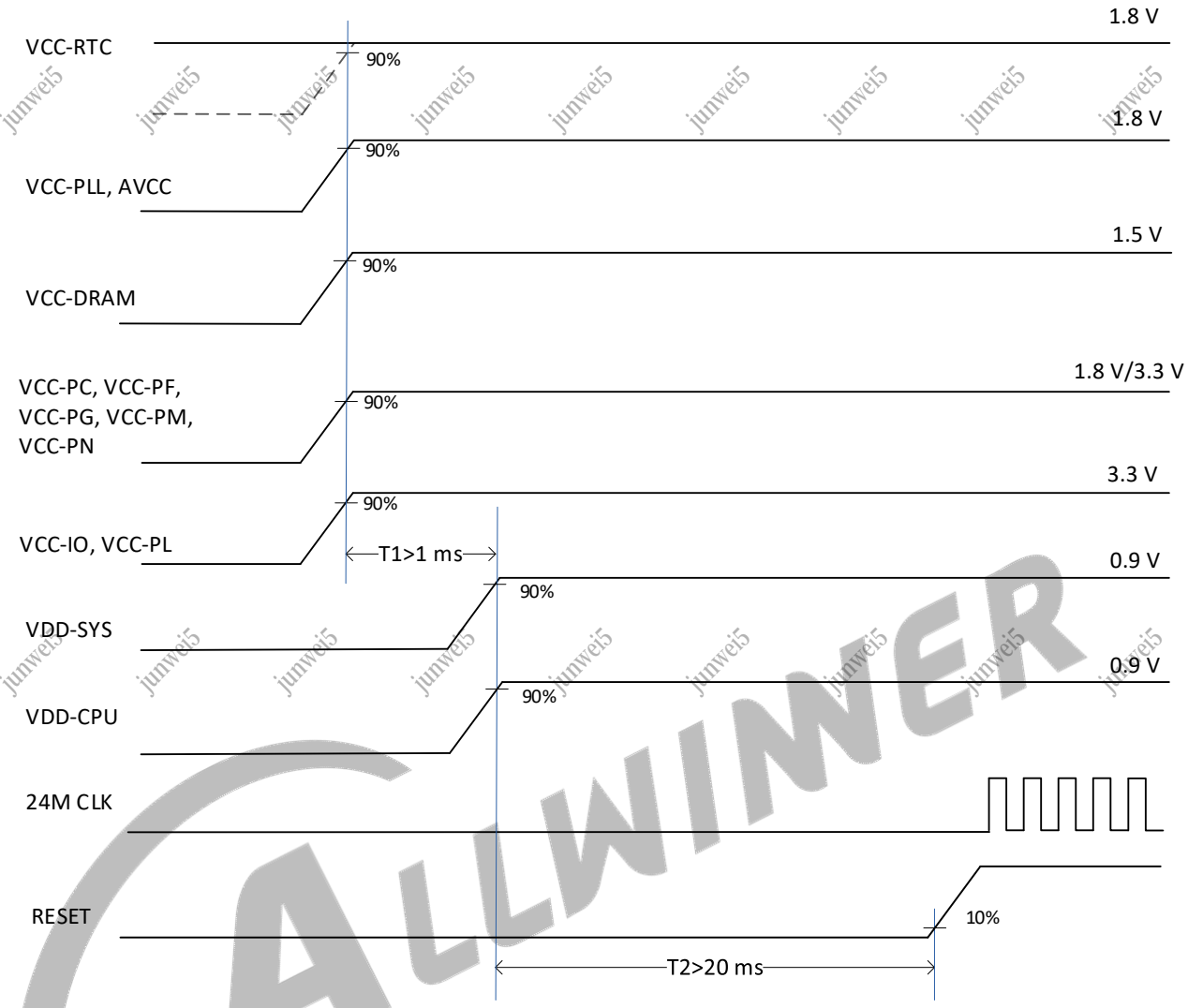
5.15. Power-On and Power-Off Sequence

5.15.1. Power-On Sequence

Figure 5-35 shows an example of the power-on sequence for the R329 device. The description of the power-on sequence is as follows.

- The consequent steps in power-on sequence should not start before the previous step supplies have been stabilized within 90~110% of their nominal voltage, unless stated otherwise.
- VCC-RTC must be ramped no later than other power rails.
- VDD-SYS and VDD-CPU must be ramped after VCC-PL with a minimum delay of 1 ms.
- VCC-DRAM needs be stable before SDRAM driver initialization.
- During the entire power on sequence, the RESET signal must be held on low until all other power rails are stable for more than 20 ms.
- The 24 MHz clock stabilizes within 4 ms after the RESET signal is released.

Figure 5-35 Power-On Timing

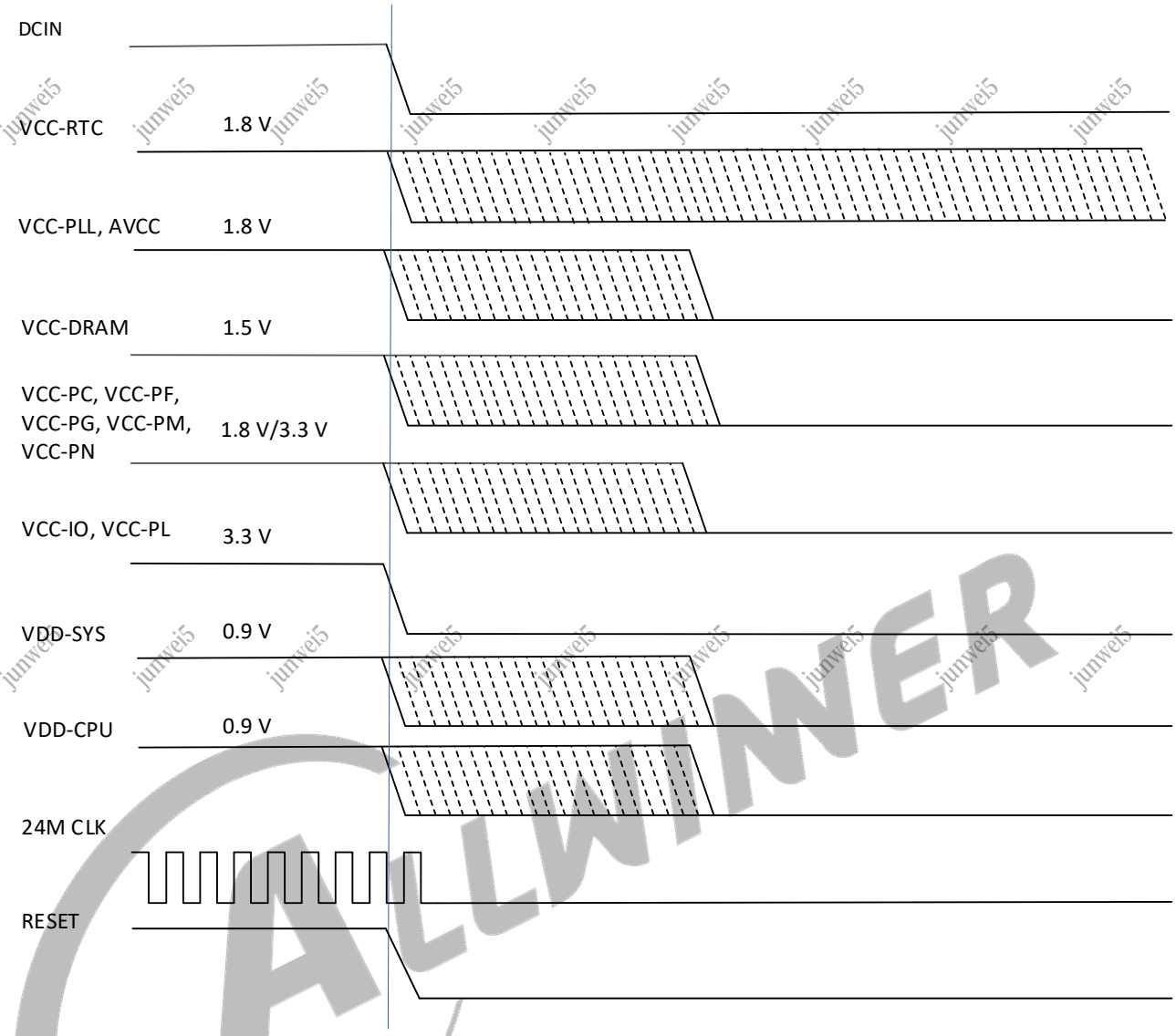


5.15.2. Power-Off Sequence

The power-off requirements are as follows.

- VCC-PL is powered-off no later than other power rails.
- After the RESET signal goes low, the 24 MHz clock starts to stop oscillating.

Figure 5-36 Power-Off Timing



6. Package Thermal Characteristics

The maximum chip junction temperature (T_J max) must never exceed the values given in *Table 5-2 Recommended Operating Conditions*.

The maximum chip-junction temperature T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_a max + (P_D max x θ_{JA})

Where:

T_a max is the maximum ambient temperature in °C.

P_D max is the maximum power dissipation.

θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W.

°C/W = degrees Celsius per watt.

Failure to maintain a junction temperature within the range specified reduces operating lifetime, reliability, and performance, and may cause irreversible damage to the system. It is useful to calculate the exact power consumption and junction temperature to determine which the temperature will be best suited to the application. Therefore, the product should include thermal analysis and thermal design to ensure the operating junction temperature of the device is within functional limits.

The following tables show the thermal resistance characteristics of the R329. These data are based on JEDEC JESD51 standard, because the actual system design and temperature could be different from JEDEC JESD51, these simulating data are a reference only and may not represent actual use-case values, please prevail in the actual application condition test.

6.1. R329-N3/R329-S3

Table 6-1 R329-N3/R329-S3 Package Thermal Characteristics

Symbol	Parameter	Min	Typ(1)	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	-	25.9	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	8.96	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	4.3	-	°C/W

1. Reference document: JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air). Available from www.jedec.org.

6.2. R329-N4

Table 6-2 R329-N4 Package Thermal Characteristics

Symbol	Parameter	Min	Typ(1)	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	-	27.82	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	12.14	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	4.22	-	°C/W

1. Reference document: JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air). Available from www.jedec.org.

7. Pin Assignment

7.1. Pin Map

7.1.1. R329-N3/R329-S3

For R329-N3/R329-S3, LFBGA 231 balls, 12 mm x 12 mm, 0.65 mm ball pitch, 0.35 mm ball size package is offered. The following figure shows the pin map of the R329-N3/R329-S3.

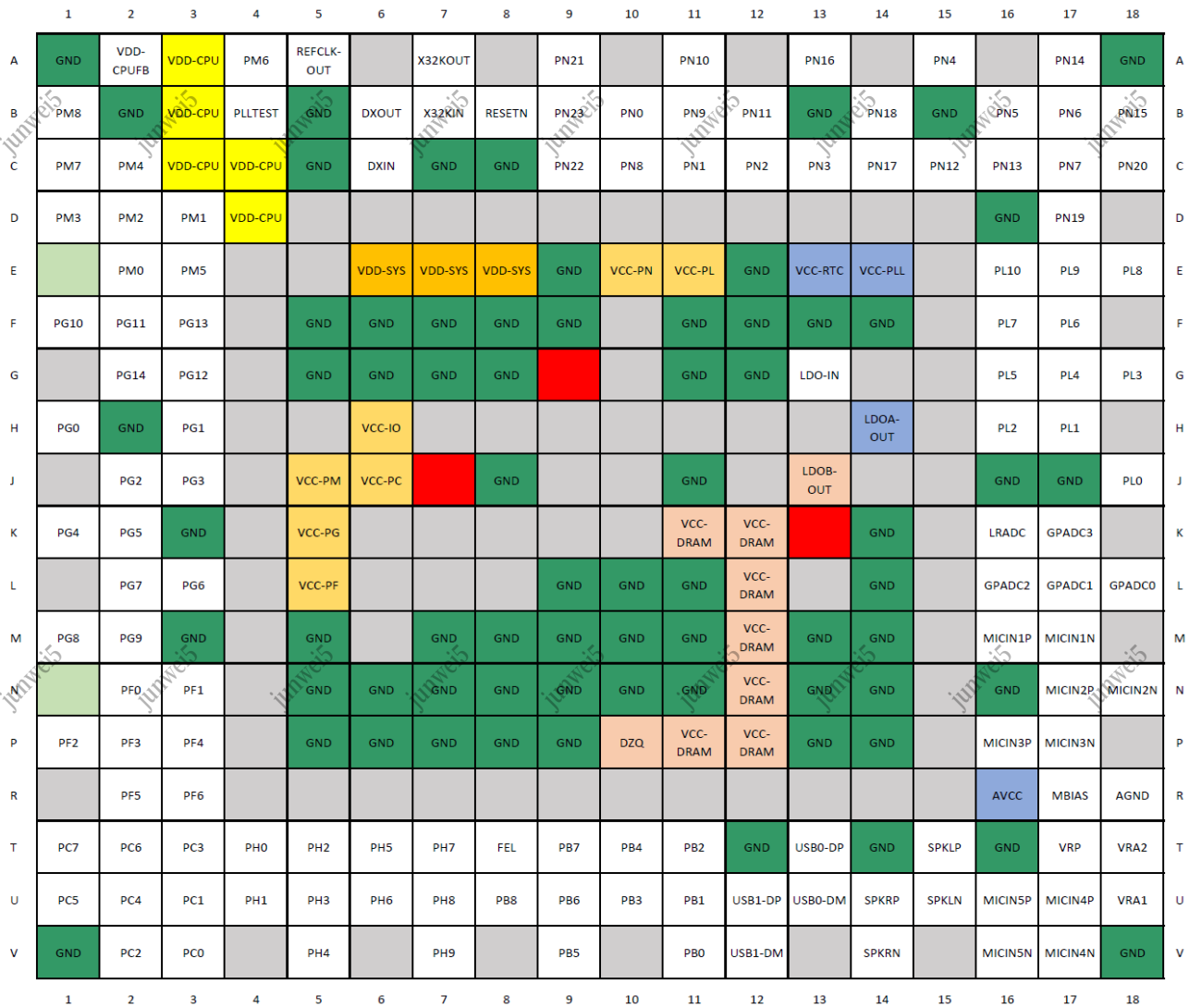
Figure 7-1 R329-N3/R329-S3 Pin Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	GND	VDD-CPUFB	VDD-CPU	PM6	REFCLK-OUT		X32KOUT		PN21		PN10		PN16		PN4		PN14	GND	A
B	PM8	GND	VDD-CPU	PLLTEST	GND	DXOUT	X32KIN	RESETN	PN23	PN0	PN9	PN11	GND	PN18	GND	PN5	PN6	PN15	B
C	PM7	PM4	VDD-CPU	VDD-CPU	GND	DXIN	GND	GND	PN22	PN8	PN1	PN2	PN3	PN17	PN12	PN13	PN7	PN20	C
D	PM3	PM2	PM1	VDD-CPU												GND	PN19		D
E		PM0	PM5			VDD-SYS	VDD-SYS	VDD-SYS	GND	VCC-PN	VCC-PL	GND	VCC-RTC	VCC-PLL		PL10	PL9	PL8	E
F	PG10	PG11	PG13		GND	GND	GND	GND	GND		GND	GND	GND	GND		PL7	PL6		F
G		PG14	PG12		GND	GND	GND	GND	GND		GND	GND	LDO-IN			PL5	PL4	PL3	G
H	PG0	GND	PG1			VCC-IO								LDOA-OUT		PL2	PL1		H
J		PG2	PG3		VCC-PM	VCC-PC	GND	GND			GND		LDOB-OUT			GND	GND	PL0	J
K	PG4	PG5	GND		VCC-PG						VCC-DRAM	VCC-DRAM	GND	GND		LRADC	GPADC3		K
L		PG7	PG6		VCC-PF				GND	GND	GND	VCC-DRAM		GND		GPADC2	GPADC1	GPADC0	L
M	PG8	PG9	GND		GND		GND	GND	GND	GND	GND	VCC-DRAM	GND	GND		MICIN1P	MICIN1N		M
N		PF0	PF1		GND	GND	GND	GND	GND	GND	GND	VCC-DRAM	GND	GND		GND	MICIN2P	MICIN2N	N
P	PF2	PF3	PF4		GND	GND	GND	GND	GND	DZQ	VCC-DRAM	VCC-DRAM	GND	GND		MICIN3P	MICIN3N		P
R		PF5	PF6													AVCC	MBIAS	AGND	R
T	PC7	PC6	PC3	PH0	PH2	PH5	PH7	FEL	PB7	PB4	PB2	GND	USB0-DP	GND	SPKLP	GND	VRP	VRA2	T
U	PC5	PC4	PC1	PH1	PH3	PH6	PH8	PB8	PB6	PB3	PB1	USB1-DP	USB0-DM	SPKRP	SPKLN	MICIN5P	MICIN4P	VRA1	U
V	GND	PC2	PC0		PH4		PH9		PB5		PB0	USB1-DM		SPKRN		MICIN5N	MICIN4N	GND	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

7.1.2. R329-N4

For R329-N4, LFBGA 228 balls, 12 mm x 14.5 mm, 0.65 mm ball pitch, 0.35 mm ball size package is offered. The following figure shows the pin map of the R329-N4.

Figure 7-2 R329-N4 Pin Map



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	GND	VDD-CPUFB	VDD-CPU	PM6	REFCLK-OUT		X32KOUT		PN21		PN10		PN16		PN4		PN14	GND	A
B	PM8	GND	VDD-CPU	PLLTEST	GND	DXOUT	X32KIN	RESETN	PN23	PN0	PN9	PN11	GND	PN18	GND	PN5	PN6	PN15	B
C	PM7	PM4	VDD-CPU	VDD-CPU	GND	DXIN	GND	GND	PN22	PN8	PN1	PN2	PN3	PN17	PN12	PN13	PN7	PN20	C
D	PM3	PM2	PM1	VDD-CPU												GND	PN19		D
E		PM0	PM5			VDD-SYS	VDD-SYS	VDD-SYS	GND	VCC-PN	VCC-PL	GND	VCC-RTC	VCC-PLL		PL10	PL9	PL8	E
F	PG10	PG11	PG13		GND	GND	GND	GND	GND		GND	GND	GND	GND		PL7	PL6		F
G		PG14	PG12		GND	GND	GND	GND			GND	GND	LDO-IN			PL5	PL4	PL3	G
H	PG0	GND	PG1			VCC-IO								LDOA-OUT		PL2	PL1		H
J		PG2	PG3		VCC-PM	VCC-PC		GND			GND		LDOB-OUT			GND	GND	PL0	J
K	PG4	PG5	GND		VCC-PG						VCC-DRAM	VCC-DRAM		GND		LRADC	GPADC3		K
L		PG7	PG6		VCC-PF				GND	GND	GND	VCC-DRAM		GND		GPADC2	GPADC1	GPADC0	L
M	PG8	PG9	GND		GND		GND	GND	GND	GND	GND	VCC-DRAM	GND	GND		MICIN1P	MICIN1N		M
N		PF0	PF1		GND	GND	GND	GND	GND	GND	GND	VCC-DRAM	GND	GND		GND	MICIN2P	MICIN2N	N
P	PF2	PF3	PF4		GND	GND	GND	GND	GND	DZQ	VCC-DRAM	VCC-DRAM	GND	GND		MICIN3P	MICIN3N		P
R		PF5	PF6													AVCC	MBIAS	AGND	R
T	PC7	PC6	PC3	PH0	PH2	PH5	PH7	FEL	PB7	PB4	PB2	GND	USB0-DP	GND	SPKLP	GND	VRP	VRA2	T
U	PC5	PC4	PC1	PH1	PH3	PH6	PH8	PB8	PB6	PB3	PB1	USB1-DP	USB0-DM	SPKRP	SPKLN	MICIN5P	MICIN4P	VRA1	U
V	GND	PC2	PC0		PH4		PH9		PB5		PB0	USB1-DM		SPKRN		MICIN5N	MICIN4N	GND	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

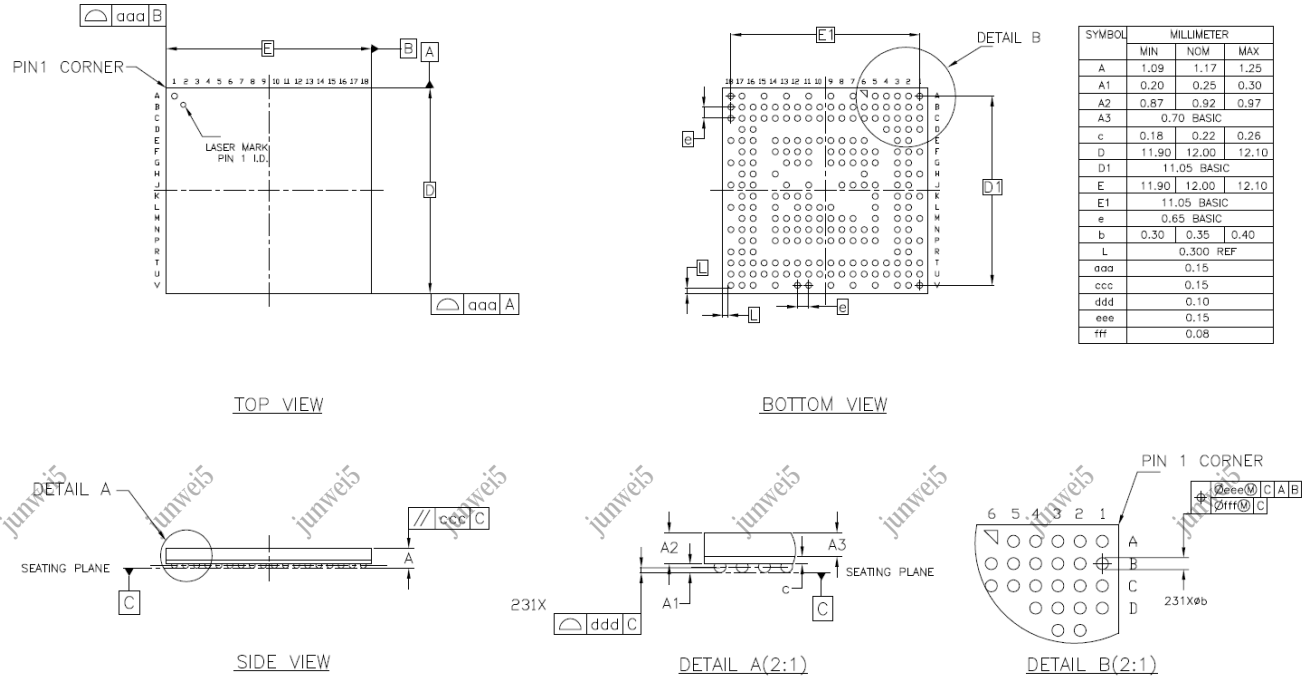
For R329-N3/R329-S3, the G9, J7, K13 are GND ball; but for R329-N4, the G9, J7, K13 are empty.

7.2. Package Dimension

7.2.1. R329-N3/R329-S3

Figure 7-3 shows the top, bottom, and side views of R329-N3/R329-S3 package dimension.

Figure 7-3 R329-N3/R329-S3 Package Dimension

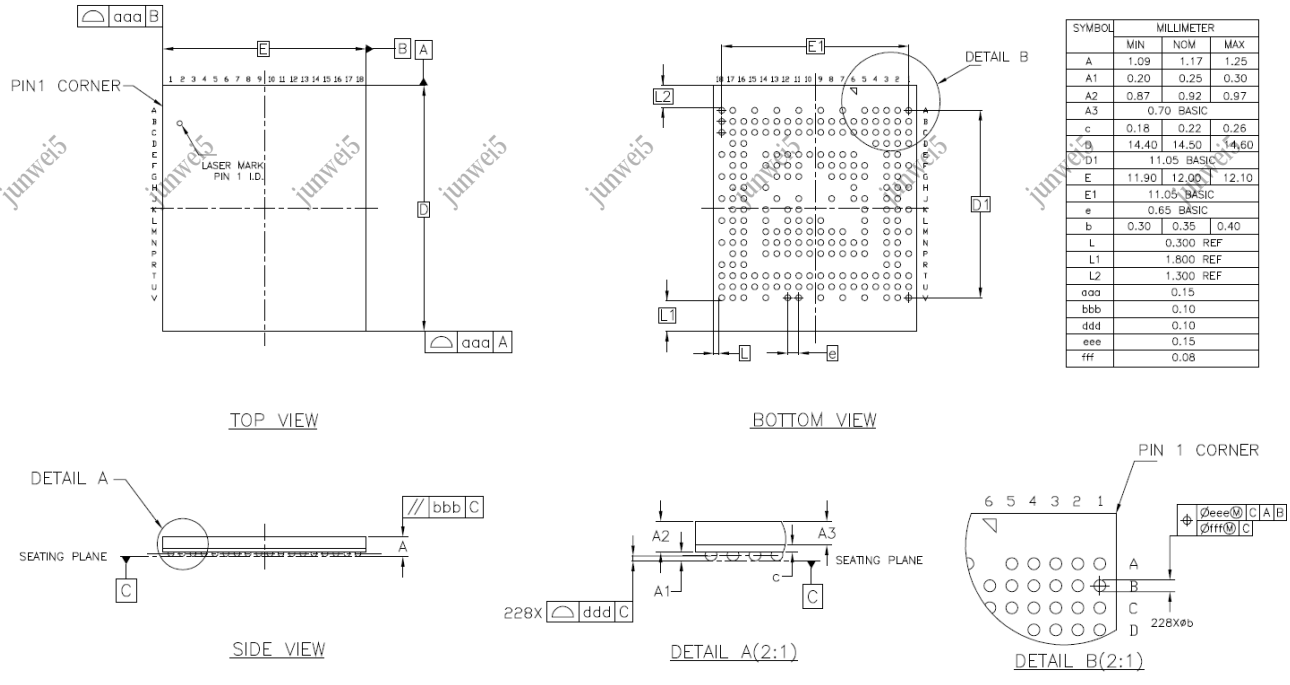


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.09	1.17	1.25
A1	0.20	0.25	0.30
A2	0.87	0.92	0.97
A3		0.70 BASIC	
c	0.18	0.22	0.26
D	11.90	12.00	12.10
D1		11.05 BASIC	
E	11.90	12.00	12.10
E1		11.05 BASIC	
e		0.65 BASIC	
b	0.30	0.35	0.40
L		0.300 REF	
aaa		0.15	
ccc		0.15	
ddd		0.10	
eee		0.15	
fff		0.08	

7.2.2. R329-N4

Figure 7-4 shows the top, bottom, and side views of R329-N4 package dimension. R329-N4 is 3 GND balls less than R329-N3/R329-S3.

Figure 7-4 R329-N4 Package Dimension



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.09	1.17	1.25
A1	0.20	0.25	0.30
A2	0.87	0.92	0.97
A3		0.70 BASIC	
c	0.18	0.22	0.26
D	14.40	14.50	14.60
D1		11.05 BASIC	
E	11.90	12.00	12.10
E1		11.05 BASIC	
e		0.65 BASIC	
b	0.30	0.35	0.40
L		0.300 REF	
L1		1.800 REF	
L2		1.300 REF	
aaa		0.15	
bbb		0.10	
ddd		0.10	
eee		0.15	
fff		0.08	

8. Carrier, Storage and Baking Information

8.1. Carrier

8.1.1. Matrix Tray Information

Table 8-1 shows the R329 matrix tray carrier information.

Table 8-1 Matrix Tray Carrier Information

Item	Color	Size	Note
Tray	Black	315 mm x 136 mm x 7.62 mm	168 Qty/Tray (only for R329-N3/R329-S3) 136 Qty/Tray (only for R329-N4)
Aluminum foil bags	Silvery white	540 mm x 300 mm x 0.14 mm	Vacuum packing Including HIC and desiccant Printing: RoHS symbol
Pearl cotton cushion (Vacuum bag)	White	12 mm x 680 mm x 185 mm	
Pearl cotton cushion (The Gap between vacuum bag and inner box)	White	Left-Right: 12 mm x 180 mm x 85 mm Front-Back: 12 mm x 350 mm x 70 mm	
Inner Box	White	396 mm x 196 mm x 96 mm	Printing: RoHS symbol 10 Tray/Inner box
Carton	White	420 mm x 410 mm x 320 mm	6 Inner box/Carton

8.1.1.1. R329-N3/R329-S3

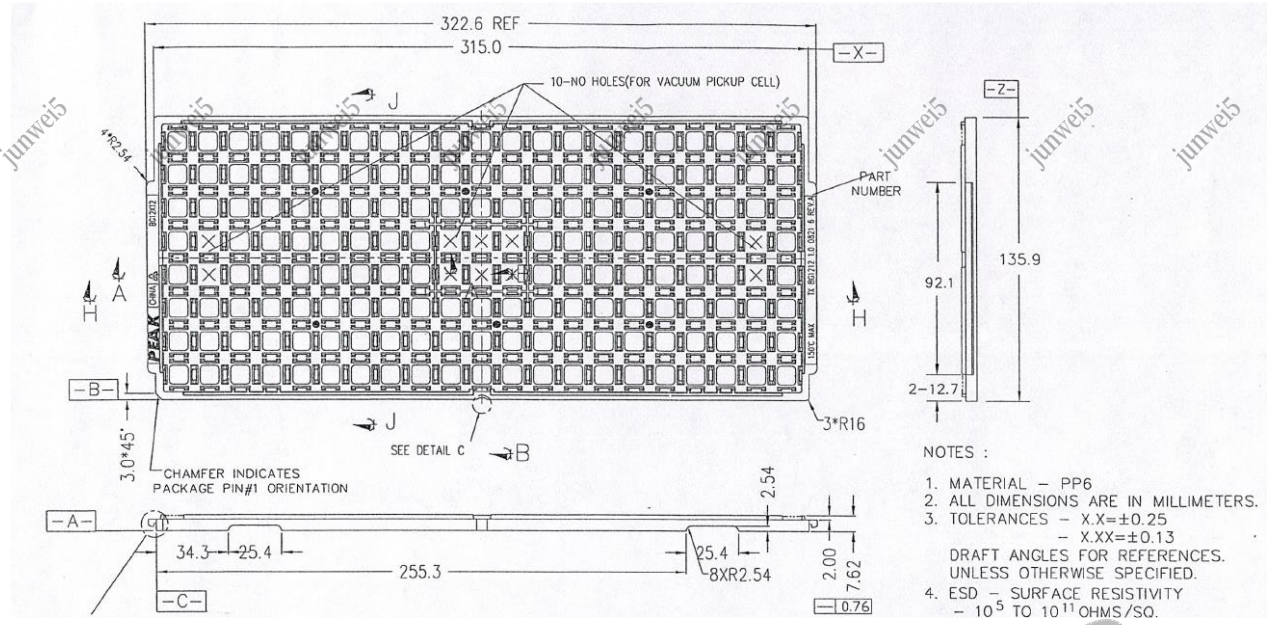
Table 8-2 shows the R329-N3/R329-S3 packing quantity.

Table 8-2 R329-N3/R329-S3 Packing Quantity Information

Sample	Size (mm)	Qty/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty
R329-N3, R329-S3	12 x 12	168	10	1680	6	10080

Figure 8-1 shows tray dimension drawing of the R329-N3/R329-S3.

Figure 8-1 R329-N3/R329-S3 Tray Dimension Drawing



8.1.1.2. R329-N4

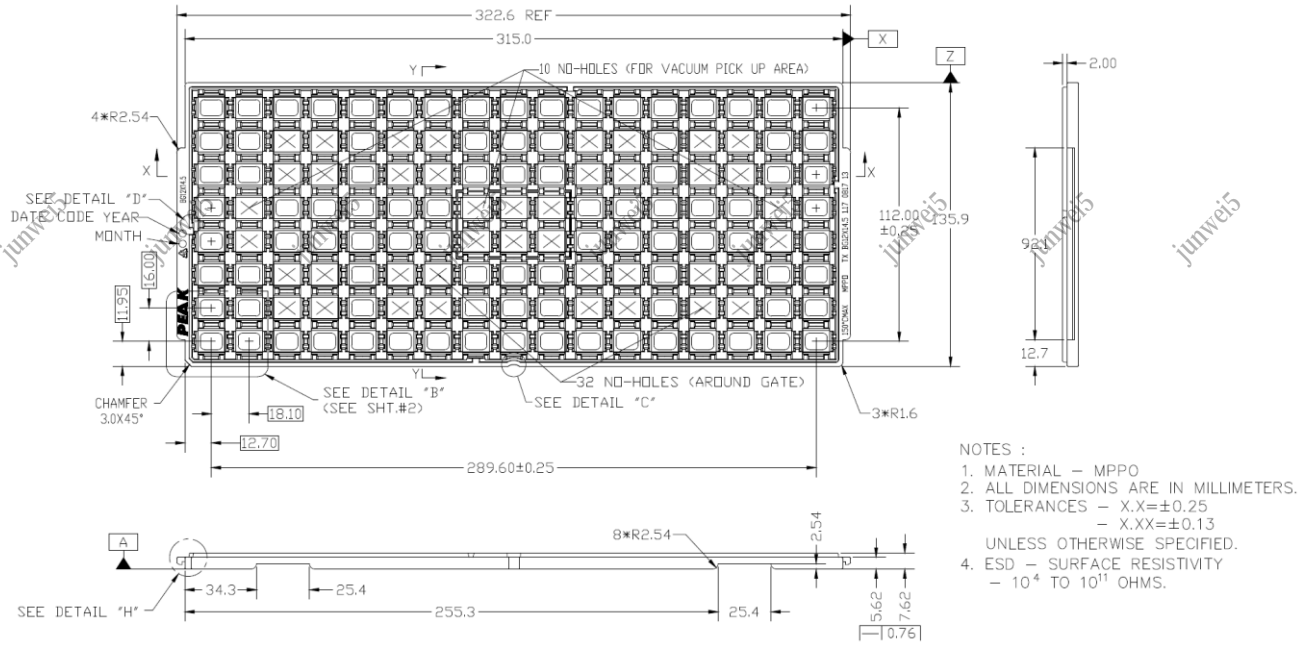
Table 8-3 shows the R329-N4 packing quantity.

Table 8-3 R329-N4 Packing Quantity Information

Sample	Size (mm)	Qty/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty
R329-N4	12 x 14.5	136	10	1360	6	8160

Figure 8-2 shows tray dimension drawing of the R329-N4.

Figure 8-2 R329-N4 Tray Dimension Drawing



8.2. Storage

Reliability is affected if any condition specified in Section 8.2.2 and Section 8.2.3 has been exceeded.

8.2.1. Moisture Sensitivity Level (MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. Table 8-4 defines all MSL.

Table 8-4 MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤30°C / 85%RH
2	1 year	≤30°C / 60%RH
2a	4 weeks	≤30°C / 60%RH
3	168 hours	≤30°C / 60%RH
4	72 hours	≤30°C / 60%RH
5	48 hours	≤30°C / 60%RH
5a	24 hours	≤30°C / 60%RH
6	Time on Label (TOL)	≤30°C / 60%RH

NOTE

The R329 device samples are classified as MSL3.

8.2.2. Bagged Storage Conditions

Table 8-5 defines the shelf life of the R329 device samples.

Table 8-5 Bagged Storage Conditions

Packing mode	Vacuum packing
Storage temperature	20°C~26°C
Storage humidity	40%~60%RH
Shelf life	12 months

8.2.3. Out-of-bag Duration

It is defined by the device MSL rating. The out-of-bag duration of the R329 is as follows.

Table 8-6 Out-of-bag Duration

Storage temperature	20°C~26°C
Storage humidity	40%~60%RH
Moisture sensitive level(MSL)	3
Floor life	168 hours

For no mention of storage rules in this document, refer to the latest ***IPC/JEDEC J-STD-020C***.

8.3. Baking

It is not necessary to bake the R329 if the conditions specified in Section 8.2.2 and Section 8.2.3 have not been exceeded. It is necessary to bake the R329 if any condition specified in Section 8.2.2 and Section 8.2.3 has been exceeded.

It is necessary to bake the R329 if the storage humidity condition has been exceeded, we recommend that the device sample removed from its shipment bag for more than 2 days shall be baked to guarantee production.

Baking conditions: 125°C, 8 hours, nitrogen protection. Note that the baking should not exceed 1 times due to

a risk of deformation.

9. Reflow Profile

All Allwinner chips provided for clients are lead-free RoHS-compliant products.

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste. If customers need to use lead solder paste, contact Allwinner FAE.

Figure 9-1 shows the appropriate reflow profile.

Figure 9-1 Lead-free Reflow Profile

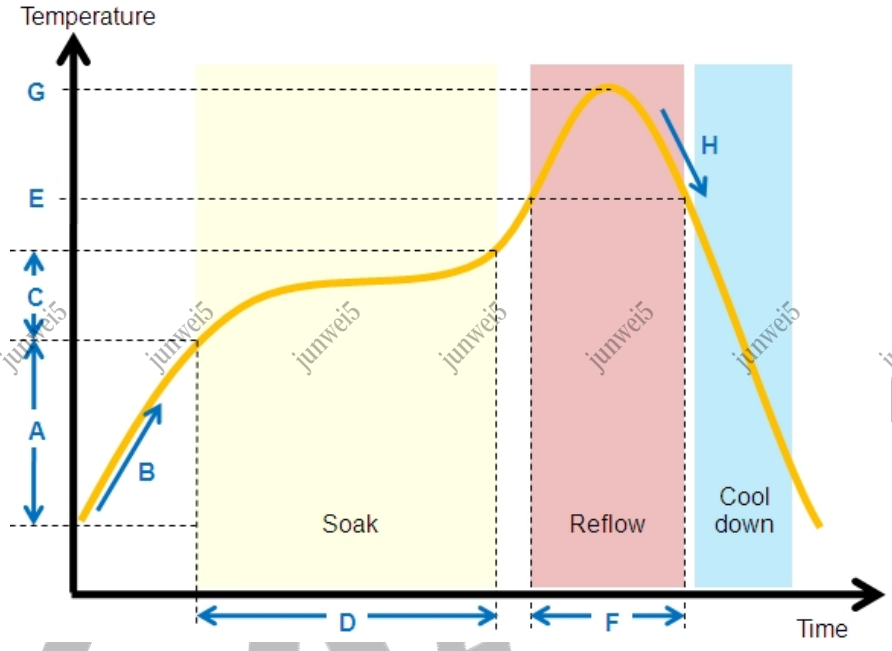


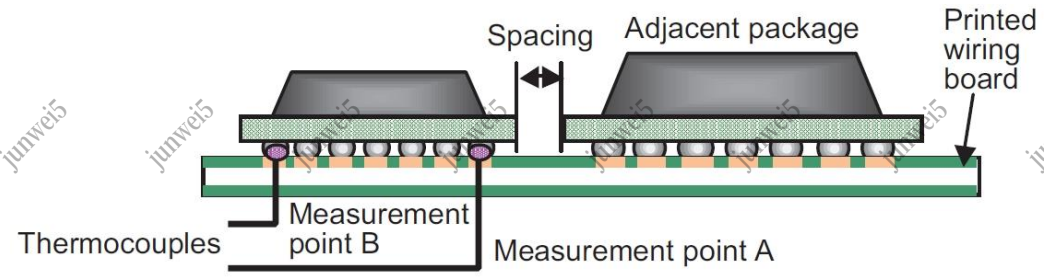
Table 9-1 Lead-free Reflow Profile Conditions

	QTI typical SMT reflow profile conditions(for reference only)	
	Step	**Reflow condition**
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25°C to 150°C
B	Preheat ramp up rate	1.5°C/s to 2.5°C/s
C	Soak temperature range	150°C to 190°C
D	Soak time	80–110 s
E	Liquidus temperature	217°C
F	Time above liquidus	60–90 s
G	Peak temperature	240°C to 250°C
H	Cool down temperature rate	≤4°C/s

The method of measuring the reflow soldering process is as follows.

Fix the thermocouple probe of the temperature measuring line at the connection point between the pin (solderable end) of the packaged device and the pad by using high-temperature solder wire or high-temperature tape, fix the packaged device at the pad by using high-temperature tape or other methods, and cover over the thermocouple probe. See Figure 9-2.

Figure 9-2 Measuring the Reflow Soldering Process



NOTE

To measure the temperature of the QFP-packaged chip, place the temperature probe directly at the pin.

If possible, the more accurate measuring way is to drill the packaged device, or drill the PCB, and fix the thermocouple probe through the drilled hole at the pad.

10. FT/QA/QC Test

10.1. FT Test

FT test is the finished product testing after the chip is packaged, and it is a functional test of all modules for each produced chip.

10.2. QA Test

QA test is a system-level sampling test for good-quality chips. According to the application level of the chip, a certain percentage of good-quality chips are selected for system-level testing to make the chip work in a typical application scenario, and judge whether the chip works normally in this scenario.

10.3. QC Test

QC test is a module-level sampling test for good-quality chips. According to the chip application level, a certain percentage of good-quality chips are selected for module-level functional testing to monitor whether the chip production process is normal.

11. Part Marking

11.1. R329-N3

Figure 11-1 shows the R329-N3 marking.

Figure 11-1 R329-N3 Marking

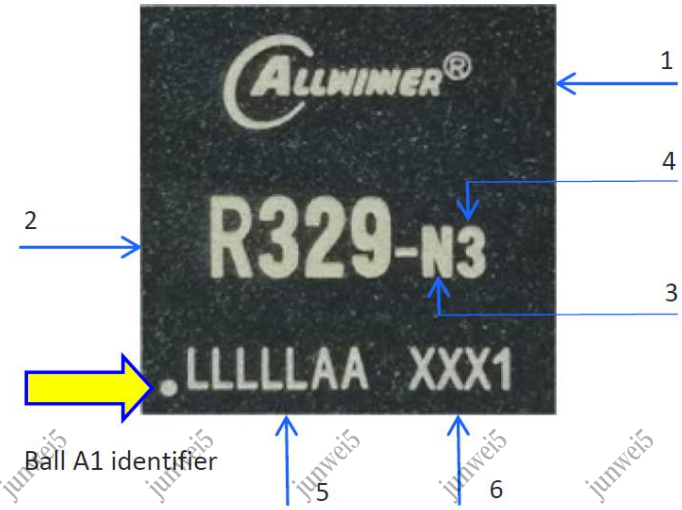


Table 11-1 describes the R329-N3 marking definitions.

Table 11-1 R329-N3 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	R329	Product name	Fixed
3	N	BGA package with AIPU	Fixed
4	3	SIP 128 MB DDR3	Fixed
5	LLLLLAA	Lot number	Dynamic
6	XXX1	Date code	Dynamic

11.2. R329-S3

Figure 11-2 shows the R329-S3 marking.

Figure 11-2 R329-S3 Marking

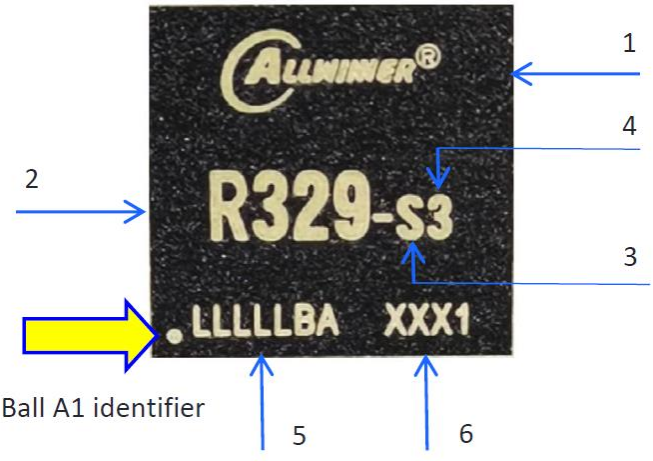


Table 11-2 describes the R329-S3 marking definitions.

Table 11-2 R329-S3 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	R329	Product name	Fixed
3	S	BGA package without AIPU	Fixed
4	3	SIP 128 MB DDR3	Fixed
5	LLLLLBA	Lot number	Dynamic
6	XXX1	Date code	Dynamic

11.3. R329-N4

Figure 11-3 shows the R329-N4 marking.

Figure 11-3 R329-N4 Marking

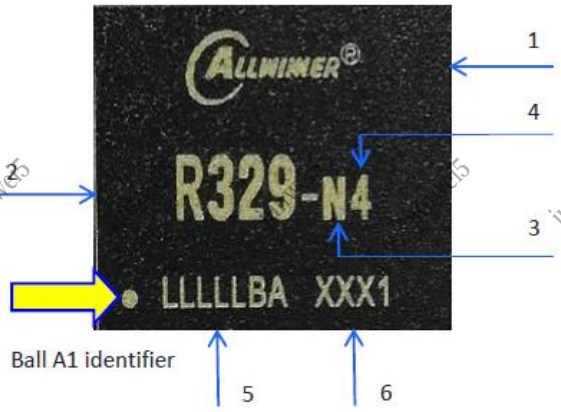


Table 11-3 describes the R329-N4 marking definitions.

Table 11-3 R329-N4 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	R329	Product name	Fixed
3	N	BGA package with AIPU	Fixed
4	4	SIP 256 MB DDR3	Fixed
5	LLLLLBA	Lot number	Dynamic
6	XXX1	Date code	Dynamic

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